

# TLC69629-Q1 Automotive, 60mA, 48-Channel LED Driver

## With Integrated Oscillator, Advance Diagnostics and Cascaded Serial Interface

### 1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C4B
- **Functional Safety-Compliant**
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL B targeted
- 48 integrated current sinks
  - Programmable 16-bit PWM / hybrid dimming
  - Programmable 7-bit analog dot correction (DC)
  - Maximum output current, voltage: 60mA, 16V
- Integrated 33MHz oscillator
  - 16-bit PWM output in 500Hz
  - $> 20\text{KHz}$  refresh rate with enhanced spectrum (ES) PWM
- High-speed communication
  - Cascaded serial interface (CSI)
  - Data rates up to 17Mbps
- Power efficiency optimization
  - Adaptive headroom voltage control (AHVC)
  - Device power save mode (PSM)
- EMI mitigation
  - Interface: programmable buffer driving capability
  - Current sinks: phase shifting / spread spectrum
- Protection and diagnostic
  - LED: open / short detection / health check
  - Current sink: adjacent-pin short / health check
  - Interface: CRC / command error / time-out error / communication watchdog
  - Device: under voltage / ISET out of range / thermal shutdown / memory CRC / OTP CRC / OSC watchdog

### 2 Applications

- Automotive central information display
- Automotive cluster display
- Automotive head-up display

### 3 Description

The TLC69629-Q1 is an LED driver with 48 constant current sink channels, which can provide up to 16-bit individual pixel-level LED PWM control. The additional 7-bit dot correction (DC) is also implemented to each channel to control peak current. Each device shares data stream by cascaded serial interface (CSI), which supports up to 511 devices connection. The interface is **software compatible with LED drivers in the same group** which can be applied to different application scenarios based on LED current and total LED number.

To optimize overall systematic power efficiency, the device is equipped with adaptive headroom voltage control (AHVC) scheme to optimize headroom voltage across each channel and device. Only the OUT47 pin from the last device of daisy chain is required to be programmed as FB pin to optimize LED supply voltage from DC/DC.

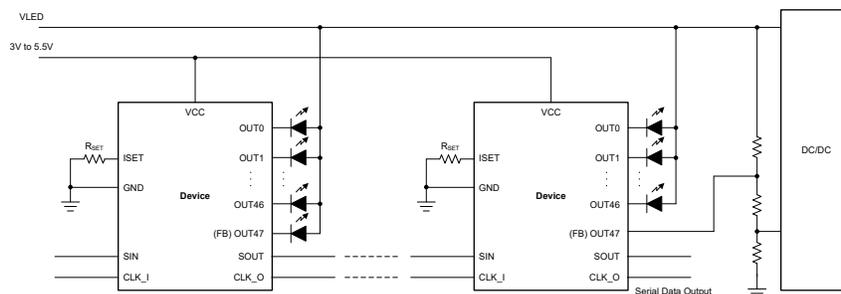
The TLC69629-Q1 is equipped diagnostics for LED, current sink, communication, and device.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TLC69629-Q1	RTQ (VQFN, 56) wetable flank	8mm × 8mm
	DCA (HTSSOP, 56)	14mm × 8.1mm
	DFD (HTSSOP, 56)	

(1) For more information, see [Section 7](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



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## 4 Device Comparison

PART NUMBER	CHANNEL NUMBER	MAX. CHANNEL CURRENT	FUNCTIONAL SAFETY CLASSIFICATION	INTERFACE	SOFTWARE COMPATIBLE
TLC69621-Q1 <sup>(1)</sup>	8	60mA	Functional Safety-Capable	SPI	Group 1
TLC69624-Q1 <sup>(1)</sup>	24				
TLC69627-Q1	48				
TLC69631-Q1 <sup>(1)</sup>	8	100mA	Functional Safety-Capable	SPI	Group 1
TLC69634-Q1 <sup>(1)</sup>	24				
TLC69637-Q1	48				
TLC69622-Q1 <sup>(1)</sup>	8	60mA	Functional Safety-Compliant	SPI	Group 2
TLC69625-Q1 <sup>(1)</sup>	24				
TLC69628-Q1	48				
TLC69632-Q1 <sup>(1)</sup>	8	100mA	Functional Safety-Compliant	SPI	Group 2
TLC69635-Q1 <sup>(1)</sup>	24				
TLC69638-Q1	48				
TLC69623-Q1 <sup>(1)</sup>	8	60mA	Functional Safety-Compliant	CSI	Group 3
TLC69626-Q1 <sup>(1)</sup>	24				
TLC69629-Q1	48				
TLC69633-Q1 <sup>(1)</sup>	8	100mA	Functional Safety-Compliant	CSI	Group 3
TLC69636-Q1 <sup>(1)</sup>	24				
TLC69639-Q1	48				

(1) Product preview

## 5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from , to , (from Revision * (January 2025) to Revision A (July 2025))	Page
• Changed document status from Advance Information to Production Data.....	1

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PTLC69629QRTQRQ1</a>	Active	Preproduction	QFN (RTQ)   56	3500   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLC69629QRTQRQ1.A	Active	Preproduction	QFN (RTQ)   56	3500   LARGE T&R	-	Call TI	Call TI	-40 to 125	
<a href="#">TLC69629QDCARQ1</a>	Active	Production	HTSSOP (DCA)   56	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC69629Q1
<a href="#">TLC69629QRTQRQ1</a>	Active	Production	QFN (RTQ)   56	3500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	69629Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

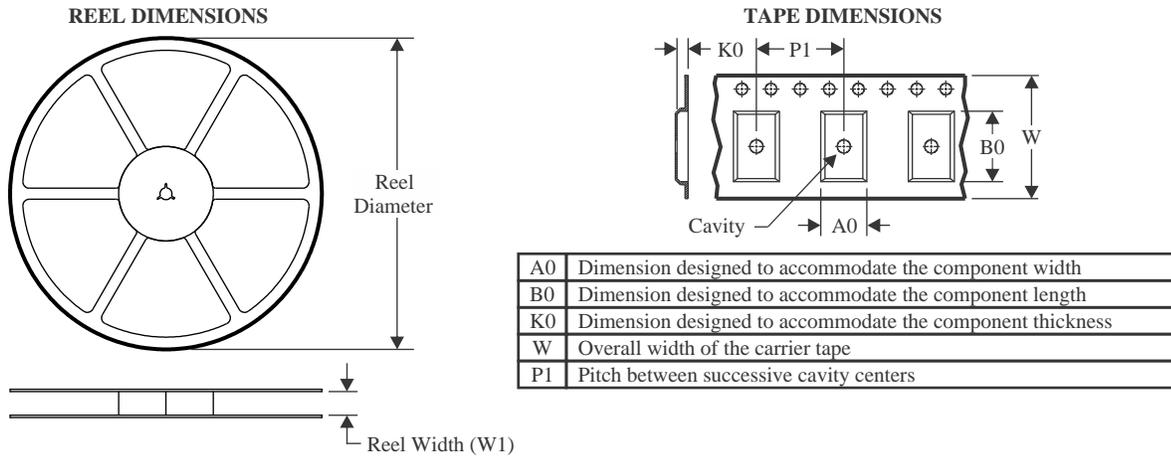
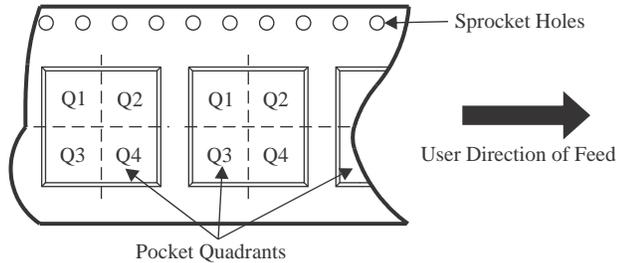
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

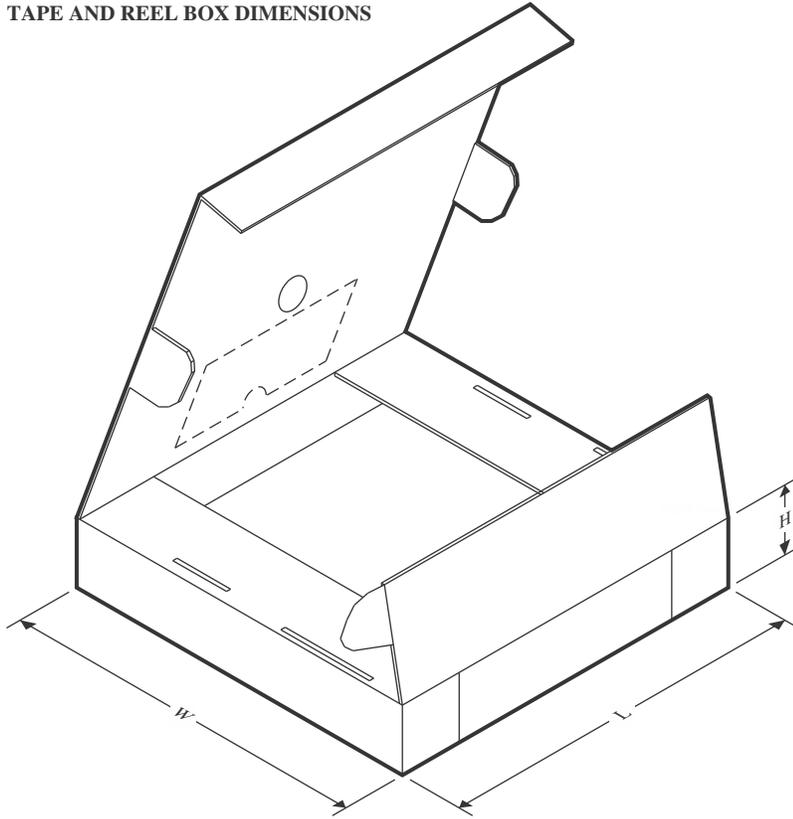
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

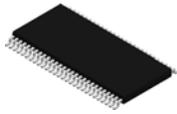
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
TLC69629QRTQRQ1	QFN	RTQ	56	3500	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	356.0	356.0	45.0
TLC69629QRTQRQ1	QFN	RTQ	56	3500	360.0	360.0	36.0

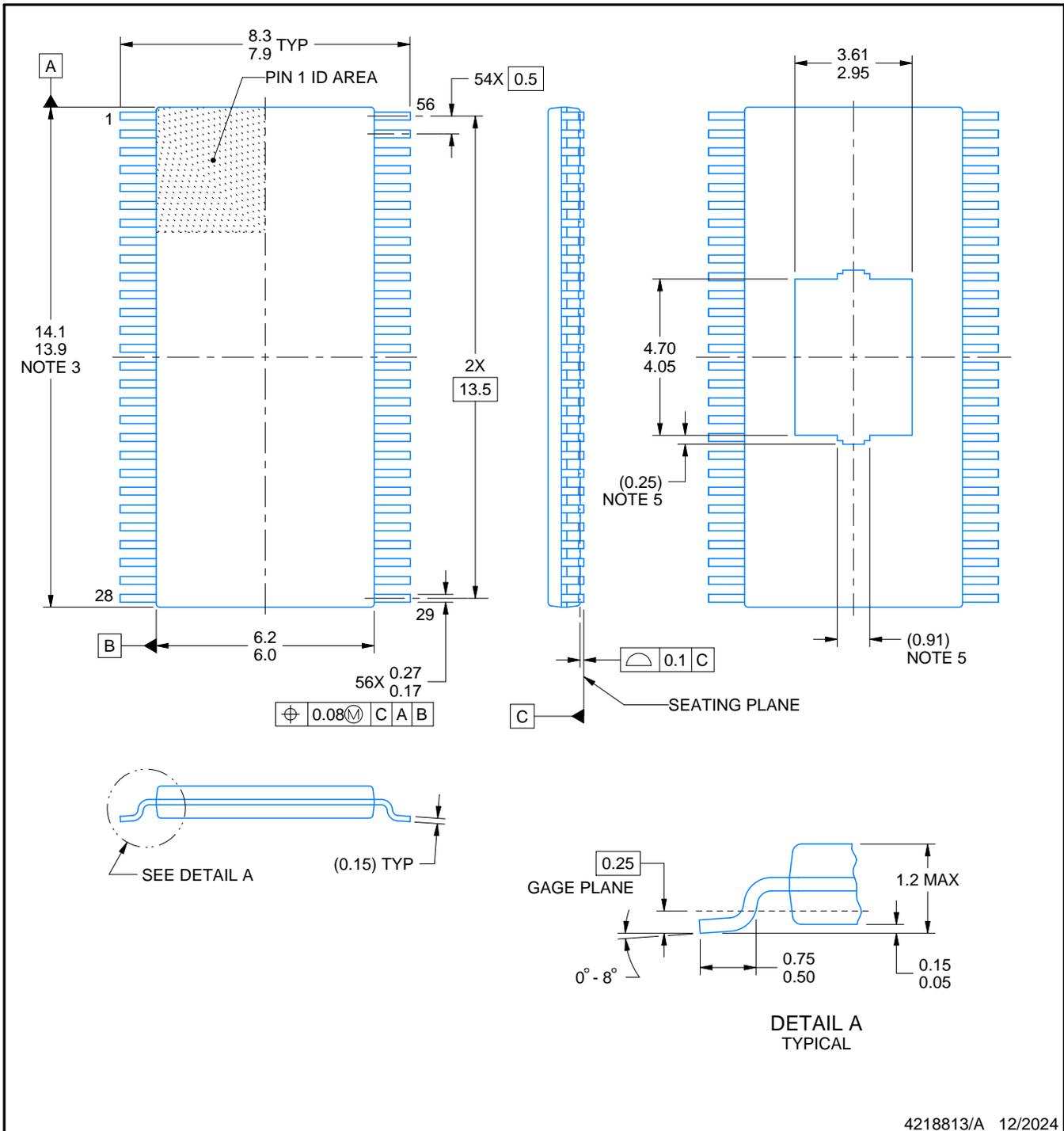
# DCA0056F



# PACKAGE OUTLINE

## PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



4218813/A 12/2024

### NOTES:

PowerPAD is a trademark of Texas Instruments.

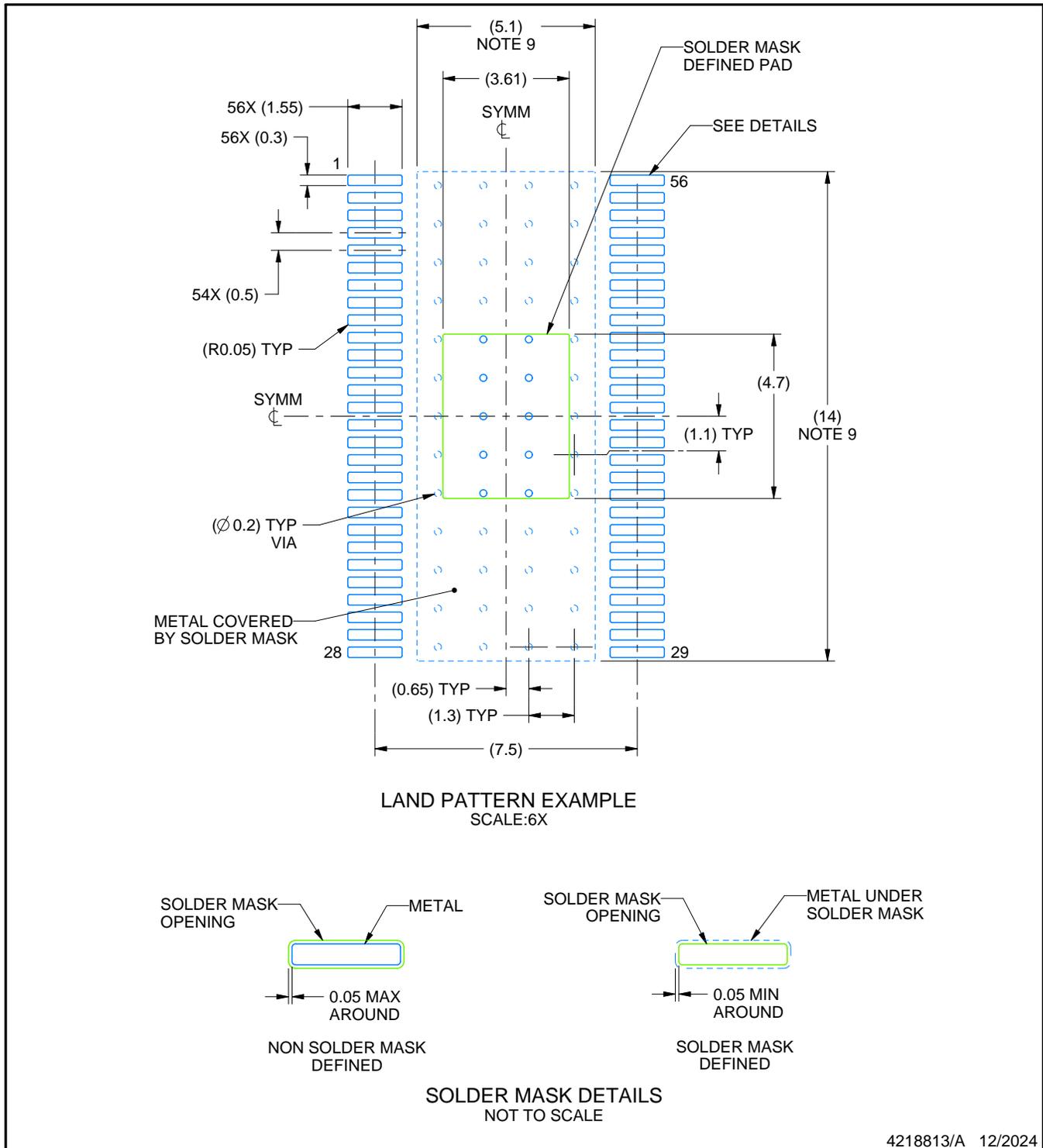
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.
- Features may not present.

# EXAMPLE BOARD LAYOUT

DCA0056F

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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NOTES: (continued)

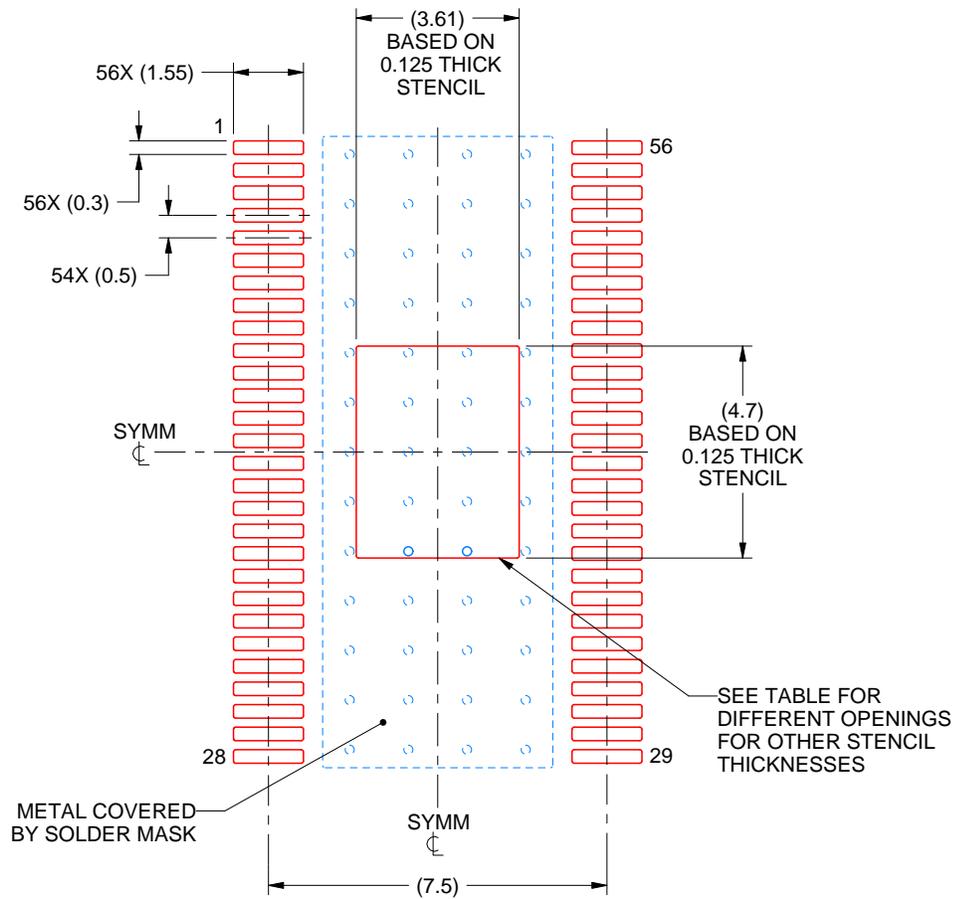
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DCA0056F

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



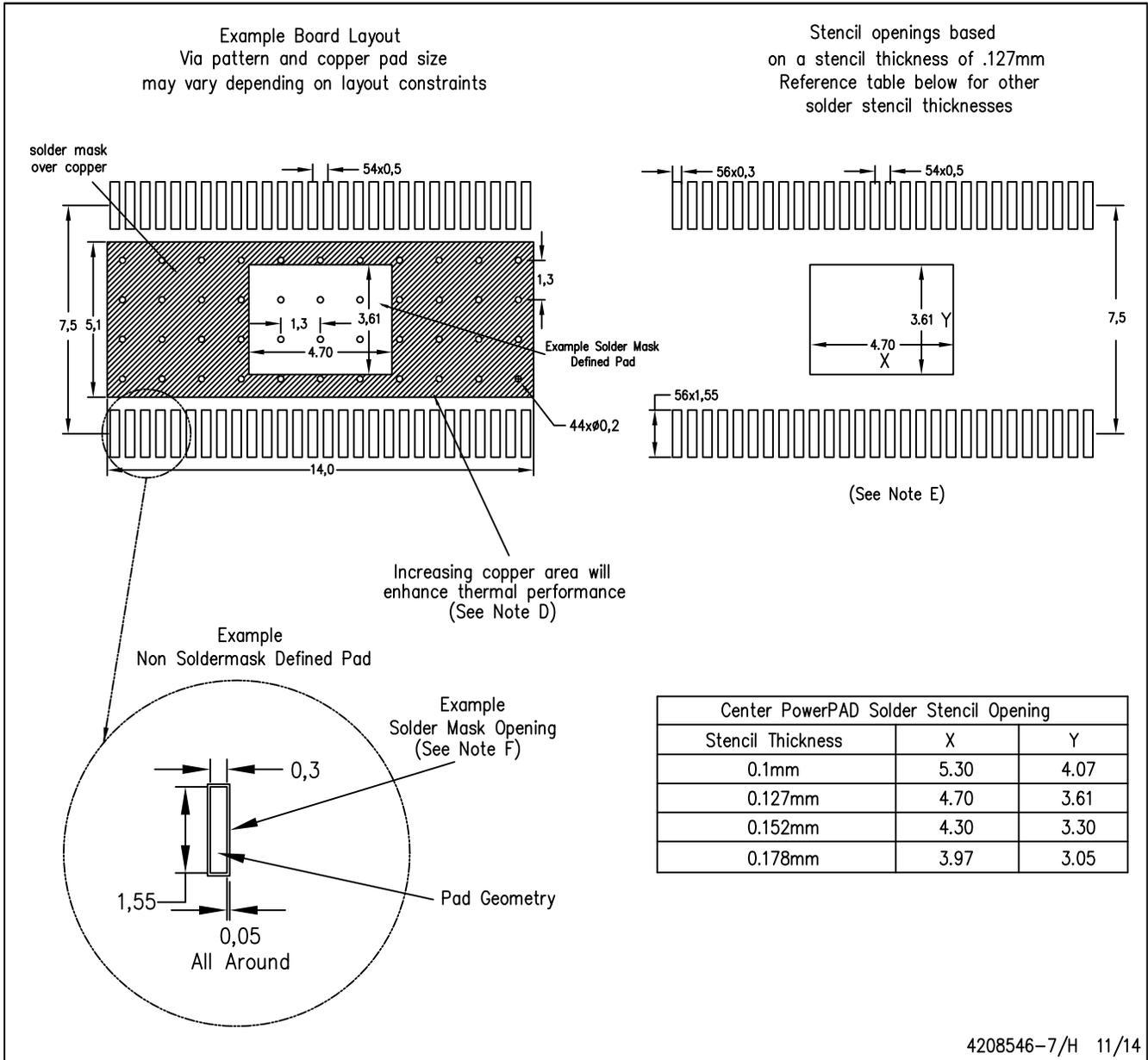
**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.04 X 5.25
0.125	3.61 X 4.70 (SHOWN)
0.15	3.30 X 4.29
0.175	3.95 X 3.97

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

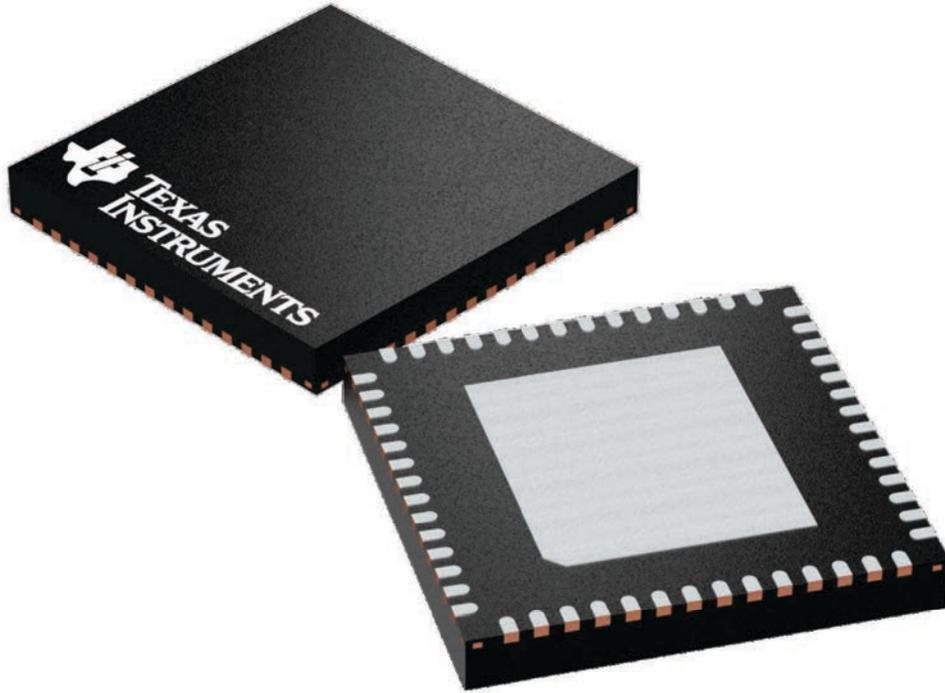
## GENERIC PACKAGE VIEW

**RTQ 56**

**VQFN - 1 mm max height**

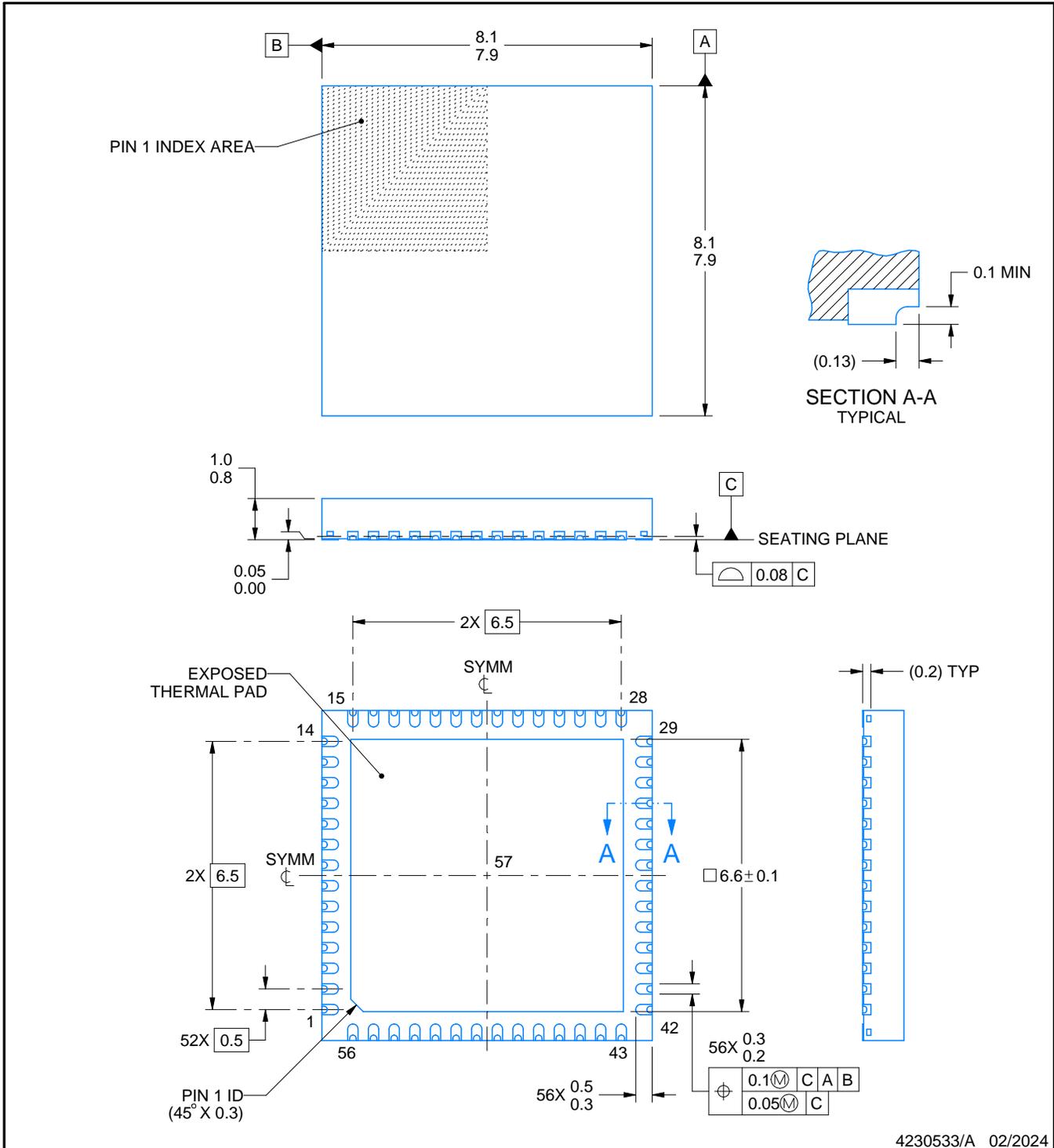
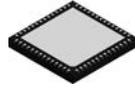
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224653/A



4230533/A 02/2024

NOTES:

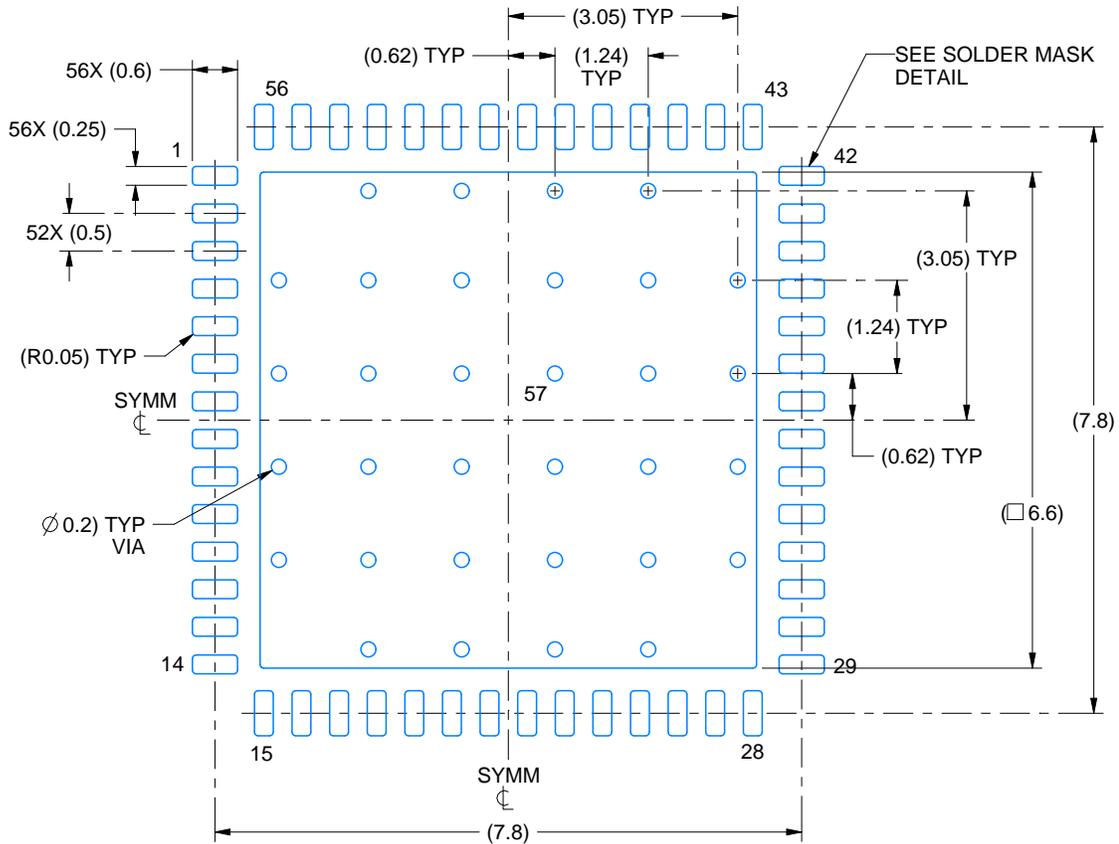
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

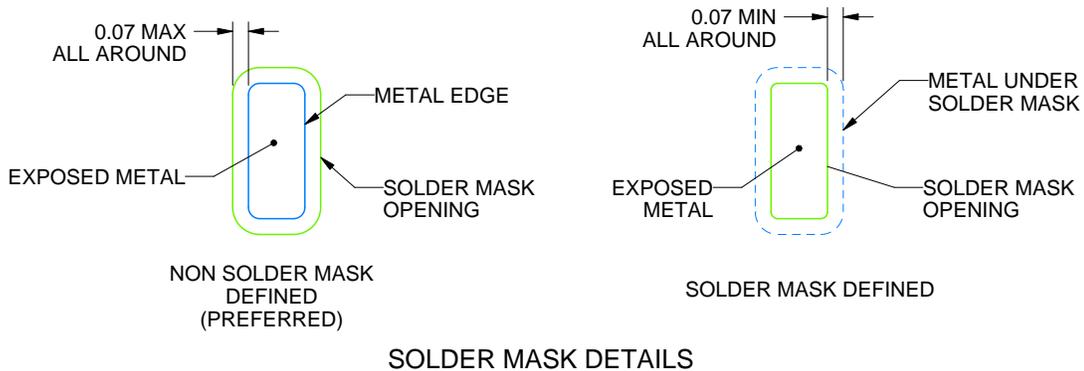
RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4230533/A 02/2024

NOTES: (continued)

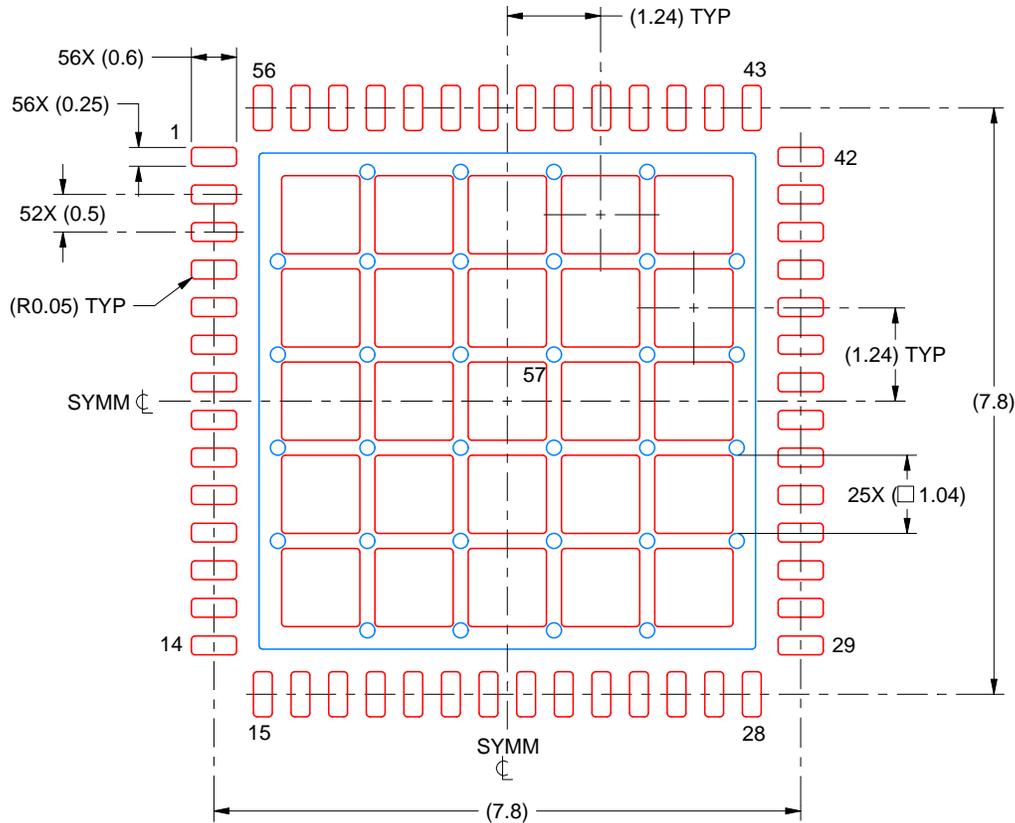
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 10X

EXPOSED PAD 57  
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230533/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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