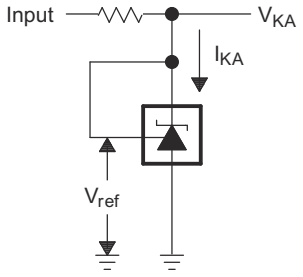
TLA431、TLA432 負荷全体が静電容量性の場合でも安定、高精度プログラマブル リファレンス

1 特長

- 出力コンデンサ不要
- 負荷がすべて容量性負荷でも安定
- 25℃ での基準電圧の許容公差
  - 1% (A グレード)
- 可変出力電圧:V_{ref}～36V
- -40℃～125℃で動作
- 標準温度ドリフト (TLA43xA)
  - 8mV (I 温度)
  - 11mV (Q 温度)
- 低い出力ノイズ
- 出力インピーダンス:0.2Ω (標準値)
- シンク電流能力:0.2mA～100mA
- 業界標準の TL431 および TL432 デバイスとピン互換

2 アプリケーション

- ラック サーバーの電源
- 産業用 AC/DC
- AC インバータと VF ドライブ
- サーボ ドライブ制御モジュール
- ノート PC 向け電源アダプタの設計



概略回路図

3 概要

TLA431 および TLA432 デバイスは、3 端子の可変シャント レギュレータで、全容量性負荷に対して安定して動作します。このデバイスは業界標準の TL431 および TL432 とピン互換ですが、全容量性負荷をサポートするために安定性が向上しています。出力カソード電圧は、2 個の外付け抵抗を使用して、V_{ref} (2.495V)～36V の範囲にある任意の値に設定できます。これらのデバイスの出力インピーダンスは 0.2Ω (標準値) です。これらのデバイスは、アクティブ出力回路により、非常にシャープな電源オン特性を持ち、オンボード レギュレーション、可変電源、スイッチング電源など多くの用途において、ツェナー ダイオードの優れた代替品となります。TLA431 は、低電圧監視用のコンパレータとしても機能します。TLA431 の内部アンプと基準電圧は、絶縁フォトカプラ フライバック電源でエラー アンプを使用します。TLA432 デバイスの機能と電気的仕様は、TLA431 デバイスと完全に同じです。

TLA431 および TLA432 デバイスは I と Q の 2 つの温度グレードで仕様が規定されており、また、これらのデバイスは全温度範囲にわたって安定したリファレンス電圧を示します。

製品情報

部品番号 (1)	パッケージ (ピン) (2)	本体サイズ (公称)
TLA431	SOT23-3	2.90mm × 1.30mm
TLA432	SOT23-3	2.90mm × 1.30mm
TLA431(3)	SOT5X3 (6)	1.20 mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) *製品プレビュー*

Table of Contents

4 Device Comparison Table

DEVICE PINOUT	INITIAL ACCURACY	OPERATING FREE-AIR TEMPERATURE (T_A)
TLA431 TLA432	A: 1%	I: -40°C to 85°C Q: -40°C to 125°C

5 Pin Configuration and Functions

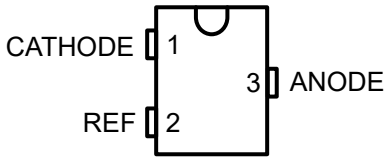


**図 5-1. DBZ Package,
3-Pin SOT-23, TLA431 (Top View)**

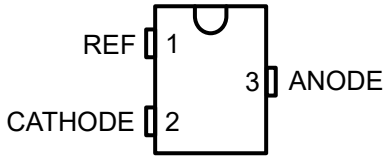


**図 5-2. DBZ Package,
3-Pin SOT-23, TLA432 (Top View)**

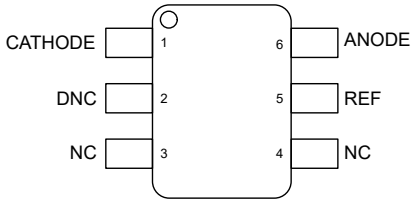


**図 5-3. DRL Package,
6-Pin SOT-563, TLA431 (Top View) *PRODUCT PREVIEW***

表 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	TLA431		TLA432		
	DBZ	DRL	DBZ		
CATHODE	1	1	2	I/O	Shunt Current/Voltage input
REF	2	5	1	I	Threshold relative to common anode
ANODE	3	6	3	O	Common pin, normally connected to ground
NC	-	3, 4	-	-	No connect
DNC	-	2	-	-	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{KA}	Cathode Voltage(2)			37	V
I_{KA}	Continuous Cathode Current Range		–100	150	mA
$I_{I(ref)}$	Reference Input Current		–0.05	10	mA
T_J	Operating Junction Temperature Range		–40	150	C
T_{stg}	Storage Temperature Range		–65	150	C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- ±1000 VC101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{KA}	Cathode Voltage		V_{REF}	36	V
I_{KA}	Continuous Cathode Current Range		0.2	100	mA
T_A	Operating Free-Air Temperature	TLA43xxI	–40	85	C
		TLA43xxQ	–40	125	C

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.4 Thermal Information

THERMAL METRIC(1)		TLA43x DBZ 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.8	C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115.8	C/W
$R_{\theta JB}$	Junction-to-boardthermal resistance	53.1	C/W
ψ_{JT}	Junction-to-top characterization resistance	16.6	C/W
ψ_{JB}	Junction-to-board characterization resistance	52.6	C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference Voltage	See 図 7-1	V_{KA} = V_{ref}, I_{KA} = 10mA	TLA43xAx devices	2470	2495	2520	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (1)	See 図 7-1	V_{KA} = V_{ref}, I_{KA} = 10mA, –40°C < T_J < 85°C	TLA43xxI devices		8	17	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (1)	See 図 7-1	V_{KA} = V_{ref}, I_{KA} = 10mA, –0°C < T_J < 90°C	TLA43xxQ devices		5	13	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (1)	See 図 7-1	V_{KA} = V_{ref}, I_{KA} = 10mA, –40°C < T_J < 125°C	TLA43xxQ devices		11	20	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See 図 7-2	I_{KA} = 10mA	ΔV_{KA} = 10V - V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36V - 10V		–1	–2	mV/V
I_{ref}	Reference Input Current	See 図 7-2	I_{KA} = 10mA, R1 = 10kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range (1)	See 図 7-2	I_{KA} = 10mA, R1 = 10kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See 図 7-1	V_{KA} = V_{ref}			0.15	0.2	mA
I_{off}	Off-state cathode current	See 図 7-3	V_{KA} = 36V, V_{ref} = 0			0.1	0.5	µA
$\|Z_{KA}\|$	Dynamic Impedance (2)	See 図 7-1	V_{KA} = V_{ref}, I_{KA} = 1mA to 100mA			0.2	0.5	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. For more details on $V_{I(dev)}$ and how it relates to the average temperature coefficient, see Parameter Measurement Information.

(2) The dynamic impedance is defined by $|Z_{KA}| = \Delta V_{KA}/\Delta I_{KA}$. For more details on $|Z_{KA}|$ and how it relates to V_{KA}, see Parameter Measurement Information.

6.6 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

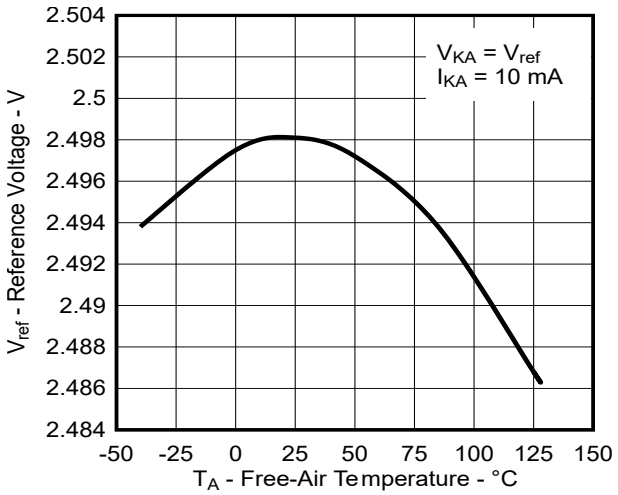


図 6-1. Reference Voltage vs Free-Air Temperature

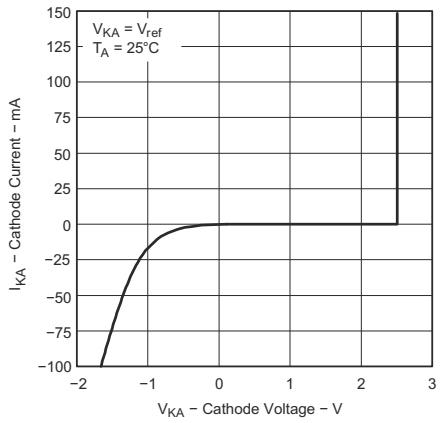


図 6-2. Cathode Current vs Cathode Voltage

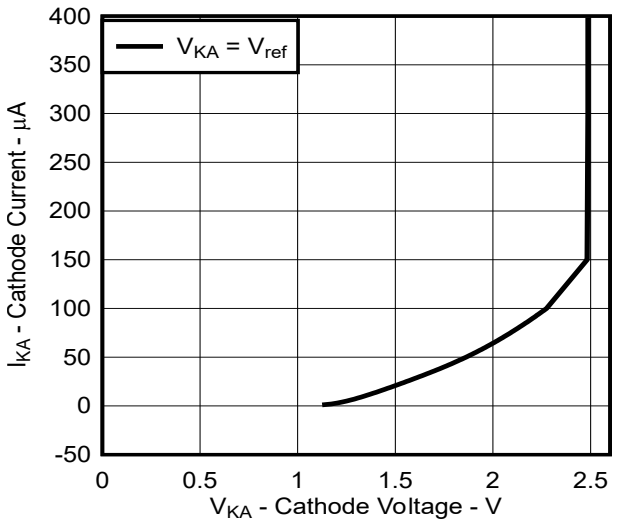


図 6-3. Cathode Current vs Cathode Voltage

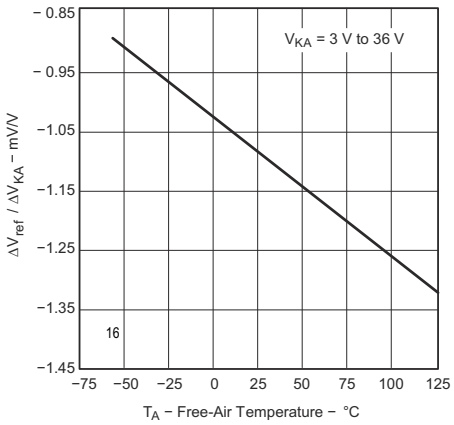


図 6-4. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-Air Temperature

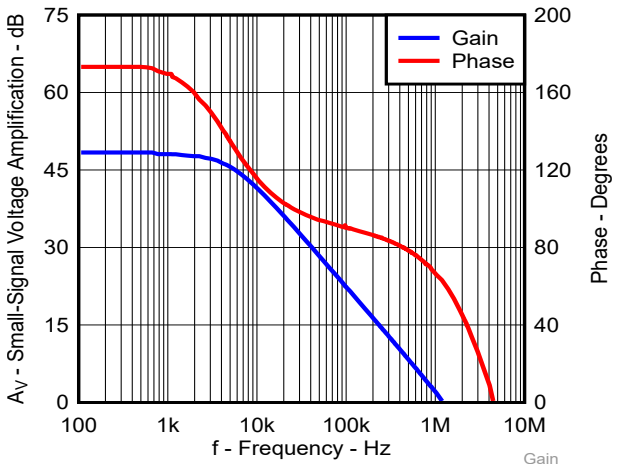


図 6-5. Small-Signal Voltage Amplification vs Frequency

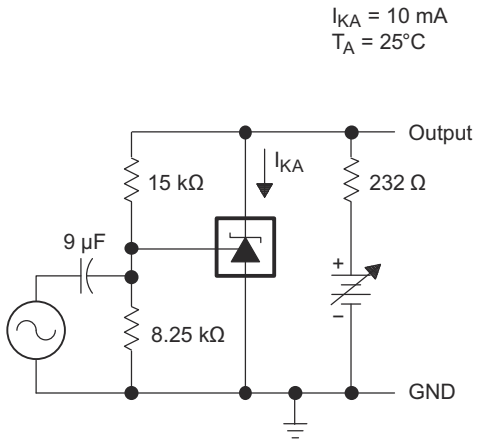


図 6-6. Test Circuit for Voltage Amplification

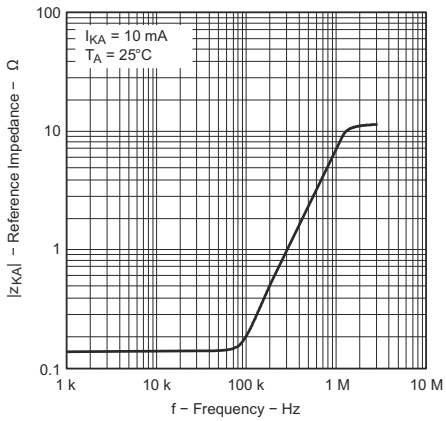


図 6-7. Reference Impedance vs Frequency

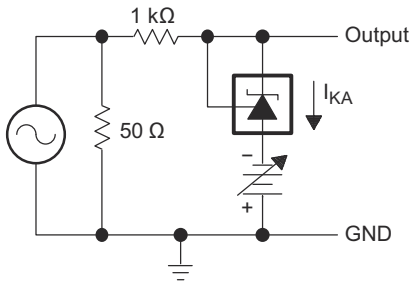


図 6-8. Test Circuit for Reference Impedance

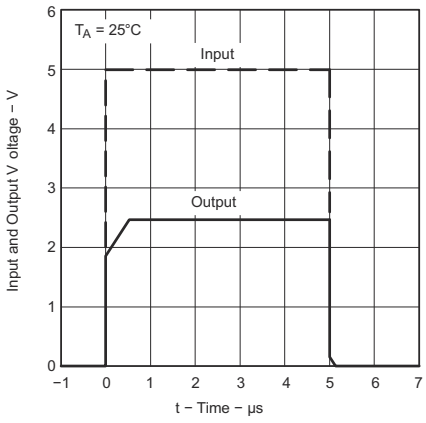


図 6-9. Pulse Response

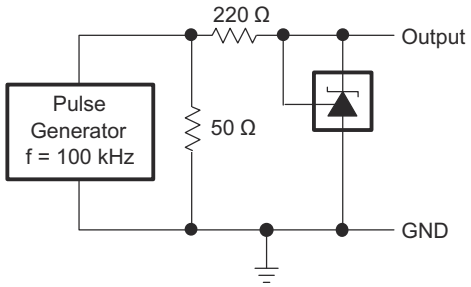


図 6-10. Test Circuit for Pulse Response

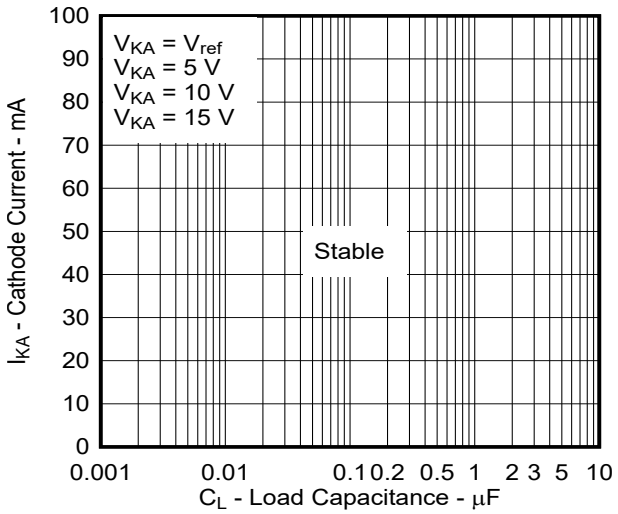
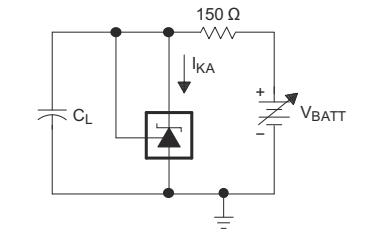
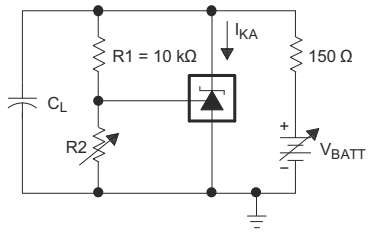


図 6-11. Stability Boundary Conditions



TEST CIRCUIT FOR CURVE A



TEST CIRCUIT FOR CURVES B, C, AND D

図 6-12. Test Circuit for Stability Boundary Conditions

7 Parameter Measurement Information

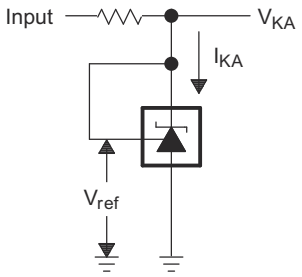


図 7-1. Test Circuit for $V_{KA} = V_{ref}$

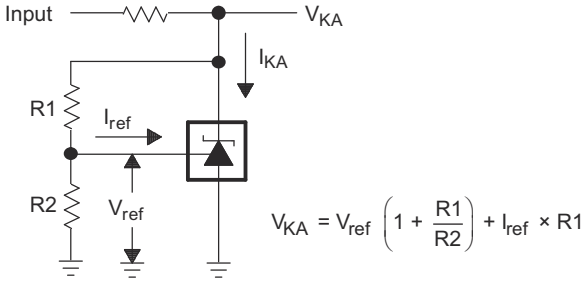


図 7-2. Test Circuit for $V_{KA} > V_{ref}$

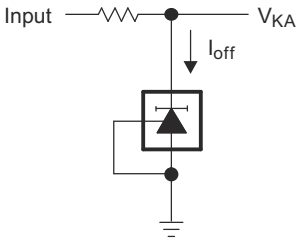


図 7-3. Test Circuit for I_{off}

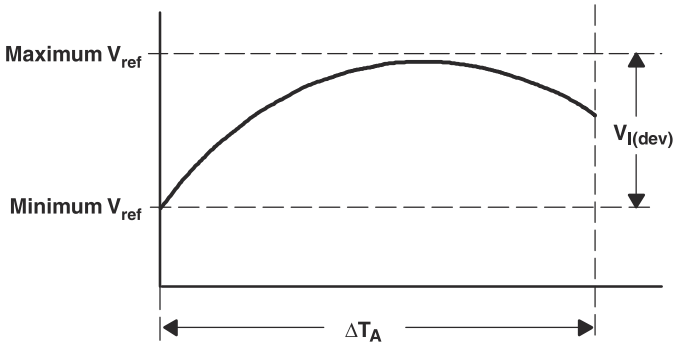
7.1 Temperature Coefficient

The deviation of the reference voltage, V_{ref}, over the full temperature range is known as $V_{I(dev)}$. The parameter of $V_{I(dev)}$ can be used to find the temperature coefficient of the device. The average full-range temperature coefficient of the reference input voltage, α_{Vref}, is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature. The full-range temperature coefficient is an average and therefore any subsection of the

rated operating temperature range can yield a value that is greater or less than the average. For more details on temperature coefficient, refer to the *Voltage Reference Selection Basics White Paper*.

7.2 Dynamic Impedance

The dynamic impedance is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$. When the device is operating with two external resistors (see 図 6-8), the total dynamic impedance of the circuit is given by $|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|Z_{KA}|\left(1+\frac{R1}{R2}\right)$.

The V_{KA} of the device can be affected by the dynamic impedance. The device test current I_{test} for V_{KA} is specified in the *Electrical Characteristics*. Any deviation from I_{test} can cause deviation on the output V_{KA}. 図 7-4 shows the effect of the dynamic impedance on the V_{KA}.

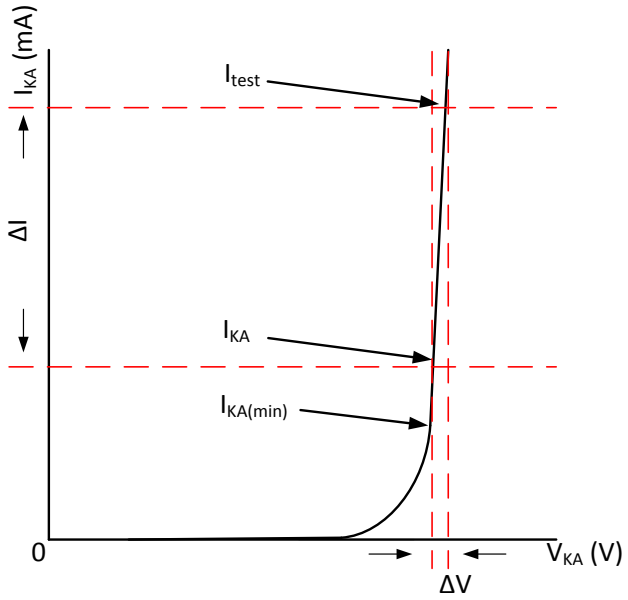


図 7-4. Dynamic Impedance

8 Detailed Description

8.1 Overview

The TLA431 and TLA432 devices are three-terminal adjustable shunt regulators that are stable with all capacitor loads. This standard device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This device is pin compatible with the industry standard TL431. The TLA431 contains an accurate voltage reference & op amp, which are very fundamental analog building blocks. TLA431 has improved the stability for capacitive loads. TLA431 is used in conjunction with external components to behave as a single voltage reference, error amplifier, current sink, voltage clamp or comparator with an integrated reference.

TLA431 can be operated and adjusted to cathode voltages from 2.495V to 36V, making this part optimum for a wide range of end equipment in industrial, auto, telecom & computing. For this device to behave as a shunt regulator or error amplifier, >0.2mA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

The TLA432 device has exactly the same functionality and electrical specifications as the TLA431 device. The TLA43xAI devices are characterized for operation from –40°C to 85°C, and the TLA43xAQ devices are characterized for operation from –40°C to 125°C.

8.2 Functional Block Diagram

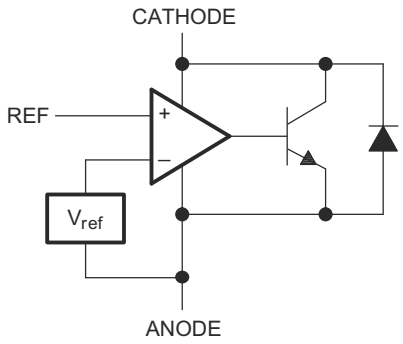


図 8-1. Equivalent Schematic

8.3 Feature Description

TLA431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair. A Darlington pair is used for this device to be able to sink a maximum current of 100mA.

When operated with enough voltage headroom (≥ 2.495V) and cathode current (I_{KA}), TLA431 forces the reference pin to 2.495V. However, the reference pin can not be left floating, as the reference pin needs I_{REF} ≥ 4µA (please see *Electrical Characteristics*). This is because the reference pin is driven into an npn, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, TLA431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations for the TLA431 to be in the proper linear region giving the TLA431 enough gain.

TLA431 is internally compensated to be stable without an output capacitor between the cathode and anode.

8.4 Device Functional Modes

8.4.1 Closed Loop

When the cathode/output voltage or current of TLA431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLA431 use the TLA431 in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting the cathode to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make the reference pin equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

8.4.1.1 Stability (Closed Loop)

TLA431 is internally compensated to be stable without an output capacitor between the cathode and anode as shown in 図 8-2. The TLA431 is also stable across all capacitive loads from cathode to anode. This includes the popular 0.1µF capacitor load. The TLA431 has been tested to have stable operation with no capacitive loads up to capacitors larger than 10µF. See 図 6-11 for stability chart and test setup.

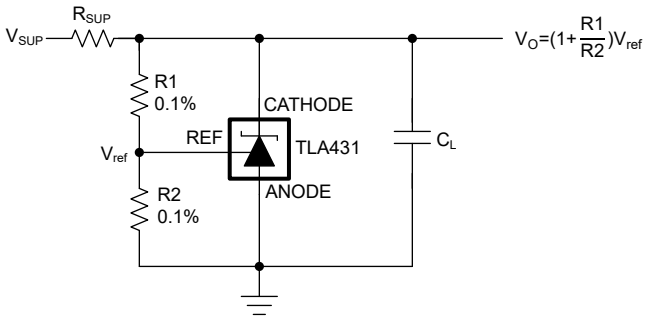


図 8-2. TLA431 with load capacitor

The TLA431 is sensitive to capacitance on the REF pin when the REF is isolated from cathode. For stable voltage regulation, do not add capacitance to the REF pin as shown in 図 8-3.

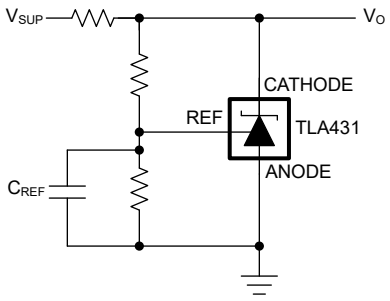


図 8-3. TLA431 with capacitor on REF pin

8.4.2 Open Loop (Comparator)

When the cathode/output voltage or current of TLA431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLA431 has the characteristics shown in 図 9-4. With such high gain in this configuration, TLA431 is typically used as a comparator. With the reference integrated makes TLA431 the prefered choice when users are trying to monitor a certain level of a single signal.

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As this device has many applications and setups, there are many situations that this data sheet can not characterize in detail.

Application note *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2 Typical Applications

9.2.1 Shunt Regulator/Reference

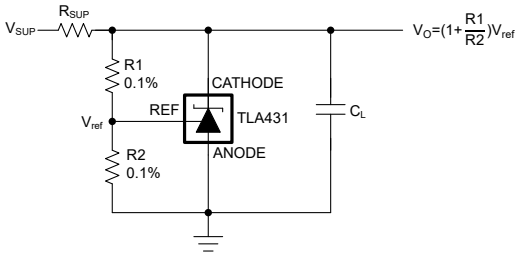


図 9-1. Shunt Regulator Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-2 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	24V
Cathode Current (Ik)	5mA
Output Voltage Level	2.5V - 36V
Load Capacitance	0.1µF
Feedback Resistor Values and Accuracy (R1 & R2)	10kΩ

9.2.1.2 Detailed Design Procedure

When using TLA431 as a Shunt Regulator, determine the following:

- Input Voltage Range
- Temperature Range
- Total Accuracy
- Cathode Current
- Reference Initial Accuracy
- Output Capacitance

9.2.1.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in 図 9-1, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in 図 9-1. The cathode voltage can be more accuratel determined by taking in to account the cathode current:

$Vo=(1+R1/R2)*V_{REF}-I_{REF}*R1$

For this equation to be valid, TLA431 must be fully biased so that the TLA431 has enough open loop gain to mitigate any gain error. This can be done by meeting the Imin spec denoted in *Electrical Characteristics*.

9.2.1.2.2 Total Accuracy

When programming the output above unity gain ($V_{KA}=V_{REF}$), TLA431 is susceptible to other errors that can effect the overall accuracy beyond V_{REF}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ - Change in reference voltage over temperature
- ΔV_{REF} / ΔV_{KA} - Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. Application note *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2.1.2.3 Start-Up Time

As shown in 図 9-2, TLA431 has a fast response up to about 2V and then slowly charges to the programmed value.

9.2.1.3 Application Curve

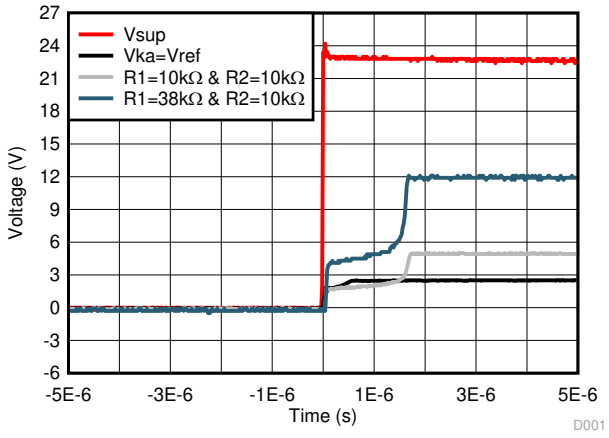


図 9-2. TLA431Start-Up Response

9.2.2 Comparator With Integrated Reference

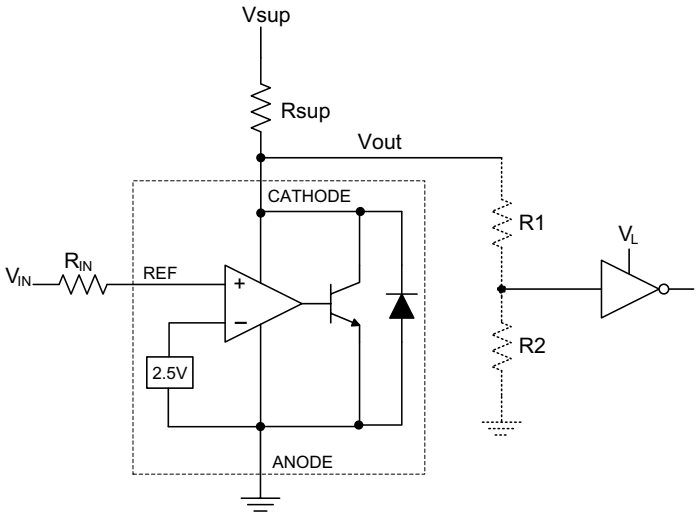


図 9-3. Comparator Application Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in *表 9-2* as the input parameters.

表 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to 5V
Input Resistance	10kΩ
Supply Voltage	24V
Cathode Current (Ik)	5mA
Output Voltage Level	2V – V_{SUP}
Logic Input Thresholds VIH/VIL	V_L

9.2.2.2 Detailed Design Procedure

When using TLA431 as a comparator with reference, determine the following:

- Input Voltage Range
- Reference Voltage Accuracy
- Output logic input high and low level thresholds
- Current Source resistance

9.2.2.2.1 Basic Operation

In the configuration shown in 図 9-3 TLA431 behaves as a comparator, comparing the V_{REF} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_K), TLA431 has enough open loop gain to provide a quick response. This can be seen in 図 9-4, where the R_{SUP}=10kΩ (I_{KA}=500µA) situation responds much slower than R_{SUP}=1kΩ (I_{KA}=5mA). Operation near and below I_{min} can result in low gain, leading to a slow response.

9.2.2.2.1.1 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The more overdrive voltage provided, the faster the TLA431 response.

For applications where TLA431 is being used as a comparator, good design practice is to set the trip point to greater than the positive expected error (i.e. +1.0% for the A version). For fast response, setting the trip point to >10% of the internal V_{REF} can suffice.

For minimal voltage drop or difference from Vin to the ref pin, use an input resistor <10kΩ to provide Iref.

9.2.2.2.2 Output Voltage and Logic Input Level

For the TLA431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} & V_{IL}.

As seen in 図 9-4, TLA431's output low level voltage in open-loop/comparator mode is approximately 2V, which is typically sufficient for 5V supplied logic. However, 5V does not work for 3.3V & 1.8V supplied logic.To accomodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLA431's output high voltage is equal to V_{SUP} due to TLA431 being open-collector. If V_{SUP} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accomadate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 & R2 in 図 9-3) is much greater than R_{SUP} to not interfere with TLA431's ability to pull close to V_{SUP} when turning off.

9.2.2.2.2.1 Input Resistance

TLA431 requires an input resistance in this application to source the reference current (I_{REF}) needed from this device to be in the proper operating regions while turing on. The actual voltage seen at the ref pin is $V_{REF}=V_{IN}-I_{REF}*R_{IN}$. Since I_{REF} can be as high as 4µA, the recommendation is to use a resistance small enough that mitigate the error that I_{REF} creates from V_{IN}.

9.2.2.3 Application Curve

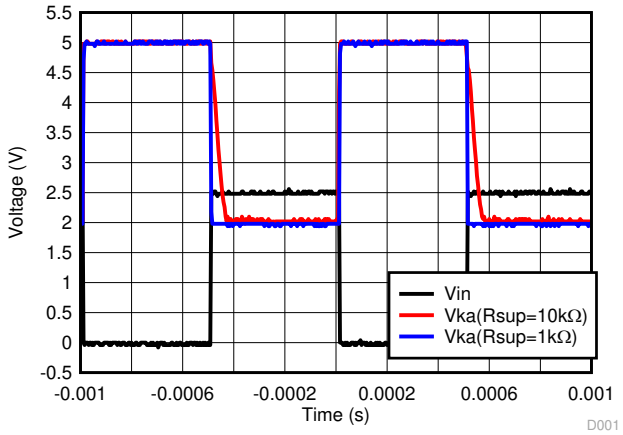
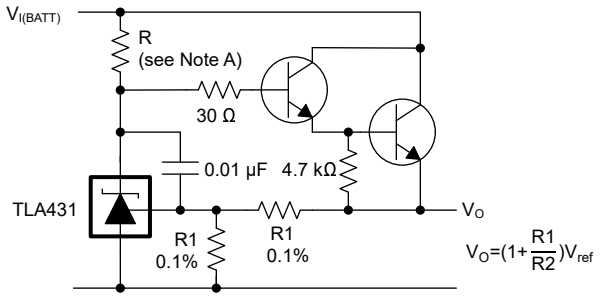


図 9-4. Output Response With Various Cathode Currents

9.3 System Examples



A. R is designed to provide cathode current ≥0.2mA to the TLA431 at minimum $V_{(BATT)}$.

図 9-5. Precision High-Current Series Regulator

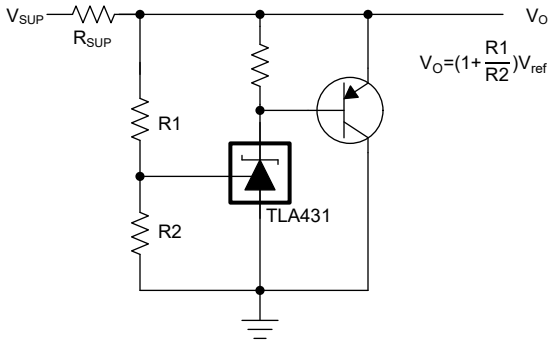
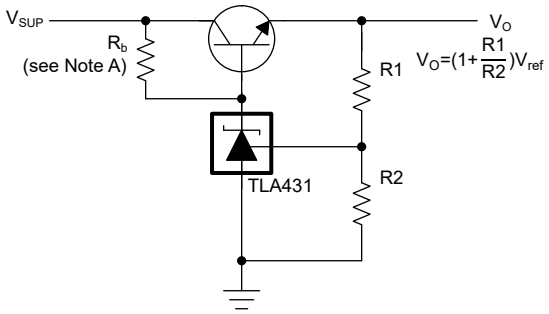
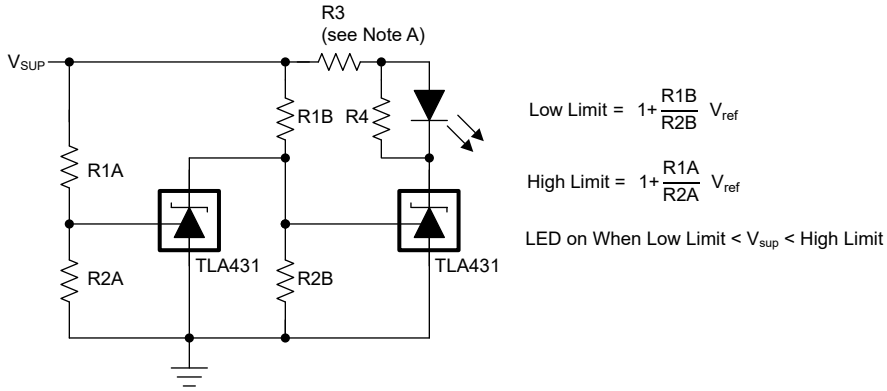


図 9-6. High-Current Shunt Regulator



A. R_b is designed to provide cathode current ≥0.2mA to the TLA431.

図 9-7. Efficient Precision Regulator



A. Select R3 and R4 to provide the desired LED intensity and cathode current ≥0.2mA to the TLA431 at the available V_{SUP}.

図 9-8. Voltage Monitor

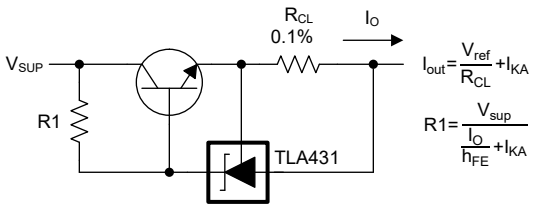


図 9-9. Precision Current Limiter

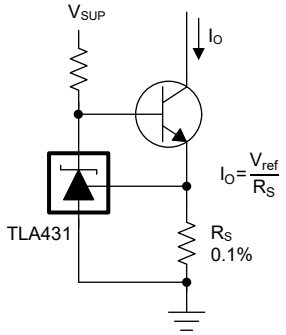


図 9-10. Precision Constant-Current Sink

9.4 Power Supply Recommendations

When using TLA431 as a Linear Regulator to supply a load, designers typically use a bypass capacitor on the output/cathode pin. The TLA431 is stable with all capacitive loads.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed the absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

9.5 Layout

9.5.1 Layout Guidelines

Bypass capacitors need to be placed as close to the part as possible to limit ESR. Current-carrying traces need to have widths appropriate for the amount of current the traces are carrying; in the case of the TLA431, the currents are be low.

9.5.2 Layout Example

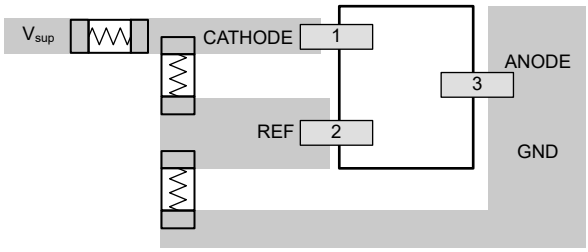
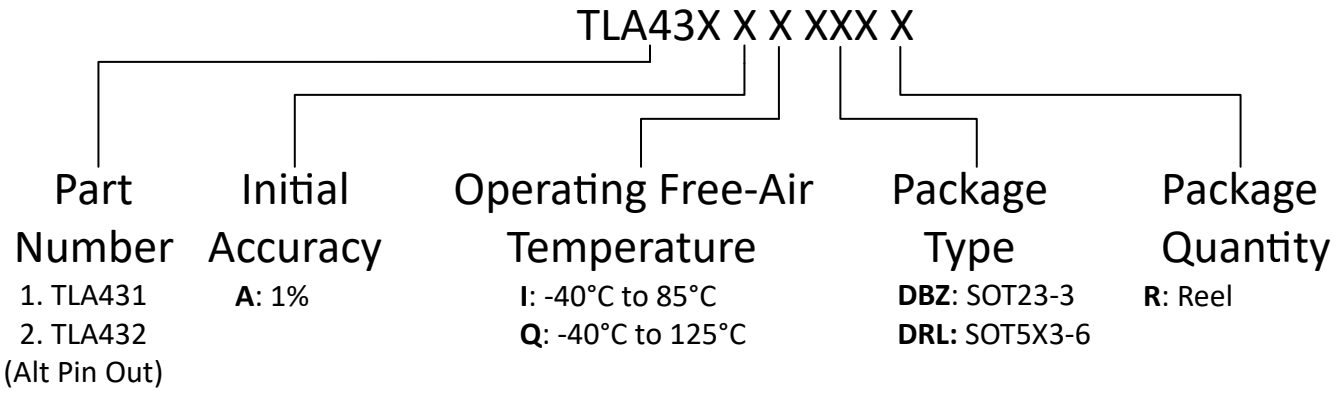


図 9-11. TLA431 DBZ Layout Example

10 Device and Documentation Support

10.1 Device Nomenclature

TI assigns suffixes and prefixes to differentiate all the combinations of the TLA43x family. The Eco Plan designator is a legacy designator that was used to differentiate Pb-free and Green devices. More details and possible orderable combinations are located on the Package Option Addendum in Mechanical, Packaging, and Orderable Information.



10.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLA431	Click here	Click here	Click here	Click here	Click here
TLA432	Click here	Click here	Click here	Click here	Click here

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2024) to Revision A (October 2024)	Page
• 量産データのリリース	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLA431AIDBZR	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
PTLA431AIDBZR.A	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
PTLA431AQDBZR	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLA431AQDBZR.A	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLA432AIDBZR	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
PTLA432AIDBZR.A	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
PTLA432AQDBZR	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLA432AQDBZR.A	Active	Preproduction	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLA431AIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3KVF
TLA431AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3KVF
TLA431AIDBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KVF
TLA431AQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KWF
TLA431AQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KWF
TLA432AIDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3KXF
TLA432AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3KXF
TLA432AIDBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KXF
TLA432AQDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KZF
TLA432AQDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KZF
TLA432AQDBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3KZF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

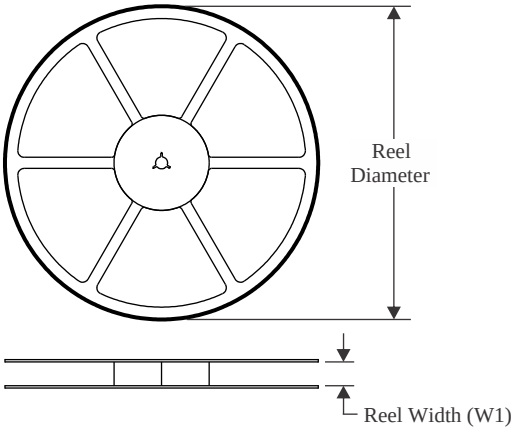
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

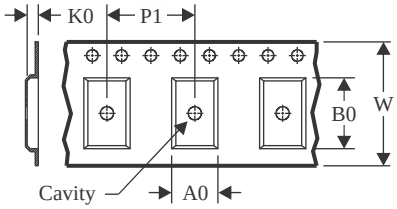
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

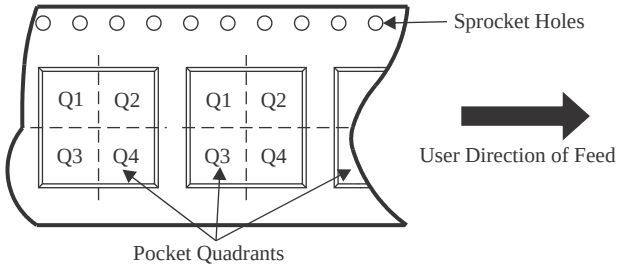


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

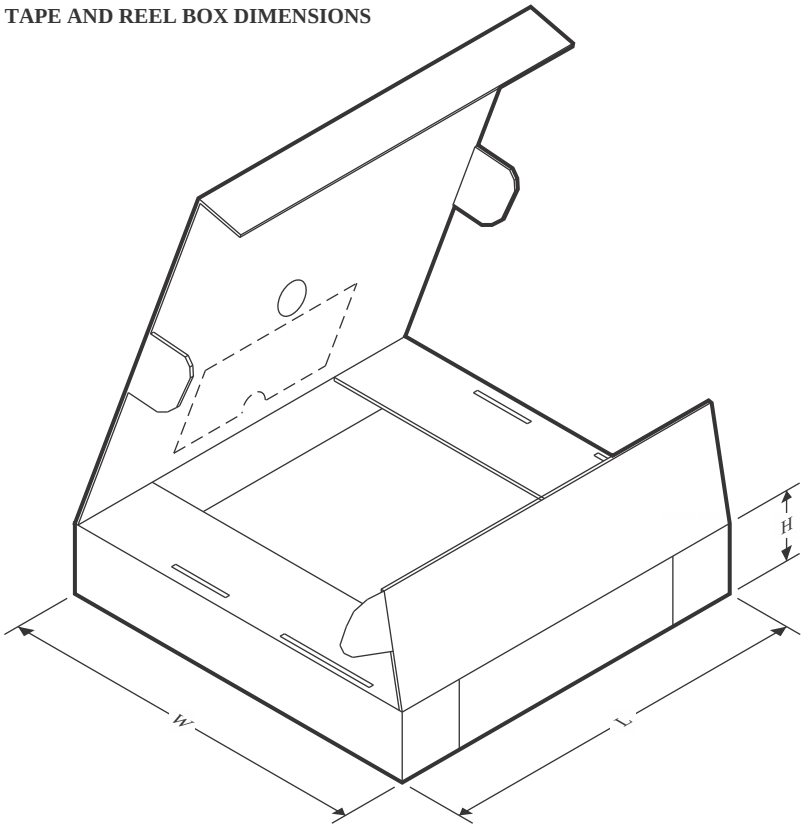
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLA431AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLA431AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLA432AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLA432AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

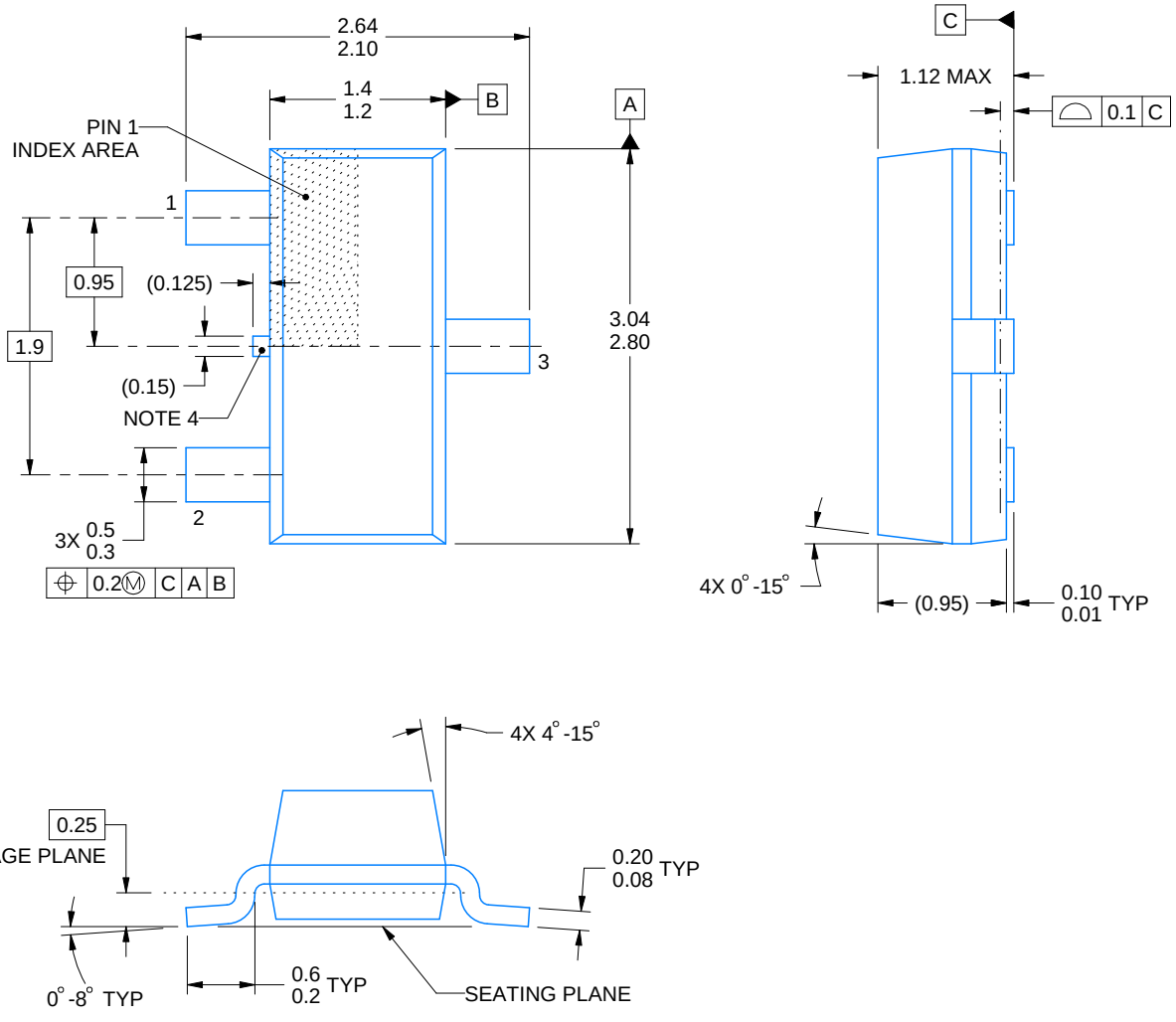
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLA431AIDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLA431AQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLA432AIDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLA432AQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

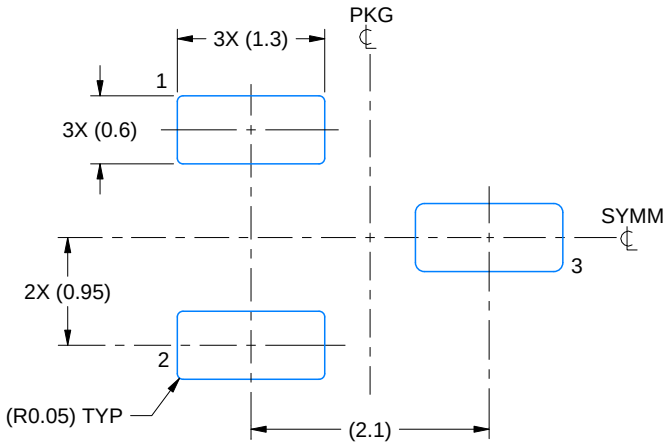
SMALL OUTLINE TRANSISTOR



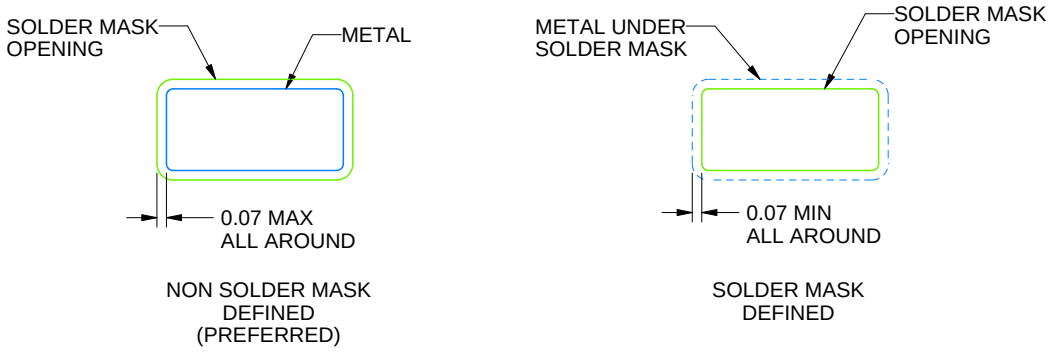
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

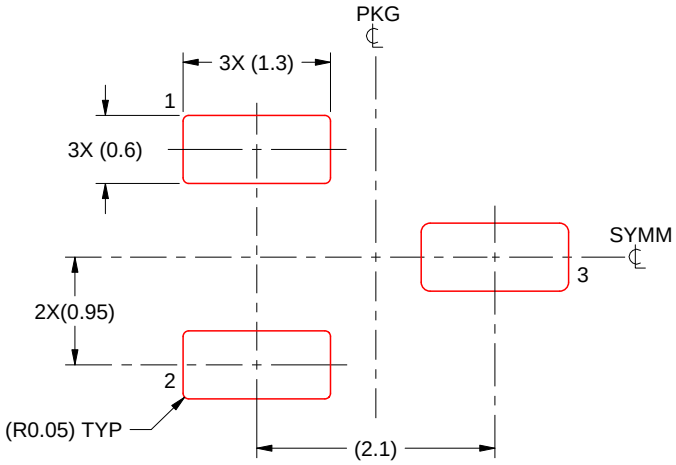


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265