TLA202x コスト最適化された超小型、12ビット、システム・モニタリングADC

1 特長

- 業界で最も低コストの12ビット、デルタ-シグマADC
- 超小型のX2QFNパッケージ: 2mm×1.5mm
- 高集積:
  - 4つのシングル・エンド入力または2つの差動入力により、TLA2024は業界で最もチャネル密度の高いADC (1チャネルあたり0.75mm²)
  - PGA (TLA2022 and TLA2024のみ)
  - 基準電圧
  - 発振器
- 低い消費電流: 150µA
- 広い電源電圧範囲: 2V～5.5V
- データ・レートをプログラム可能: 128SPS～3.3kSPS
- I²C™互換のインターフェイス:
  - 標準モードとファースト・モードをサポート
  - 3つのI²Cアドレスをピン選択可能
- 動作温度範囲: -40℃～+85℃

2 アプリケーション

- パーソナル・エレクトロニクス:
  - TV、タブレット、携帯電話
  - ウェアラブル
  - ドローン、玩具
- 家電機器および調理器具
- ビルディング・オートメーション:
  - HVAC、煙感知器
- バッテリの電圧と電流の監視
- 温度センシング
- バッテリ駆動の携帯用計測機器

3 概要

TLA2021, TLA2022, and TLA2024デバイス(TLA202x)は使いやすい低消費電力の12ビット、デルタ-シグマ(ΔΣ)アナログ/デジタル・コンバータ(ADC)で、電源やバッテリ電圧の監視、電流センシング、温度測定など、各種のシステム監視用途を対象としています。TLA2021およびTLA2022はシングル・チャネルADCで、TLA2024は2つの差動または4つのシングル・エンド入力測定オプションを持つ柔軟な入力マルチプレクサ(MUX)を搭載しており、どれも超小型のリードレス10ピンX2QFNパッケージで供給されます。

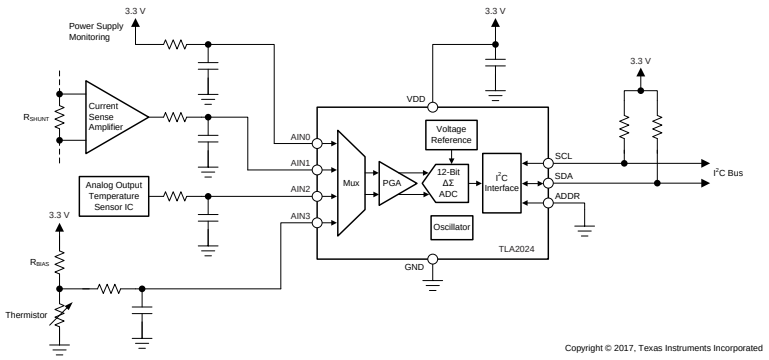
TLA202xには基準電圧および発振器が内蔵されています。さらに、TLA2022 and TLA2024にはプログラム可能なゲイン・アンプ(PGA)が内蔵され、入力を±256mV～±6.144Vの範囲で選択でき、大きな信号から小さな信号まで測定できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLA2021	X2QFN (10)	1.50mm×2.00mm
TLA2022		
TLA2024		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

システム監視アプリケーションの例



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年11月	*	初版

5 概要（続き）

TLA202xはI²C互換のインターフェイスを使用して通信を行い、連続またはシングル・ショットの変換モードで動作します。これらのデバイスは、シングル・ショットの変換モードでは1回の変換後に自動的に電源がオフになり、アイドル期間は消費電力が大幅に低減します。

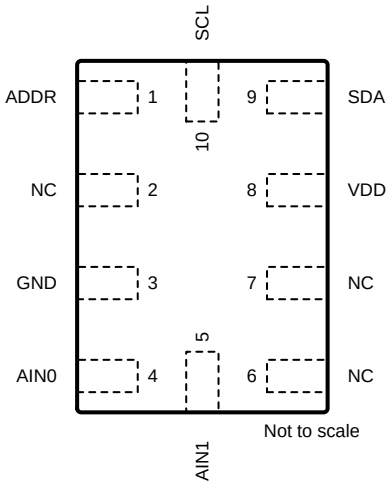
これらの機能すべてと、動作電源電圧範囲が広いことから、TLA202xは省電力と省スペースが要求されるシステム監視アプリケーションに適しています。

6 Device Comparison Table

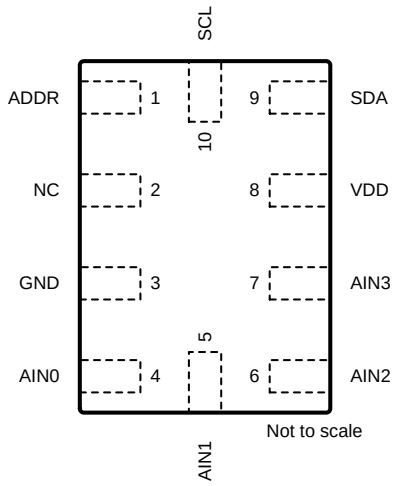
DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS, DIFFERENTIAL (Single-Ended)	PGA	INTERFACE
TLA2021	12	3300	1 (1)	No	I^2C
TLA2022	12	3300	1 (1)	Yes	I^2C
TLA2024	12	3300	2 (4)	Yes	I^2C

7 Pin Configuration and Functions

TLA2021 and TLA2022 RUG Package
10-Pin X2QFN
Top View



TLA2024 RUG Package
10-Pin X2QFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TLA2021, TLA2022	TLA2024		
ADDR	1	1	Digital input	I^2C slave address select pin. See the *I2C Address Selection* section for details.
AIN0	4	4	Analog input	Analog input 0 (1)
AIN1	5	5	Analog input	Analog input 1 (1)
AIN2	—	6	Analog input	Analog input 2 (1)
AIN3	—	7	Analog input	Analog input 3 (1)
GND	3	3	Supply	Ground
NC	2, 6, 7	2	—	No connect; always leave floating
SCL	10	10	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
SDA	9	9	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.
VDD	8	8	Supply	Power supply. Connect a 0.1-µF, power-supply decoupling capacitor to GND.

(1) Float unused analog inputs, or tie unused analog inputs to GND.

8 Specifications

8.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	
Digital input voltage	SDA, SCL, ADDR	GND – 0.3	7	
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J	–40	125	°C
	Storage, T_{stg}	–60	125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
	VDD to GND	2		5.5	V
ANALOG INPUTS(1)					
FSR	Full-scale input voltage range(2) ($V_{IN} = V_{AINP} – V_{AINN}$)	±0.256		±6.144	V
$V_{(AINx)}$	Absolute input voltage	GND		VDD	V
DIGITAL INPUTS					
	Digital input voltage	GND		5.5	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		85	°C

(1) AIN_P and AIN_N denote the selected positive and negative inputs. On the TLA2024, AINx denotes one of the four available analog inputs.
(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device. See the *Full-Scale Range (FSR) and LSB Size* section more information.

8.4 Thermal Information

THERMAL METRIC(1)		TLA202x RUG (X2QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	245.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	172.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	170.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +85°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 3.3 V, data rate = 128 SPS, and FSR = ±2.048 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Common-mode input impedance	FSR = ±6.144 V(1)		10		MΩ
		FSR = ±4.096 V(1), FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V(1)		22		MΩ
		FSR = ±4.096 V(1)		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, ±0.256 V		710		kΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		12			Bits
DR	Data rate		128, 250, 490, 920, 1600, 2400, 3300			SPS
	Data rate variation	All data rates	–10%		10%	
INL	Integral nonlinearity(2)			1		LSB
	Offset error			±1		LSB
	Offset drift			0.01		LSB/°C
	Gain error(3)			0.05%		
	Gain drift(3)			10		ppm/°C
PSRR	Power-supply rejection ratio			85		dB
CMRR	Common-mode rejection ratio			90		dB
DIGITAL INPUT/OUTPUT						
V_{IL}	Logic input level, low		GND		0.3 VDD	V
V_{IH}	Logic input level, high		0.7 VDD		5.5	V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	GND	0.15	0.4	V
	Input leakage current	GND < $V_{Digital\ Input}$ < VDD	–10		10	µA
POWER SUPPLY						
I_{VDD}	Supply current	Power-down		0.5		µA
		Operating		150		
P_D	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device. See the *Full-Scale Range (FSR) and LSB Size* section for more information.
(2) Best-fit INL; covers 99% of full-scale.
(3) Includes all errors from onboard PGA and voltage reference.

8.6 I²C Timing Requirements

over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
STANDARD-MODE				
f_{SCL}	SCL clock frequency	10	100	kHz
t_{LOW}	Pulse duration, SCL low	4.7		µs
t_{HIGH}	Pulse duration, SCL high	4.0		µs
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	4		µs
$t_{SU;STA}$	Setup time, repeated START condition	4.7		µs
$t_{HD;DAT}$	Hold time, data	0		µs
$t_{SU;DAT}$	Setup time, data	250		ns
t_r	Rise time, SCL, SDA		1000	ns
t_f	Fall time, SCL, SDA		250	ns
$t_{SU;STO}$	Setup time, STOP condition	4.0		µs
t_{BUF}	Bus free time, between STOP and START condition	4.7		µs
$t_{VD;DAT}$	Valid time, data		3.45	µs
$t_{VD;ACK}$	Valid time, acknowledge		3.45	µs
FAST-MODE				
f_{SCL}	SCL clock frequency	10	400	kHz
t_{LOW}	Pulse duration, SCL low	1.3		µs
t_{HIGH}	Pulse duration, SCL high	0.6		µs
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	0.6		µs
$t_{SU;STA}$	Setup time, repeated START condition	0.6		µs
$t_{HD;DAT}$	Hold time, data	0		µs
$t_{SU;DAT}$	Setup time, data	100		ns
t_r	Rise time, SCL, SDA	20	300	ns
t_f	Fall time, SCL, SDA		300	ns
$t_{SU;STO}$	Setup time, STOP condition	0.6		µs
t_{BUF}	Bus free time, between STOP and START condition	1.3		µs
$t_{VD;DAT}$	Valid time, data		0.9	µs
$t_{VD;ACK}$	Valid time, acknowledge		0.9	µs

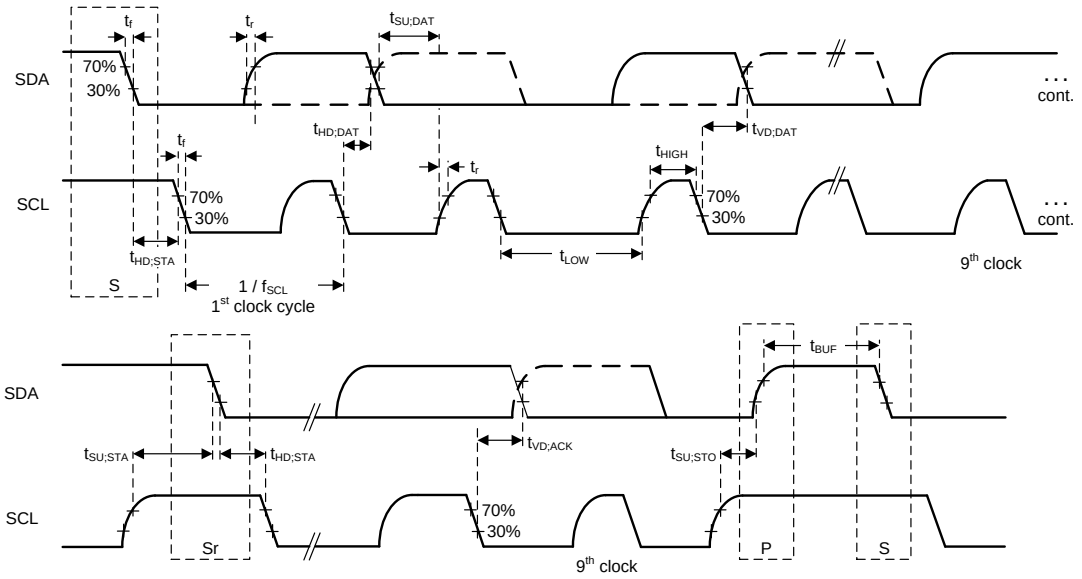


図 1. I²C Timing Requirements

8.7 Typical Characteristics

at FSR = ±2.048 V and DR = 128 SPS (unless otherwise noted)

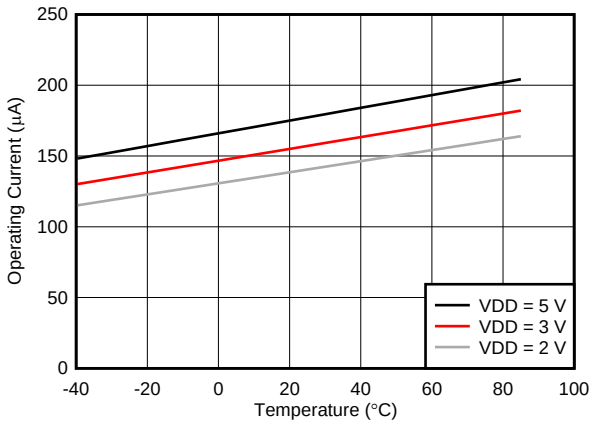


図 2. Operating Current vs Temperature

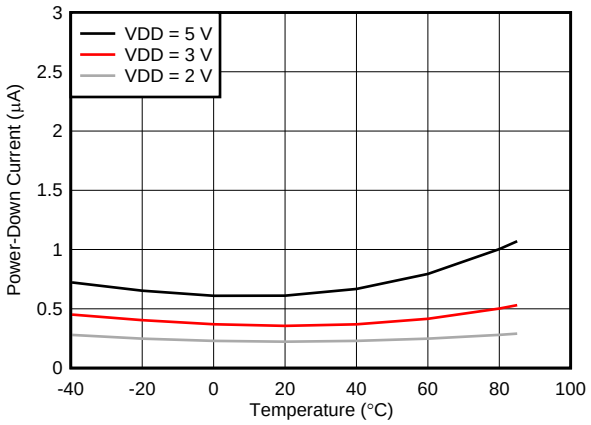


図 3. Power-Down Current vs Temperature

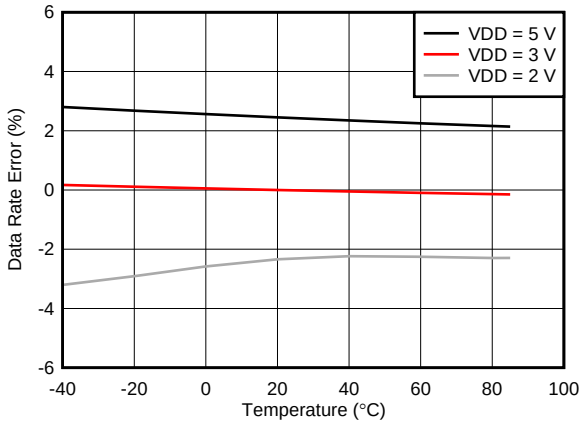


図 4. Data Rate vs Temperature

9 Detailed Description

9.1 Overview

The TLA202x are a family of very small, low-power, 12-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The TLA202x consist of a ΔΣ ADC core with an internal voltage reference, a clock oscillator, and an I^2C interface. The TLA2022 and TLA2024 also integrate a programmable gain amplifier (PGA). 図 5, 図 6, and 図 7 show the functional block diagrams of the TLA2024, TLA2022, and TLA2021, respectively.

The TLA202x ADC core measures a differential signal, V_{IN}, that is the difference of V_{AINP} and V_{AINN}. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation of any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The TLA202x have two available conversion modes: single-shot and continuous-conversion. In single-shot conversion mode, the ADC performs one conversion of the input signal upon request, stores the conversion value to an internal conversion register, and then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is complete. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

9.2 Functional Block Diagrams

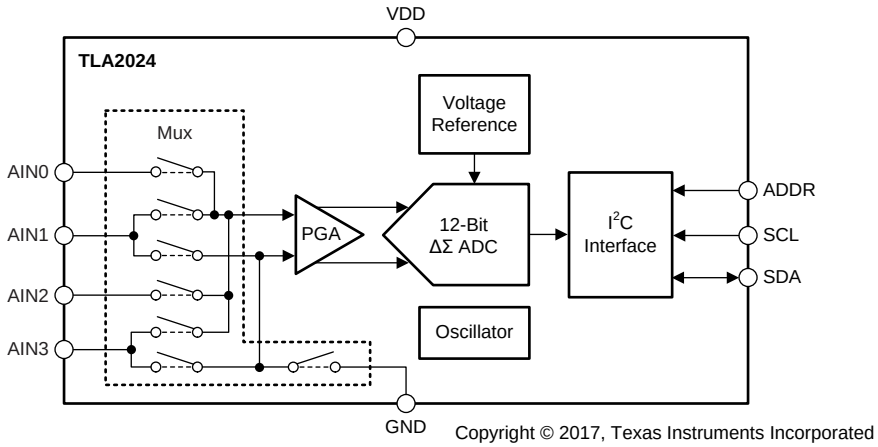


図 5. TLA2024 Block Diagram

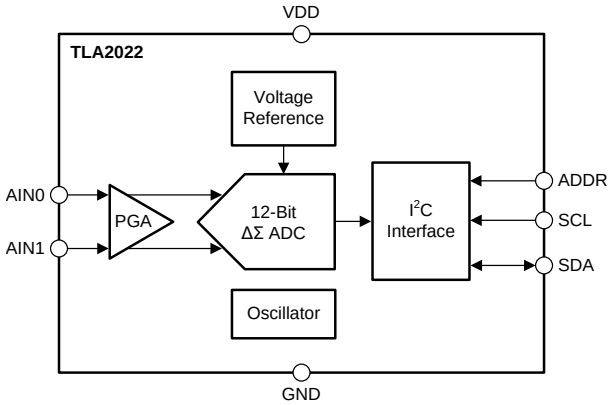


図 6. TLA2022 Block Diagram

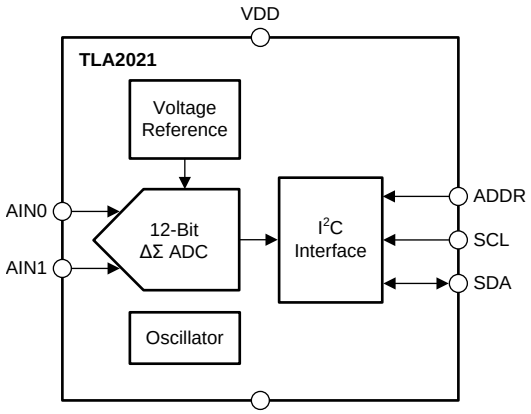


図 7. TLA2021 Block Diagram

9.3 Feature Description

9.3.1 Multiplexer

図 8 shows that the TLA2024 contains an analog input multiplexer (MUX). Four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the *configuration register*. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

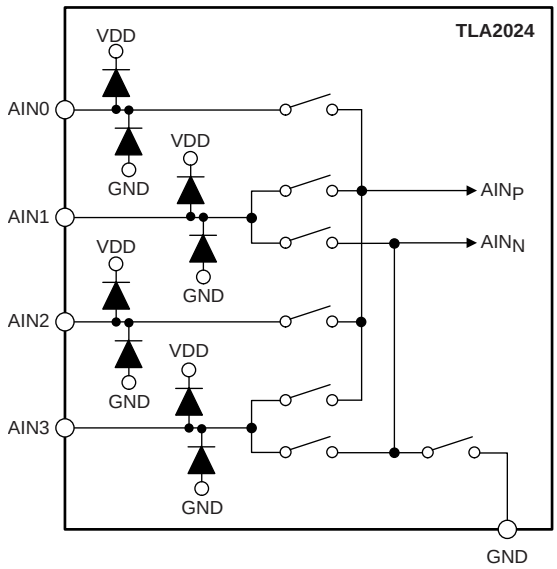


図 8. Input Multiplexer

The TLA2021 and TLA2022 do not have an input multiplexer and can either measure one differential signal or one single-ended signal. For single-ended measurements, connect the AIN1 pin to GND externally. In subsequent sections of this data sheet, AIN_P refers to AIN0 and AIN_N refers to AIN1 for the TLA2021 and TLA2022.

Electrostatic discharge (ESD) diodes connected to VDD and GND protect the TLA202x analog inputs. Keep the absolute voltage on any input within the range shown in 式 1 to prevent the ESD diodes from turning on.

$$GND - 0.3\ V < V_{(AINX)} < VDD + 0.3\ V \quad (1)$$

If the voltages on the analog input pins can potentially violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Feature Description (continued)

9.3.2 Analog Inputs

The TLA202x use a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The frequency at which the input signal is sampled is referred to as the *sampling frequency* or the *modulator frequency* (f_{MOD}). The TLA202x have a 1-MHz internal oscillator that is further divided by a factor of 4 to generate f_{MOD} at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. 図 9 shows this structure. The capacitor values set the resistance and switching rate. 図 10 shows the timing for the switches in 図 9. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to V_{AINP}, C_{A2} to V_{AINN}, and C_B to ($V_{AINP} – V_{AINN}$). During the discharge phase, S_1 is first opened and then S_2 is closed. C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the TLA202x analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

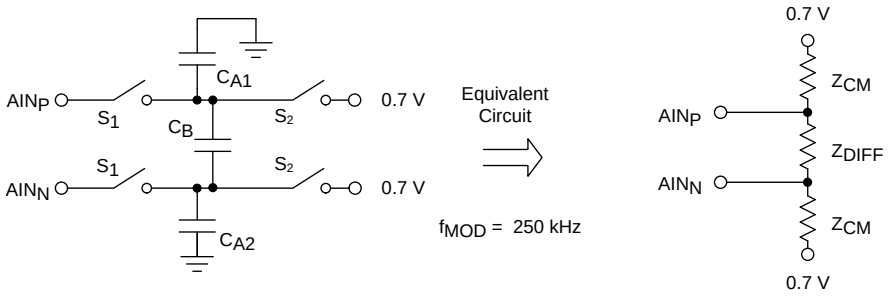


図 9. Simplified Analog Input Circuit

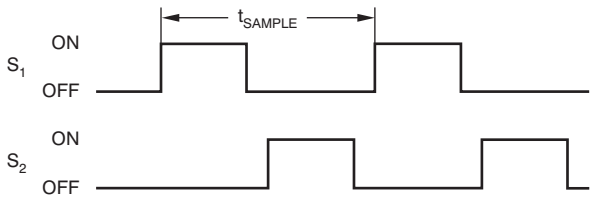


図 10. S_1 and S_2 Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 MΩ for the default full-scale range. In 図 9, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to the AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In 図 9, the differential input impedance is Z_{DIFF}.

Consider the typical value of the input impedance. Unless the input source has a low impedance, the TLA202x input impedance may affect the measurement accuracy. For sources with high-output impedance, buffering may be necessary. Active buffers introduce noise, offset, and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible and can be ignored.

Feature Description (continued)

9.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the ΔΣ ADC of the TLA2022 and TLA2024. The full-scale range is configured by bits PGA[2:0] in the *configuration register* and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V. 表 1 shows the FSR together with the corresponding LSB size. 式 2 shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{12} \quad (2)$$

表 1. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144 V(1)	3 mV
±4.096 V(1)	2 mV
±2.048 V	1 mV
±1.024 V	0.5 mV
±0.512 V	0.25 mV
±0.256 V	0.125 mV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

The FSR of the TLA2021 is fixed at ±2.048 V.

Analog input voltages must never exceed the analog input voltage limits given in the *Absolute Maximum Ratings* table. If a VDD supply voltage greater than 4 V is used, the ±6.144-V full-scale range allows input voltages to extend up to the supply. Although in this case (or whenever the supply voltage is less than the full-scale range) a full-scale ADC output code cannot be obtained. For example, with VDD = 3.3 V and FSR = ±4.096 V, only signals up to V_{IN} = ±3.3 V can be measured. The code range that represents voltages $|V_{IN}| > 3.3$ V is not used in this case.

9.3.4 Voltage Reference

The TLA202x have an integrated voltage reference. An external reference cannot be used with these devices. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics* table.

9.3.5 Oscillator

The TLA202x have an integrated oscillator running at 1 MHz. No external clock can be applied to operate these devices. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

9.3.6 Output Data Rate and Conversion Time

The TLA202x offer programmable output data rates. Use the DR[2:0] bits in the *configuration register* to select output data rates of 128 SPS, 250 SPS, 490 SPS, 920 SPS, 1600 SPS, 2400 SPS, or 3300 SPS.

Conversions in the TLA202x settle within a single cycle, which means the conversion time equals 1 / DR.

9.4 Device Functional Modes

9.4.1 Reset and Power-Up

The TLA202x reset on power-up and set all bits in the *configuration register* to the respective default settings. The TLA202x enter a power-down state after completion of the reset process. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the TLA202x relieves systems with tight power-supply requirements from encountering a surge during power-up.

The TLA202x respond to the I^2C general-call reset command. When the TLA202x receive a general-call reset command (06h), an internal reset is performed as if the device is powered up.

9.4.2 Operating Modes

The TLA202x operate in one of two modes: continuous-conversion or single-shot. The MODE bit in the configuration register selects the respective operating mode.

9.4.2.1 Single-Shot Conversion Mode

When the MODE bit in the configuration register is set to 1, the TLA202x enter a power-down state, and operate in single-shot conversion mode. This power-down state is the default state for the TLA202x when power is first applied. Although powered down, the devices respond to commands. The TLA202x remain in this power-down state until a 1 is written to the operational status (OS) bit in the configuration register. When the OS bit is asserted, the device powers up in approximately 25 µs, resets the OS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the OS bit is set to 1 and the device powers down again. Writing a 1 to the OS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the configuration register.

9.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the TLA202x perform conversions continuously. When a conversion is complete, the TLA202x place the result in the *conversion data register* and immediately begin another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configuration settings start. To switch to single-shot conversion mode, write a 1 to the MODE bit in the configuration register or reset the device.

9.5 Programming

9.5.1 I²C Interface

The TLA202x use an I²C-compatible (inter-integrated circuit) interface for serial communication. I²C is a 2-wire, open-drain communication interface that allows communication of a master device with multiple slave devices on the same bus through the use of device addressing. Each slave device on an I²C bus must have a unique address. Communication on the I²C bus always takes place between two devices: one acting as the master and the other as the slave. Both the master and slave can receive and transmit data, but the slave can only read or write under the direction of the master. The TLA202x always act as I²C slave devices.

An I²C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. Devices on the I²C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors; thus, the bus wires are always high when a device is not driving the lines low. As a result of this configuration, two devices do not conflict. If two devices drive the bus simultaneously, there is no driver contention.

See the *I²C-Bus Specification and User Manual* from NXP Semiconductors™ for more details.

9.5.1.1 I²C Address Selection

The TLA202x have one address pin (ADDR) that configures the I²C address of the device. The ADDR pin can connect to GND, VDD, or SCL (as shown in 表 2), which allows three different addresses to be selected with one pin. At the start of every transaction, that is between the START condition (first falling edge of SDA) and the first falling SCL edge of the address byte, the TLA202x decode its address configuration again.

表 2. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN CONNECTION	SLAVE ADDRESS
GND	1001 000
VDD	1001 001
SCL	1001 011

9.5.1.2 I²C Interface Speed

The TLA202x support I²C interface speeds up to 400 kbit/s. Standard-mode (Sm) with bit rates up to 100 kbit/s, and fast-mode (Fm) with bit rates up to 400 kbit/s are supported. Fast-mode plus (Fm+) and high-speed mode (Hs-mode) are not supported.

9.5.1.3 Serial Clock (SCL) and Serial Data (SDA)

The serial clock (SCL) line is used to clock data in and out of the device. The master always drives the clock line. The TLA202x cannot act as a master and as a result can never drive SCL.

The serial data (SDA) line allows for bidirectional communication between the host (the master) and the TLA202x (the slave). When the master reads from a TLA202x, the TLA202x drives the data line; when the master writes to a TLA202x, the master drives the data line.

Data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the SCL line is low. One clock pulse is generated for each data bit transferred. When in an idle state, the master should hold SCL high.

9.5.1.4 I²C Data Transfer Protocol

図 11 shows the format of the data transfer. The master initiates all transactions with the TLA202x by generating a START (S) condition. A high-to-low transition on the SDA line while SCL is high defines a START condition. The bus is considered to be busy after the START condition.

Following the START condition, the master sends the 7-bit slave address corresponding to the address of the TLA202x that the master wants to communicate with. The master then sends an eighth bit that is a data direction bit (R/$\overline{W}$). An R/$\overline{W}$ bit of 0 indicates a write operation, and an R/$\overline{W}$ bit of 1 indicates a read operation. After the R/$\overline{W}$ bit, the master generates a ninth SCLK pulse and releases the SDA line to allow the TLA202x to acknowledge (ACK) the reception of the slave address by pulling SDA low. In case the device does not recognize the slave address, the TLA202x holds SDA high to indicate a not acknowledge (NACK) signal.

Next follows the data transmission. If the transaction is a read (R/$\overline{W}$ = 1), the TLA202x outputs data on SDA. If the transaction is a write (R/$\overline{W}$ = 0), the host outputs data on SDA. Data are transferred byte-wise, most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be acknowledged (via the ACK bit) by the receiver. If the transaction is a read, the master issues the ACK. If the transaction is a write, the TLA202x issues the ACK.

The master terminates all transactions by generating a STOP (P) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The bus is considered free again t_{BUF} (bus-free time) after the STOP condition.

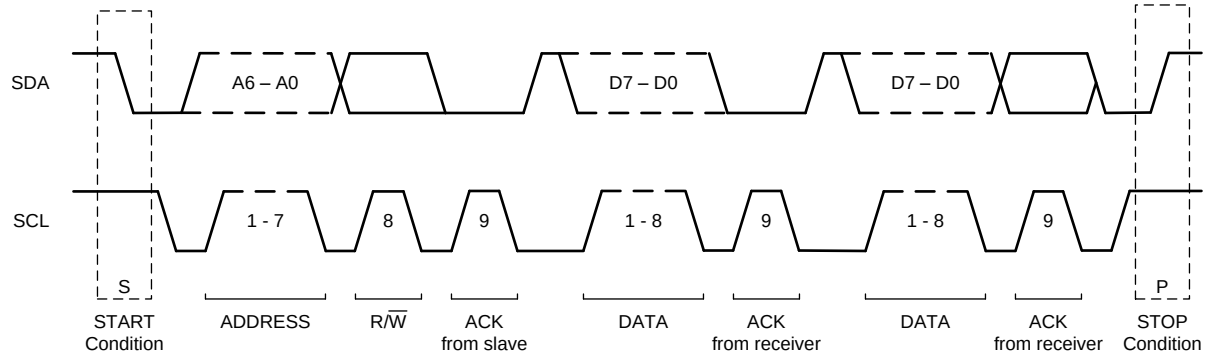


図 11. I²C Data Transfer Format

9.5.1.5 Timeout

The TLA202x offer a I²C timeout feature that can be used to recover communication when a serial interface transmission is interrupted. If the host initiates contact with the TLA202x but subsequently remains idle for 25 ms before completing a command, the TLA202x interface is reset. If the TLA202x interface resets because of a timeout condition, the host must abort the transaction and restart the communication again by issuing a new START condition.

9.5.1.6 I²C General-Call (Software Reset)

The TLA202x respond to the I²C general-call address (0000 000) if the R/$\overline{W}$ bit is 0. The devices acknowledge the general-call address and, if the next byte is 06h, the TLA202x reset the internal registers and enter a power-down state.

9.5.2 Reading and Writing Register Data

The host can read the *conversion data register* from the TLA202x, or read and write the *configuration register* from and to the TLA202x, respectively. The value of the register pointer (RP), which is the first data byte after the slave address of a write transaction (R/$\overline{W}$ = 0), determines the register that is addressed. 表 3 shows the mapping between the register pointer value and the register that is addressed.

Register data are sent with the most significant byte first, followed by the least significant byte. Within each byte, data are transmitted most significant bit first.

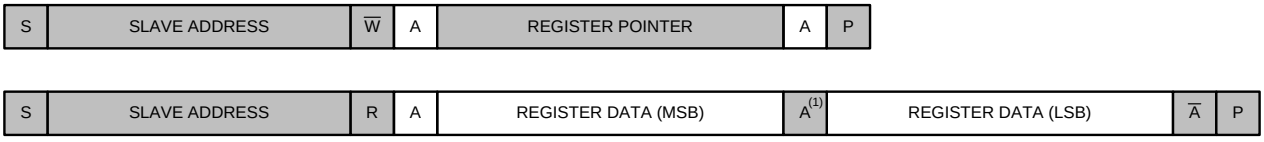
表 3. Register Pointer (RP)

REGISTER POINTER (Hex)	REGISTER
00h	Conversion data register
01h	Configuration register

9.5.2.1 Reading Conversion Data or the Configuration Register

Read the *conversion data register* or *configuration register* as shown in 図 12 by using two I^2C communication frames. The first frame is an I^2C write operation where the R/$\overline{W}$ bit at the end of the slave address is 0 to indicate a write. In this frame, the host sends the register pointer that points to the register to read from. The second frame is an I^2C read operation where the R/$\overline{W}$ bit at the end of the slave address is 1 to indicate a read. The TLA202x transmits the contents of the register in this second I^2C frame. The master can terminate the transmission after any byte by not acknowledging or issuing a START or STOP condition.

When repeatedly reading the same register, the register pointer does not need to be written every time again because the TLA202x store the value of the register pointer until a write operation modifies the value.



(1) The master can terminate the transmission after the first byte by not acknowledging.

図 12. Reading Register Data

9.5.2.2 Writing the Configuration Register

Write the *configuration register* as shown in 図 13 using a single I^2C communication frame. The R/$\overline{W}$ bit at the end of the salve address is 0 to indicate a write. The host first sends the register pointer that points to the configuration register, followed by two bytes that represent the register content to write. The TLA202x acknowledge each received byte.

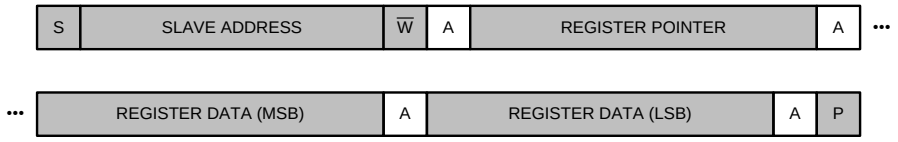


図 13. Writing Register Data

図 14 provides a legend for 図 12 and 図 13.

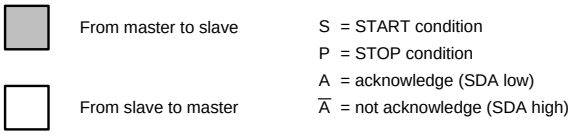


図 14. Legend for the I^2C Sequence Diagrams

9.5.3 Data Format

The TLA202x provide 12 bits of data in binary two's-complement format that is left-justified within the 16-bit data word. A positive full-scale (+FS) input produces an output code of 7FF0h and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. 表 4 summarizes the ideal output codes for different input signals. 図 15 shows code transitions versus input voltage.

表 4. Input Signal Versus Ideal Output Code

INPUT SIGNAL $V_{IN} = (V_{AINP} - V_{AINN})$	IDEAL OUTPUT CODE(1)
≥ +FS ($2^{11} - 1$) / 2^{11}	7FF0h
+FS / 2^{11}	0010h
0	0000h
–FS / 2^{11}	FFF0h
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

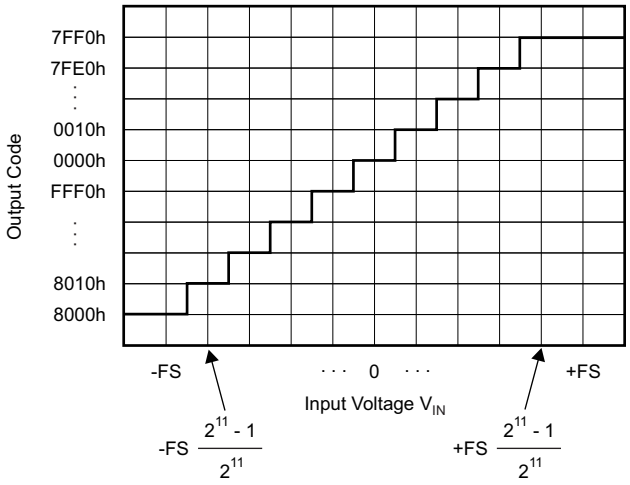


図 15. Code Transition Diagram

注

Single-ended signal measurements, where V_{AINN} = 0 V and V_{AINP} = 0 V to +FS, only use the positive code range from 0000h to 7FF0h. However, because of device offset, the TLA202x can still output negative codes in case V_{AINP} is close to 0 V.

9.6 Register Maps

The TLA202x have two registers that are accessible through the I^{2}C interface using the register pointer (RP). The *conversion data register* contains the result of the last conversion and the *configuration register* changes the TLA202x operating modes and queries the status of the device. 表 5 lists the access codes for the TLA202x.

表 5. TLA202x Access Type Codes

Access Type	Code	Description
R	R	Read
R-W	R/W	Read or write
W	W	Write
-n		Value after reset or the default value

9.6.1 Conversion Data Register (RP = 00h) [reset = 0000h]

The 16-bit conversion data register contains the result of the last conversion in binary two's-complement format. Following power-up, the conversion data register clears to 0, and remains at 0 until the first conversion is complete.

図 16. Conversion Data Register

15	14	13	12	11	10	9	8
D11	D10	D9	D8	D7	D6	D5	D4
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D3	D2	D1	D0	RESERVED			
R-0h	R-0h	R-0h	R-0h	R-0h			

表 6. Conversion Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	Reserved	R	0h	Always reads back 0h

9.6.2 Configuration Register (RP = 01h) [reset = 8583h]

The 16-bit configuration register controls the operating mode, input selection, data rate, and full-scale range.

図 17. Configuration Register

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			RESERVED				
R/W-4h			R/W-03h				

表 7. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OS	R/W	1h	**Operational Status or Single-Shot Conversion Start** This bit determines the operational status of the device. OS can only be written when in a power-down state and has no effect when a conversion is ongoing. When writing: 0 : No effect 1 : Start a single conversion (when in a power-down state) When reading: 0 : The device is currently performing a conversion 1 : The device is not currently performing a conversion (default)
14:12	MUX[2:0]	R/W	0h	**Input Multiplexer Configuration (TLA2024 only)** These bits configure the input multiplexer. These bits serve no function on the TLA2021 and TLA2022 and are always set to 000. 000 : AIN_P = AIN0 and AIN_N = AIN1 (default) 001 : AIN_P = AIN0 and AIN_N = AIN3 010 : AIN_P = AIN1 and AIN_N = AIN3 011 : AIN_P = AIN2 and AIN_N = AIN3 100 : AIN_P = AIN0 and AIN_N = GND 101 : AIN_P = AIN1 and AIN_N = GND 110 : AIN_P = AIN2 and AIN_N = GND 111 : AIN_P = AIN3 and AIN_N = GND
11:9	PGA[2:0]	R/W	2h	**Programmable Gain Amplifier Configuration (TLA2022 and TLA2024 Only)** These bits set the FSR of the programmable gain amplifier. These bits serve no function on the TLA2021 and are always set to 010. 000 : FSR = ±6.144 V(1) 001 : FSR = ±4.096 V(1) 010 : FSR = ±2.048 V (default) 011 : FSR = ±1.024 V 100 : FSR = ±0.512 V 101 : FSR = ±0.256 V 110 : FSR = ±0.256 V 111 : FSR = ±0.256 V
8	MODE	R/W	1h	**Operating Mode** This bit controls the operating mode. 0 : Continuous-conversion mode 1 : Single-shot conversion mode or power-down state (default)
7:5	DR[2:0]	R/W	4h	**Data Rate** These bits control the data rate setting. 000 : DR = 128 SPS 001 : DR = 250 SPS 010 : DR = 490 SPS 011 : DR = 920 SPS 100 : DR = 1600 SPS (default) 101 : DR = 2400 SPS 110 : DR = 3300 SPS 111 : DR = 3300 SPS
4:0	Reserved	R/W	03h	Always write 03h

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The following sections give example circuits and suggestions for using the TLA202x in various applications.

10.1.1 Basic Interface Connections

図 18 shows the principle I²C connections for the TLA202x.

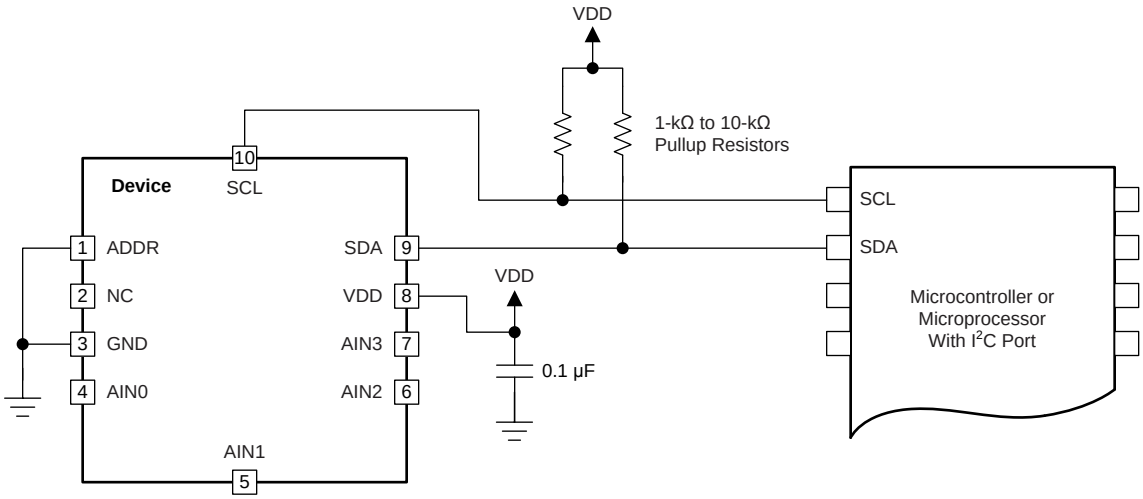


図 18. Typical Interface Connections of the TLA202x

The TLA202x interface directly to standard-mode or fast-mode I²C controllers. Any microcontroller I²C peripheral, including master-only and single-master I²C peripherals, operates with the TLA202x. The TLA202x do not perform clock-stretching (that is, the devices never pull the clock line low), so this function does not need to be provided for unless other clock-stretching devices are present on the same I²C bus.

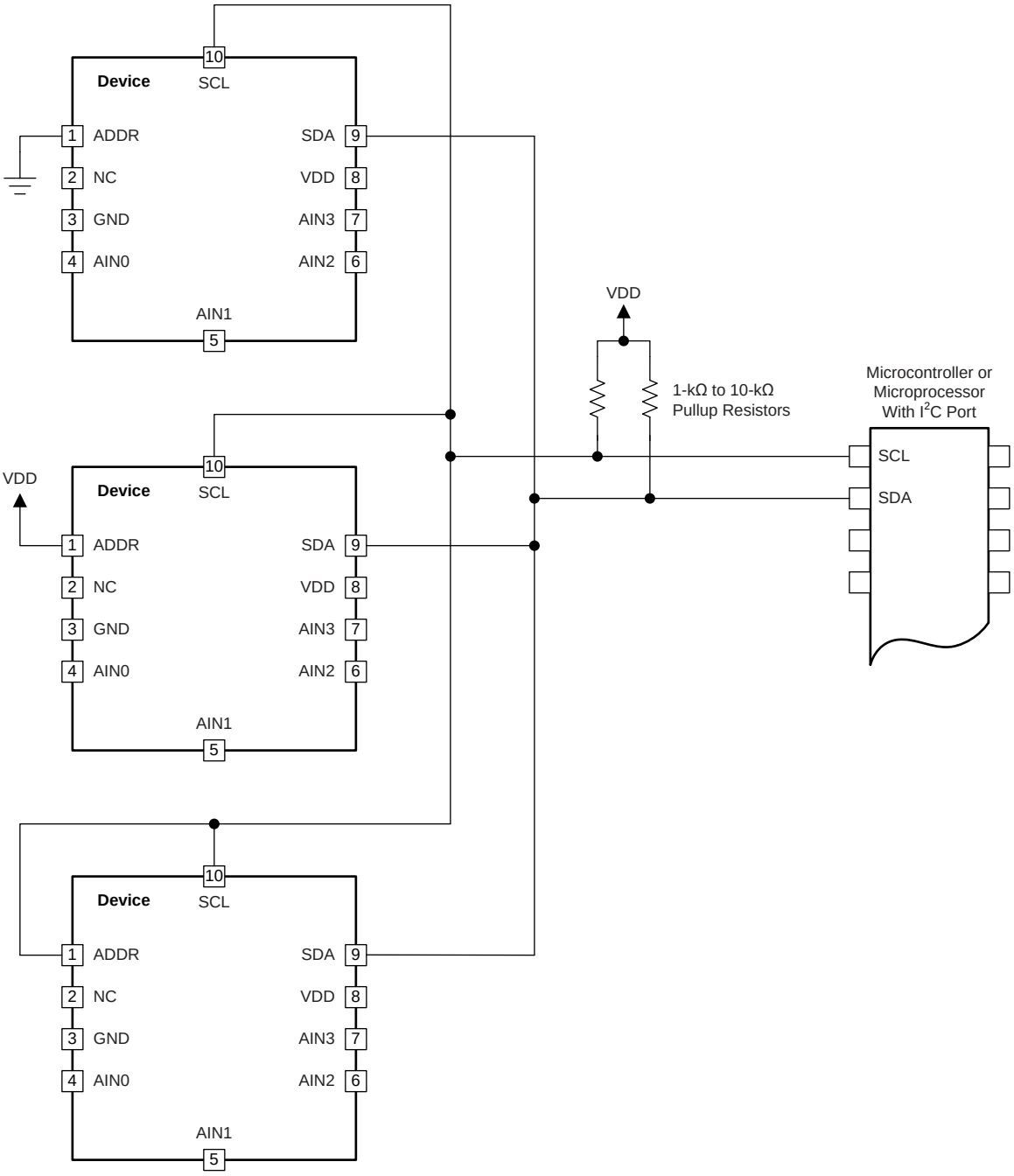
Pullup resistors are required on both the SDA and SCL lines because I²C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors yield lower power consumption when the bus lines are pulled low, but increase the transition times on the bus, which limits the bus speed. Lower-value resistors allow higher interface speeds, but at the expense of higher power consumption when the bus lines are pulled low. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. Do not use resistors that are too small because the bus drivers may be unable to pull the bus lines low.

See the *I²C-Bus Specification and User Manual* from NXP Semiconductors for more details on pullup resistor sizing.

Application Information (continued)

10.1.2 Connecting Multiple Devices

Up to three TLA202x devices can be connected to a single I^2C bus by using different address pin configurations for each device. Use the address pin to set the TLA202x to one of three different I^2C addresses. 図 19 shows an example with three TLA202x devices on the same I^2C bus. One set of pullup resistors is required per bus line. The pullup resistor values may need to decrease to compensate for the additional bus capacitance presented by multiple devices and increased line length.



NOTE: The TLA202x power and input connections are omitted for clarity. The ADDR pin selects the I^2C address.

図 19. Connecting Multiple TLA202x Devices

Application Information (continued)

10.1.3 Single-Ended Signal Measurements

The TLA2021 and TLA2022 can measure one single-ended signal, and the TLA2024 up to four single-ended signals. To measure single-ended signals with the TLA2021 and TLA2022, connect AIN1 to GND externally. The TLA2024 measures single-ended signals by properly configuring the MUX[2:0] bits (settings 100 to 111) in the configuration register. 図 20 shows a single-ended connection scheme for the TLA2024 highlighted in red (a differential connection scheme is shown in green). The single-ended signal range is from 0 V up to the positive supply or +FS (whichever is lower). Negative voltages cannot be applied to these devices because the TLA202x can only accept positive voltages with respect to ground. Only the code range from 0000h to 7FF0h (or a subset thereof in case +FS > VDD) is used in this case.

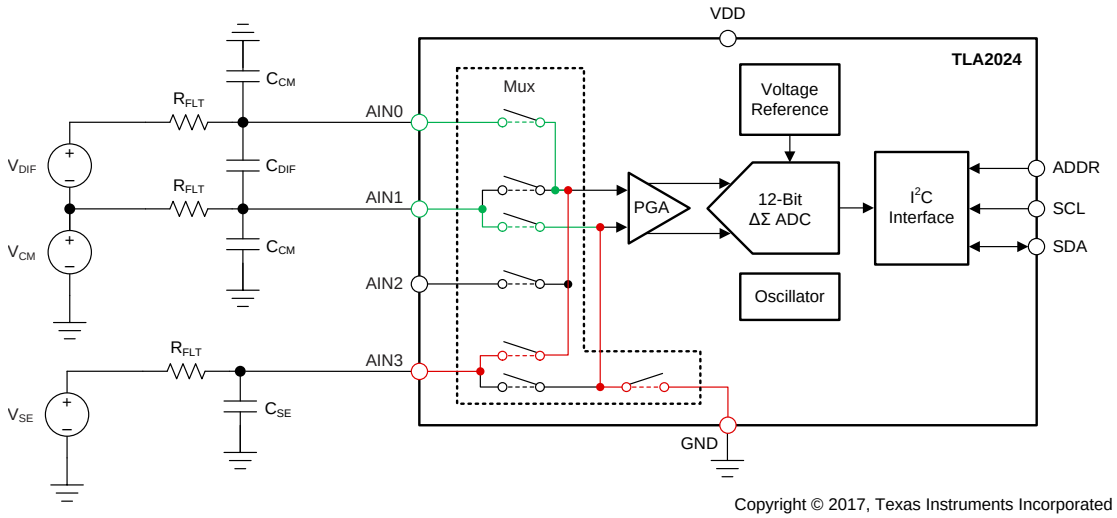


図 20. Filter Implementation for Single-Ended and Differential Signal Measurements

The TLA2024 also allows AIN3 to serve as a common point for measurements by appropriately setting the MUX[2:0] bits. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the usable voltage and code range, respectively, is increased over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD. Assume the following settings for example: VDD = 5 V, FSR = ±2.048 V, AIN_P = AIN0, and AIN_N = AIN3 = 2.5 V. In this case, the voltage at AIN0 can swing from $V_{(AIN0)}$ = 2.5 V – 2.048 V to 2.5 V + 2.048 V using the entire full-scale range.

10.1.4 Analog Input Filtering

Analog input filtering serves two purposes:

1. Limits the effect of aliasing during the ADC sampling process
2. Attenuates unwanted noise components outside the bandwidth of interest

In most cases, a first-order resistor capacitor (RC) filter is sufficient to completely eliminate aliasing or to reduce the effect of aliasing to a level within the noise floor of the sensor. A good starting point for a system design with the TLA202x is to use a differential RC filter with a cutoff frequency set somewhere between the selected output data rate and 25 kHz. Make the series resistor values as small as possible to reduce voltage drops across the resistors caused by the device input currents to a minimum. However, the resistors should be large enough to limit the current into the analog inputs to less than 10 mA in the event of an overvoltage. Then choose the differential capacitor value to achieve the target filter cutoff frequency. Common-mode filter capacitors to GND can be added as well, but should always be at least ten times smaller than the differential filter capacitor.

図 20 shows an example of filtering a differential signal (AIN0, AIN1), and a single-ended signal (AIN3). 式 3 and 式 4 show how to calculate the filter cutoff frequencies (f_{CO}) in the differential and single-ended cases, respectively.

$$f_{CO\ DIF} = 1 / (2\pi \cdot 2 \cdot R_{FLT} \cdot C_{DIF}) \quad (3)$$

$$f_{CO\ SE} = 1 / (2\pi \cdot R_{FLT} \cdot C_{SE}) \quad (4)$$

Application Information (continued)

10.1.5 Duty Cycling To Reduce Power Consumption

For applications where power consumption is critical, the TLA202x support duty cycling that yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an TLA202x in power-down state with a data rate set to 3300 SPS can be operated by a microcontroller that instructs a single-shot conversion every 7.81 ms (128 SPS). A conversion at 3300 SPS requires approximately 0.3 ms, so the TLA202x enters power-down state for the remaining 7.51 ms. In this configuration, the TLA202x consume approximately 1/25th the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is arbitrary and is defined by the master controller.

10.1.6 I^2C Communication Sequence Example

This section provides an example of an I^2C communication sequence between a microcontroller (the master) and a TLA2024 (the slave) configured with a slave address of 1001 000 to start a single-shot conversion and subsequently read the conversion result.

1. Write the configuration register as shown in 図 21 to configure the device (for example, write MUX[2:0] = 000, PGA[2:0] = 010, MODE = 1, and DR[2:0] = 110) and start a single-shot conversion (OS = 1):

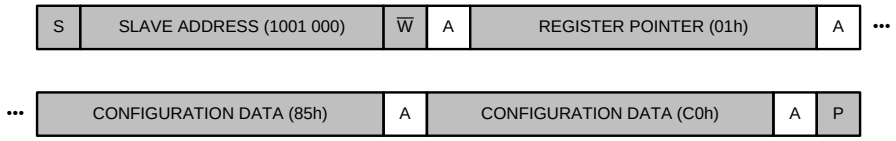


図 21. Write the Configuration Register

2. Wait at least t = 1 / DR ± 10% for the conversion to complete.

   Alternatively, poll the OS bit for a 1 as shown in 図 22 to determine when the conversion result is ready for retrieval. This option does not work in continuous-conversion mode because the OS bit always reads 0.

図 22. Read the Configuration Register to Check for OS = 1

3. Then, as shown in 図 23, read the conversion data register:

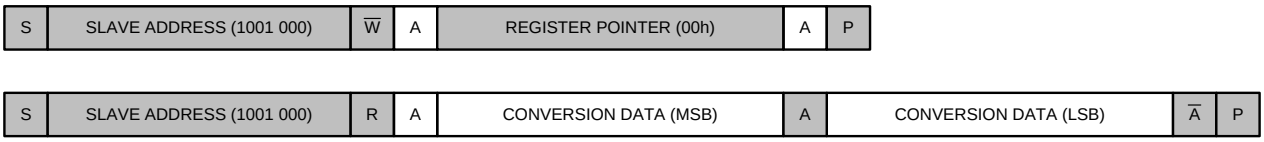


図 23. Read the Conversion Data Register

4. Start a new single-shot conversion by writing a 1 to the OS bit in the configuration register.

   To save time, a new conversion can also be started (step 4) before reading the conversion result (step 3). 図 24 lists a legend for 図 21 to 図 23.

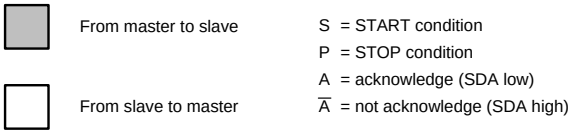


図 24. Legend for the I^2C Sequence Diagrams

10.2 Typical Application

This application example describes how to use the TLA2024 to monitor two different supply voltage rails in a system. 図 25 shows a typical implementation for monitoring two supply voltage rails.

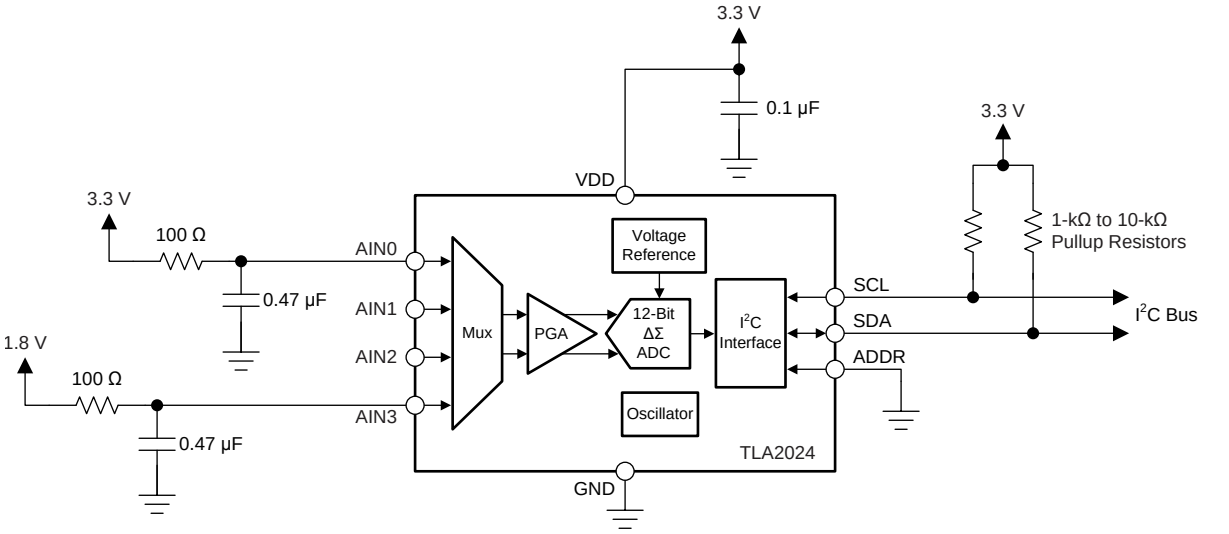


図 25. Monitoring Two Supply Voltage Rails Using the TLA2024

10.2.1 Design Requirements

表 8 lists the design requirements for this application.

表 8. Design Requirements

DESIGN PARAMETER	VALUE
Device supply voltage	3.3 V
Voltage rails to monitor	1.8 V, 3.3 V
Measurement accuracy	±0.5%
Update rate	1 ms per rail

10.2.2 Detailed Design Procedure

The analog inputs, AIN0 and AIN3, connect directly to the supply voltage rails that are monitored through RC filter resistors. Small filter resistor values of 100 Ω are chosen to reduce voltage drops, and therefore offset errors, caused by the input currents of the TLA2024 to a minimum. Filter capacitors of 0.47 µF are chosen to set the filter cutoff frequencies at 3.39 kHz. In order to get one reading from each of the two supplies within 2 ms, a data rate of 2400 SPS is selected. The device is set up for single-ended measurements using MUX[2:0] settings 100 and 101. A FSR = ±4.096 V is selected to measure the 3.3-V rail. The same FSR can also be used to measure the 1.8-V rail or the FSR can be set to FSR = ±2.048 V.

10.2.3 Application Curve

The measurement results in 図 26 show that the two supplies can be measured with ±0.5% accuracy over the complete operating ambient temperature range without any offset or gain calibration.

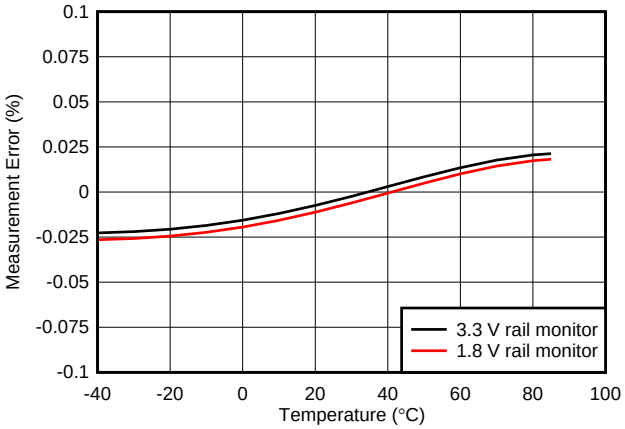


図 26. Measurement Error vs Temperature

11 Power Supply Recommendations

The device requires a single unipolar supply (VDD) to power the analog and digital circuitry of the device.

11.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in 図 27, VDD must be decoupled with at least a 0.1-µF capacitor to GND. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the device is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoid using vias to connect the capacitors to the device pins for better noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

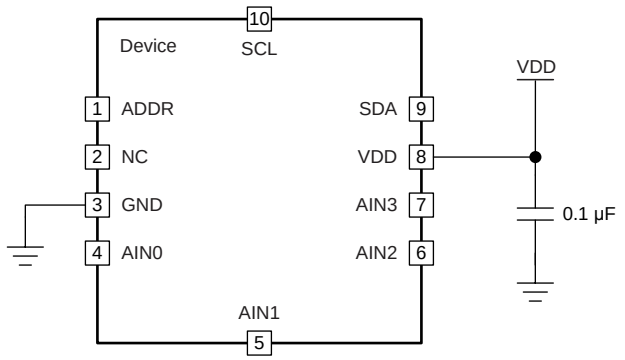


図 27. TLA202x Power-Supply Decoupling

12 Layout

12.1 Layout Guidelines

Employ best design practices when laying out a printed-circuit board (PCB) for both analog and digital components. For optimal performance, separate the analog components such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs from digital components such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators. 図 28 shows an example of good component placement. Although 図 28 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

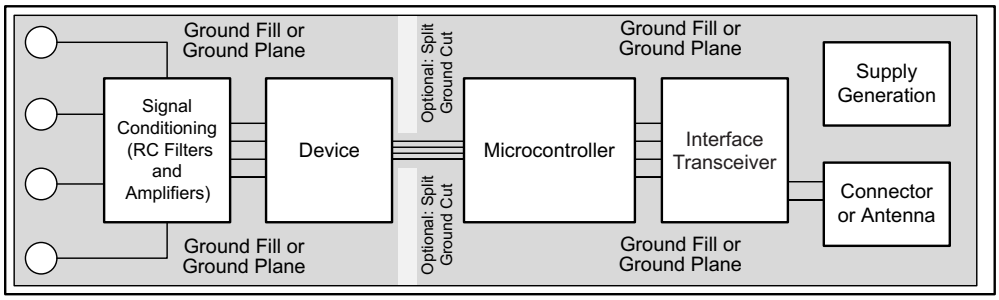


図 28. System Component Placement

The following points outline some basic recommendations for the layout of the TLA202x to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate the analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines to prevent digital noise from coupling back into analog signals.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, the ground plane must find another path to return to the source and complete the circuit. If the ground plane is forced into a larger path, there is an increased chance of signal radiation. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to minimize high-frequency noise. Do not place vias between bypass capacitors and the active device. For best results, place the bypass capacitors on the same layer as close as possible to the active device.
- Consider the resistance and inductance of the routing. Input traces often have resistances that react with the input bias current and cause an added error voltage. Reduce the loop area enclosed by the source signal and the return current to minimize the inductance in the path.
- For best input combinations with differential measurements, use adjacent analog input lines such as AIN0, AIN1 and AIN2, AIN3. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO) capacitors, which have stable properties and low-noise characteristics.

12.2 Layout Example

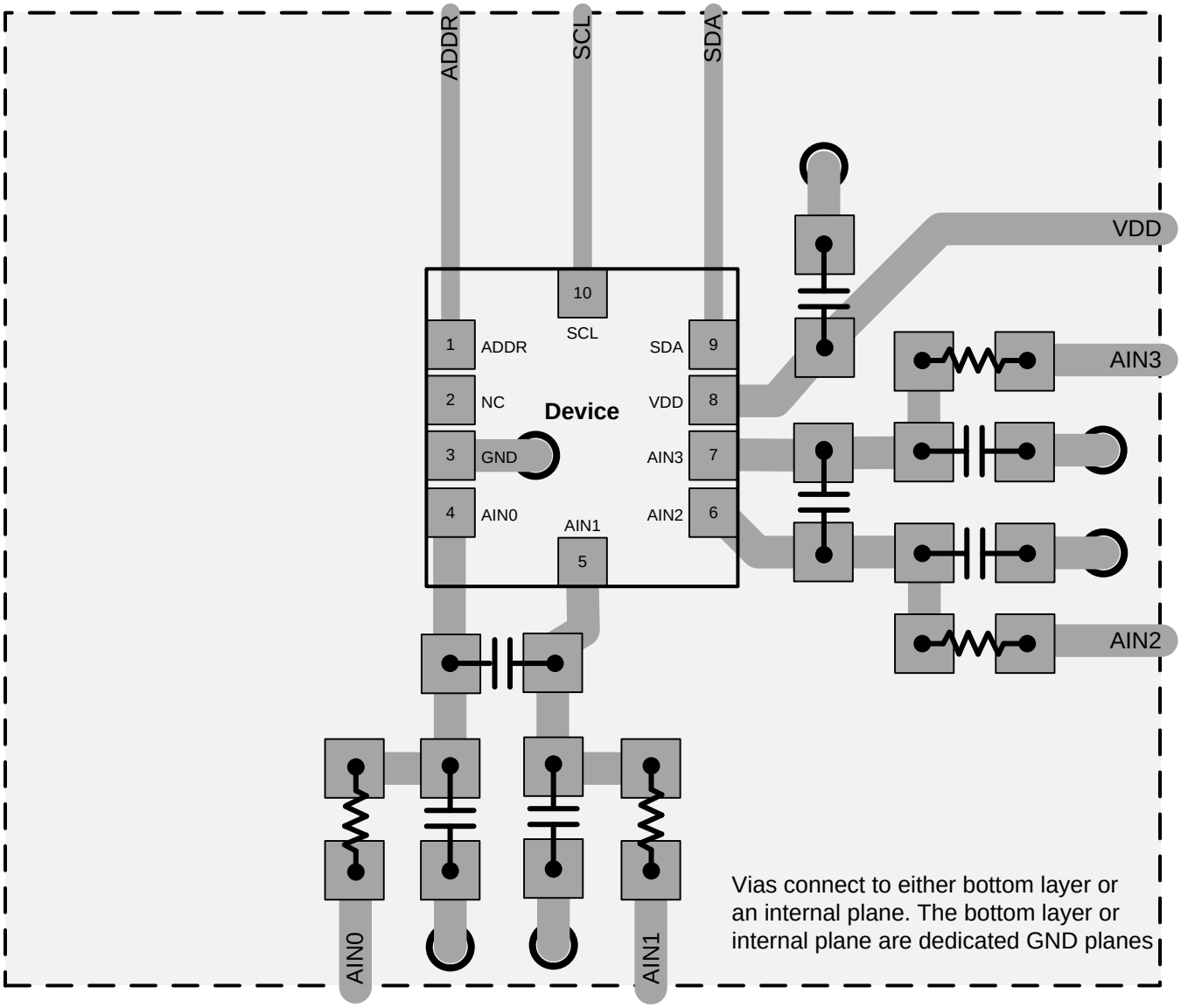


図 29. TLA2024 X2QFN Package

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 デベロッパー・ネットワークの製品に関する免責事項

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次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 9. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLA2021	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLA2022	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLA2024	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLA2021IRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9AZ
TLA2021IRUGR.B	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9AZ
TLA2021IRUGT	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9AZ
TLA2021IRUGT.B	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9AZ
TLA2022IRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	19J
TLA2022IRUGR.B	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	19J
TLA2022IRUGT	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	19J
TLA2022IRUGT.B	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	19J
TLA2024IRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ
TLA2024IRUGR.B	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ
TLA2024IRUGRG4	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ
TLA2024IRUGRG4.B	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ
TLA2024IRUGT	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ
TLA2024IRUGT.B	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9IJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

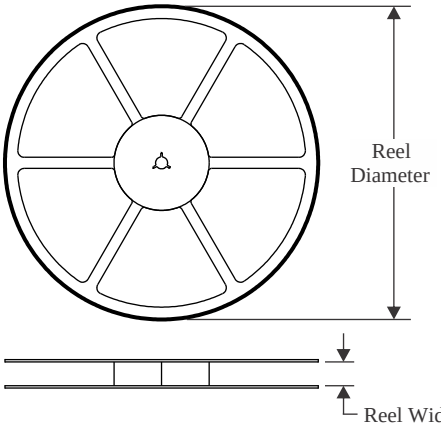
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

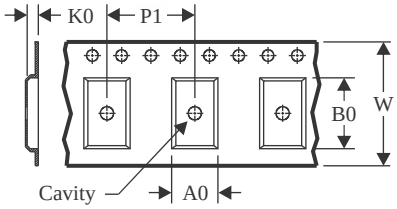
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

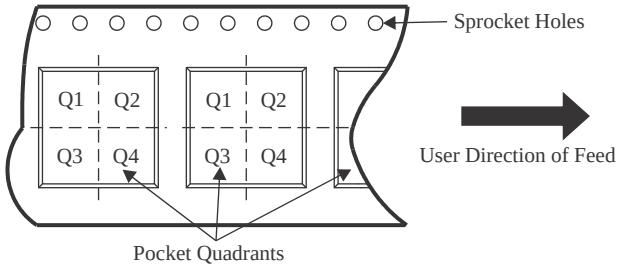


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

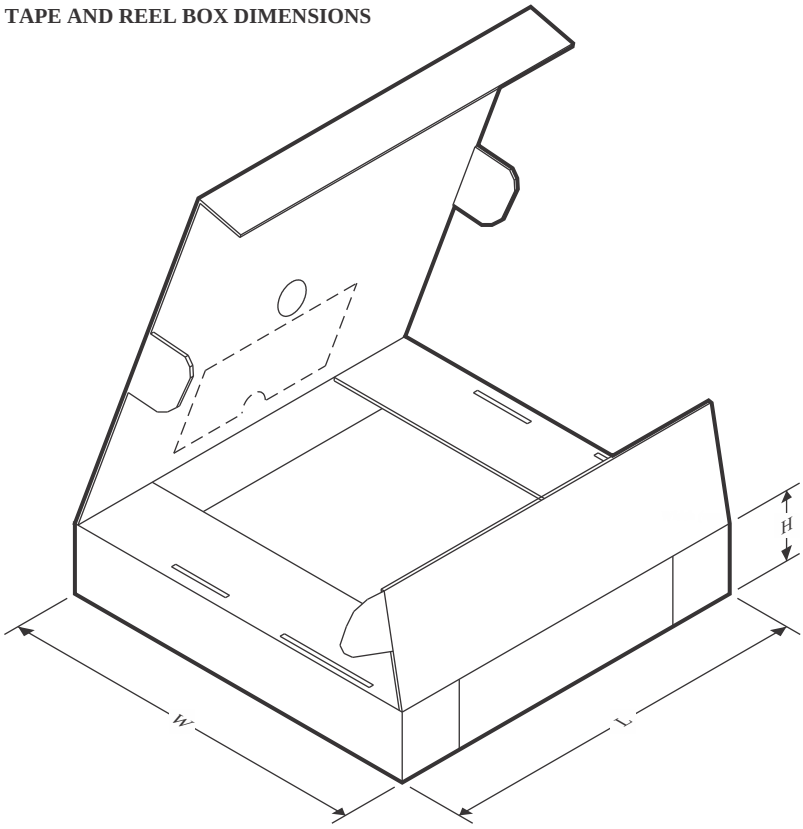
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLA2021IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2021IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2022IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2022IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2024IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2024IRUGRG4	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLA2024IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

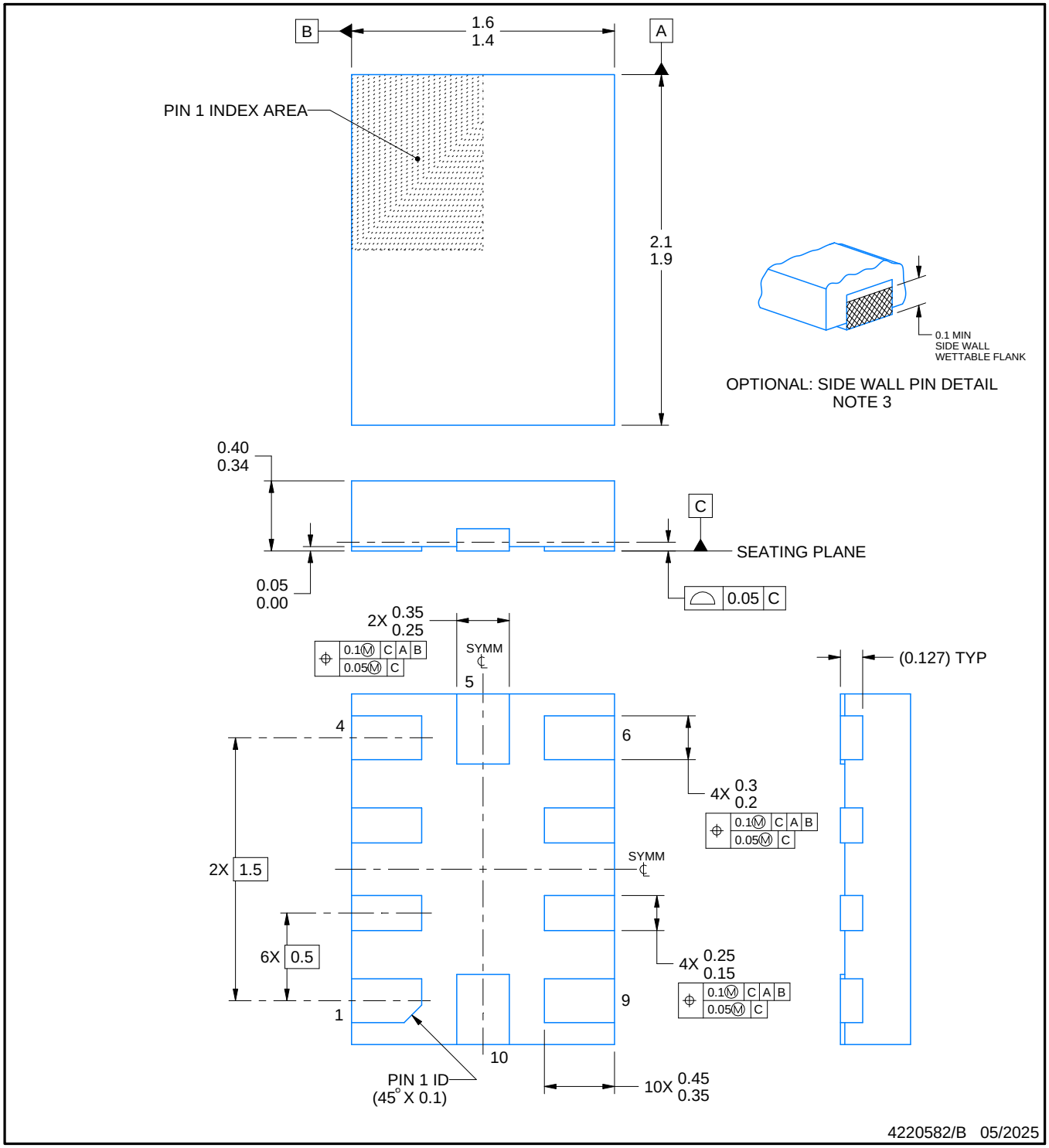
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLA2021IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLA2021IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0
TLA2022IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLA2022IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0
TLA2024IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLA2024IRUGRG4	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLA2024IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0

RUG0010B

PACKAGE OUTLINE

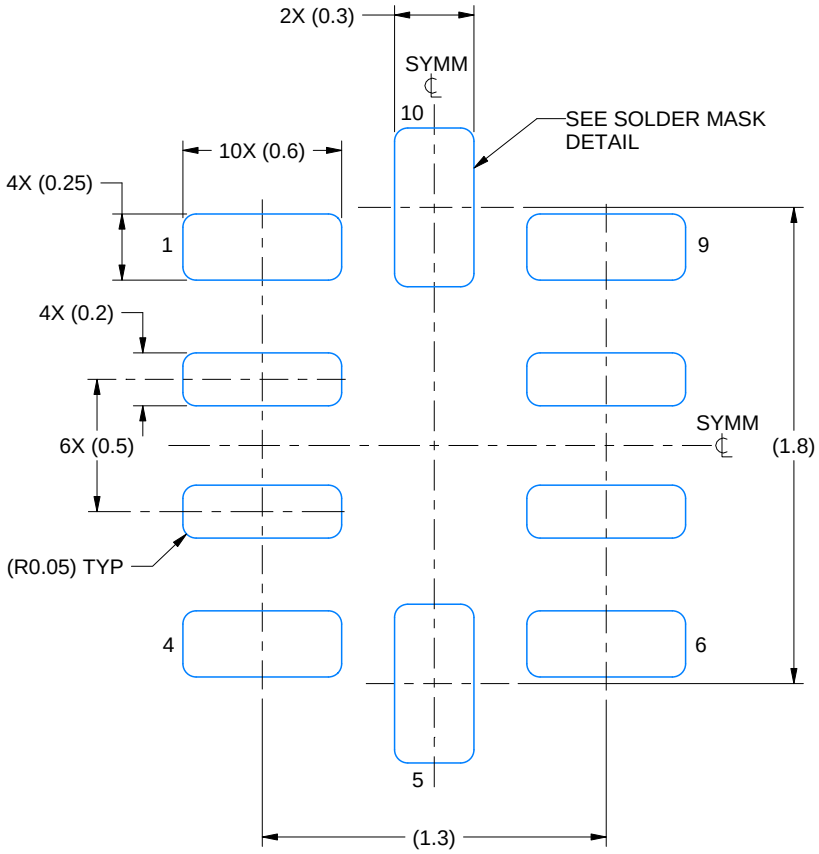
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

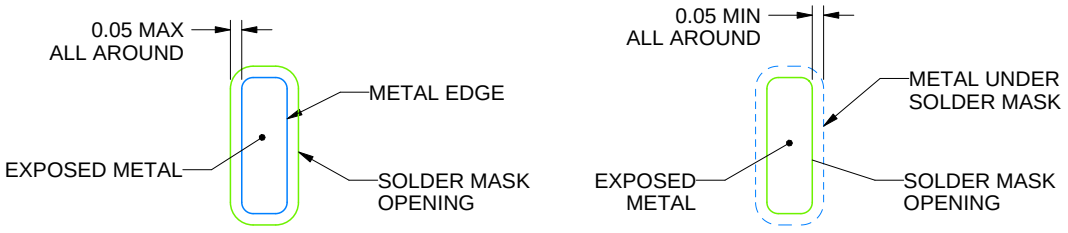


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X

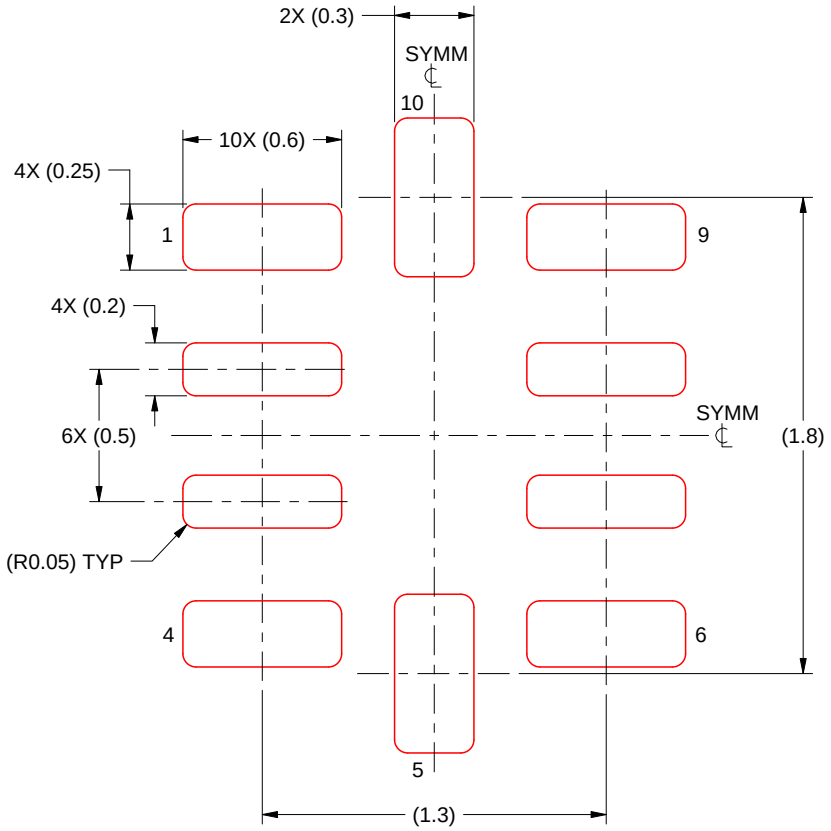


SOLDER MASK DETAILS

4220582/B 05/2025

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4220582/B 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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