

TIOS102 および TIOS102x 小型パッケージに封止したサージ保護機能内蔵デジタル・センサ出力ドライバ

1 特長

- 広い動作電源電圧
 - 4.75V～36V の電源電圧 (TIOS102, TIOS1023)
 - 7V～36V の電源電圧 (TIOS1025)
- PNP、NPN、またはプッシュプルとして構成可能な出力
- 機能安全に対応
 - 機能安全システムの設計に役立つ資料を利用可能
- TIOS101(x) とピン互換 (性能は向上)
 - 低い残留電圧: 200mA で 0.5V (標準値)
 - アクティブ・ドライバの電流制限機能
 - 優れたパッケージ放熱性能
 - ドライバ・スルーレートを遅くすることでオーバーシュートを低減 (最大 750ns)
- 内蔵保護機能によるシステムの信頼性向上
 - ドライバの過電流制限を設定可能 (50mA～350mA)
 - VCC、OUT、GND で最大 65V のアクティブ逆極性保護
 - 過電流、過熱、UVLO フォルトのフォルト・インジケータ
 - 大きな誘導性負荷の安全で高速な消磁
 - 拡張周囲温度範囲での動作: -40°C～125°C
- VCC および OUT の EMC 保護を搭載
 - ±8kV IEC 61000-4-2 ESD 接触放電
 - ±4kV IEC 61000-4-4 電気的高速過渡
 - ±1.2kV/500Ω IEC 61000-4-5 サージ
- 大容量負荷駆動能力
- 1.5mA 未満 (標準値) の静止消費電流 (ドライバがデイスレーブルのとき)
- 最大電流 20mA の内蔵 LDO オプション
 - TIOS1023: 3.3V LDO
 - TIOS1025: 5V LDO
 - TIOS1023L (DSBGA): 3.3V/5V の LDO 出力を選択可能
- スペースを節約する小型のパッケージ・オプション
 - 3mm × 3mm の 10 ピン VSON パッケージ (TIOS101 とピン互換)
 - 2.45mm × 1.7mm の DSBGA パッケージ

2 アプリケーション

- 近接スイッチ
- 容量性および誘導性センサ
- アクチュエータ
- デジタル出力

3 概要

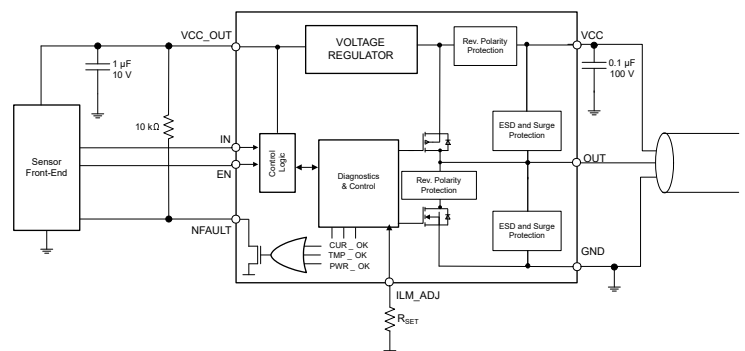
TIOS102(x) デバイスは、ハイサイド、ローサイド、またはプッシュプル・ドライバとして構成可能です。これらのデバイスは、最高 1.2kV (500Ω) の IEC 61000-4-5 サージに耐えられ、逆極性保護機能が内蔵されています。

ピンによりプログラム可能なインターフェイスにより、回路と簡単に接続できます。出力電流制限は、外付けの抵抗を使用して構成できます。低電圧、過電流、過熱状態に対するフォルト通知および内部保護機能が備わっています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ・サイズ ⁽²⁾
TIOS102	VSON (10)	3mm×3mm
TIOS1023		
TIOS1025		
TIOS102	DSBGA (12)	2.45mm × 1.7mm
TIOS1023L		

- 利用可能なデバイスについては、このデータシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーションの図



Table of Contents

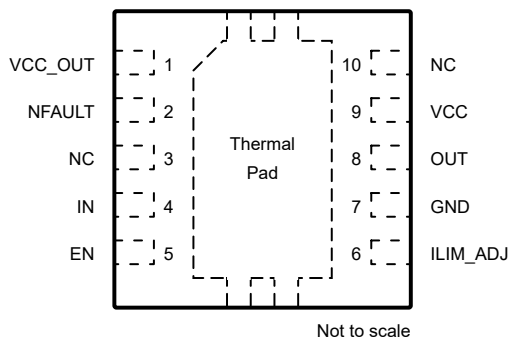
1 特長	1	8.3 Feature Description.....	12
2 アプリケーション	1	8.4 Device Functional Modes.....	16
3 概要	1	9 Application Information Disclaimer	18
4 Revision History	2	9.1 Application Information.....	18
5 Pin Configuration and Functions	3	9.2 Typical Application.....	18
6 Specifications	5	10 Power Supply Recommendations	22
6.1 Absolute Maximum Ratings.....	5	11 Layout	23
6.2 ESD Ratings.....	5	11.1 Layout Guidelines.....	23
6.3 ESD Ratings - IEC Specifications.....	5	11.2 Layout Example.....	23
6.4 Recommended Operating Conditions.....	5	12 Device and Documentation Support	24
6.5 Thermal Information.....	6	12.1 ドキュメントの更新通知を受け取る方法.....	24
6.6 Electrical Characteristics.....	6	12.2 サポート・リソース.....	24
6.7 Switching Characteristics.....	8	12.3 Trademarks.....	24
6.8 Typical Characteristics.....	9	12.4 静電気放電に関する注意事項.....	24
7 Parameter Measurement Information	10	12.5 用語集.....	24
8 Detailed Description	11	13 Mechanical, Packaging, and Orderable Information	24
8.1 Overview.....	11	13.1 Mechanical Data.....	25
8.2 Functional Block Diagrams.....	11		

4 Revision History

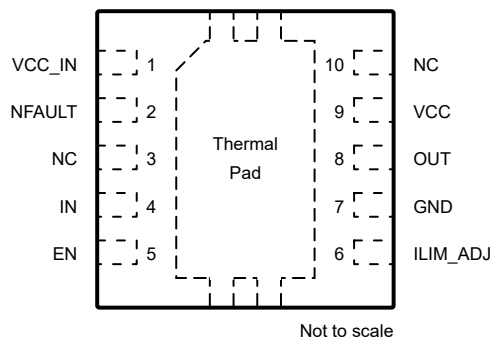
Changes from Revision A (December 2022) to Revision B (June 2023)	Page
• 「製品情報」表で DSBGA パッケージから「製品プレビュー」の注記を削除	1
• 「製品情報」表を「パッケージ情報」表に変更	1
• Changed the DRC package images.....	3
• Added the custom images for the YAH (DSBGA) 12-pin package.....	24

Changes from Revision * (February 2022) to Revision A (December 2022)	Page
• データシートで VSON パッケージを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions



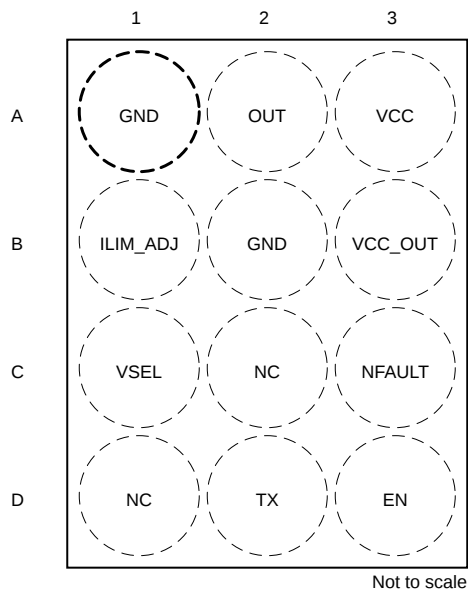
**図 5-1. TIOS1023, TIOS1025
DRC, 10-Pin VSON
(Top View)**



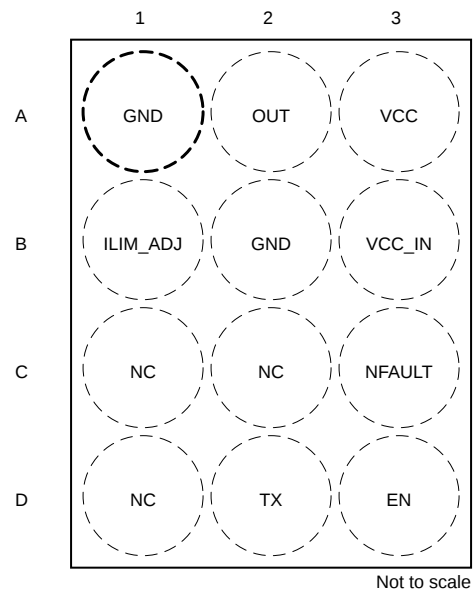
**図 5-2. TIOS102
DRC, 10-Pin VSON
(Top View)**

表 5-1. Pin Functions (VSON Package)

PIN NO	PIN NAME		Type	DESCRIPTION
	TIOS102	TIOS1023, TIOS1025		
1	VCC_IN	VCC_OUT	P	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
2	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. Connect this pin via pull-up resistor to VCC_IN (TIOS102) or VCC_OUT (TIOS1023, TIOS1025)
3	NC	NC	-	Do not connect to GND. Leave floating
4	IN	IN	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
5	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
6	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R _{SET} between ILIM_ADJ and GND.
7	GND	GND	GND	Device ground connection
8	OUT	OUT	O	Driver output
9	VCC	VCC	P	Supply voltage (24 V nominal)
10	NC	NC	-	Do not connect to GND. Leave floating
	Thermal Pad	Thermal Pad	—	Connect to GND plane for optimal thermal and electrical performance



**图 5-3. TIOS1023L
YAH, 12-Pin DSBGA
(Top View)**



**图 5-4. TIOS102
YAH, 12-Pin DSBGA
(Top View)**

表 5-2. Pin Functions (DSBGA)

PIN NO	PIN NAME		Type	DESCRIPTION
	TIOS102	TIOS1023L		
B3	VCC_IN	VCC_OUT	P	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
C3	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. Connect this pin via pull-up resistor to VCC_IN (TIOS102) or VCC_OUT (TIOS1023, TIOS1025)
D2	TX	TX	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
D3	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
B1	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and GND.
A1, B2	GND	GND	GND	Device ground connection
A2	OUT	OUT	O	Switch output
A3	VCC	VCC	P	Supply voltage (24 V nominal)
D1, C2	NC	NC	-	Leave floating. Do not connect.
C1	NC	VSEL	I	TIOS102: Leave floating. Do not connect TIOS1023L: VSEL: Connect to GND for 5V LDO output. Please leave this pin floating for 3.3V LDO output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for VCC and OUT	−65	65	V
	Transient pulse width < 100 μs for VCC and OUT	−70	70	V
Voltage difference	$ V_{(VCC)} - V_{(OUT)} $		65	V
Logic supply voltage (TIOS102)	VCC_IN	−0.3	6	V
Input logic voltage	IN, EN, VSEL, ILIM_ADJ	−0.3	$\min(V_{CC_IN} + 0.3, 6)$	V
Output current	NFAULT	−5	5	mA
Storage temperature, T _{stg}		−55	170	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the GND pin, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins	±4000	V
V _(ESD)	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	All pins	±750	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), VCC, OUT and GND ⁽¹⁾	±8,000	V
	Electrostatic discharge	IEC 61000-4-5, 1.2 μs/50 μs Surge with 500 Ω in series, VCC, OUT and GND ⁽¹⁾	±1,200	
	Electrostatic discharge	IEC 61000-4-4 EFT (Fast transient or burst), VCC, OUT and GND ⁽¹⁾	±4,000	

- (1) Minimum 100-nF capacitor is required between VCC and GND. Minimum 1-μF capacitor is required between VCC_IN/VCC_OUT and GND.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _(VCC)	Supply voltage	TIOS102, TIOS1023, TIO1023L (3.3V output)	4.75	24	36	V
		TIOS1025, TIOS1023L (5V output)	7	24	36	V
V _(VCC_IN)	Logic level input voltage (TIOS102 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R _{SET}	External resistor for CQ current limit		0		110	kΩ
1/t _{BIT}	Data rate (Communication mode)				250	kbps
I _(VCC_OUT)	LDO output current (TIOS1023, TIOS1023L, TIOS1025 only)				20	mA
T _A	Operating ambient temperature		−40		125	°C
T _J	Junction temperature				150	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TIOS102, TIOS1023, TIOS1025	TIOS102, TIOS1023L	UNIT
		DRC (10 Pins)	YAH (12 Pins)	
R _{θJA}	Junction-to-ambient thermal resistance	45.9	79.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	45.9	0.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.9	19.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.7	0.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	17.8	19.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typical values are at V_{VCC} = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCC)						
I _(VCC)	Quiescent supply current	EN = LOW, no load		1	1.5	mA
		EN = HIGH, no load		2.1	2.95	mA
LOGIC-LEVEL INPUTS (EN, IN, VSEL)						
V _{IL}	Input logic low voltage				0.8	V
V _{IH}	Input logic high voltage		2			V
R _{PD}	Pull-down (EN) resistance			100		kΩ
R _{PU}	Pull-up (IN) resistance			200		kΩ
R _{PU}	Pull-up (VSEL) resistance			1000		kΩ
CONTROL OUTPUTS (NFAULT)						
V _{OL}	Output logic low voltage	I _O = 4 mA			0.5	V
I _{OZ}	Output high impedance leakage	Output in Hi-Z, V _O = 0 V or VCC_IN/OUT	-1		1	μA
DRIVER OUTPUT (OUT)						
R _{DS(ON)}	High-side driver on-resistance			2.5	4.5	Ω
V _{DS(ON)}	High-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
R _{DS(ON)}	Low-side driver on-resistance			2.5	4.5	Ω
V _{DS(ON)}	Low-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
I _{PD}	OUT pull-down current	EN = LOW, IN = LOW, R _{SET} : ≥ 10 kΩ	40	50	80	μA
I _{PU}	OUT pull-up current	EN = LOW, IN = HIGH				
I _{O(LIM)}	Driver output current limit	R _{SET} = 10 kΩ; V(OUT) = (V _(VCC) -3) V or 3 V	300	350	400	mA
		R _{SET} = 110 kΩ; V(OUT) = (V _(VCC) -3) V or 3 V	35	50	70	mA
		R _{SET} = 0 to 5 kΩ; ⁽³⁾ V(OUT) = (V _(VCC) -3) V or 3 V T _J < T _(SDN) or t < 200 μs	500			mA
		(Fast-detect mode) R _{SET} = OPEN ⁽¹⁾ V(OUT) = (V _(VCC) -3) V or 3 V	260	330	400	mA

6.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typical values are at $V_{VCC} = 24\text{ V}$, $V_{VCC_IN} = 3.3\text{ V}$, $V_{VCC_OUT} = 3.3\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS							
V _(UVLO)	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z	TIOS102 and 3.3V LDO version	4.2	4.4		V
V _(UVLO)	VCC under voltage lockout	VCC rising; NFAULT = Hi-Z			4.6	4.75	V
V _(UVLO)	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z	TIOS1025	6	6.3		V
		VCC rising; NFAULT = Hi-Z			6.5	6.8	V
V _(UVLO,HYS)	VCC under voltage lockout hysteresis	Rising to falling threshold	Rising to falling threshold	200			mV
V _(UVLO_IN)	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z			2.3		V
		VCC_IN rising; NFAULT = LOW			2.5		V
V _(UVLO_IN,HYS)	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold			190		mV
T _(WRN)	Thermal warning	Die temperature T _J		125			°C
T _(SDN)	Thermal shutdown			150	160		°C
T _(HYS)	Hysteresis for thermal shutdown and warning thresholds				14		°C
I _{REV}	Leakage current in reverse polarity	EN=LOW, IN=x; V _(OUT) < V _(GND) or V _(OUT) > V _(VCC) , up to 36 V				60	μA
		EN=LOW, IN=x; V _(OUT) < V _(GND) or V _(OUT) > V _(VCC) , up to 55 V				110	μA
		EN = HIGH, IN = LOW; V _(OUT to VCC) = 3 V				640	μA
		EN = HIGH, IN = HIGH; V _(OUT to GND) = -3 V				10	μA
LINEAR REGULATOR (LDO)							
V _(VCC_OUT)	Voltage regulator output	5 V LDO version		4.75	5	5.25	V
		3.3 V LDO version		3.13	3.3	3.46	V
V _(DROP)	Voltage regulator drop-out voltage (V _(VCC) – V _(VCC_OUT))	I _{CC} = 20 mA load current	5 V LDO			1.9	V
			3.3 V LDO			1.4	V
REG	Line regulation (dV _(VCC_OUT) /dV _(VCC))	I _(VCC_OUT) = 1 mA				1.7	mV/V
L _{REG}	Load regulation (dV _(VCC_OUT) /V _(VCC_OUT))	V _(VCC) = 24 V, I _(VCC_OUT) = 100 μA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, I _(VCC_OUT) = 20 mA			40		dB

- (1) Current fault indication will be active. Current fault auto recovery will be de-activated.
- (2) If operating continuously with this current limit, ensure that the current through the device does not cause the T_J to be greater than $T_{(SDN)}$ for a given ambient temperature and thermal property of the system. For pulse durations $t < 200\text{ }\mu\text{s}$, the device can source or sink current of at least 500 mA across the recommended operating conditions.

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{PLH}, t_{PHL}	Driver propagation delay	See § 7-3 $R_L = 2\text{ k}\Omega$ $C_L = 5\text{ nF}$ $R_{(SET)} = 10\text{ k}\Omega$		600	1200	ns
$t_{P(skew)}$	Driver propagation delay skew. $ t_{PLH} - t_{PHL} $			75		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	μs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	μs
t_r, t_f	Driver output rise, fall time		200		700	ns
$ t_r - t_f $	Difference in rise and fall time			50		ns
t_{SC}	Current fault blanking time		175	200		μs
t_{pSC}	Current fault indication delay				280	μs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	OUT re-enable delay after UVLO ⁽¹⁾	$V_{(UVLO)}$ rising threshold crossing time to CQ enable time	10	30	50	ms

(1) CQ output remains Hi-Z for this time

6.8 Typical Characteristics

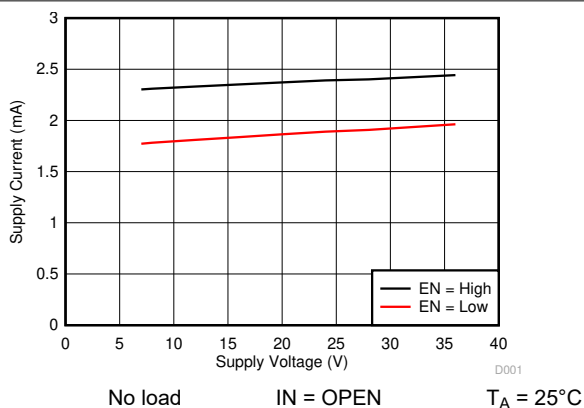


Figure 6-1. Supply Current vs Supply Voltage

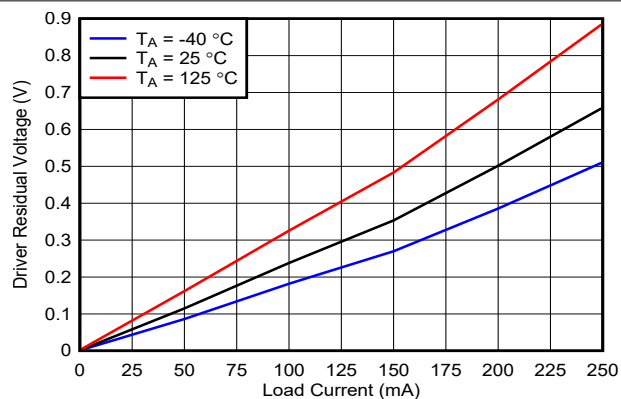


Figure 6-2. Residual Voltage vs Load Current: High Side

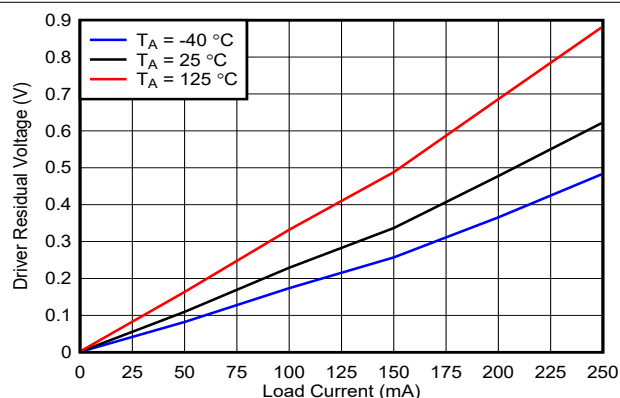


Figure 6-3. Residual Voltage vs Load Current: Low Side

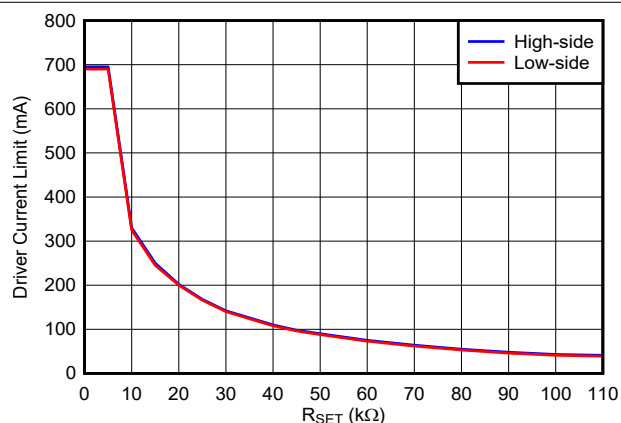
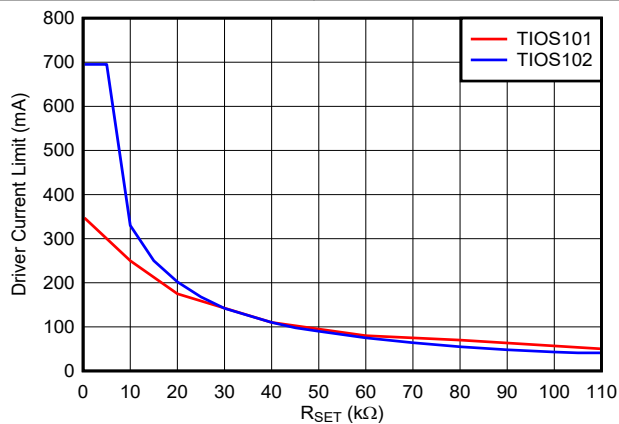


Figure 6-4. Current Limit vs R_{SET}



$T_A = 25^\circ\text{C}$

Figure 6-5. Current Limit vs R_{SET} : TIOS102(x) vs TIOS101(x)

7 Parameter Measurement Information

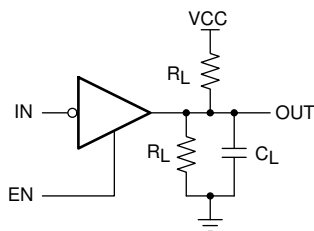


图 7-1. Test Circuit for Driver Switching

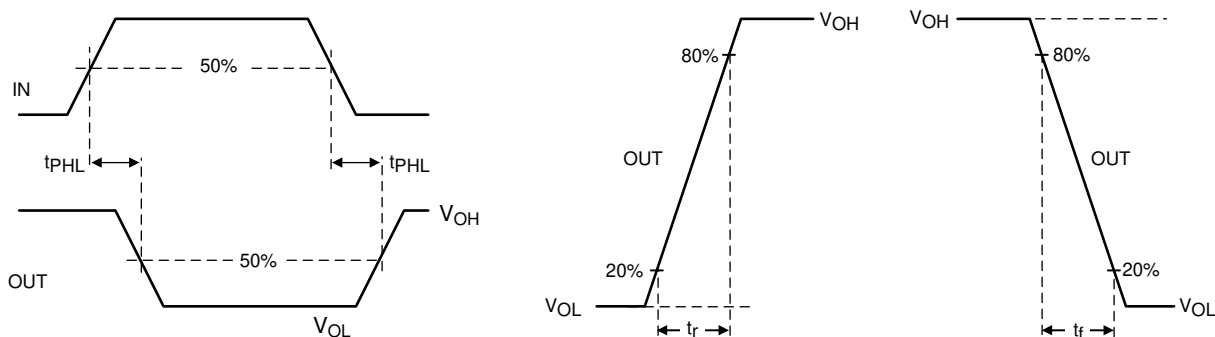


图 7-2. Waveforms for Driver Output Switching Measurements

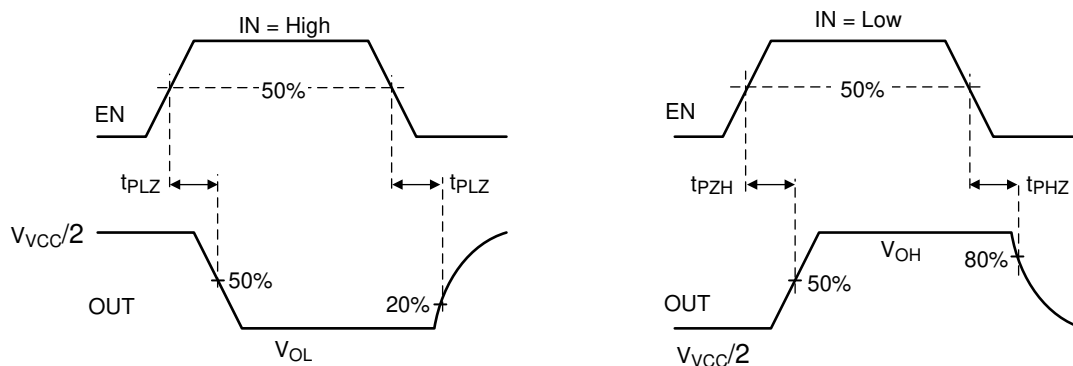


图 7-3. Waveforms for Driver Enable or Disable Time Measurements

8 Detailed Description

8.1 Overview

Figure 8-1 shows that the device driver output (OUT) can be used in a push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (IN) input pins. OUT can drive resistive, large capacitive or large inductive loads.

TIOS102 and TIOS102x devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ± 65 -V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system-level design by reducing the external protection circuitry.

These devices implement protection features for over-current, over-voltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The TIOS102x devices derive the low voltage supply from the typical 24 V industrial supply via an internal linear regulator to provide power to the local controller and sensor circuitry.

8.2 Functional Block Diagrams

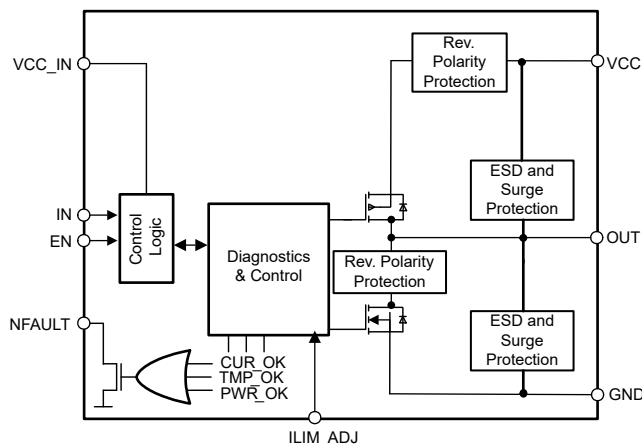


Figure 8-1. Block Diagram, TIOS102

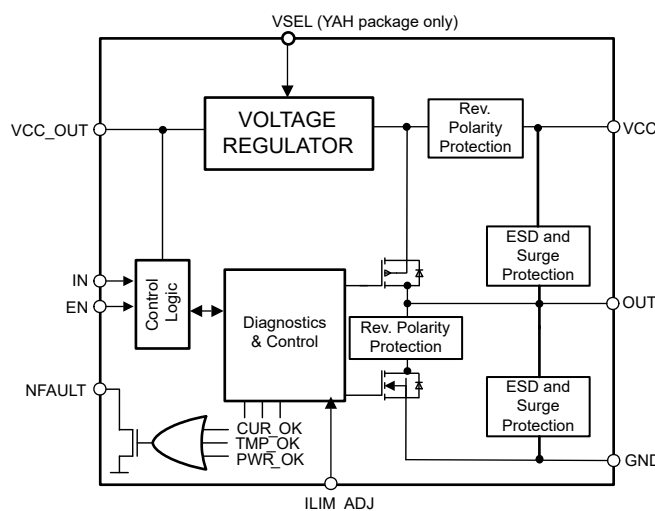


Figure 8-2. Block Diagram, TIOS102x

8.3 Feature Description

8.3.1 Current Limit Configuration

The output current can be configured with an external resistor on ILIM_ADJ pin. The highest current limit setting with an external resistor of 10 k Ω specifies a minimum of 300 mA over the operating temperature and voltage range.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitance.

When the ILIM_ADJ pin is shorted to ground, the TIOS102(x) is configured to source or sink a minimum of 500 mA. In this mode, current fault indication is disabled. Output Disable and Auto Recovery feature is also disabled in this mode. The driver is disabled if the power dissipation in the device causes the junction temperature to reach $T_{(SDN)}$.

表 8-1. Current Limitation

ILIM_ADJ Pin Condition	OUT Current Limit (Min.)	NFAULT Indication Due to Current Fault	Output Disable and Auto Recovery
R_{SET} resistor to GND (R_{SET} : 10 k Ω to 110 k Ω)	Variable (35 mA to 300 mA)	Yes	Yes
Connected to GND (R_{SET} 0 to 5 k Ω)	500 mA	No	No
OPEN	260 mA	Yes	No

8.3.2 Current Fault Detection, Indication and Auto Recovery

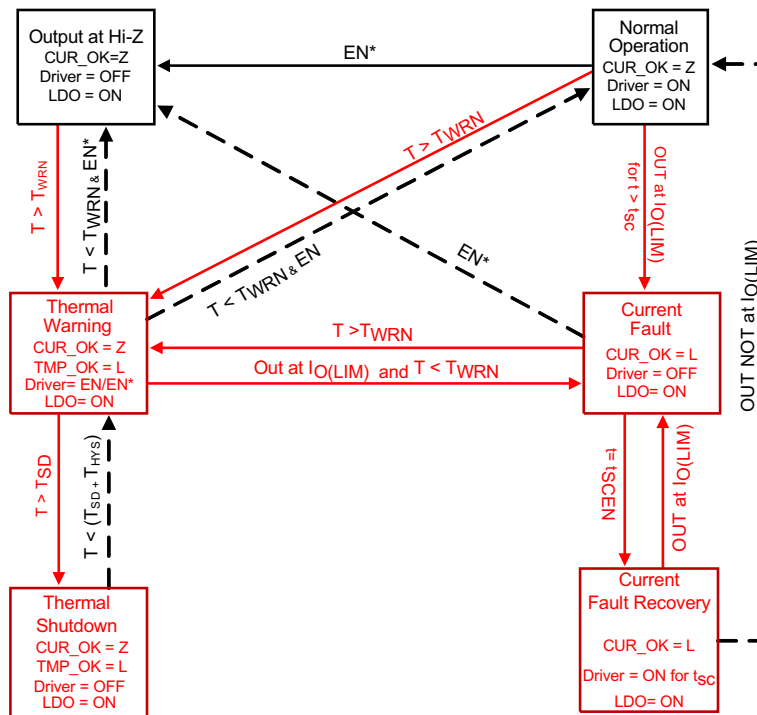
If the output current at OUT exceeds the internally set current limit $I_{O(LIM)}$ for a duration longer than t_{SC} , the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN or GND. See 表 8-3. Toggling EN will clear NFAULT.

8.3.3 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and IN pins.

8.3.4 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



NFAULT = [CUR_OK && PWR_OK && TMP_OK]

8-3. Device State Diagram

8.3.5 Device Function Tables

表 8-2. Driver Function

EN	IN	OUT	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	OUT is sourcing current (high-side drive)
H	H / Open	L	OUT is sinking current (low-side drive)

表 8-3. Current Limit Indicator Function ($t > t_{SC}$)

EN	IN	OUT CURRENT	NFAULT	COMMENT
H	H / Open	$ I_{(OUT)} > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$ I_{(OUT)} < I_{O(LIM)}$	Z	Normal operation
H	L	$ I_{(OUT)} > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$ I_{(OUT)} < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, current limit indicator is inactive

8.3.6 The Integrated Voltage Regulator (LDO)

The TIOS1023 and TIOS1025 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for VCC voltages in the range of 7 V to 36 V (TIOS1025) or in the range of 5 V to 36 V (TIOS102, TIOS1023) with respect to GND. The LDO is capable of delivering up to 20 mA. The LDO output is current limited to 35-mA to limit the inrush current onto VCC_OUT decoupling capacitors during initial power up.

In the DSBGA (YAH) package, TIOS1023L offers pin-configurable LDO output via VSEL pin. When VSEL is connected to GND, VCC_OUT is configured to provide a 5-V output. When VSEL is left floating, VCC_OUT provides a 3.3-V output.

表 8-4. LDO Output Configuration via VSEL pin (YAH Package)

VSEL pin connection	VCC_OUT
GND	5 V
Floating	3.3 V

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μ F or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω . With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μ F.

8.3.7 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the VCC, OUT and GND pins. The maximum voltage between any of the pins may not exceed 65 V DC at any time.

Figure 8-4 and Figure 8-5 shows all the possible connection combinations.

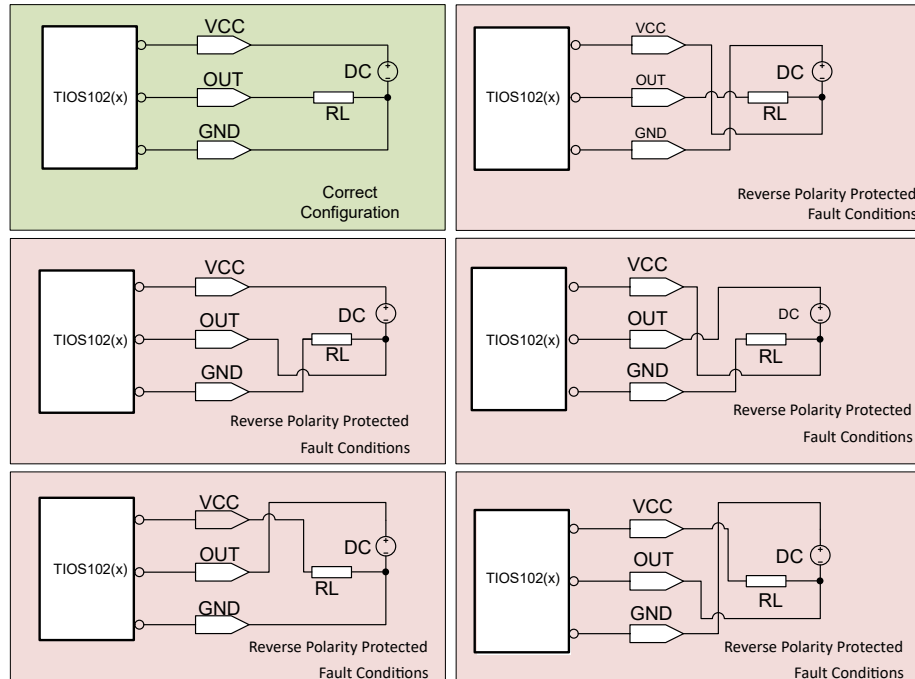


Figure 8-4. High-Side Driver Configuration

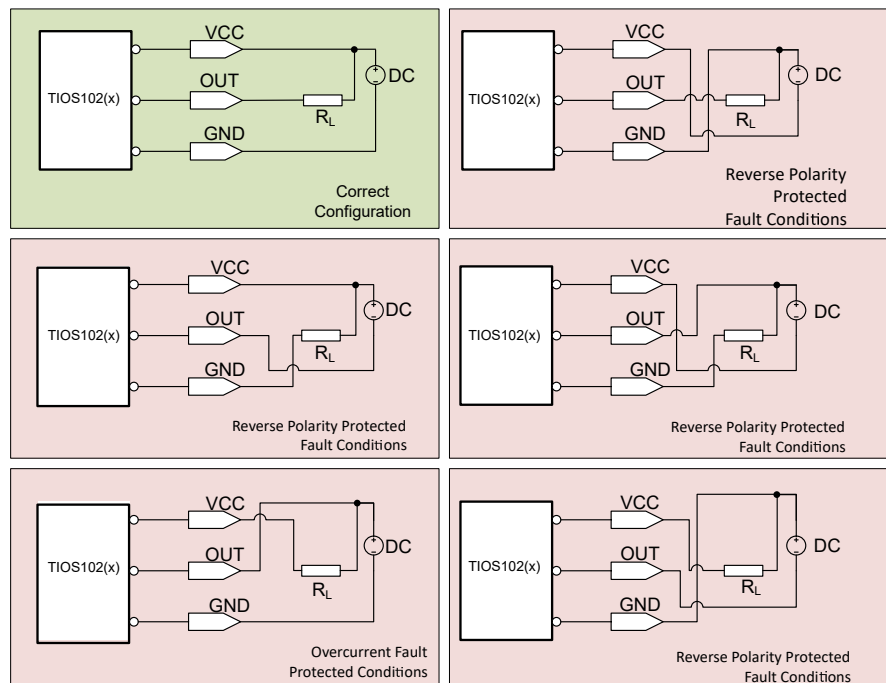
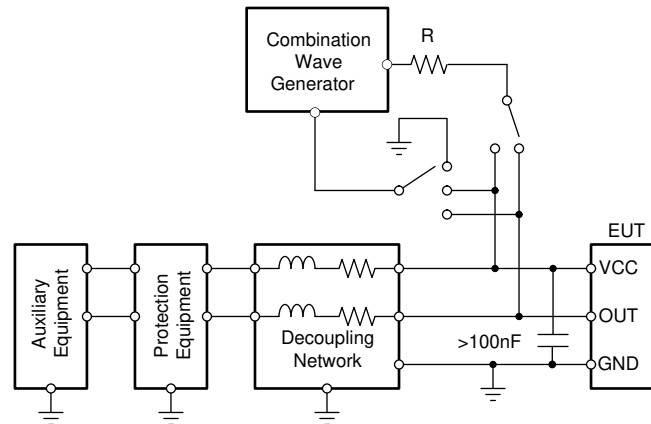


Figure 8-5. Low-Side Driver Configuration

8.3.8 Integrated Surge Protection and Transient Waveform Tolerance

The VCC and OUT pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 μ s IEC 61000-4-5 surge with a source impedance of 500 Ω . The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between VCC and GND, and 1 μ F between VCC_IN/OUT and GND.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to $\pm$ 65-V transient pulses < 100 μ s.



1.2/50 - 80/20 μ s CWG
 R = 500 Ω

8-6. Surge Test Setup

8.3.9 Power Up Sequence

VCC_IN and VCC domains can be powered up in any sequence. In the event of VCC is powered and VCC_IN is not, the OUT pin remains in high impedance.

8.3.10 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the VCC voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to VCC. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$, NFAULT is pulled low, the LDO is turned off and the OUT output is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present) and the LDO will be enabled immediately. The OUT output will be turned on after $T_{(UVLO)}$ delay.

8.4 Device Functional Modes

These devices can operate in three different modes.

8.4.1 NPN Configuration (N-Switch Mode)

Set IN pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on OUT.

8.4.2 PNP Configuration (P-Switch Mode)

Set IN pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on OUT.

8.4.3 Push-Pull Mode

Set EN pin high and toggle IN as control for realizing the function of a push-pull output on OUT. 表 8-5, 表 8-6, and 表 8-7 summarize the pin configurations to accomplish the functional modes.

表 8-5. NPN Mode

EN	IN	OUT
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 8-6. PNP Mode

EN	IN	OUT
L / Open	L	Hi-Z
H	L	P-Switch

表 8-7. Push-Pull Mode

EN	IN	OUT
L / Open	X	Hi-Z
H	H / Open	N-Switch
H	L	P-Switch

9 Application Information Disclaimer

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

TIOS102 and TIOS102x are robust 24-V digital drivers for industrial sensors.

9.2 Typical Application

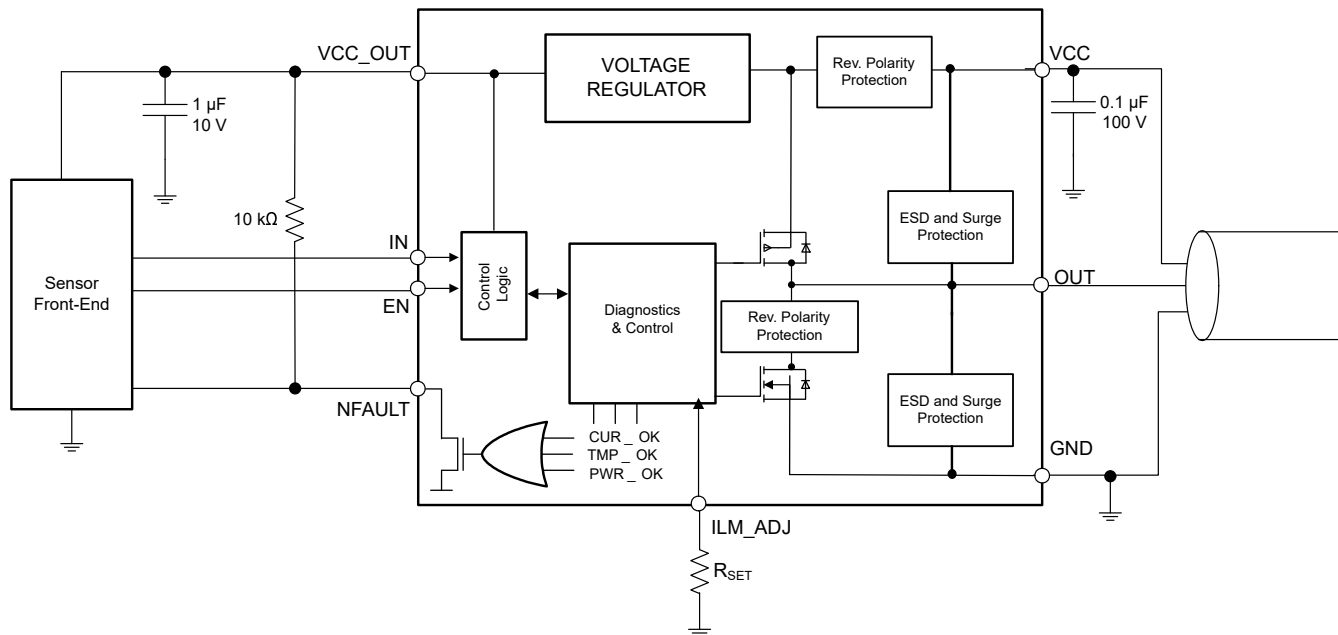


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

表 9-1 shows recommended components for a typical system design.

表 9-1. Design Parameters

PARAMETERS	Design Requirement	TIOS102(x) Specification
Input voltage range (VCC)	24 V, 30 V (max)	7 V to 36 V (TIOS1025)
Output current (OUT)	200 mA	Choose 250 mA limit with $R_{SET} = 27 \text{ k}\Omega$
Output voltage (VCC_OUT), Pick TIOS1025	5 V	Choose TIOS1025; VCC_OUT = 5 V
Maximum LDO output current ($I_{VCC(OUT)}$)	5 mA	I_{VCC_OUT} : Up to 20 mA
Pull-up resistors for NFAULT	10 k Ω	10 k Ω
VCC decoupling capacitor	0.1 μF / 100 V	0.1 μF / 100 V
LDO output capacitor	1 μF / 10 V	1 μF / 10 V
Maximum Ambient Temperature, T_A	105°C	TIOS102(x) can support up to T_A of 125 °C if $T_J < T_{(SDN)}$

9.2.2 Detailed Design Procedure

9.2.2.1 最大接合部温度チェック

200mA の電流制限の場合:

- ドライバ出力電流制限、 $I_{O(LIM)} = 250\text{mA}$ (電流制限許容誤差を許容)、 $R_{SET} = 27\text{k}\Omega$ を選択します
- 250mA の電流でのハイサイド・スイッチの最大電圧降下は、 $V_{DS(on)} = 1.1\text{V}$ です

その結果、消費電力は次のようになります。

$$PD_{OP} = V_{DS(on)} \times I_{O(LIM)} = 1.1\text{V} \times 250\text{mA} = 275\text{mW} \quad (1)$$

5mA の LDO 電流出力の場合、

$$PD_{LDO} = (V_L + -V_{VCC_OUT}) \times I_{VCC_OUT} = (30 - 5)\text{V} \times 5\text{mA} = 125\text{mW} \quad (2)$$

合計消費電力、

$$PD = PD_{LDO} + PD_{OP} = 275\text{mW} + 125\text{mW} = 400\text{mW} \quad (3)$$

接合部-周囲間熱抵抗 $\theta_{JA} = 45.9^\circ\text{C/W}$ (「熱情報」表から取得) を使用してこの値を乗算し、接合部温度、 T_J 、周囲温度の差を求めます。 T_A :

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 400\text{mW} \times 45.9^\circ\text{C/W} = 18.36^\circ\text{C} \quad (4)$$

最終的な接合部温度を受け取るには、 $T_A = 105^\circ\text{C}$ の最大周囲温度にこの値を追加します。

$$T_J = T_A + \Delta T = T_A + PD \times \theta_{JA} = 105^\circ\text{C} + 400\text{mW} \times 45.9^\circ\text{C/W} = 105^\circ\text{C} + 18.36^\circ\text{C} = 123.36^\circ\text{C} \quad (5)$$

T_J が 推奨最大値の 150°C を下回っている限り、サーマル・シャットダウンは発生しません。ただし、接合部温度が T_{WRN} に近い場合、接合部温度が T_{WRN} を上回ると過熱警告が生成される場合があります。

PCB や筐体のサイズが小さい場合、エアフローなしで接合部温度を予測するには、システム全体のモデル化が必要な場合があります。ことに注意してください。

9.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the OUT output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \times t_{SC}]}{V_{(VCC)}} \quad (6)$$

To drive higher capacitive loads and avoid overcurrent condition disabling the driver, it is recommended to leave ILIM_ADJ pin floating. With ILIM_ADJ floating, TIOS102(x) indicates overcurrent fault without blanking time delay (t_{SC}) but does not disable the driver. Another approach is to drive high capacitive loads with a series resistor between the output and the load to avoid overcurrent condition. Capacitive loads can be connected to GND or VCC

9.2.2.3 Driving Inductive Loads

The TIOS102(x) family is capable of magnetizing and demagnetizing large inductive loads. These devices contain internal circuitry that enables fast demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the OUT pin is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the OUT pin. This voltage is clamped internally at about -15 V.

Similarly, in N-switch configuration, the load inductor L is magnetized when the OUT pin is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the OUT pin. This voltage is clamped internally at about 15 V.

The equivalent protection circuits are shown in [Figure 9-2](#) and [Figure 9-3](#). The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(VCC)}}{I_{O(LIM)}} \quad (7)$$

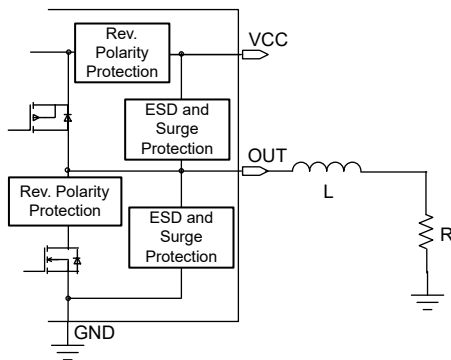


Figure 9-2. PNP Mode

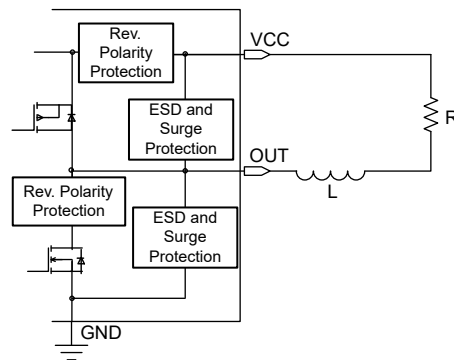
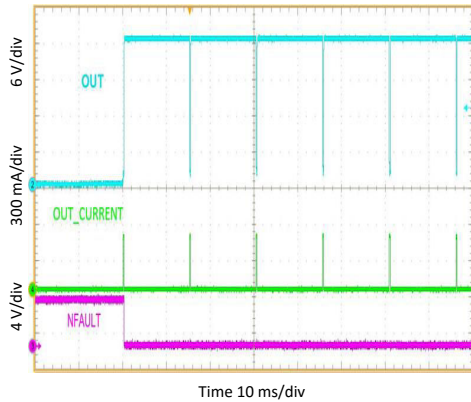
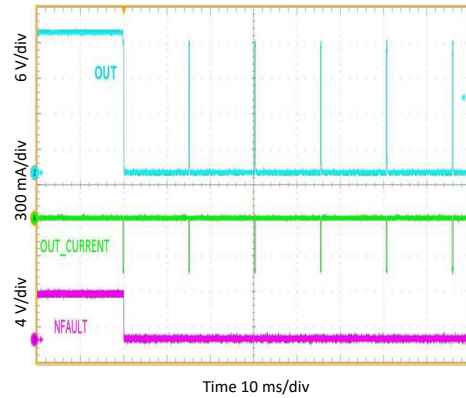


Figure 9-3. NPN Mode

9.2.3 Application Curves



9-4. OUT In Current Fault Auto Recovery, Low Side Mode

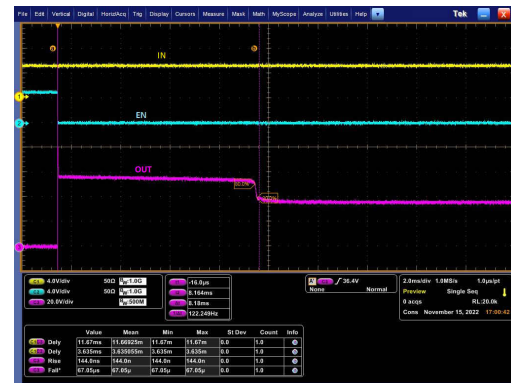


9-5. OUT In Current Fault Auto Recovery, High Side Mode



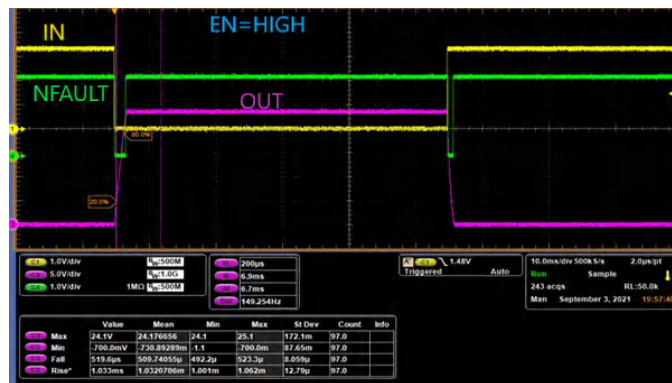
VCC = 36 V
R_{SET} = 10 kΩ
L = 1.5 H R_L = 360 Ω
T_A = 25 °C

9-6. OUT Driving Inductive Load, High Side Mode (PNP)



VCC = 36 V
R_{SET} = 10 kΩ
L = 1.5 H R_L = 360 Ω
T_A = 25 °C

9-7. OUT Driving Inductive Load, Low Side Mode (NPN)



NFAULT indicated for the duration of charging and discharging of the capacitor but driver is not disabled when ILIM_ADJ is floating.
VCC = 24 V
C_L = 20 μF R_L = 100 Ω
R_{SET} = 1 MΩ (ILIM_ADJ Floating)
T_A = 25 °C

9-8. OUT Driving Capacitive Load, Push-Pull Mode

10 Power Supply Recommendations

The TIOS102 and TIOS102x are designed to operate from a 24-V nominal supply at VCC, but can operate from supply voltage range of 7 V to 36 V (TIOS1025) or 4.75 V to 36 V (TIOS102, TIOS1023). This supply should be buffered with at least a 100-nF/100-V capacitor.

11 Layout

11.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as GND, layer 3 for the 24-V supply plane (VCC), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to GND with maximum amount of thermal vias for best thermal performance.
- Use entire planes for VCC, VCC_IN/OUT and GND to assure minimum inductance.
- The VCC terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor with a minimum value of 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- The optimum placement of the capacitor is closest to the VCC and GND terminals to reduce supply drops during large supply current loads. See [Figure 11-1](#) for a PCB layout example.
- Connect all open-drain control outputs via 10 k Ω pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and GND.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, 1 μ F, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

11.2 Layout Example

- VIA to Layer 2: Power Ground Plane (VCC)
- VIA to Layer 3: 24V Supply Plane (GND)
- VIA to Layer 4: Regulated Supply Plane (VCC_IN/OUT)

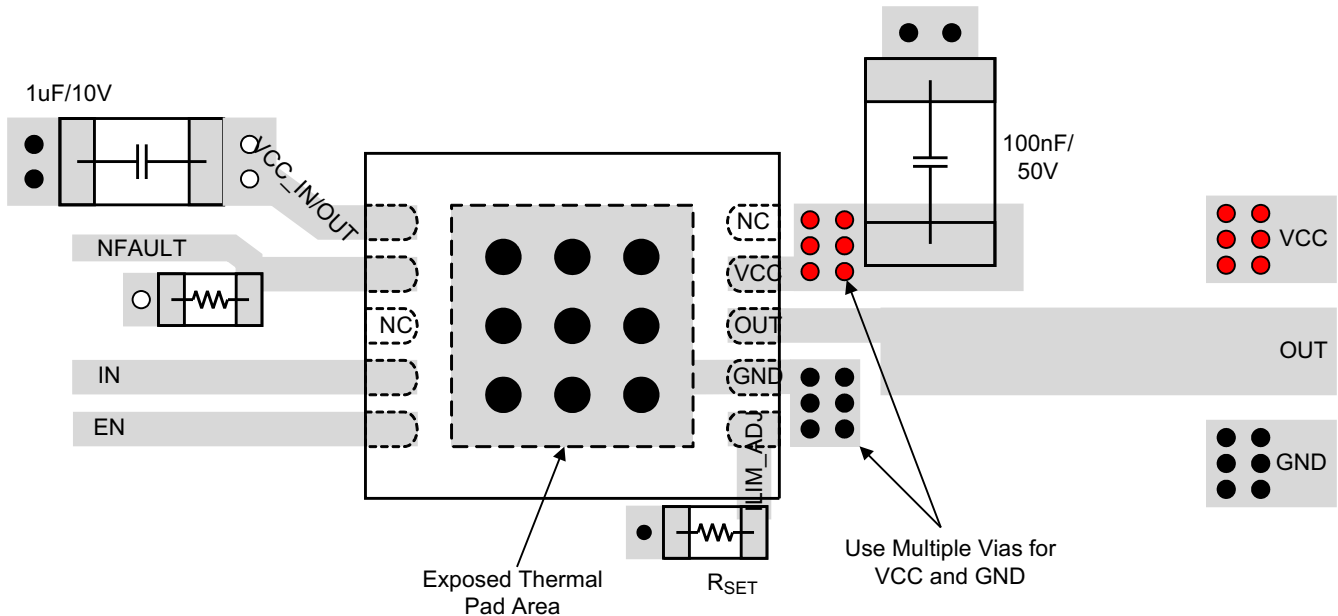


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

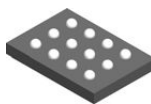
12.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Mechanical Data

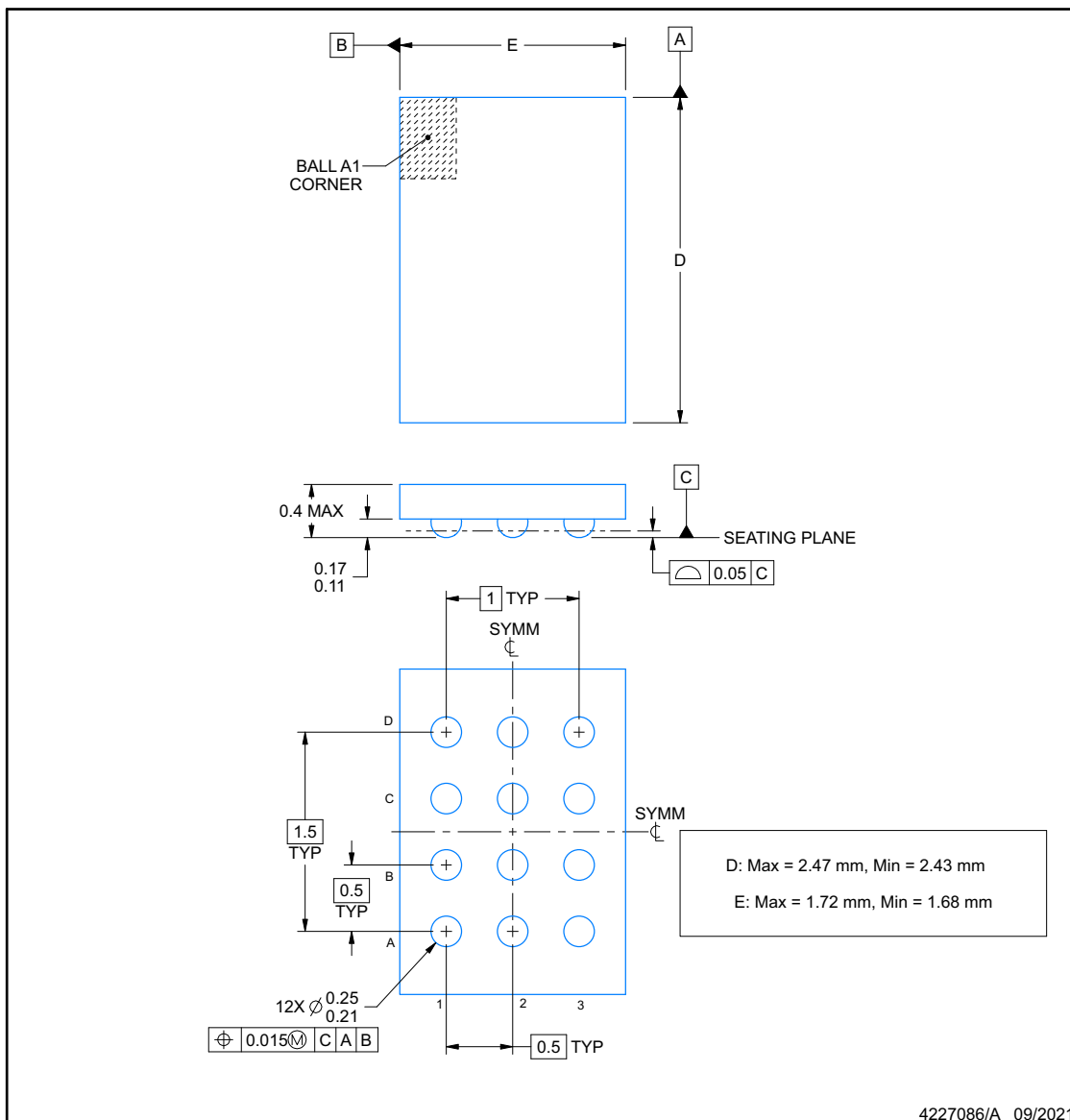


YAH0012-C01

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



4227086/A 09/2021

NOTES:

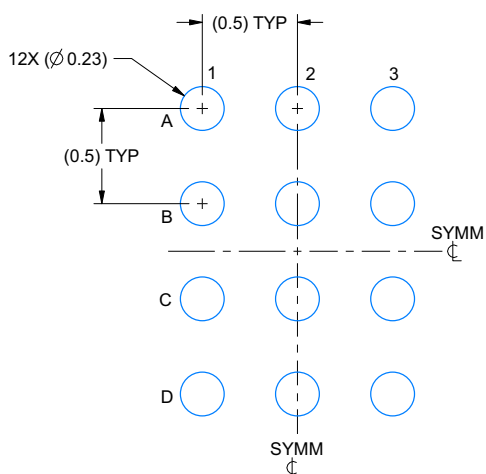
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

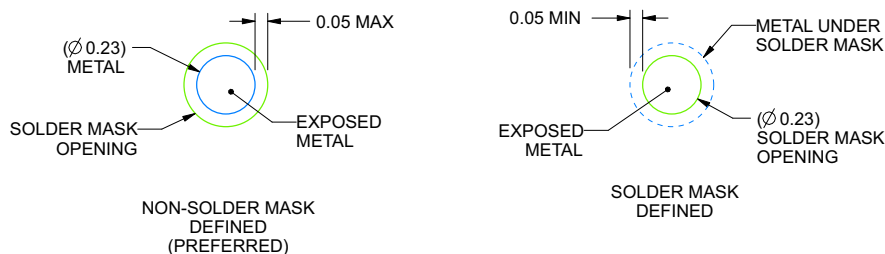
YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4227086/A 09/2021

NOTES: (continued)

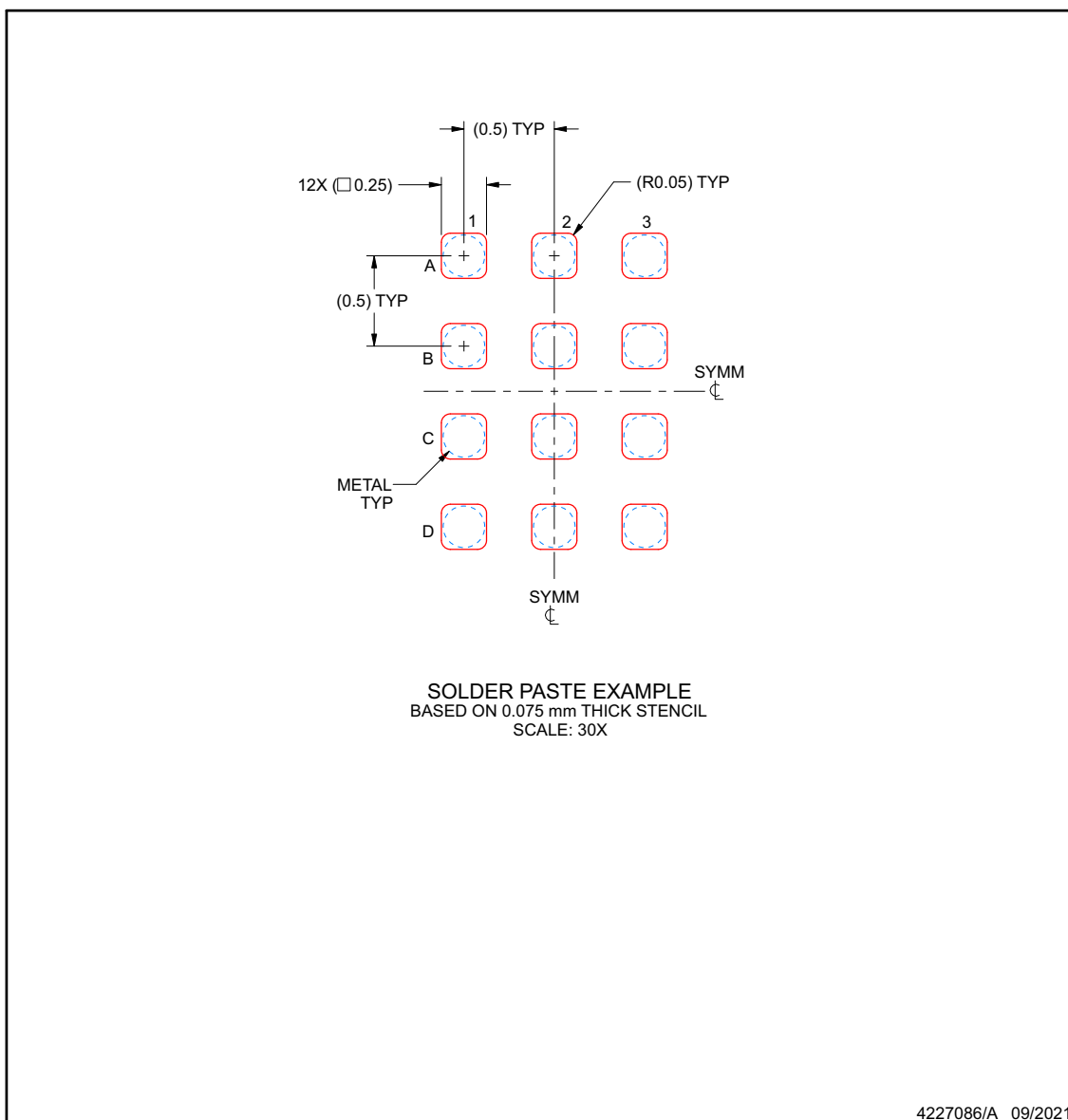
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TIOS1023DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1023
TIOS1023DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1023
TIOS1023LYAHR	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T102L
TIOS1023LYAHR.A	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T102L
TIOS1025DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1025
TIOS1025DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1025
TIOS102DRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	102
TIOS102DRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	102
TIOS102YAHR	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TS102
TIOS102YAHR.A	Active	Production	DSBGA (YAH) 12	1500 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TS102

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

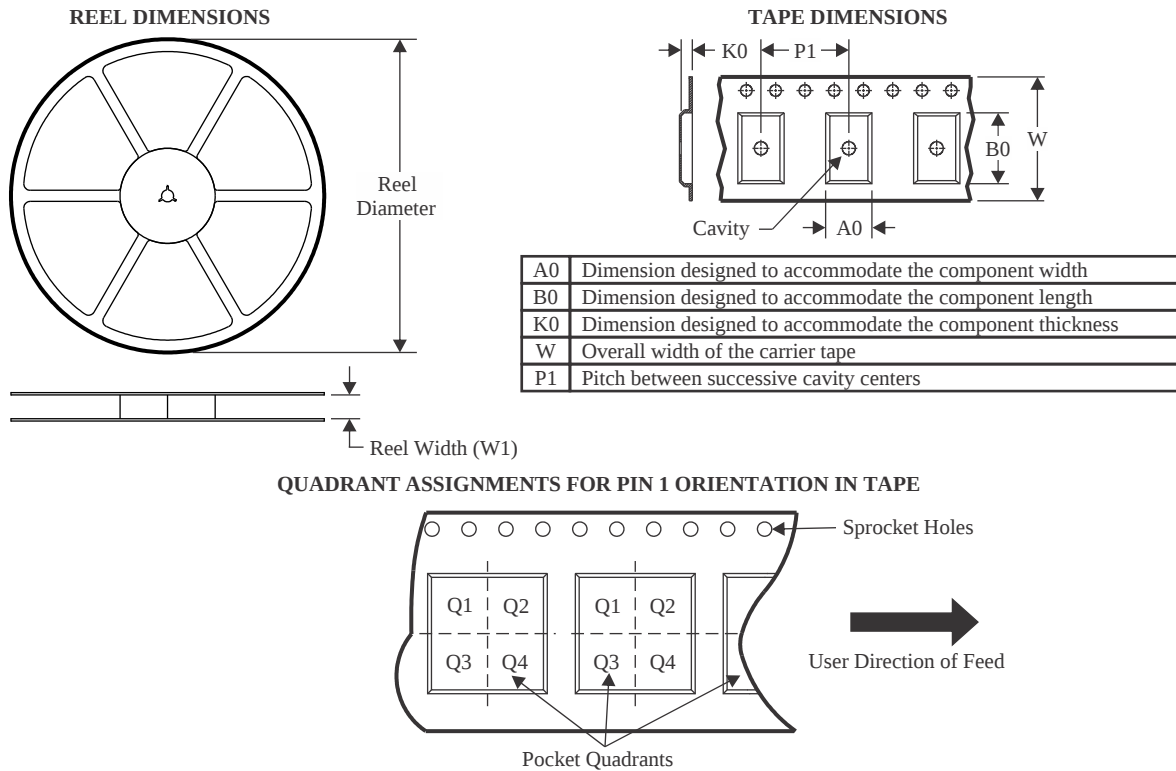
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

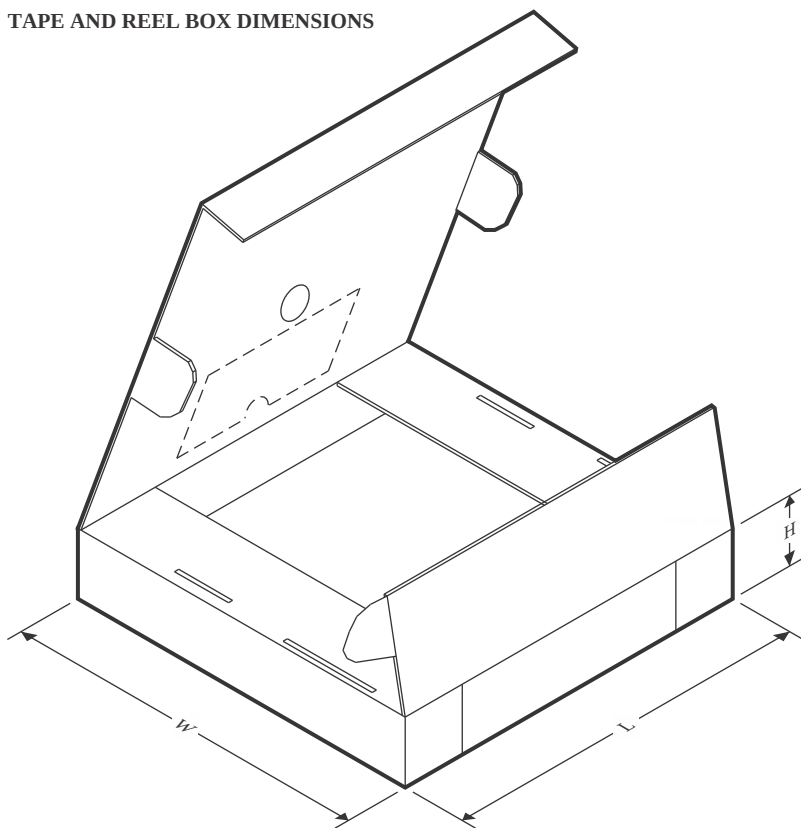
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOS1023DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOS1023LYAHR	DSBGA	YAH	12	1500	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q1
TIOS1025DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOS102DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOS102YAHR	DSBGA	YAH	12	1500	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOS1023DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOS1023LYAHR	DSBGA	YAH	12	1500	182.0	182.0	20.0
TIOS1025DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOS102DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOS102YAHR	DSBGA	YAH	12	1500	182.0	182.0	20.0

GENERIC PACKAGE VIEW

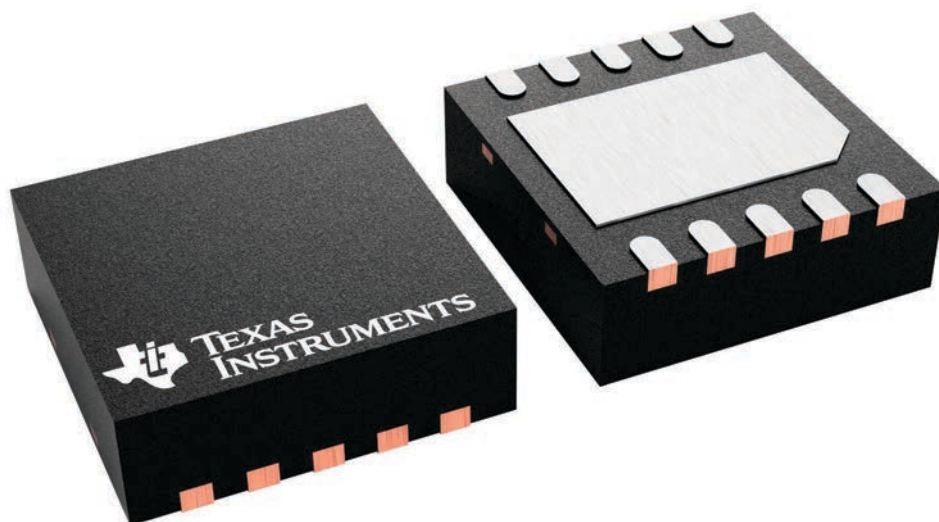
DRC 10

VSON - 1 mm max height

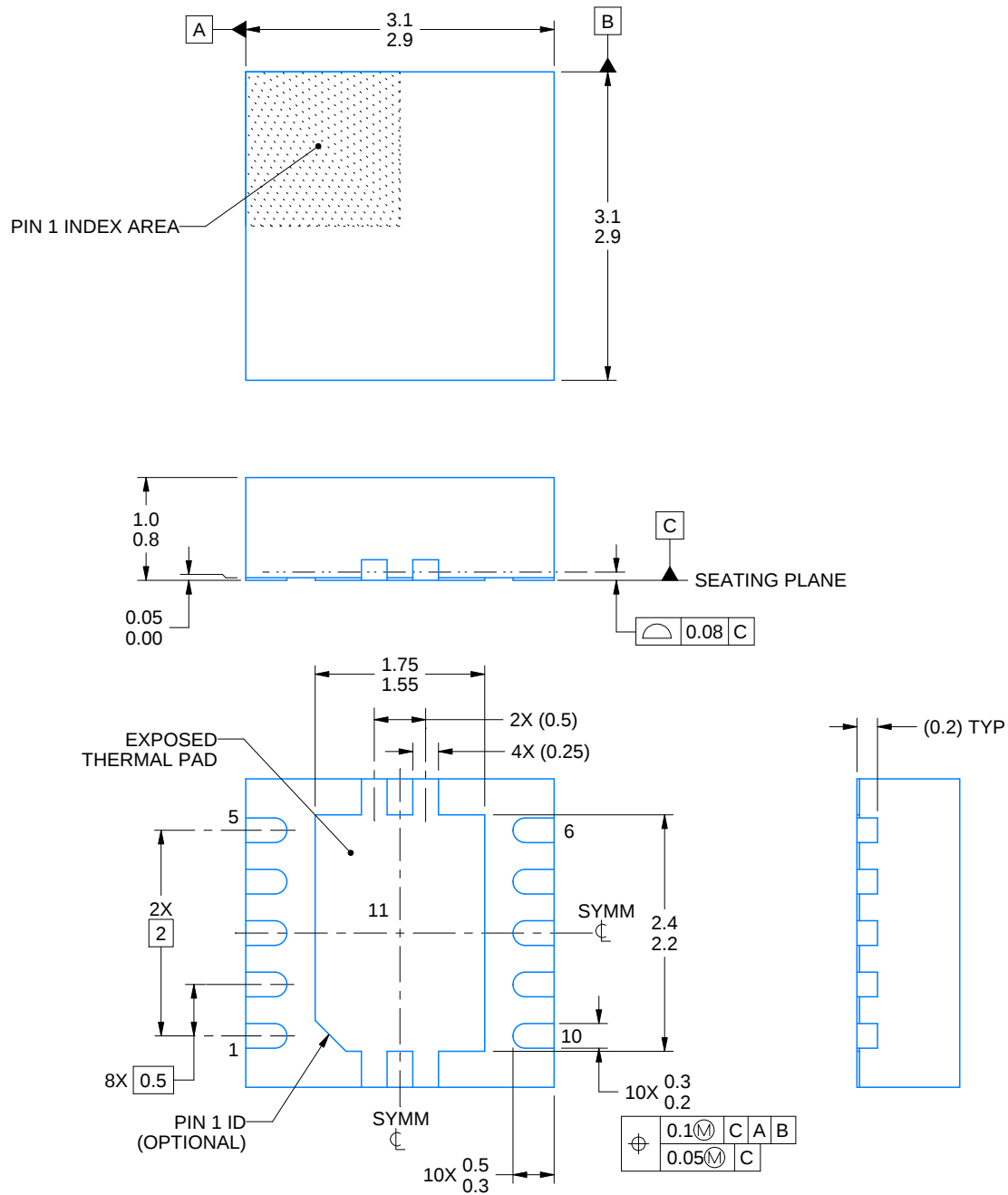
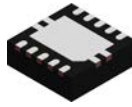
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A



4226575/A 02/2021

NOTES:

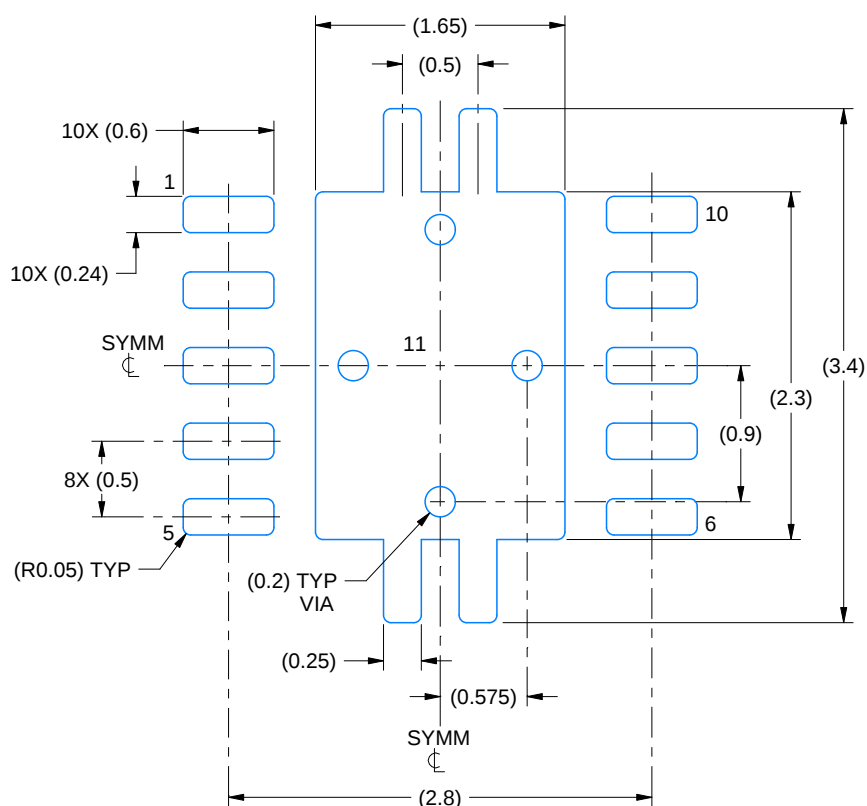
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

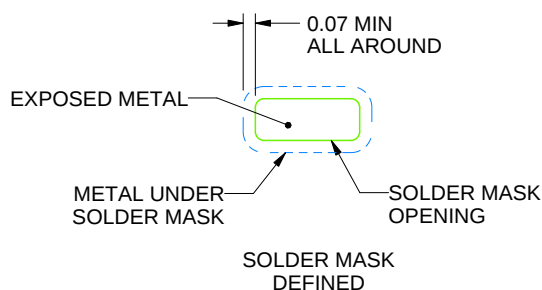
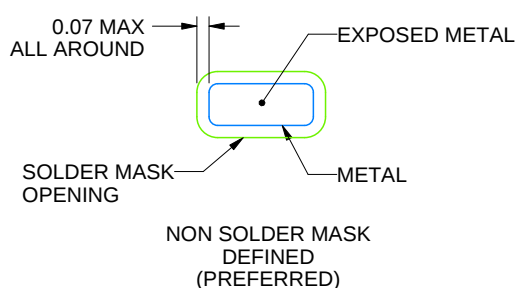
DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4226575/A 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

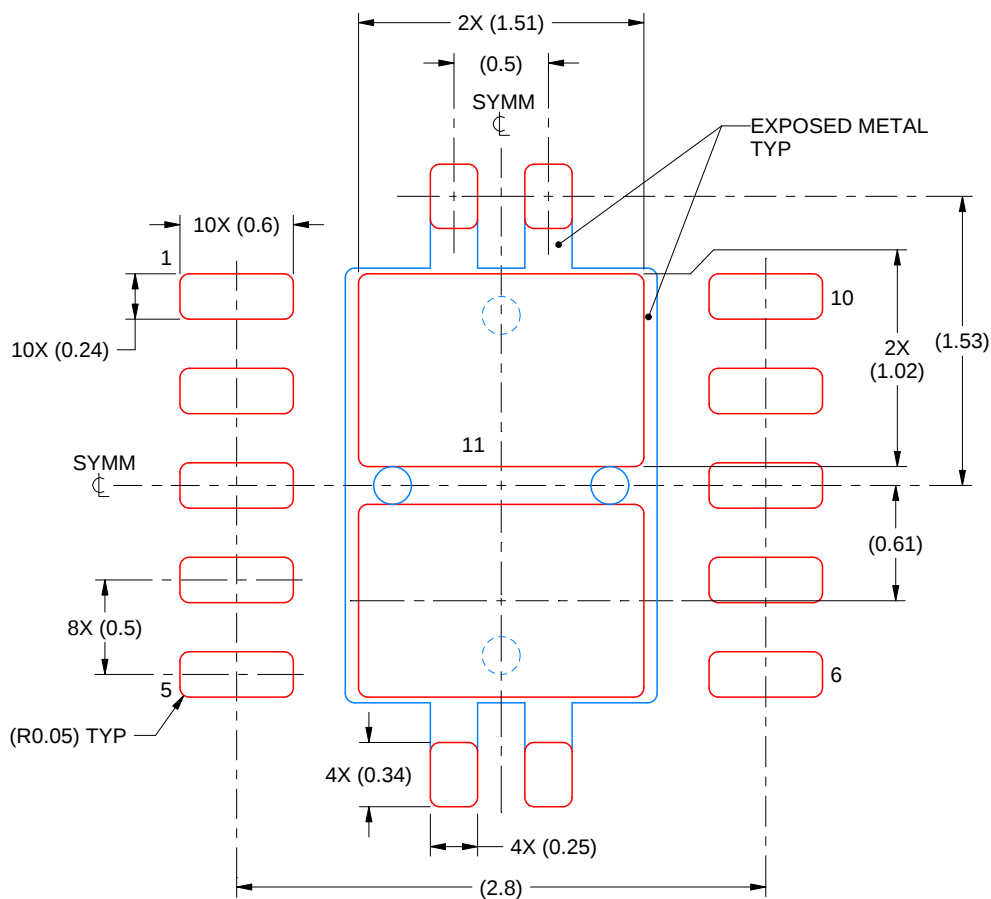
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226575/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated