TIOL111、TIOL111x サージ保護機能内蔵、IO-Link デバイス・トランシーバ

1 特長

- 7V～36V の電源電圧
- PNP、NPN、またはIO-Linkとして構成可能な出力
  - IEC 61131-9 COM1、COM2、COM3データ・レートのサポート
- 低い残留電圧: 250mAで1.75V
- 電流制限を50mA～350mAに設定可能
- ±65Vの過渡耐性、100µs未満
- L+、CQ、L- で最大 60V の逆極性保護
- L+およびCQの内蔵EMC保護
  - ±16kV IEC 61000-4-2 ESD接触放電
  - ±4kV IEC 61000-4-4電気的高速過渡
  - ±1.2kV/500Ω IEC 61000-4-5サージ
- 誘導性負荷の高速消磁: 最大1.5H
- 大きな容量性負荷駆動能力
- CQリーク電流2µA未満
- 静止電流1.5mA未満
- 最大電流20mAの内蔵LDOオプション
  - TIOL111: LDOなし
  - TIOL1113: 3.3V LDO
  - TIOL1115: 5V LDO
- 過熱警告とサーマル保護
- リモート・ウェイクアップ・インジケータ
- 障害インジケータ
- 拡張周囲温度範囲: -40℃～125℃
- 2.5mm×3mmの10ピンVSONパッケージ

2 アプリケーション

- IO-Linkセンサおよびアクチュエータ
- ファクトリ・オートメーション
- プロセス・オートメーション

3 概要

TIOL111(x) ファミリのトランシーバには、産業用の双方向ポイント・ツー・ポイント通信向けに IO-Link インターフェイスが実装されています。デバイスが 3 線式のインターフェイス経由で IO-Link マスタに接続されているとき、マスタはリモート・ノードとの通信を開始してデータを交換でき、TIOL111(x) は通信の完全な物理レイヤとして機能します。

これらのデバイスは、1.2kV (500Ω)のIEC 61000-4-5サージに耐えられ、逆極性保護が内蔵されています。

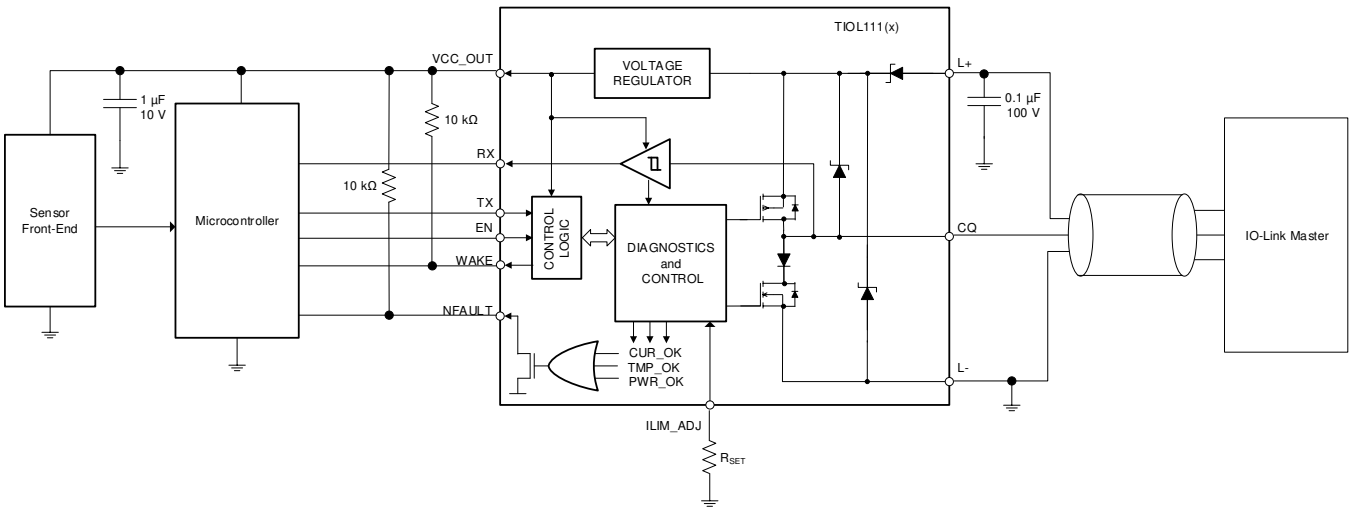
ピンによりプログラム可能なシンプルなインターフェイスにより、コントローラの回路と簡単に接続できます。出力電流制限は、外付けの抵抗を使用して構成できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TIOL111	VSON (10)	2.50mm×3.00mm
TIOL1113		
TIOL1115		

(1) 利用可能なすべてのデバイスについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの図



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4 改訂履歴

Revision C (May 2019) から **Revision D** に変更 — **Page**

- データシートに型番 TIOL1113 および TIOL1115 を追加 ... 1
- TIOL111-3 をすべて TIOL1113 に変更、TIOL111-5 をすべて TIOL1115 に変更 ... 1

Revision B (August 2018) から **Revision C** に変更 — **Page**

- 「*特長*」の「最大 55V の逆極性保護」を「最大 60V の逆極性保護」に変更 ... 1
- Changed Supply voltage From: MIN = -55 V, MAX = 55 V To: MIN = -60 V, MAX = 60 V in the *Absolute Maximum Ratings* ... 5
- Changed the Voltage difference Max value From: 55 V to 60 V *Absolute Maximum Ratings* ... 5
- Changed the I_{REV} test conditions From: up to |55 V| To: up to |60 V| in the *Electrical Characteristics* ... 7
- Changed text From: "pins may not exceed 55 V DC at any time." To: "pins may not exceed 60 V DC at any time." in *Reverse Polarity Protection* ssection ... 15

Revision A (October 2017) から **Revision B** に変更 — **Page**

- Added V_{IM} to the *Electrical Characteristics* table ... 6

2017年7月発行のものから更新 — **Page**

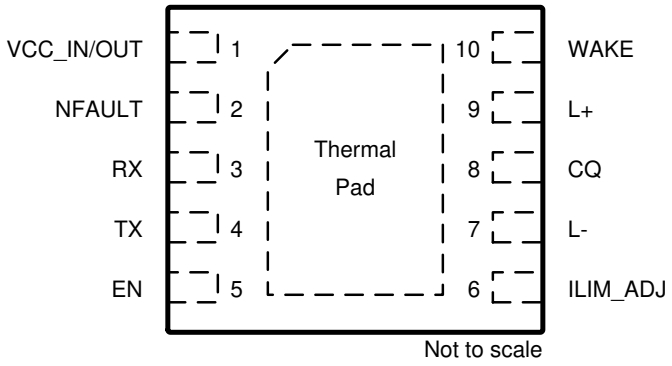
- Changed From: 1.25 mW To: 125 mW in 式 2 ... 21

5 概要（続き）

電圧不足、過電流、過熱状況に対して、フォルト通知および内部的な保護機能が搭載されています。

6 Pin Configuration and Functions

DMW Package
10-Pin (VSON)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IO-Link Interface			
CQ	8	I/O	IO-Link data signal (bidirectional)
L+	9	POWER	IO-Link supply voltage (24 V nominal)
L-	7	POWER	IO-Link ground potential
Local Controller Interface			
EN	5	I	Driver enable input signal from the local controller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
WAKE	10	OPEN-DRAIN	Wake up indicator to the local controller. Connect this pin via pull-up resistor to VCC_IN/OUT.
RX	3	O	Receive data output to the local controller
TX	4	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
Thermal Pad	—	—	Connect to L- for optimal thermal and electrical performance
Internal LDO			
VCC_IN/OUT	1	POWER	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply for option without LDO.
Special Connect Pins			
ILIM_ADJ	6	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and L-.
NFAULT	2	OPEN-DRAIN	Fault indicator output signal to the microcontroller. A low level indicates either an over- current, an undervoltage supply or an overtemperature condition.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for L+ and CQ	–60	60	V
	Transient pulse width < 100 µs for L+ and CQ	–65	65	V
Voltage difference	$\lvert V_{(L+)} - V_{(CQ)} \rvert$		60	V
Logic supply voltage (TIOL111)	VCC_IN	–0.3	6	V
Input logic voltage	TX, EN, ILIM_ADJ	–0.3	6	V
Output current	RX, WAKE, NFAULT	–5	5	mA
Storage temperature, T_{stg}		-55	170	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with reference to the L- pin, unless otherwise specified.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
		Contact discharge, per IEC 61000-4-2(2)(3)	Pins L+, CQ and L-	±16000	
		Electrical fast transient, per IEC 61000-4-4(2)		±4000	
		Surge protection with 500 Ω, per IEC 61000-4-5; 1.2/50 µs (2)		±1200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Minimum 100-nF capacitor is required between L+ and L-. Minimum 1-µF capacitor is required between VCC_IN/OUT and L-.
(3) Passing level is ±4500 V if the device is powered and EN=TX=HIGH.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(L+)}$	Supply voltage		7	24	36	V
$V_{(VCC\_IN)}$	Logic level input voltage (TIOL111 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R_{SET}	External resistor for CQ current limit		0		100	kΩ
$1/t_{BIT}$	Data rate (Communication mode)				250	kbps
$I_{(VCC\_OUT)}$	LDO output current (TIOL1113 and TIOL1115 only)				20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Junction temperature				150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TIOL111(x) DMW (10 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (L+)						
$I_{(L+)}$	Quiescent supply current	EN = LOW, no load		1	1.5	mA
		EN = HIGH, no load		2	2.7	mA
LOGIC-LEVEL INPUTS (EN, TX)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
R_{PD}	Pull-down (EN) resistance			100		kΩ
R_{PU}	Pull-up (TX) resistance			200		kΩ
CONTROL OUTPUTS (WAKE, NFAULT)						
V_{OL}	Output logic low voltage	I_O = 4 mA			0.5	V
I_{OZ}	Output high impedance leakage	Output in Hi-Z, V_O = 0 V or VCC_IN/OUT	–1		1	µA
DRIVER OUTPUT (CQ)						
$V_{DS(ON)}$	High-side driver residual voltage	I = 250 mA			1.75	V
		I = 200 mA			1.5	V
		I = 100 mA			1.1	V
	Low-side driver residual voltage	I = 250 mA			1.75	V
		I = 200 mA			1.5	V
		I = 100 mA			1.1	V
V_{IM}	Voltage between CQ and L- during IO-Link Master wake-up pulse	High-side configuration, R_{load} = 26 Ω between CQ and L-, 18 V ≤ $V_{(L+)}$ ≤ 30 V	14.5			V
		Low-side configuration, R_{load} = 24 Ω between CQ and L+, $V_{(L+)}$ = 20 V			4	V
		Low-side configuration, R_{load} = 44 Ω between CQ and L+, $V_{(L+)}$ = 30 V			4	V
I_{OZ}	CQ leakage	EN = LOW, 0 ≤ $V_{(CQ)}$ ≤ ($V_{(L+)}$ - 0.1 V)	–2		2	µA
$I_{O(LIM)}$	Driver output current limit	R_{SET} = 100 kΩ	35	50	70	mA
		R_{SET} = 0 kΩ	300	350	400	mA
		R_{SET} = OPEN(1)	300	350	400	mA

(1) Current fault indication will be active. Current fault auto recovery will be de-activated.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RECEIVER INPUT (CQ)							
$V_{(THH)}$	Input threshold “H”	$V_{(L+)}$ > 18 V		10.5		13	V
$V_{(THL)}$	Input threshold “L"			8		11.5	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)				0.75		V
$V_{(THH)}$	Input threshold “H”	$V_{(L+)}$ < 18 V		See Note (2)		See Note (3)	V
$V_{(THL)}$	Input threshold “L"			See Note (4)		See Note (5)	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)				0.75		V
V_{OL}	RX output low voltage	I_{OL} = 4 mA				0.4	V
V_{OH}	RX output high voltage	I_{OL} = –4 mA		VCC_IN/ OUT–0.5			V
PROTECTION CIRCUITS							
$V_{(UVLO)}$	L+ under voltage lockout	L+ falling; NFAULT = Hi-Z				6	V
		L+ rising; NFAULT = LOW				6.5	V
$V_{(UVLO,HYS)}$	L+ under voltage hysteresis	Rising to falling threshold		100			mV
$V_{(UVLO\_IN)}$	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z			2.4		V
		VCC_IN rising; NFAULT = LOW			2.5		V
$V_{(UVLO,HYS)}$	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold			100		mV
$T_{(WRN)}$	Thermal warning	Die temperature T_J		125			°C
$T_{(SDN)}$	Thermal shutdown			150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown				10		°C
I_{REV}	Leakage current in reverse polarity	EN = LOW, TX=x; $V_{(CQ)}$ < $V_{(L-)}$ or $V_{(CQ)}$ > $V_{(L+)}$, up to |36 V|				50	µA
		EN = LOW, TX=x; $V_{(CQ)}$ < $V_{(L-)}$ or $V_{(CQ)}$ > $V_{(L+)}$, up to |60 V|				80	µA
		EN = HIGH, TX = LOW; $V_{(CQ\ to\ L+)}$ = 3 V				550	µA
		EN = HIGH, TX = HIGH; $V_{(CQ\ to\ L-)}$ = -3 V				10	µA
LINEAR REGULATOR (LDO)							
$V_{(VCC\_OUT)}$	Voltage regulator output	TIOL1115		4.75	5	5.25	V
		TIOL1113		3.13	3.3	3.46	V
$V_{(DROP)}$	Voltage regulator drop-out voltage ($V_{(L+)}$ – $V_{(VCC\_OUT)}$)	I_{CC} = 20 mA load current	TIOL1115			1.9	V
			TIOL1113			2.3	V
REG	Line regulation ($dV_{(VCC\_OUT)}$/dV(L+))	$I_{(VCC\_OUT)}$ = 1 mA				1.7	mV/V
L_{REG}	Load regulation ($dV_{(VCC\_OUT)}$/$V_{(VCC\_OUT)}$)	$V_{(L+)}$ = 24 V, $I_{(VCC\_OUT)}$ = 100 µA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)}$ = 20 mA			40		dB

(2) V_{THH} (min) = 5 V + (11/18) [$V_{(L+)}$ - 8 V]
(3) V_{THH} (max) = 6.5 V + (13/18) [$V_{(L+)}$ - 8 V]
(4) V_{THL} (min) = 4 V + (8/18) [$V_{(L+)}$ -8 V]
(5) V_{THL} (max) = 6 V + (11/18) [$V_{(L+)}$ -8 V]

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SECTION NAME						
t_{PLH}, t_{PHL}	Driver propagation delay	See 図 6 See 図 7 See 図 8 R_L = 2 kΩ C_L = 5 nF $R_{(SET)}$ = 0 Ω		600	800	ns
$t_{P(skew)}$	Driver propagation delay skew. $\lvert t_{PLH} - t_{PHL} \rvert$			100		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	µs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	µs
t_r, t_f	Driver output rise, fall time				150	ns
$\lvert t_r - t_f \rvert$	Difference in rise and fall time				50	ns
t_{WU1}	Wake-up recognition begin	See 図 10	45	60	75	µs
t_{WU2}	Wake-up recognition end		85	100	135	µs
t_{pWAKE}	Wake-up output delay				140	µs
t_{SC}	Current fault blanking time		175	200		µs
t_{pSC}	Current fault indication delay				260	µs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	CQ re-enable delay after UVLO (1)	$V_{(UVLO)}$ rising threshold crossing time to CQ enable time	10	30	50	ms
RECEIVER						
t_{ND}	Noise suppression time (2)				250	ns
t_{PLH}, t_{PHL}	Receiver propagation delay	See 図 9 15-pF load on RX		150	300	ns

(1) CQ output remains Hi-Z for this time
(2) Noise suppression time is defined as the permissible duration of a receive signal above/below the detection threshold without detection taking place.

7.7 Typical Characteristics

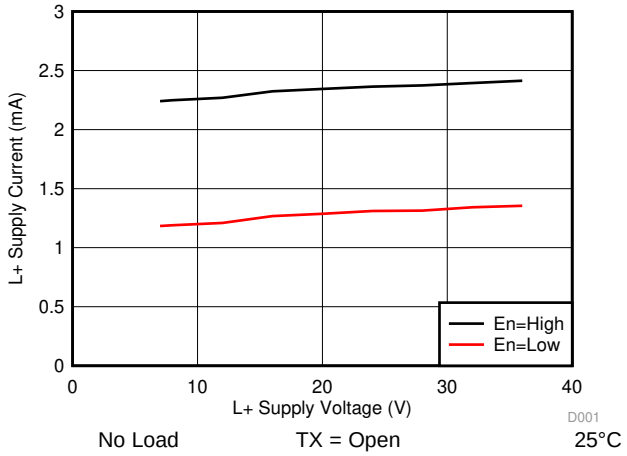


図 1. Supply Current vs Supply Voltage

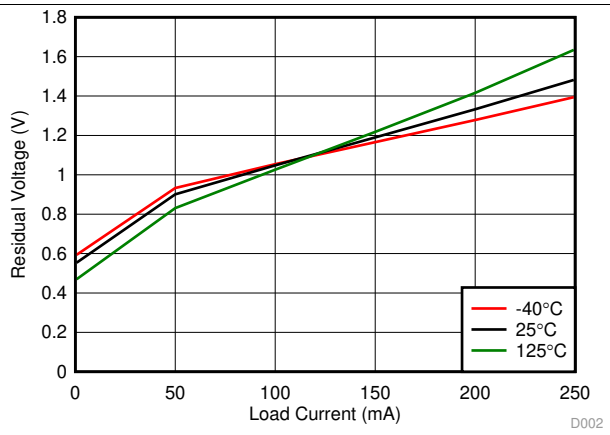


図 2. Residual Voltage vs Load Current: High Side

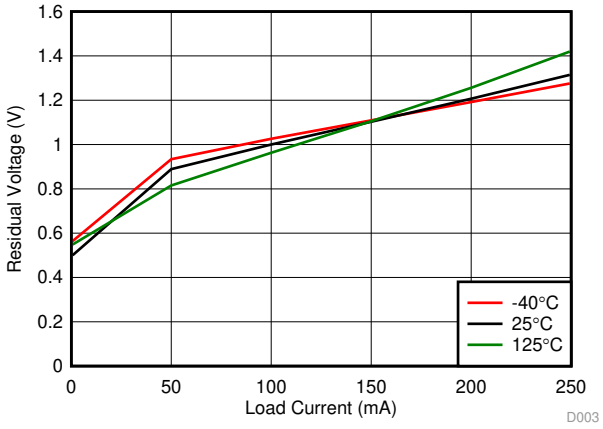


図 3. Residual Voltage vs Load Current: Low Side

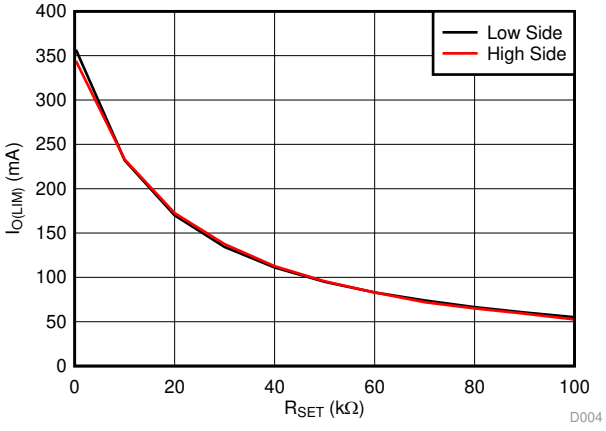


図 4. Current Limit vs R_{SET}

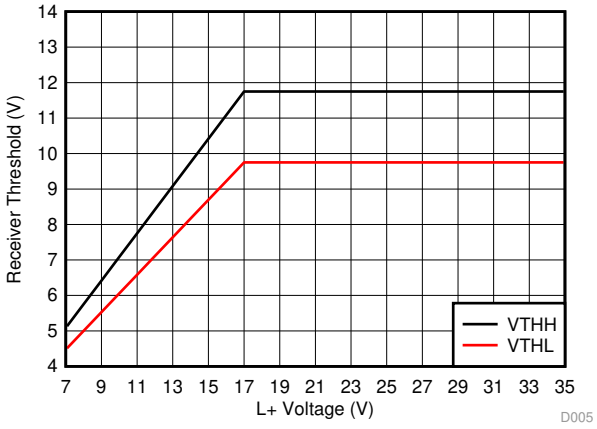


図 5. Receiver Threshold Boundaries

8 Parameter Measurement Information

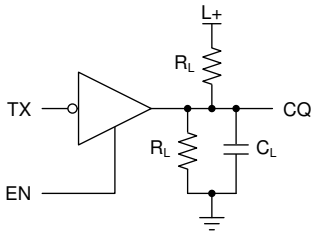


図 6. Test Circuit for Driver Switching

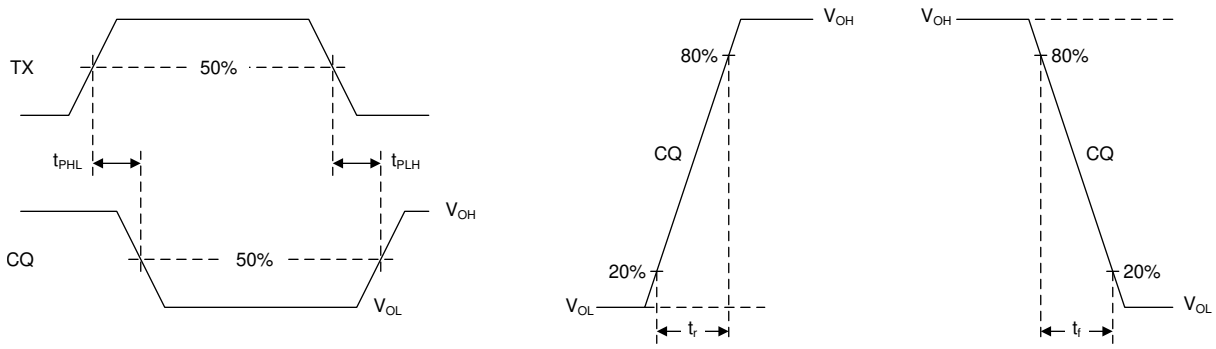


図 7. Waveforms for Driver Output Switching Measurements

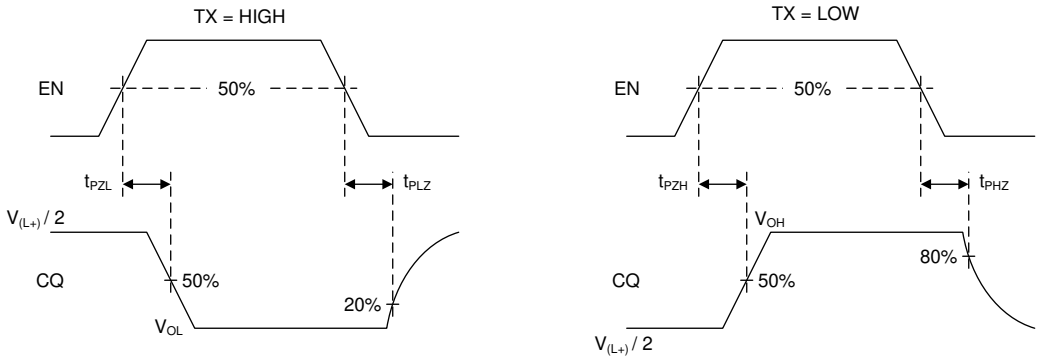


図 8. Waveforms for Driver Enable/Disable Time Measurements

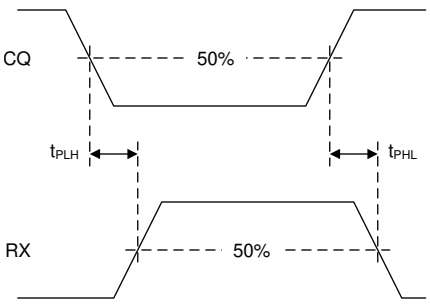


図 9. Receiver Switching Measurements

Parameter Measurement Information (continued)

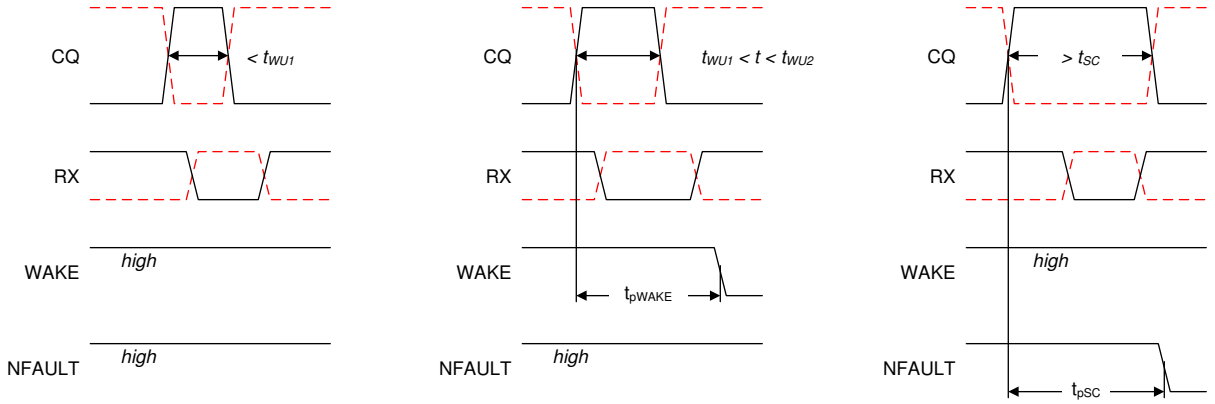


図 10. Overcurrent and Wake Conditions for EN = H, TX = H (Full Lines); and TX = L (Red Dotted Lines)

9 Detailed Description

9.1 Overview

図 11 shows that the TIOL111 or TIOL111x driver output (CQ) can be used in either push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (TX) input pins. The internal receiver converts the 24-V signal on the CQ line to standard logic levels on the receive data (RX) pin. A simple parallel interface is used to receive/transmit data and status information between the slave and the local controller.

These devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ±65-V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system level design by reducing external protection circuitry.

TIOL111 or TIOL111x transceivers implement protection features for overcurrent, overvoltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The devices derive the low-voltage supply from the IO-Link L+ voltage (24 V nominal) via an internal linear regulator to provide power to the local controller and sensor circuitry.

9.2 Functional Block Diagrams

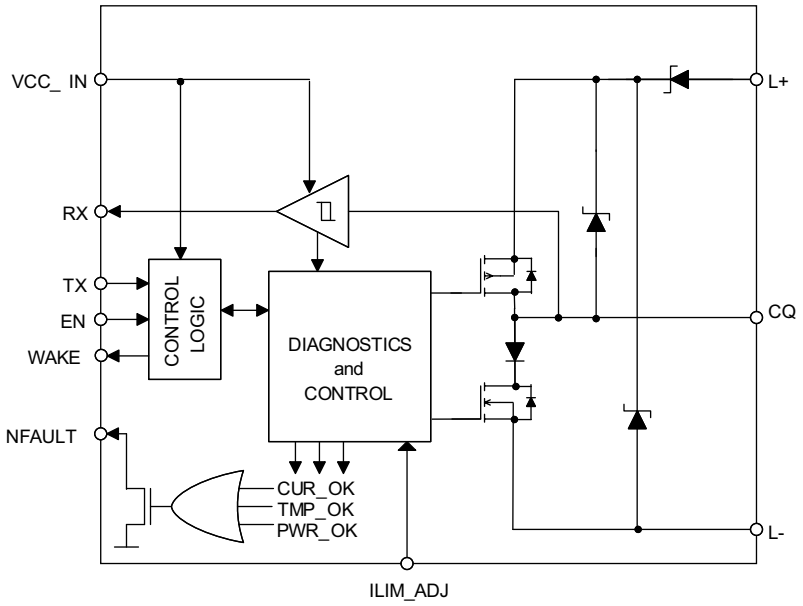


図 11. Block Diagram TIOL111

Functional Block Diagrams (continued)

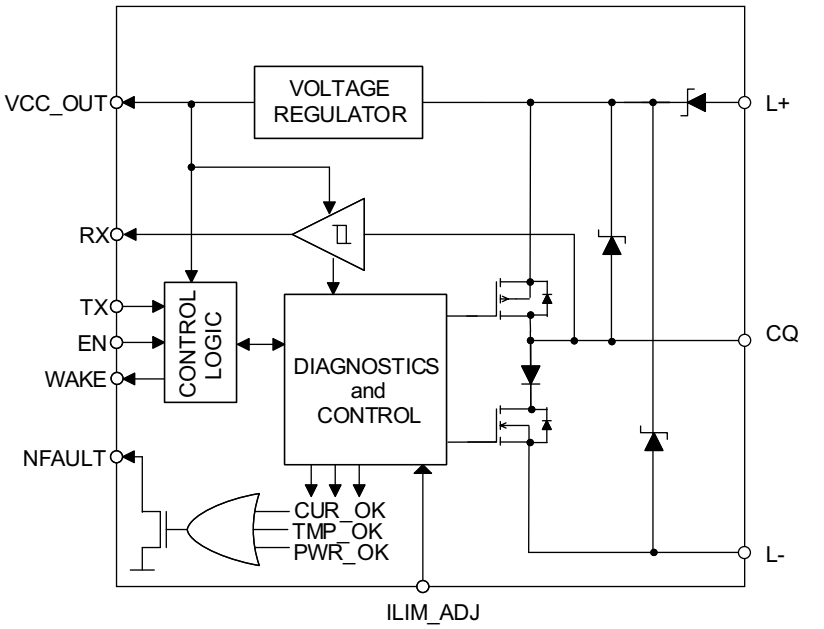


図 12. Block Diagram TIOL111x

9.3 Feature Description

9.3.1 Wake Up Detection

The TIOL111(x) may be operated in IO-Link mode or Standard Input / Output (SIO) mode. If the device is in SIO mode and the master node wants to initiate communication with the device node, the master drives the CQ line to the opposite of its present state, and will either sink or source the wake up current (≥ 500 mA) for the wake-up duration (typically 80 µs) depending on the CQ logic level as per the IO-Link specification. The TIOL111(x) detects this wake-up condition and communicates to the local microcontroller via the WAKE pin. The IO-Link communication specification requires the device node to switch to receive mode within 500 µs after receiving the wake-up signal.

For overcurrent conditions shorter or longer than a valid wake-up pulse, the WAKE pin remains in a high-impedance (inactive) state. This is illustrated in 図 10.

9.3.2 Current Limit Configuration

The output current can be configured with an external resistor on ILIM_ADJ pin. The maximum settable current limit is 300 mA. This maximum setting specifies a minimum of 300 mA over temperature and voltage.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

表 1. Current Limit Configuration

ILIM_ADJ Pin Condition	CQ Current Limit	NFAULT Indication During Fault	Output Disable and Auto Recovery
R_{SET} resistor to L-	Variable	Yes	Yes
Connected to L-	300 mA	Yes	Yes
OPEN	300 mA	Yes	No

9.3.3 Current Fault Detection, Indication and Auto Recovery

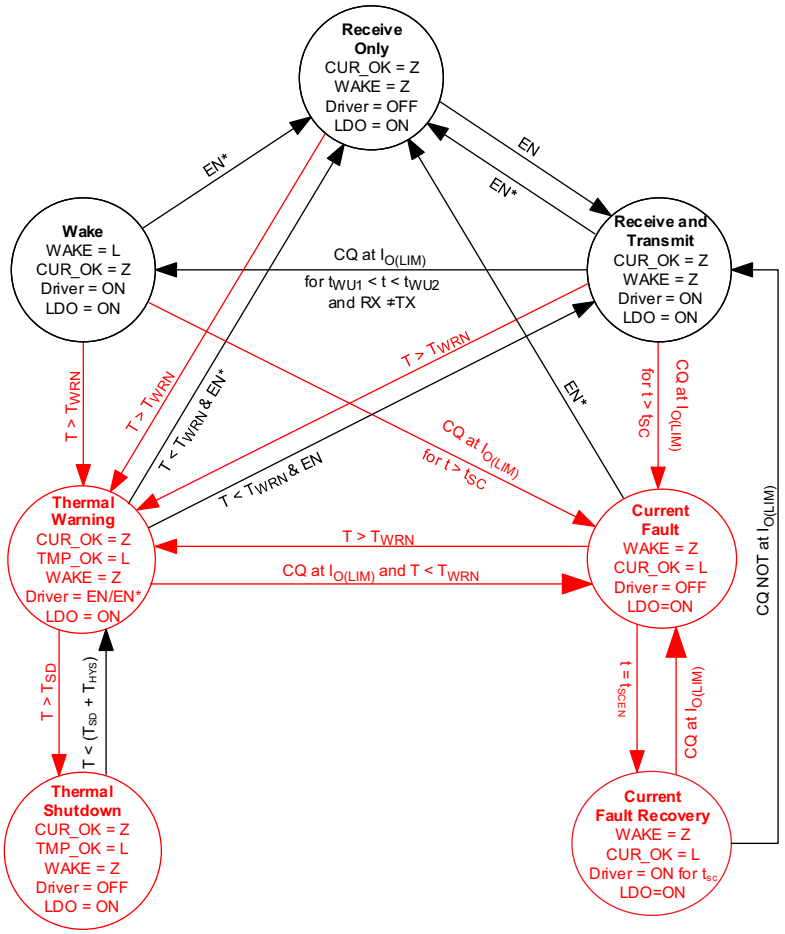
If the output current at CQ exceeds the internally-set current limit $I_{O(LIM)}$ for a duration longer than t_{SC}, the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN. See 表 5. Toggling EN will clear NFAULT.

9.3.4 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and TX pins.

9.3.5 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



NFAULT = [CUR_OK && PWR_OK && TMP_OK]

図 13. Device State Diagram

9.3.6 Transceiver Function Tables

表 2. Driver Function

EN	TX	CQ	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	CQ is sourcing current (high-side drive)
H	H / Open	L	CQ is sinking current (low-side drive)

表 3. Receiver Function

CQ VOLTAGE	RX	COMMENT
$V_{(CQ)} < V_{(THL)}$	H	Normal receive mode, input low
$V_{(THL)} < V_{(CQ)} < V_{(THH)}$	?	Indeterminate output, may be either high or low
$V_{(THH)} < V_{(CQ)}$	L	Normal receive mode, input high
Open	?	Indeterminate output, may be either high or low

表 4. Wake-Up Function ($t_{WU1} < t < t_{WU2}$)

EN	TX	CQ CURRENT	WAKE	COMMENT
L / Open	X	X	Z	Device is in ready-to-receive state
H	H / Open	$\lvert I_{(CQ)} \rvert \geq 500$ mA	L	Device receives high-level wake-up request from IO-Link Master
H	L	$\lvert I_{(CQ)} \rvert \geq 500$ mA	L	Device receives low-level wake-up request from IO-Link Master

表 5. Current Limit Indicator Function ($t > t_{SC}$)

EN	TX	CQ CURRENT	NFAULT	COMMENT
H	H / Open	$\lvert I_{(CQ)} \rvert > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$\lvert I_{(CQ)} \rvert < I_{O(LIM)}$	Z	Normal operation
H	L	$\lvert I_{(CQ)} \rvert > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$\lvert I_{(CQ)} \rvert < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, Current limit indicator is inactive

9.3.7 The Integrated Voltage Regulator (LDO)

The TIOL1113 and TIOL1115 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for L+ voltages in the range of 7 V to 36 V with respect to L-. The LDO is capable of delivering up to 20 mA.

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μF.

The voltage regulator has an internal 35-mA current limit to protect against initial startup inrush current due to large decoupling capacitors and accidental short circuit conditions.

9.3.8 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the L+, CQ and L- pins. The maximum voltage between any of the pins may not exceed 60 V DC at any time.

図 14 and 図 15 shows all the possible connection combinations.

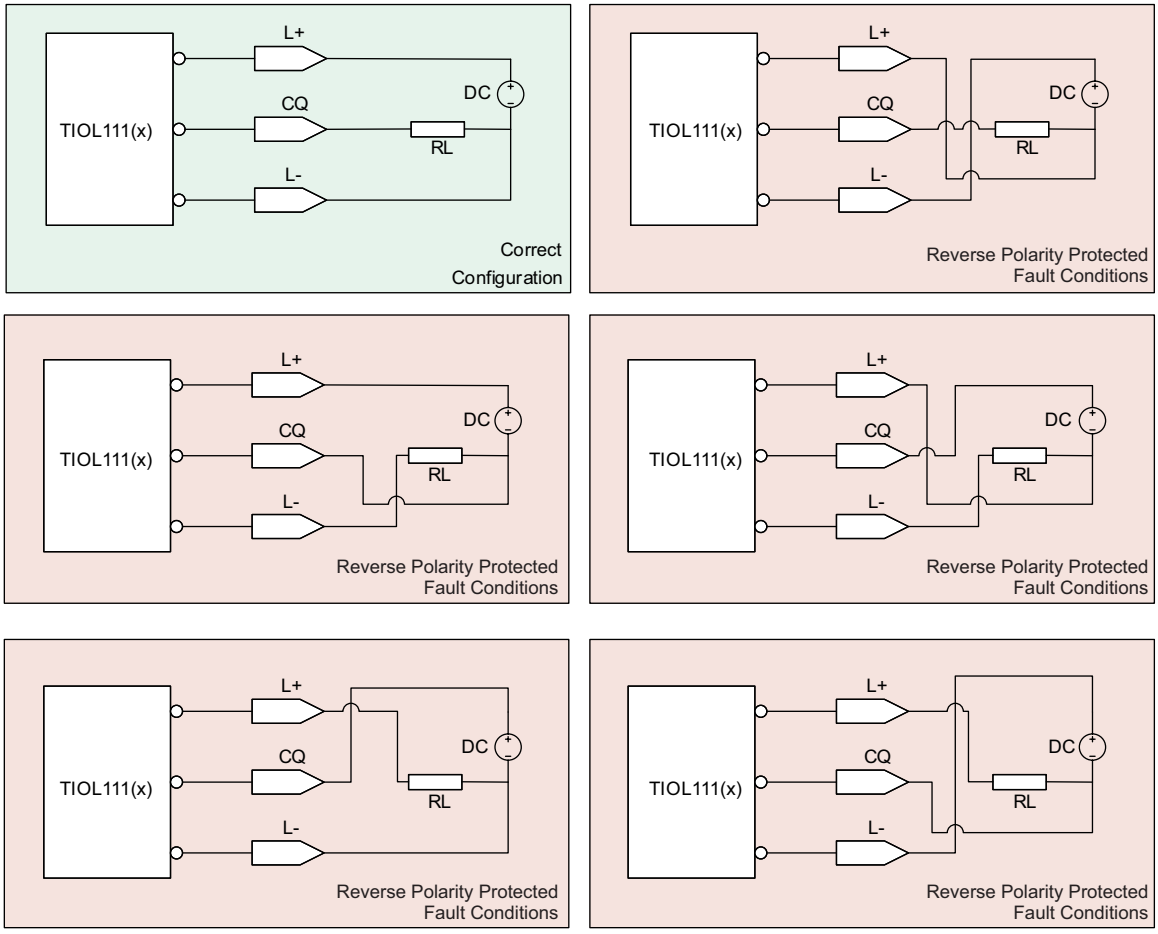


図 14. High-Side Driver Configuration

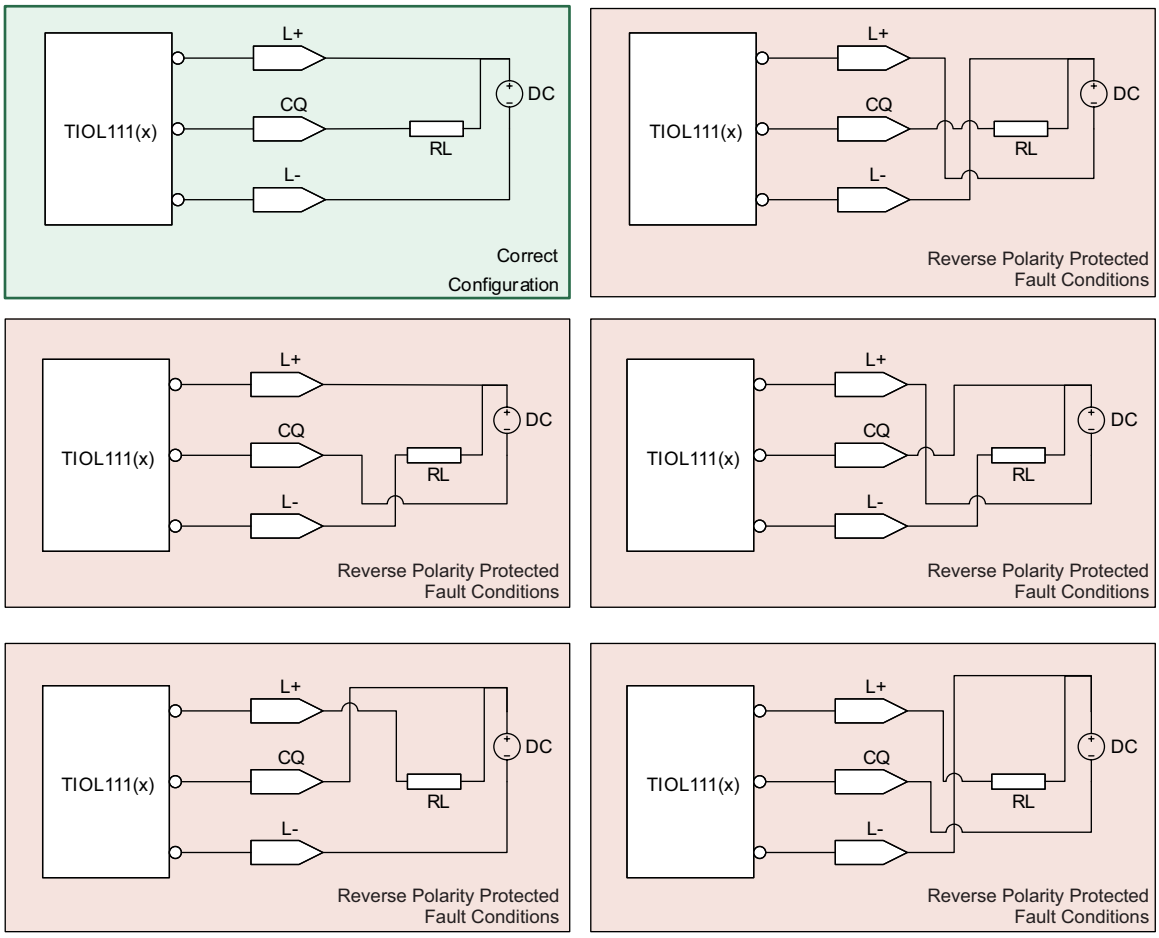
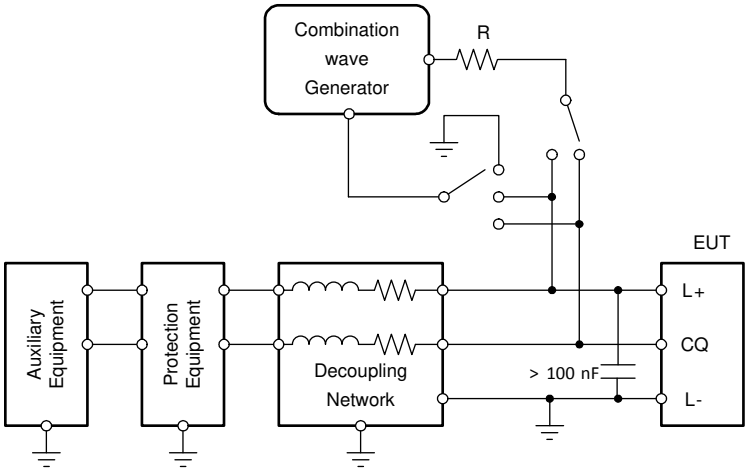


図 15. Low-Side Driver Configuration

9.3.9 Integrated Surge Protection and Transient Waveform Tolerance

The L+ and CQ pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 µs IEC 61000-4-5 surge with a source impedance of 500 Ω. The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between L+ and L-, and 1 µF between VCC_IN/OUT and L-.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to ±65-V transient pulses < 100 µs.



1.2/50 – 8/20 µs CWG

R = 500 Ω

図 16. Surge Test Setup

9.3.10 Power Up Sequence (TIOL111)

VCC_IN and L+ domains can be powered up in any sequence. In the event of L+ is powered and VCC_IN is not, the CQ pin will remain in high impedance.

9.3.11 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the L+ voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to L+. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$, NFAULT is pulled low, the LDO is turned off and the CQ output is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present) and the LDO will be enabled immediately. The CQ output is turned on after $T_{(UVLO)}$ delay.

9.4 Device Functional Modes

These devices can operate in three different modes.

9.4.1 NPN Configuration (N-Switch SIO Mode)

Set TX pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on CQ.

9.4.2 PNP Configuration (P-Switch SIO Mode)

Set TX pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on CQ.

Device Functional Modes (continued)

9.4.3 Push-Pull, Communication Mode

Set EN pin high and toggle TX as control for realizing the function of a push-pull output on CQ. 表 6, 表 7 and 表 8 summarize the pin configurations to accomplish the functional modes.

表 6. NPN Mode

EN	TX	CQ
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 7. PNP Mode

EN	TX	CQ
L / Open	L	Hi-Z
H	L	P-Switch

表 8. Push-Pull, Communication Mode

EN	TX	CQ
L / Open	X	Hi-Z
H	H	N-Switch
H	L	P-Switch

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

When TIOL111(x) is connected to an IO-Link master through a three-wire interface (図 17), the master can initiate communication and exchange data with a remote node with the TIOL111(x) IO-Link transceiver acting as a complete physical layer for the communication.

10.2 Typical Application

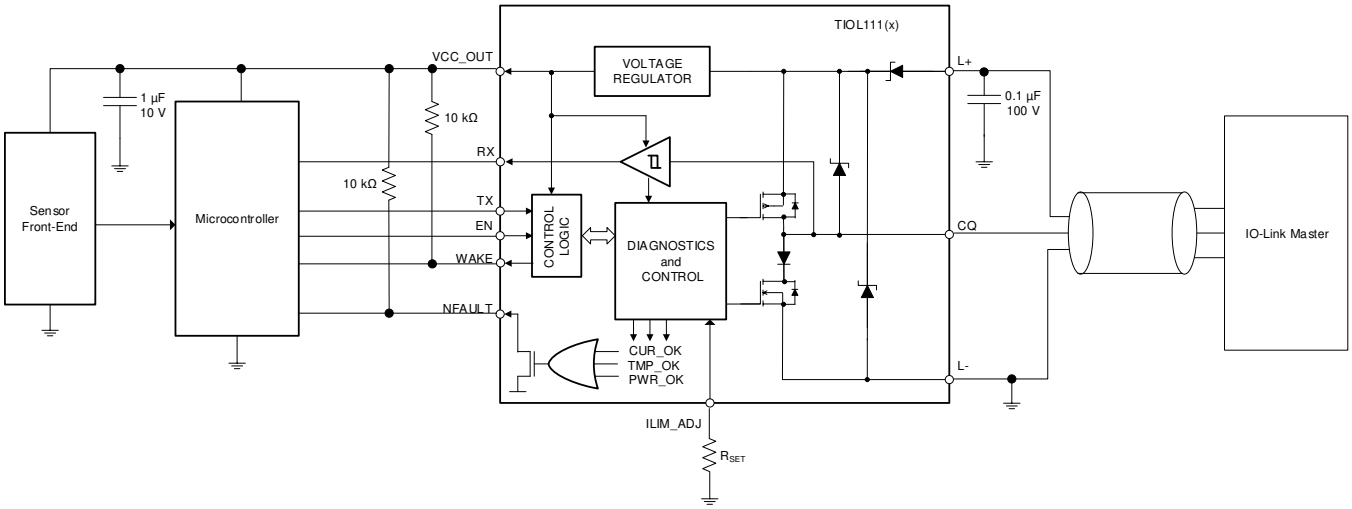


図 17. Typical Application Schematic

10.2.1 Design Requirements

TIOL111 and TIOL111x IO-Link transceivers can be used in slave devices communicating with an IO-Link master, or as standard digital outputs to either sense or drive a wide range of sensors and loads. 表 9 shows recommended components for a typical system design.

表 9. Design Parameters

PARAMETERS	VALUE
Input voltage range (L+)	24 V, 30 V (max)
Output current (CQ)	200 mA
Output voltage (VCC_OUT), Pick TIOL1115	5 V
Maximum LDO output current ($I_{VCC(OUT)}$)	5 mA
Pull-up resistors for NFAULT and WAKE	10 kΩ
L+ decoupling capacitor	0.1 µF / 100 V
LDO output capacitor	1 µF / 10 V
ILIM_ADJ resistor (R_{SET})	10 kΩ
Maximum Ambient Temperature, T_A	105 °C

10.2.2 Detailed Design Procedure

10.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- The maximum driver output current limit, $I_{O(LIM)}$ = 250 mA (allowed for current limit tolerance).
- The maximum voltage drop is given with $V_{DS(ON)}$ = 1.75 V.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \, x \, I_{O(LIM)} = 1.75V \, x \, 250 \, mA = 437.5 \, mW \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = \left(V_{L+} - V_{VCC\_OUT}\right) \text{ x } I_{VCC\_OUT} = (30 - 5)\text{V x 5 mA} = 125 \text{ mW} \quad (2)$$

Total power dissipation,

$$PD = PD_{OP} + PD_{LDO} = 437.5 \, mW + 125 \, mW = 562.5 \, mW \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of θ_{JA} = 68.1°C/W (taken from the *Thermal Information* table) to receive the difference between junction temperature, T_J, and ambient temperature, T_A:

$$\Delta T = T_J - T_A = PD \text{ x } \theta_{JA} = 562.5 \, mW \, x \, 68.1°C/W = 38.3°C \quad (4)$$

Add this value to the maximum ambient temperature of T_A = 105°C to receive the final junction temperature:

$$T_{J-max} = T_{A-max} + \Delta T = 105°C + 38.3°C = 143.3°C \quad (5)$$

As long as $T_{J\text{-max}}$ is below the recommended maximum value of 150°C, no thermal shutdown will occur. However, thermal warning may occur as the junction temperature is greater than T_{WRN}.

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

10.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the CQ output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \text{ x } t_{SC}]}{V_{(L+)}} \quad (6)$$

Higher capacitive loads can be driven if a series resistor is connected between the CQ output and the load. Capacitive loads can be connected to L- or L+.

10.2.2.3 Driving Inductive Loads

The TIOL111(x) family is capable of magnetizing and demagnetizing inductive loads up to 1.5H. These devices contain internal circuitry that enables fast demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the CQ output is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the CQ pin. This voltage is clamped internally at about -75 V.

Similarly in N-switch configuration, the load inductor L is magnetized when the CQ output is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the CQ pin. This voltage is clamped internally at about 75 V.

The equivalent protection circuits are shown in 図 18 and 図 19. The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(L+)}}{I_{O(LIM)}} \quad (7)$$

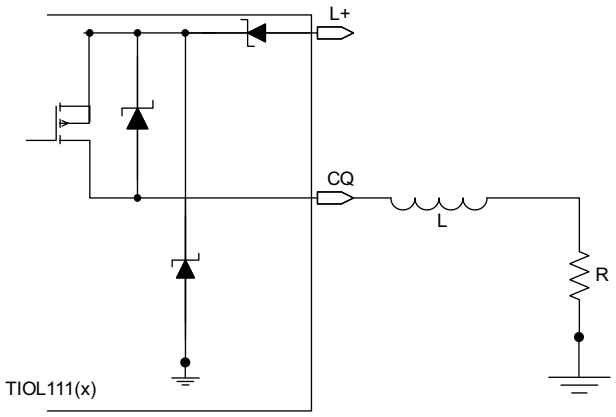


図 18. P-Switch Mode

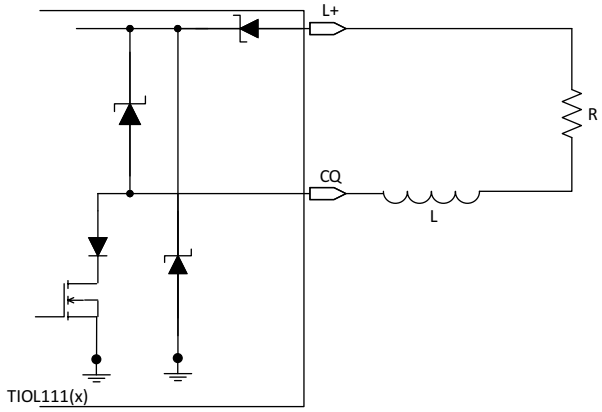
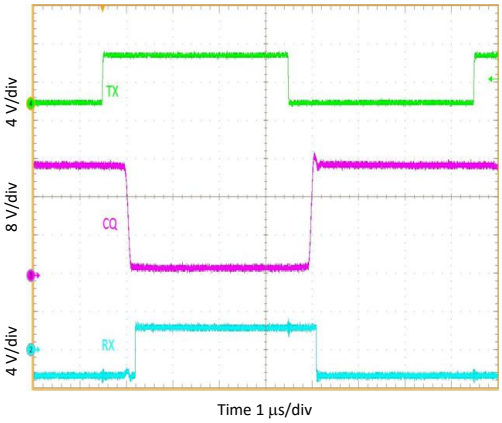


図 19. N-Switch Mode

10.2.3 Application Curves



125 kHz

図 20. CQ in Communication Mode

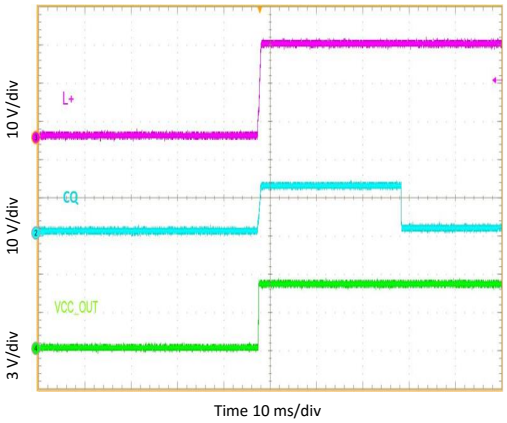


図 21. CQ Power Up Delay, Low Side Mode

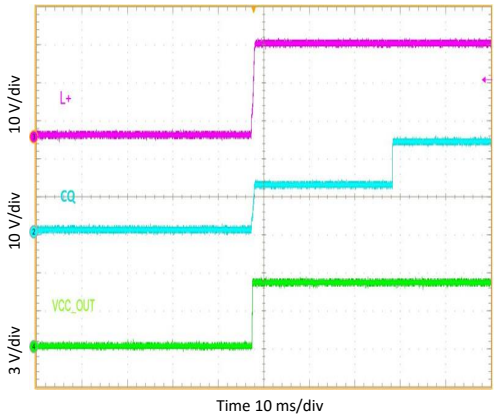


図 22. CQ Power Up Delay, High Side Mode

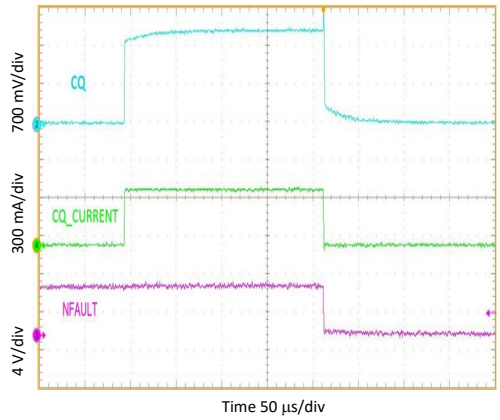


図 23. CQ in Current Fault, Low Side Mode

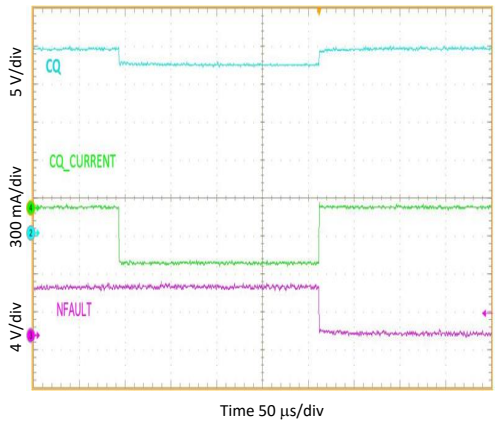


図 24. CQ in Current Fault, High Side Mode

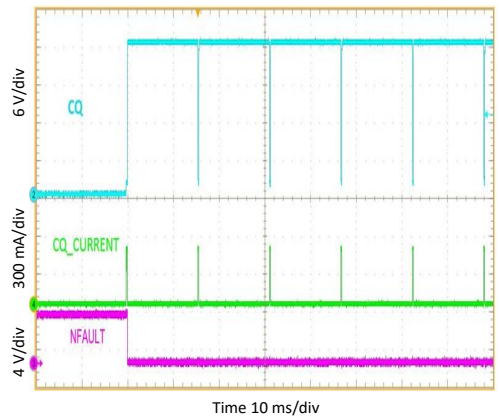


図 25. CQ in Current Fault Auto Recovery, Low Side Mode

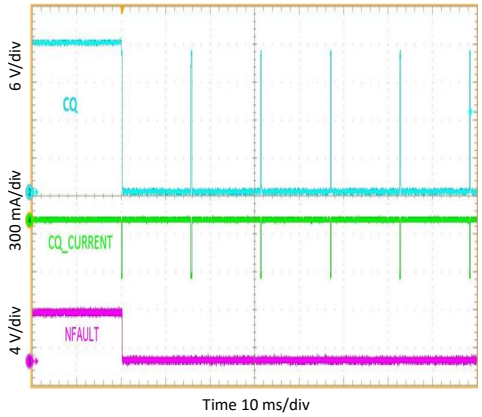


図 26. CQ in Current Fault Auto Recovery, High Side Mode

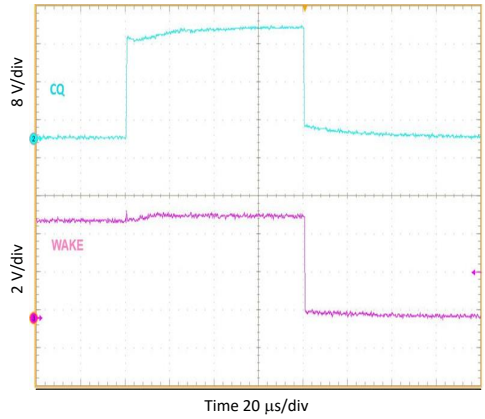


図 27. IO-Link WAKE, Low Side Mode

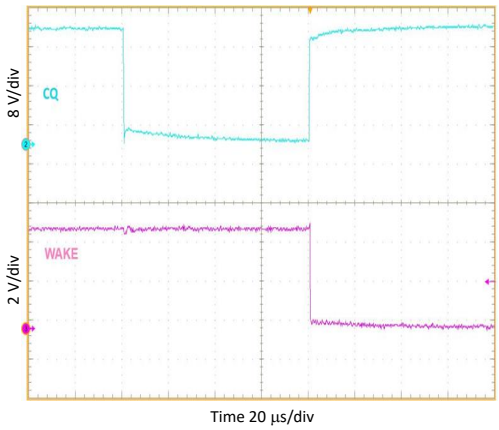
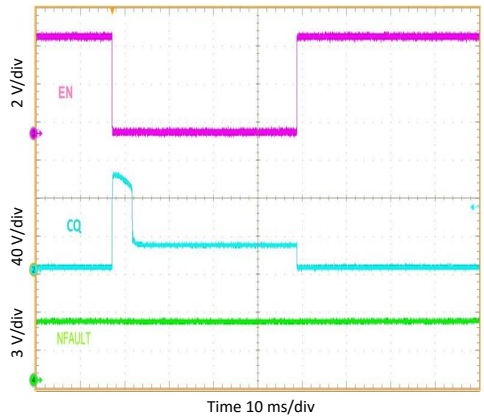
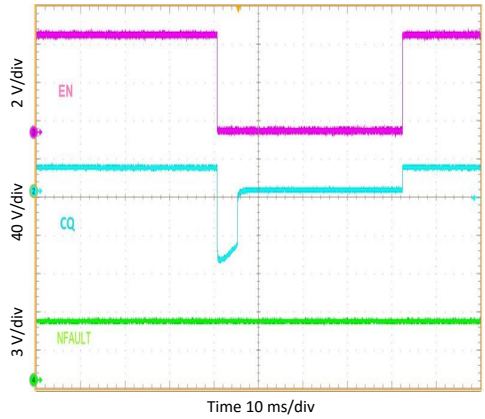


図 28. IO-Link WAKE, High Side Mode



1.5-H Inductor With 100 Ω R_{SET} = OPEN

図 29. CQ Driving, Low Side Mode



1.5-H Inductor With 100 Ω R_{SET} = OPEN

図 30. CQ Driving, High Side Mode

11 Power Supply Recommendations

The TIOL111 and TIOL111x transceivers are designed to operate from a 24-V nominal supply at L+, which can vary by +12 V and -17 V from the nominal value to remain within the device's recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

12 Layout

12.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as power ground layer for L-, layer 3 for the 24-V supply plane (L+), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to L- with maximum amount of thermal vias for best thermal performance.
- Use entire planes for L+, VCC_IN/OUT and L- to assure minimum inductance.
- The L+ terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor. The recommended minimum capacitor value is 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- The optimum placement of the capacitor is closest to the transceiver's L+ and L- terminals to reduce supply drops during large supply current loads. See 図 31 for a PCB layout example.
- Connect all open-drain control outputs via 10 kΩ pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and L-.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, ≥ 1-µF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

12.2 Layout Example

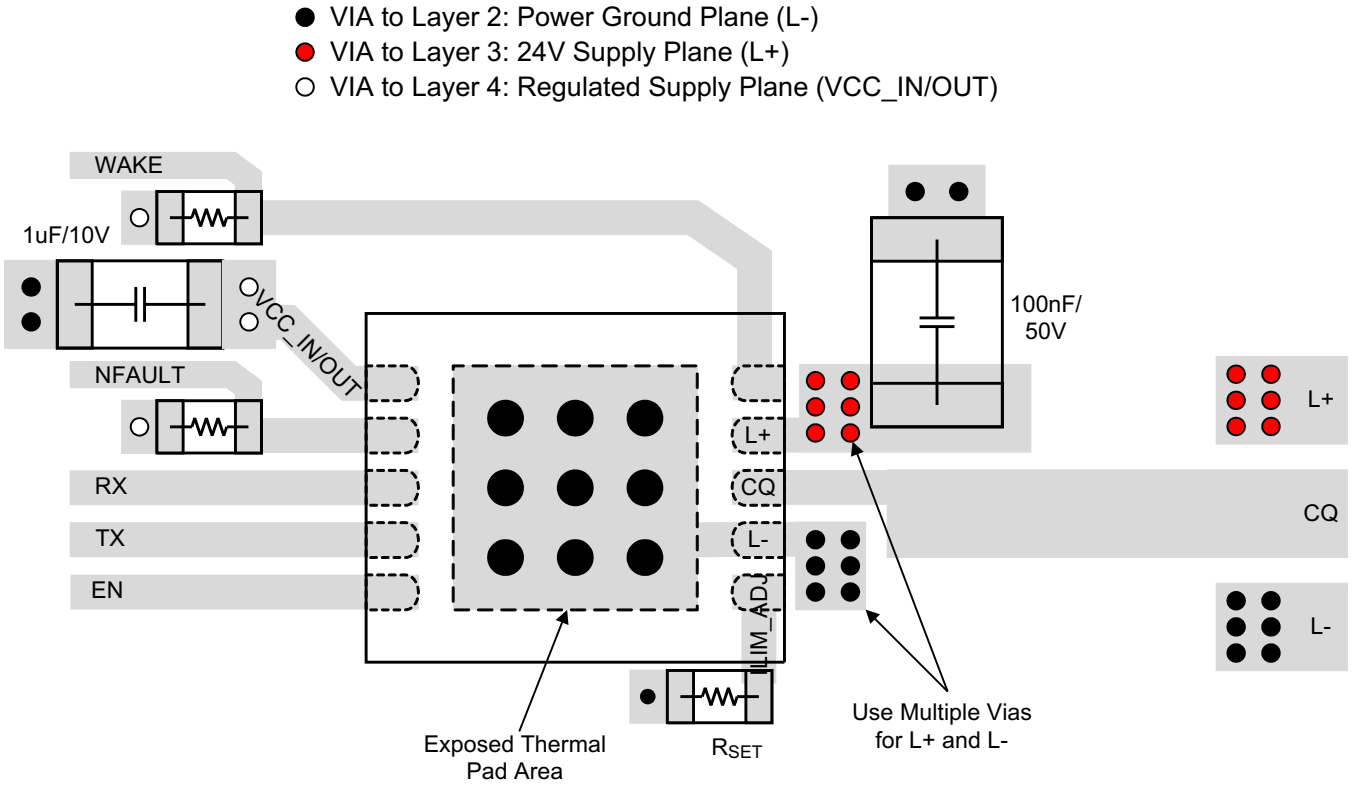


図 31. Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商標

E2E is a trademark of Texas Instruments.

13.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TIOL1113DMWR	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1113
TIOL1113DMWR.A	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1113
TIOL1113DMWR.B	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TIOL1113DMWT	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1113
TIOL1113DMWT.A	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1113
TIOL1113DMWT.B	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TIOL1115DMWR	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1115
TIOL1115DMWR.A	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1115
TIOL1115DMWR.B	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TIOL1115DMWT	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1115
TIOL1115DMWT.A	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1115
TIOL1115DMWT.B	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TIOL111DMWR	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL111
TIOL111DMWR.A	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL111
TIOL111DMWR.B	Active	Production	VSON (DMW) | 10	1500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TIOL111DMWT	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL111
TIOL111DMWT.A	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL111
TIOL111DMWT.B	Active	Production	VSON (DMW) | 10	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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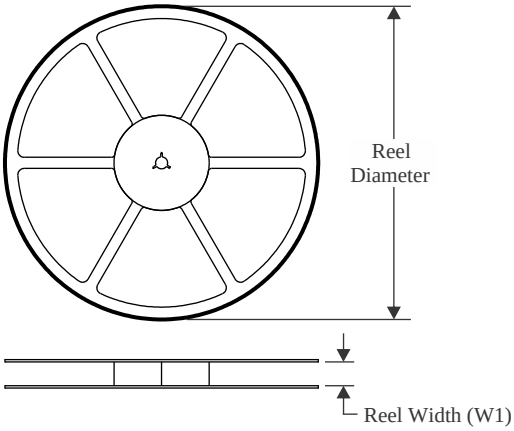
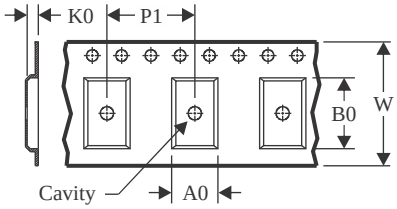
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

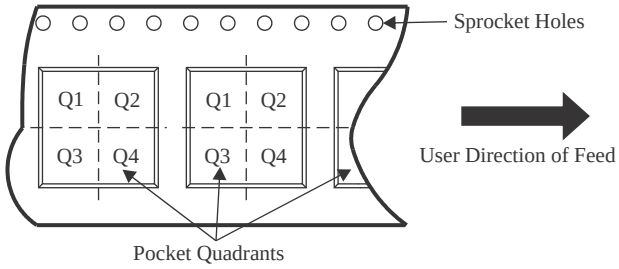


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

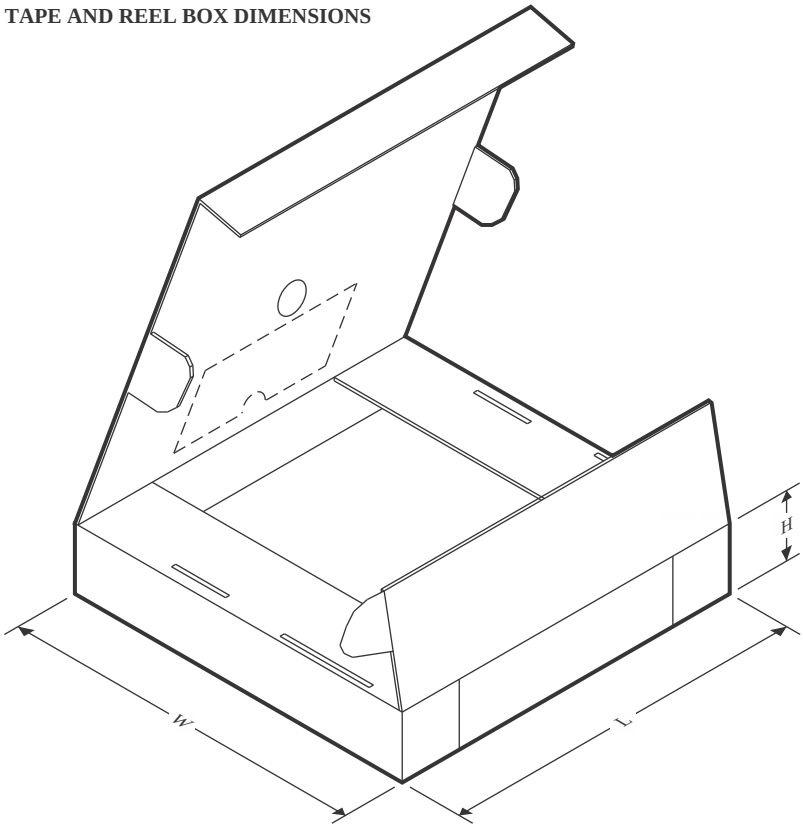
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

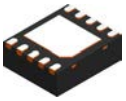
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOL1113DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOL1113DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOL1115DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOL1115DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOL111DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOL111DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOL1113DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOL1113DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOL1115DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOL1115DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOL111DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOL111DMWT	VSON	DMW	10	250	189.0	185.0	36.0

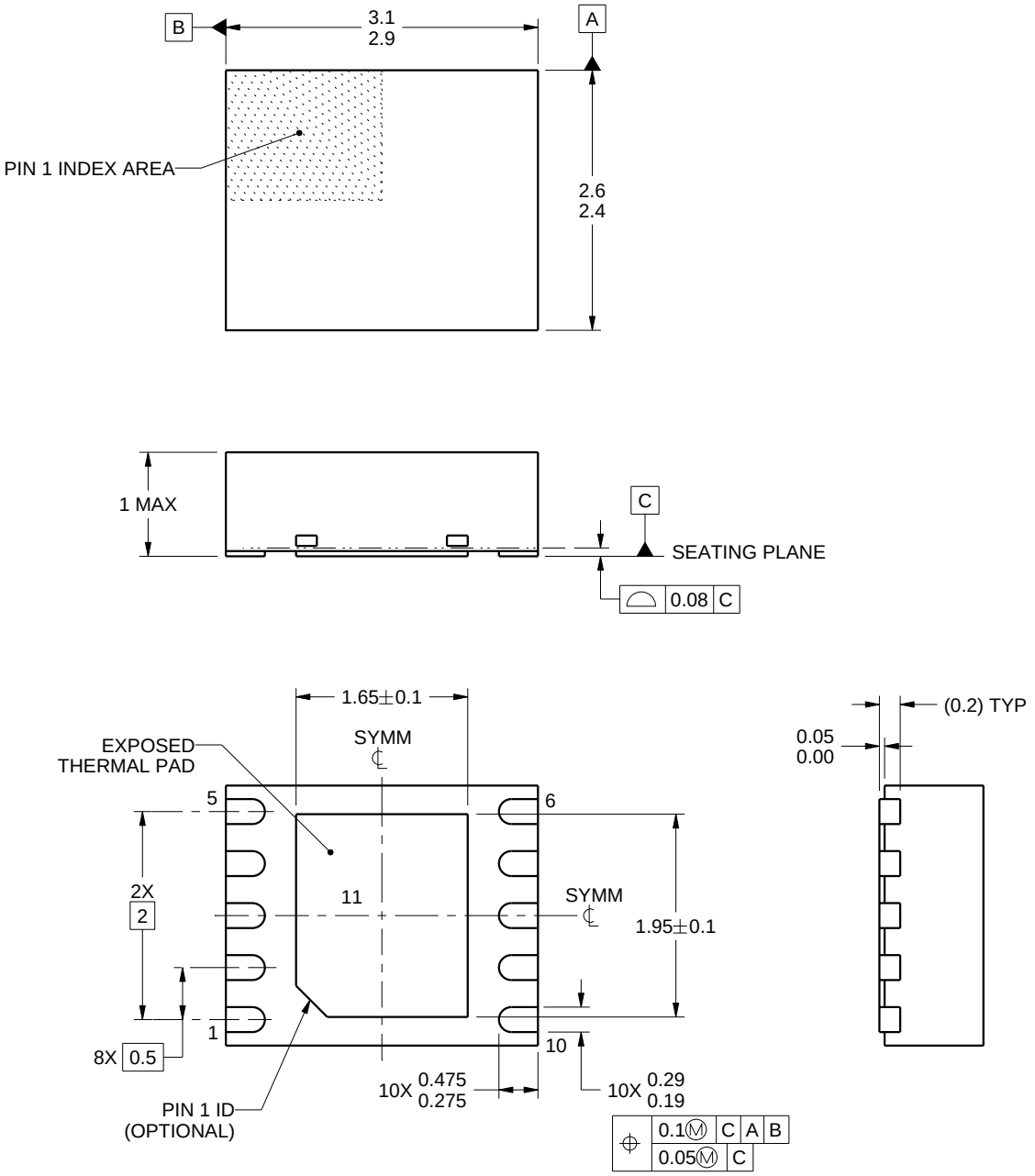


PACKAGE OUTLINE

DMW0010A

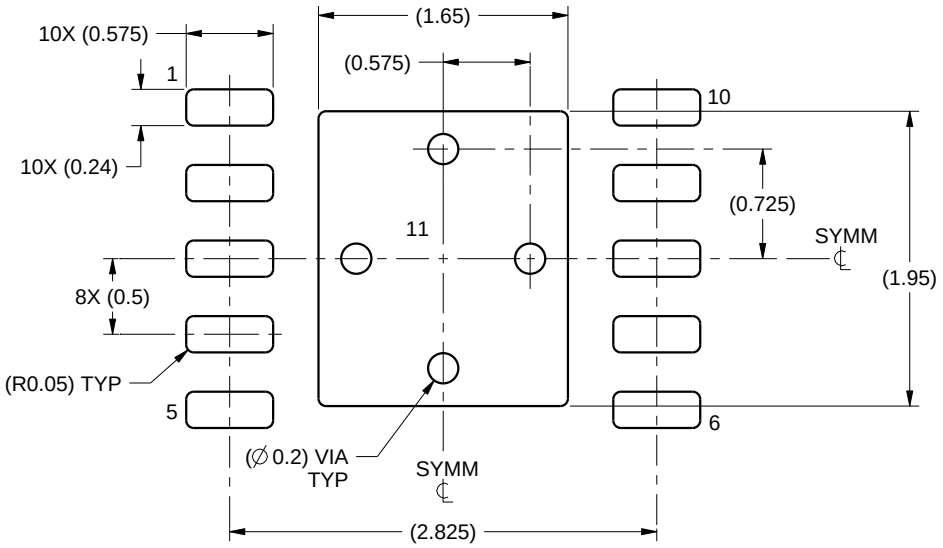
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

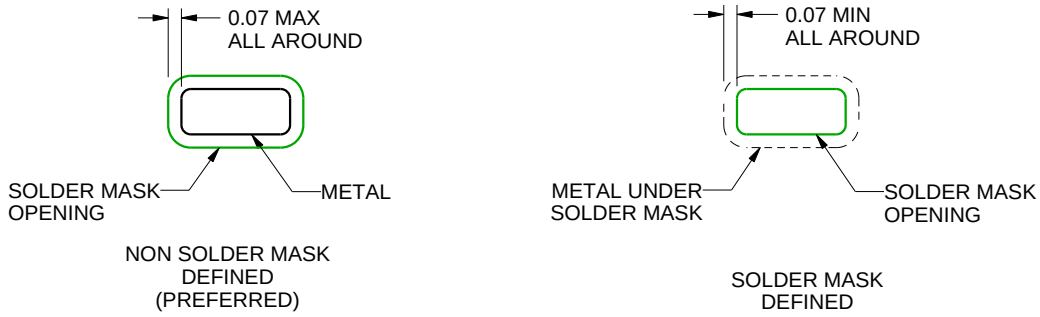


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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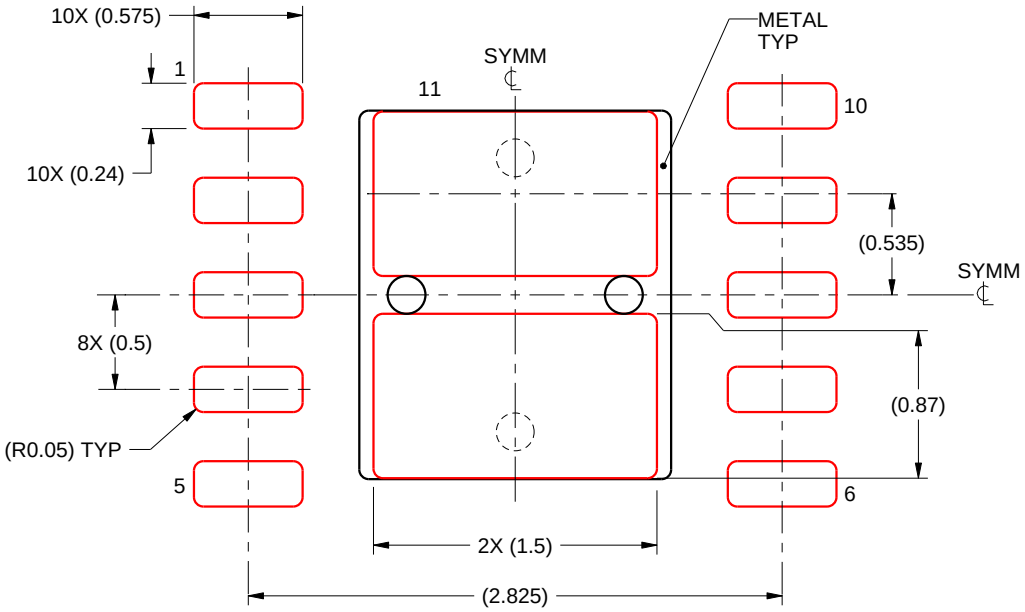
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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