THVD9491-SEP 耐放射線特性、フレキシブルな I/O 電源および IEC ESD 保護機能搭載、3V～5.5V、RS-485 トランシーバ

1 特長

- VID V62/24626
- TIA/EIA-485A および TIA/EIA-422B 規格の要件に適合またはそれを上回る性能
- 30krad (Si) まで、累積線量 (TID) 特性を評価済み
  - ウェハー ロットごとに 30krad (Si) までの累積線量耐性放射線ロット受け入れ試験 (TID RLAT)
- シングルイベント効果 (SEE) の特性評価
  - シングル イベント ラッチアップ (SEL) 耐性：線エネルギー付与 (LET) = 43MeVcm2 /mg (125℃)
- 宇宙用強化プラスチック (宇宙用 EP)
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 金ボンド ワイヤ
  - NiPdAu リード仕上げ
  - ミリタリー温度範囲 (-55℃～125℃)
  - 長期にわたる製品ライフ サイクル
  - 製品のトレーサビリティ
  - NASA ASTM E595 アウトガス仕様に適合
- 電源電圧：3V～5.5V
- データおよびイネーブル信号用の 1.65V～5.5V 電源
- SLR ピンで選択可能なデータ レート：
  - 20Mbps、50Mbps
- バス I/O 保護
  - DC ±40V バス フォルト
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 接触放電
  - ±4kV IEC 61000-4-4 高速過渡バースト
- 対称同相範囲：±12V
- レシーバのヒステリシスを大きくすることでノイズ耐性を確保
- グリッチのない電源投入 / 切断によるホット プラグイン機能
- 開放、短絡、アイドル バスのフェイルセーフ
- 1/8 単位負荷 (最大 256 のバス ノード)
- 有鉛 14 ピン SOIC パッケージ

2 アプリケーション

- 低軌道 (LEO) 衛星用途
- コマンドおよびデータ処理
- 通信ペイロード システム
- 光学画像処理
- レーダー画像処理ペイロード

3 概要

THVD9491-SEP は、データおよびイネーブル ロジック信号用の 1.65V～5.5V のロジック電源と、3V～5.5V のバス側電源を使用する、宇宙用強化型 ± 40V 故障保護機能付き全二重 RS-422/RS-485 トランシーバです。このデバイスはスルーレート選択機能を備えており、これを使うと、SLR ピンの設定に基づいて 2 つの最大速度でこのデバイスを使うことができます。

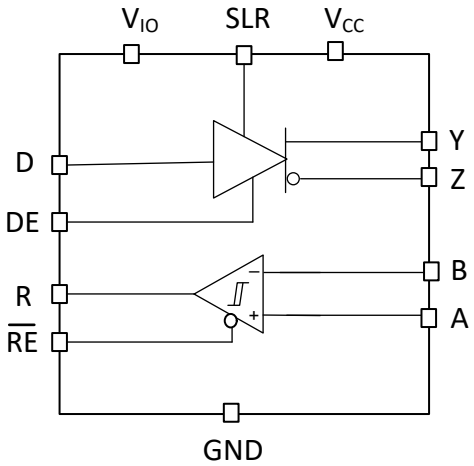
IEC ESD 保護機能を内蔵しているため、システムレベルの外部保護部品は不要です。±12V 入力同相範囲により、長いケーブルを使用する場合やグランド ループ電圧が大きい場合でもデータ通信の信頼性を高めることができます。250mV のレシーバ ヒステリシスを強化することで、高いノイズ除去性能を実現します。また、レシーバのフェイルセーフ機能により、入力が開放または短絡した場合、出力が確実に論理 High に固定されます。

THVD9491-SEP デバイスは、標準
14 ピン VSON パッケージで供給されます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
THVD9491-SEP	SOIC (D) (14)	8.65mm × 6mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Pin Configuration and Functions

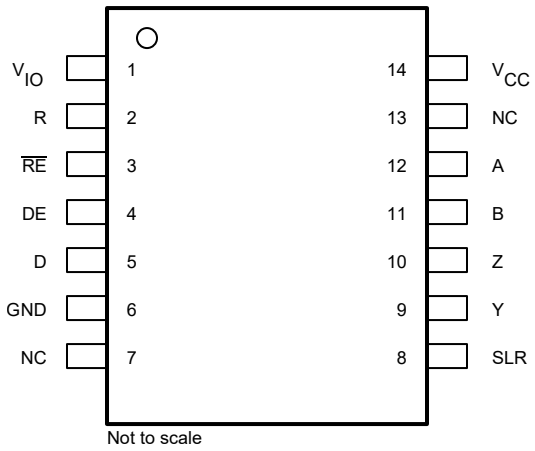


図 4-1. D (SOIC) Package 14-Pin (Top View)

表 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
V_{IO}	1	Logic Supply	1.65V to 5.5V supply for logic I/O signals (R, $\overline{RE}$, D, DE, and SLR)
R	2	Digital Output	Receive data output
$\overline{RE}$	3	Digital Input	Receiver enable input
DE	4	Digital Input	Driver enable input
D	5	Digital Input	Transmission data input
GND	6	Reference Potential	Local device ground
NC	7,13	No Connect	Not connected internally.
SLR	8	Digital Input	Slew rate selection pin: Low = 50Mbps, High = 20Mbps. Defaults to 50Mbps if left floating.
Y	9	Bus Output	RS-485 bus output, Y
Z	10	Bus Output	RS-485 bus output, Z
B	11	Bus Input	RS-485 bus input, B
A	12	Bus Input	RS-485 bus input, A
V_{CC}	14	Bus Supply	3V to 5.5V supply for A and B bus lines

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	–0.5	V_{CC} + 0.2	V
Bus supply voltage	V_{CC}	–0.5	6.5	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-40	40	V
Input voltage	Range at any logic pin (D, DE, SLR or $\overline{RE}$)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2 (1)	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2 (1)	Bus terminals and GND	±8,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

(1) For optimized IEC ESD performance, it is recommended to have series resistor (≥ 50 Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–12		12	V
V_{IH}	High-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0.7*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0		0.3*V_{IO}	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8 V or 2.5 V	–4		4	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3 V or 5 V	–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	SLR = V_{IO}			20	Mbps
		SLR = 0 or floating			50	Mbps
T_A	Operating ambient temperature		-55		125	°C
T_J	Junction temperature		-55		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.5 Thermal Information

THERMAL METRIC(1)		THVD9491-SEP	UNIT
		D (SOIC)	
		14-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS		VALUE	UNIT
P_D	Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z) V_{CC} = 5.5 V, T_A = 125 °C, square wave at 50% duty cycle	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	20Mbps	335	mW
			50 Mbps	571	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	20Mbps	325	mW
			50 Mbps	522	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	20Mbps	355	mW
			50 Mbps	526	

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, –12 V ≤ V_{test} ≤ 12 V. See 図 6-1		1.5	2.8		V
		R_L = 60 Ω, –12 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V. See 図 6-1		2.1	3.3		V
		R_L = 100 Ω See 図 6-2		2	4		V
		R_L = 54 Ω. See 図 6-2		1.5	3.3		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω or 100 Ω. See 図 6-2		–200		200	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See 図 6-2		1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω. See 図 6-2		–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{IO}, -40 V ≤ (V_A or V_B) ≤ 40 V, or A shorted to B (A,B are driver terminals for half duplex, Y/Z are for full duplex)		–250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V			75	125	μA
			V_I = –7 V	–100	–60		μA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of ± 12 V		40	125	200	mV
V_{TH-}	Negative-going input threshold voltage(1)			–200	–125	-40	mV
V_{HYS}	Input hysteresis				250		mV
V_{TH_FSH}	Input fail-safe threshold			–40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz			50		pF
V_{OH}	Output high voltage	I_{OH} = –8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	V_O = 0 V or V_{IO}, $\overline{RE}$ = V_{IO}		–1		1	μA
Logic							
I_{IN}	Input current (DE , SLR)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}				5	μA
I_{IN}	Input current (D, $\overline{RE}$)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}		–5			μA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	180		°C
T_{HYS}	Thermal shutdown hysteresis				10		°C
Supply							
$UV_{VCC (rising)}$	Rising under-voltage threshold on V_{CC}				2.3	2.6	V
$UV_{VCC (falling)}$	Falling under-voltage threshold on V_{CC}			1.95	2.2		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				150		mV
$UV_{VIO (rising)}$	Rising under-voltage threshold on V_{IO}				1.4	1.6	V
$UV_{VIO (falling)}$	Falling under-voltage threshold on V_{IO}			1.2	1.35		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				40		mV

5.7 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		4	7.2	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		3	4.2	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		2.5	3	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		30	100	µA
I_{CC}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		3.5	5	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		2.5	3	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		2	3	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		30	100	µA
I_{IO}	Logic supply current (quiescent), V_{IO} = 3 to 3.6 V	Driver disabled, Receiver enabled, SLR = GND	DE = 0 V, $\overline{RE}$ = 0 V, No load		4.5	10	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}			3.3	10	µA
		Driver disabled, Receiver disabled, SLR = GND	DE = 0 V, $\overline{RE}$ = V_{IO}, No load		4.5	8.4	µA
		Driver disabled, Receiver disabled, SLR = V_{IO}			3.3	8.4	µA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than $V_{TH–}$.
(2) A and B are receiver inputs, Y and Z are driver output terminals for the device

5.8 Switching Characteristics: 20Mbps

20-Mbps (SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 6-3	4	8	15	ns
t_{PHL}, t_{PLH}	Propagation delay			6	15	30	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				1	3	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 図 6-4 and 図 6-3		17	35	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			14	39	ns
		$\overline{RE}$ = V_{IO}			3	4.5	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 6-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay			25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				1	5	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}	See 図 6-7		50	82	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 図 6-8		2.8	5	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 図 6-9	7	11	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			19	32	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 図 6-8	50		500	ns

(1) A and B are receiver inputs, Y and Z are driver output terminals for the device

5.9 Switching Characteristics: 50Mbps

50-Mbps (SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See 図 6-3	1	5	7	ns
t_{PHL}, t_{PLH}	Propagation delay			7	12	22	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				1	3	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 図 6-4 and 図 6-5		14	30	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			20	35	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = V_{IO}			2.5	4.5	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 図 6-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay			25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				1	5	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}	See 図 6-7		50	82	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 図 6-8		3	5	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 図 6-9	7	10	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			19	35	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 図 6-8	50		500	ns

(1) A and B are receiver inputs, Y and Z are driver output terminals for the device

5.10 Typical Characteristics

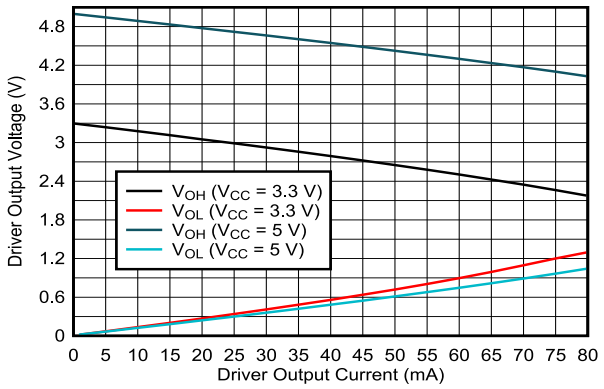


図 5-1. Driver Output Voltage vs. Driver Output Current

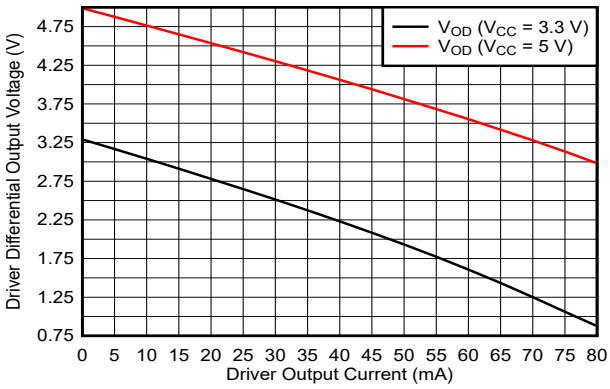


図 5-2. Driver Differential Output Voltage vs. Driver Output Current

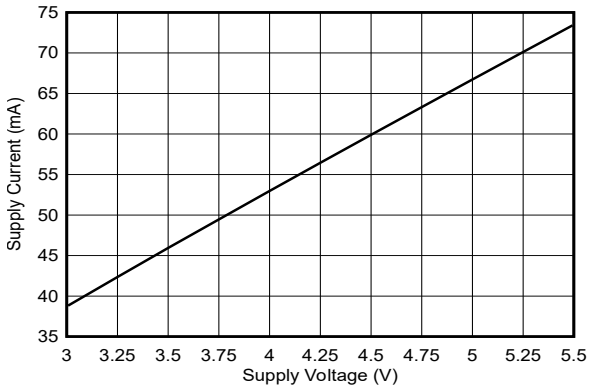


図 5-3. Supply Current vs. Supply Voltage

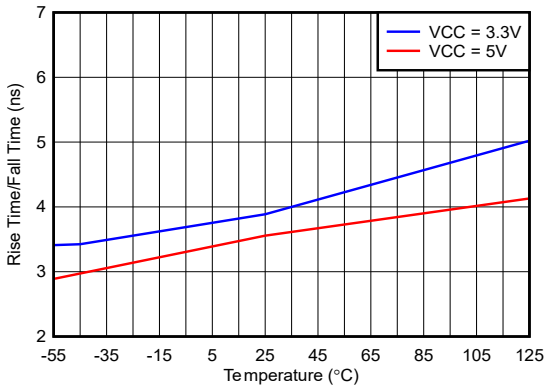


図 5-4. Rise and Fall Time vs. Temperature

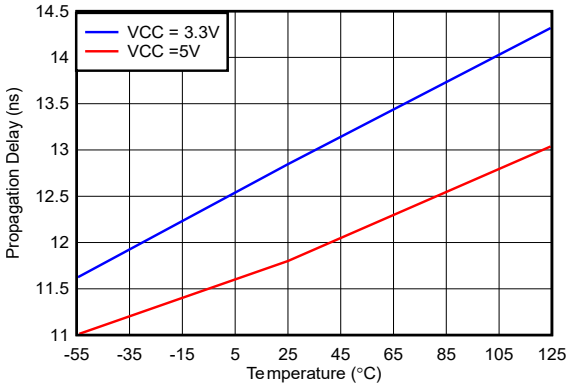


図 5-5. Propagation Delay vs. Temperature

6 Parameter Measurement Information

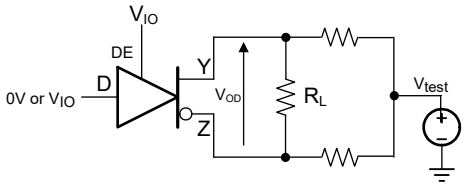


図 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

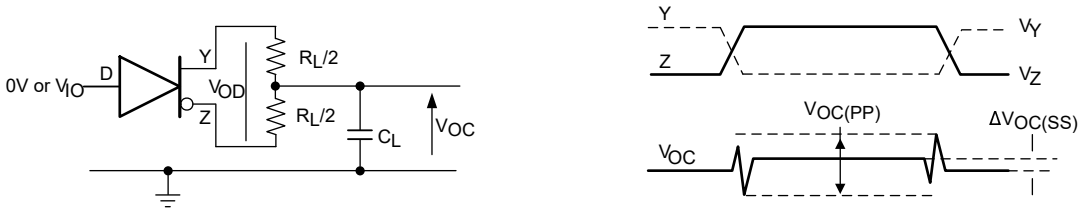


図 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

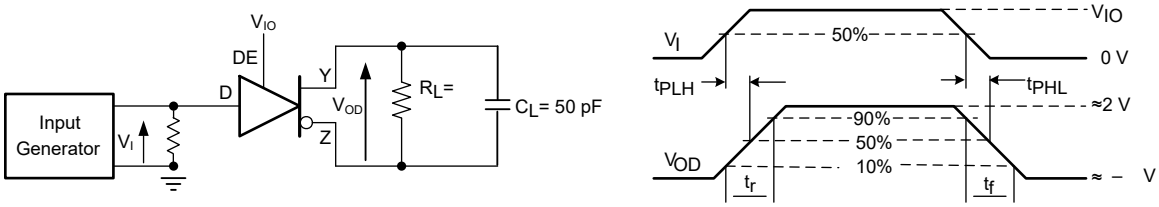


図 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

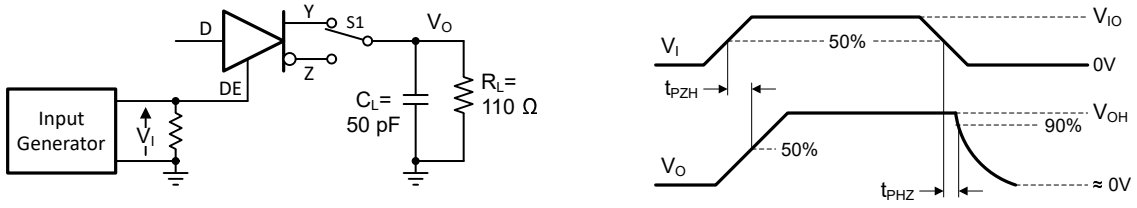


図 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

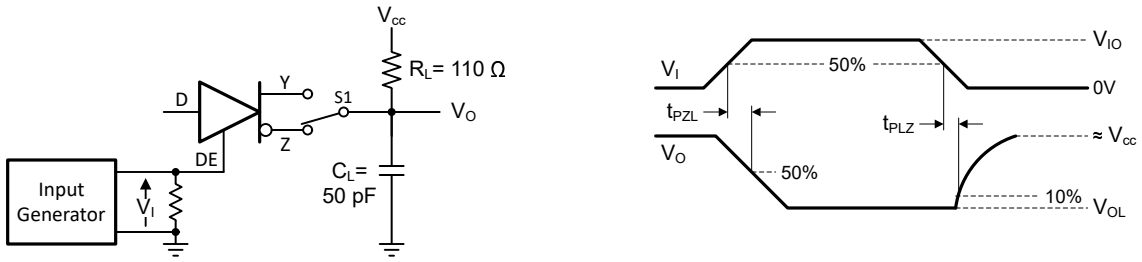


図 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

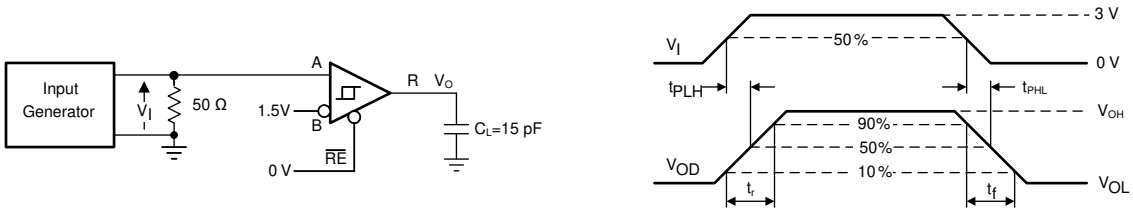


図 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

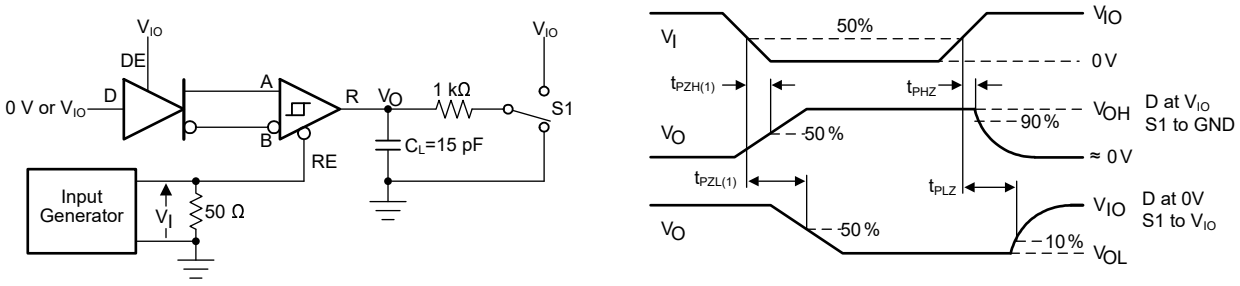


図 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

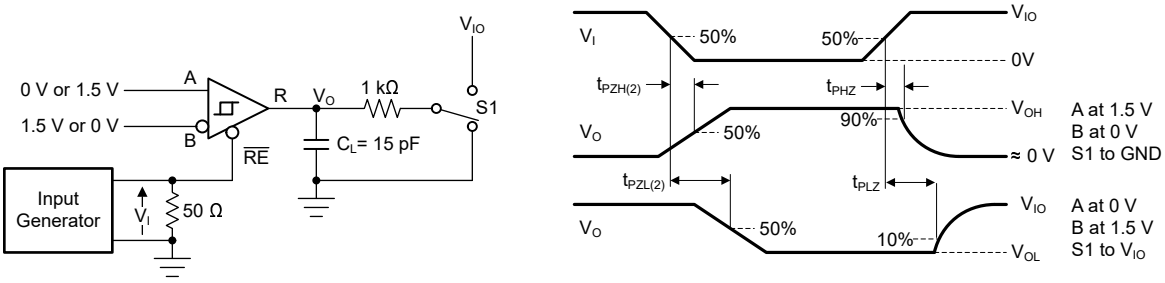


図 6-8. Measurement of Receiver Enable Times With Driver Disabled

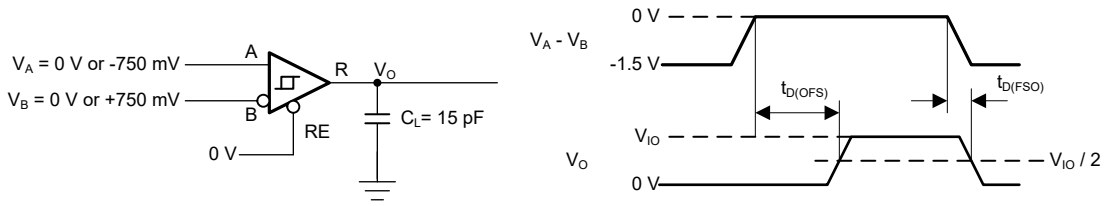


図 6-9. Measurement of Fail-Safe Delay

7 Detailed Description

7.1 Overview

THVD9491-SEP is a fault-protected, full duplex RS-485 transceiver that can support two speed grades suitable for data transmission up to 20Mbps and 50Mbps respectively, based on the logic level on the SLR pin. The device has active-high driver enable and active-low receiver enables.

7.2 Functional Block Diagrams

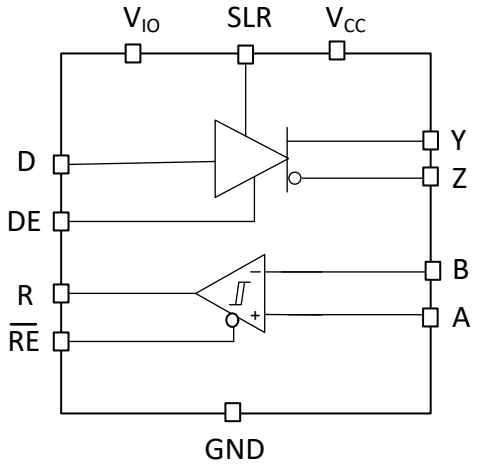


図 7-1. THVD9491-SEP Block Diagram

7.3 Feature Description

7.3.1 ±40-V Fault Protection

THVD9491-SEP transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7V to +12V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, the device is protected up to ±40V without the need for any external components.

7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±8kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4kV. The integrated ESD structures help to limit voltage excursions and recover from them quickly that they allow EFT Criterion A at the system level (no data loss when transient noise is present).

7.3.3 Driver Overvoltage and Overcurrent Protection

The THVD9491-SEP driver is protected against any DC supply shorts in the range of -40V to +40V. The devices internally limit the short circuit current to ±250mA to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5mA if the output fault voltage exceeds |±25V|.

The device features thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

7.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD9491-SEP feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. 250mV (typical) hysteresis provides excellent noise immunity.

7.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

7.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 7-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 7-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

表 7-3 shows SLR (slew rate select) pin functionality. SLR has integrated pull-down, so the device remains in higher speed mode until SLR is pulled high which limits the slew rate and puts the device in slower speed mode.

表 7-3. SLR pin control

Device	Functionality w.r.t SLR pin
THVD9491-SEP	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 50Mbps SLR = High: Both TX and RX maximum speed is limited to 20Mbps

表 7-4 shows the device behavior in undervoltage scenarios:

表 7-4. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
> $UV_{VCC(rising)}$	> $UV_{VIO(rising)}$	Determined by DE and D inputs	Determined by $\overline{RE}$ and A-B
< $UV_{VCC(falling)}$	> $UV_{VIO(rising)}$	High impedance	Failsafe H (gated by $\overline{RE}$)
> $UV_{VCC(rising)}$	< $UV_{VIO(falling)}$	High impedance	High impedance
< $UV_{VCC(falling)}$	< $UV_{VIO(falling)}$	High impedance	High impedance

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a fault-protected, full-duplex RS-485 transceiver commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

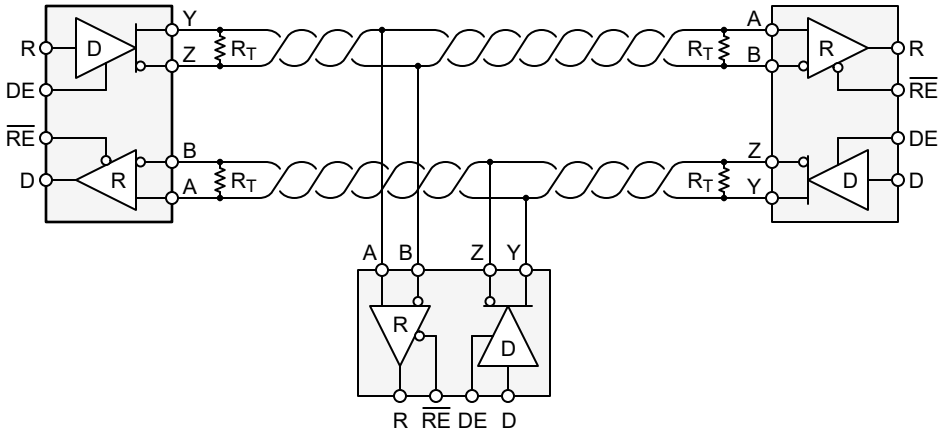


図 8-1. Typical RS-485 Network With Half-Duplex Transceivers

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

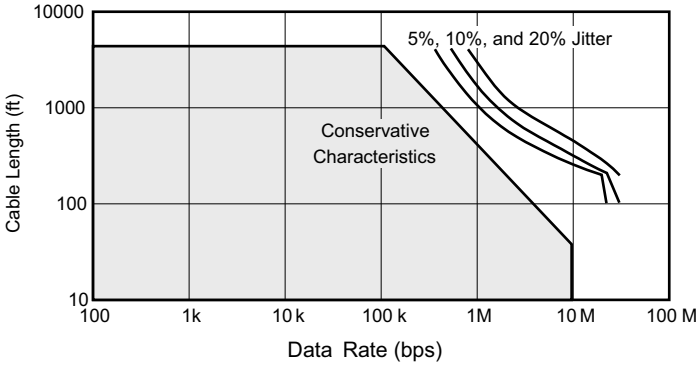


図 8-2. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (up to 50Mbps) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD9491-SEP device consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

8.2.1.4 Transient Protection

The bus pins of the THVD9491-SEP transceivers include on-chip ESD protection against ±16kV HBM and ±8kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

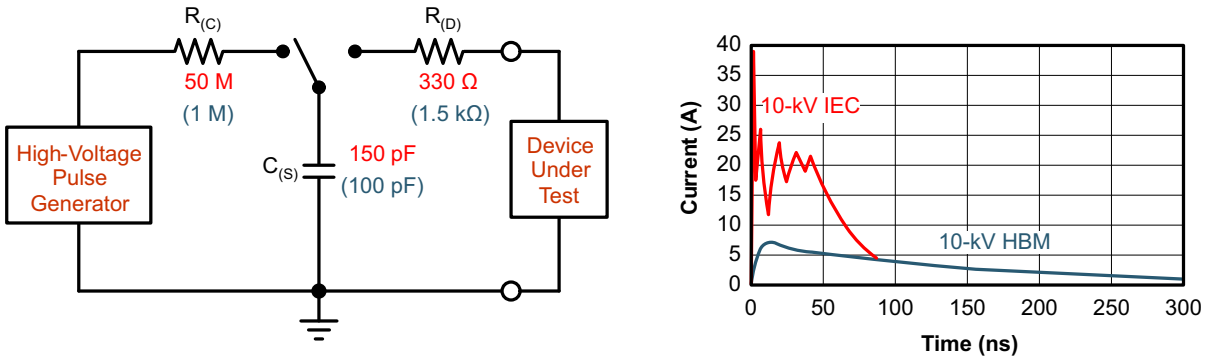


図 8-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 8-4 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side diagram shows the relative pulse-power for a 0.5kV surge transient and 4kV EFT transient, both of which dwarf the 10kV ESD transient visible in the lower-left corner. 500V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side diagram shows the pulse power of a 6kV surge transient, relative to the same 0.5kV surge transient. 6kV surge transients are most likely to occur in power generation and power-grid systems.

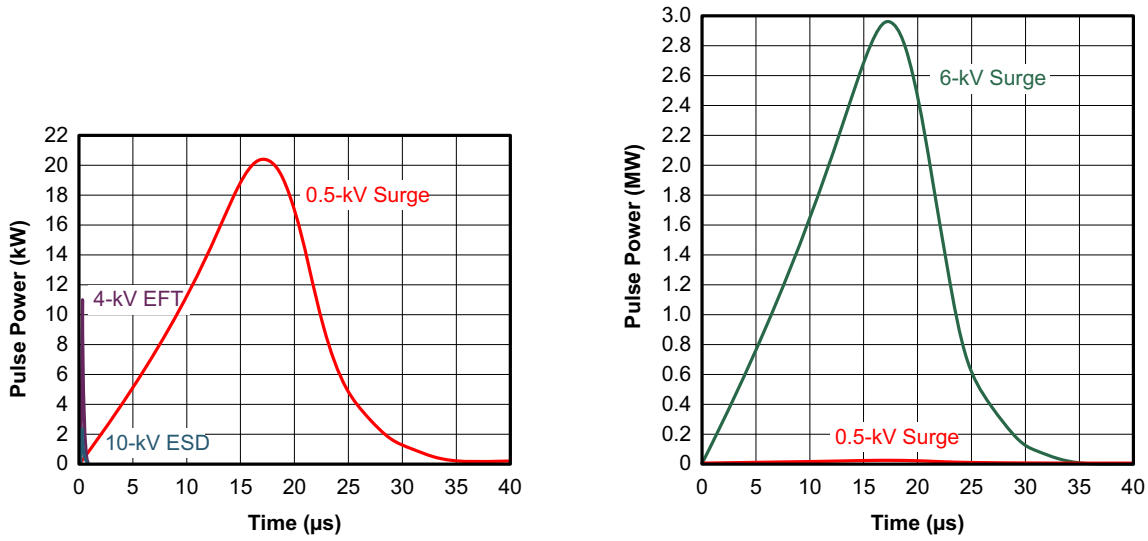


図 8-4. Power Comparison of ESD, EFT, and Surge Transients

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 8-5 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

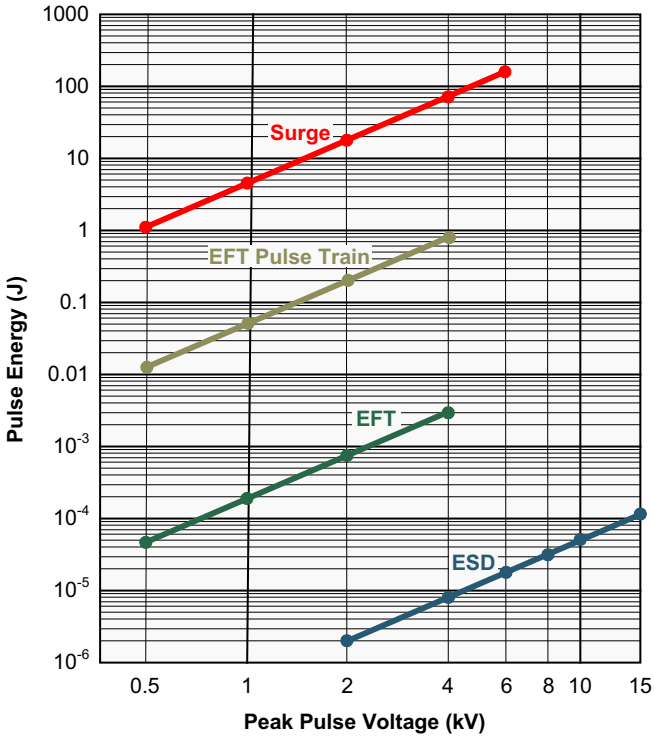


図 8-5. Comparison of Transient Energies

8.2.2 Detailed Design Procedure

図 8-6 suggests a protection circuit against 1kV surge (IEC 61000-4-5) transients. 表 8-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30V. This provides the protection diodes do not conduct if a direct RS-485 bus shorts to 24V DC industrial power rail.

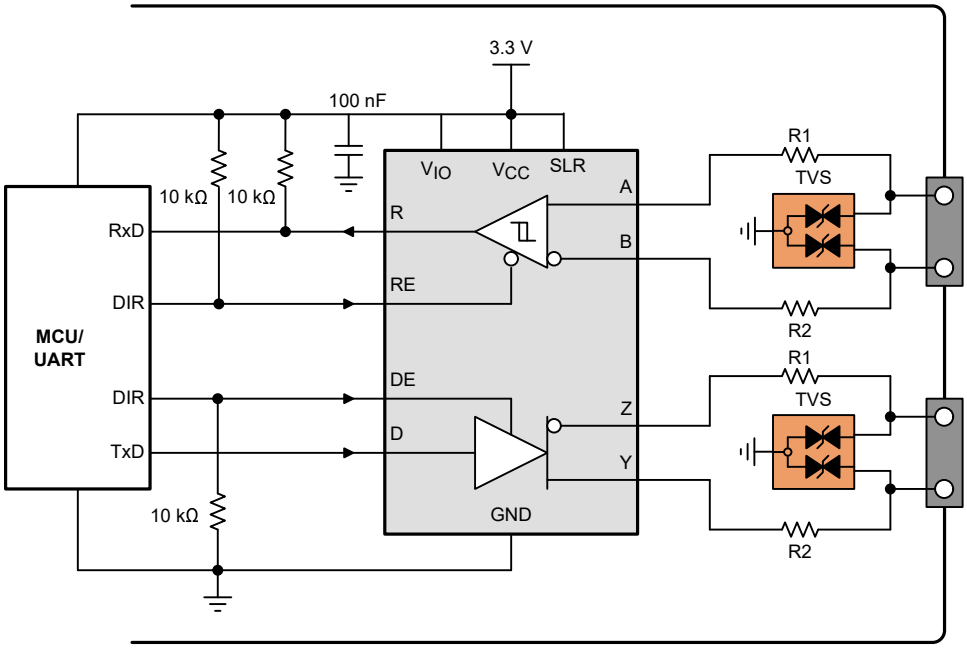


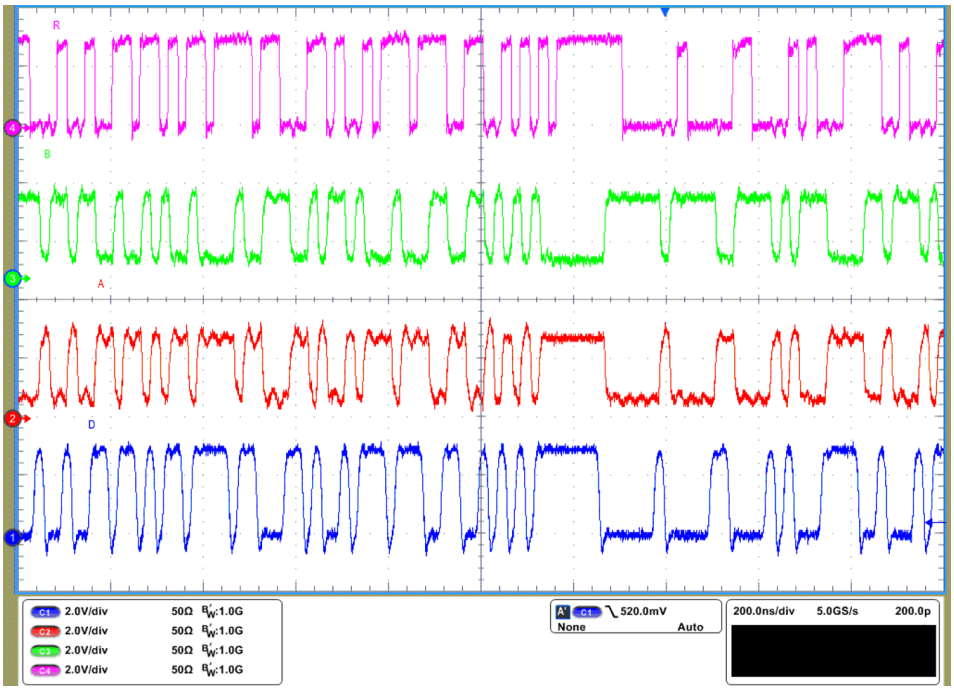
図 8-6. Transient Protection Against Surge Transients for Full-Duplex Devices

表 8-1. Components List

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD9491-SEP	TI
TVS	Bidirectional 400W transient suppressor	SMAJ30CA	Littelfuse

(1) See Third-Party Products Disclaimer

8.2.3 Application Curve



PRBS data at 50 Mbps | V_{CC} = V_{IO}= 3.3V | SLR = GND | R_L = 50 Ω

図 8-7. Driver input (D), bus (A/Y,B/Z) and receiver output (R) waveforms

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF decoupling capacitors as close as possible to the V_{CC}/V_{IO} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC}/V_{IO} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1kΩ to 10kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

8.4.2 Layout Example

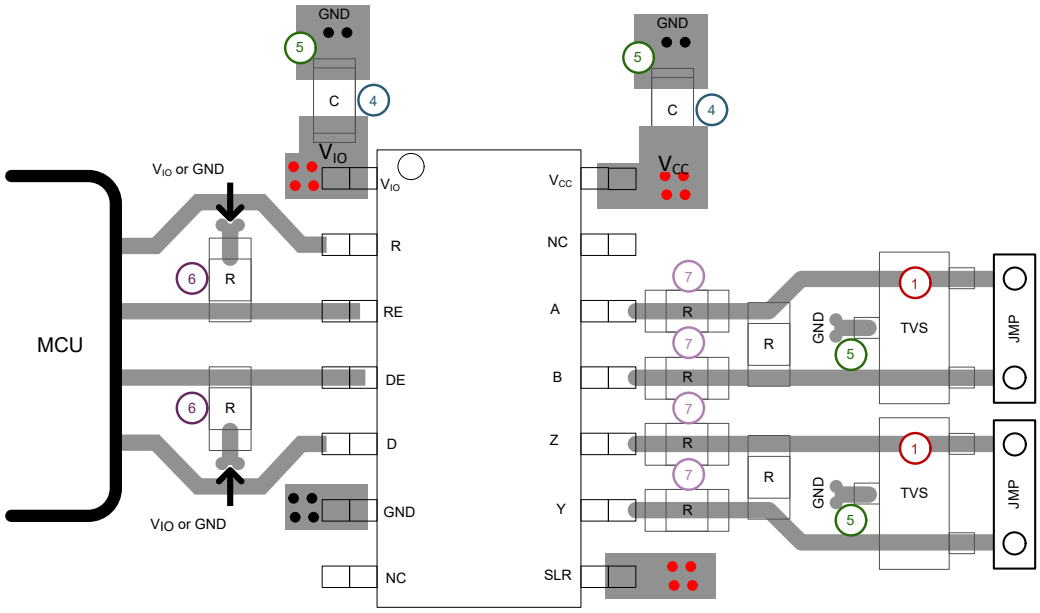


図 8-8. Full-Duplex Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision A (December 2024) to Revision B (December 2024)	Page
• Updated the I_{IO} (receiver enabled) max value from 8.4µA to 10µA	6

Changes from Revision * (January 2024) to Revision A (December 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD9491DTSEP	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	T9491SEP
THVD9491DTSEP.A	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	T9491SEP
V62/24626-01XE	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	T9491SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

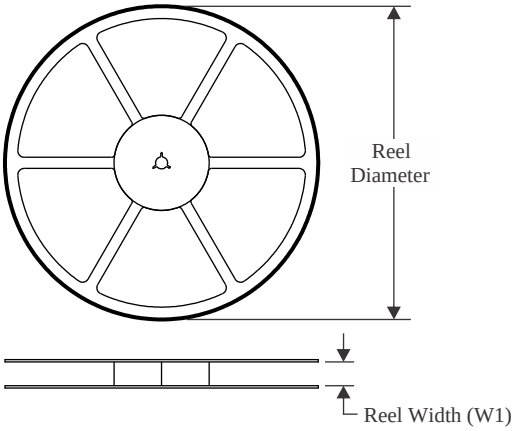
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

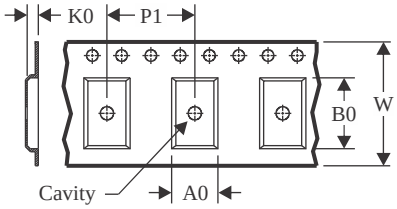
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

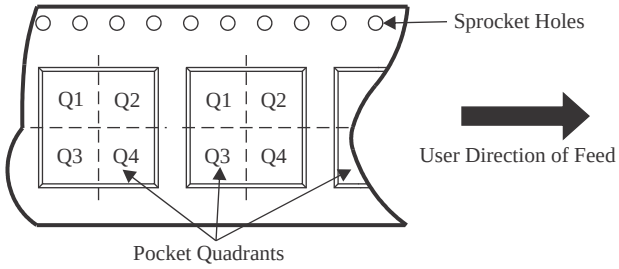


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

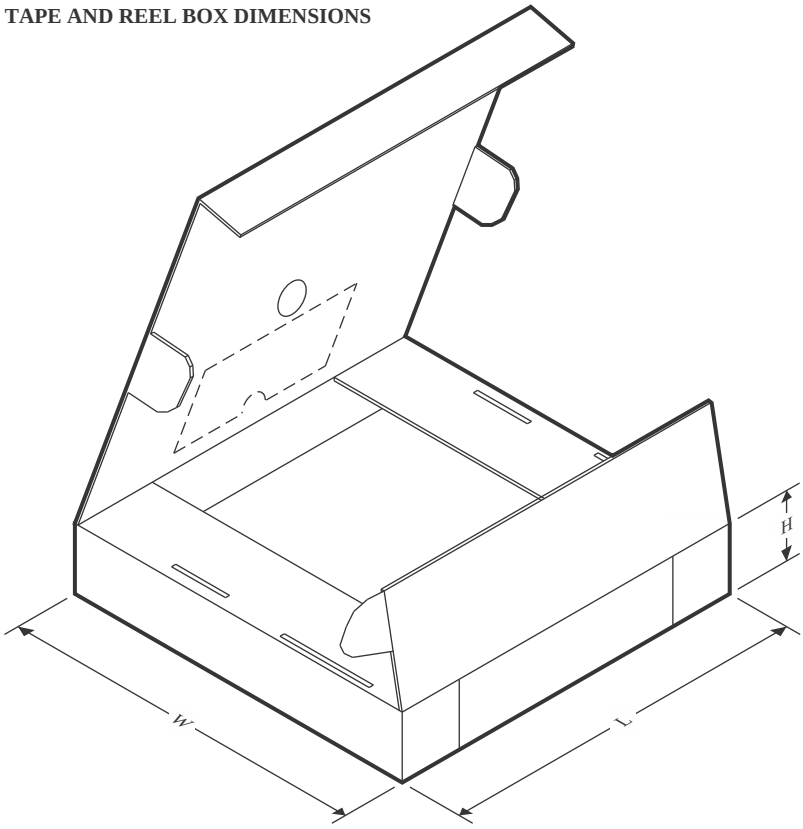
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

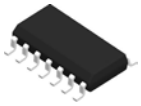
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD9491DTSEP	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD9491DTSEP	SOIC	D	14	250	353.0	353.0	32.0

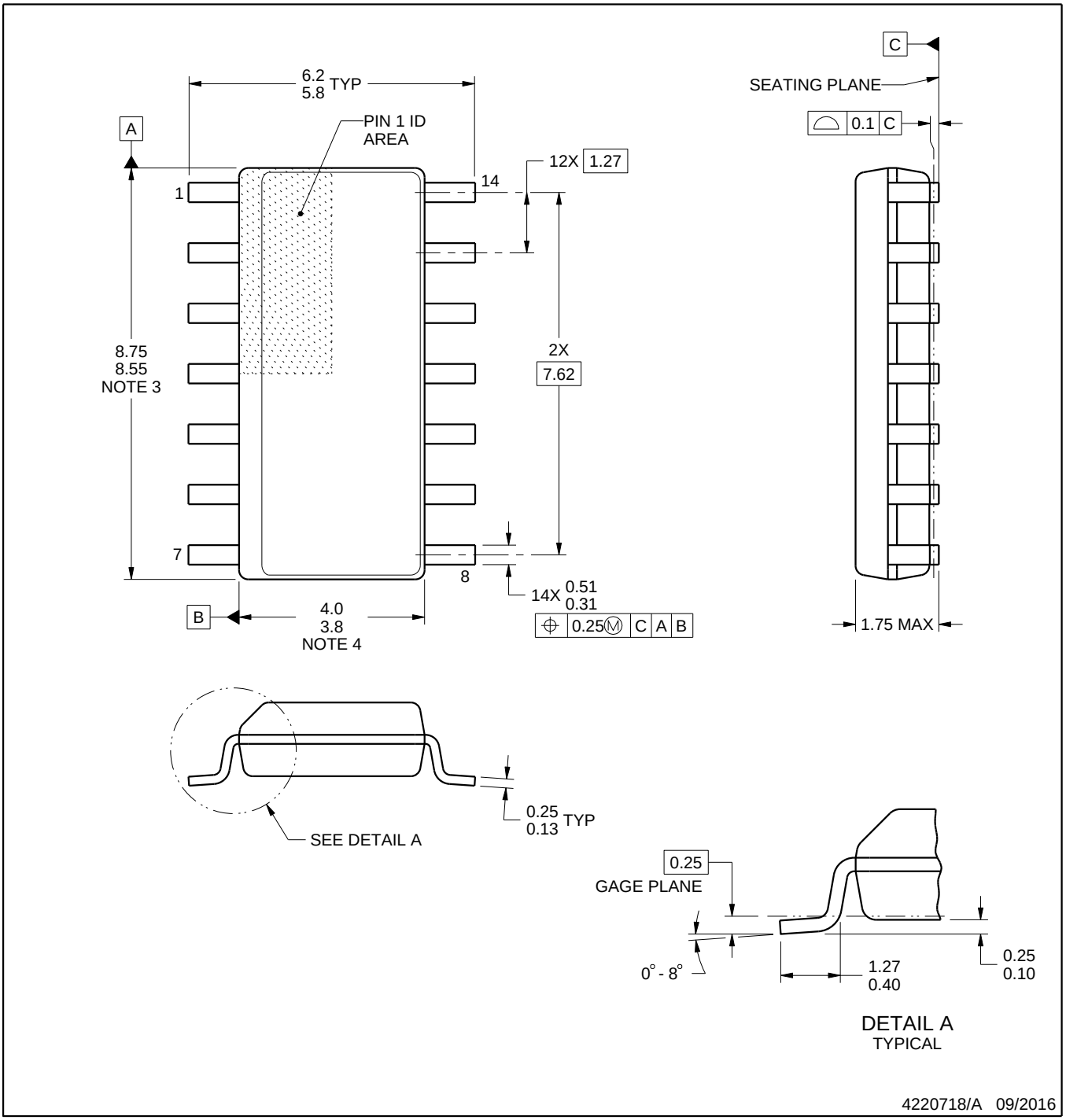


PACKAGE OUTLINE

D0014A

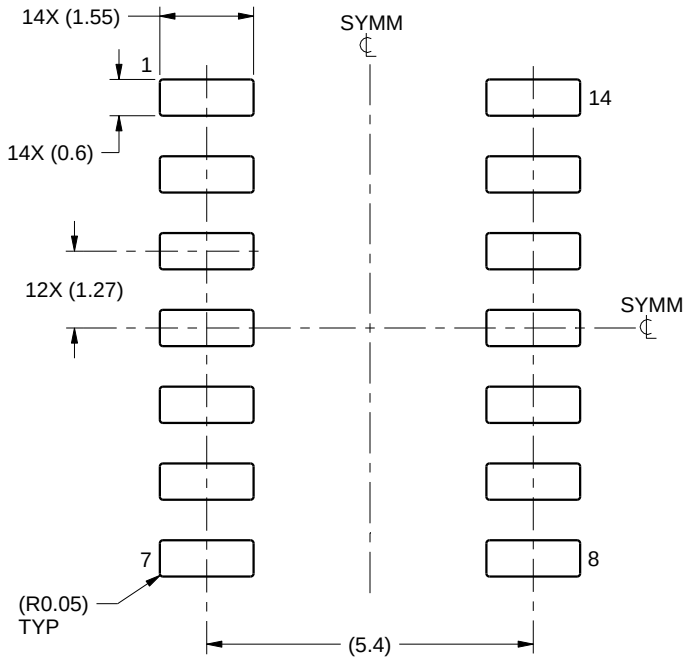
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

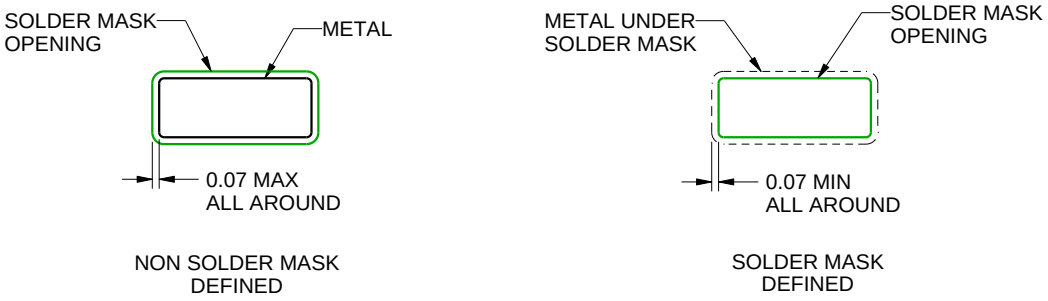


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

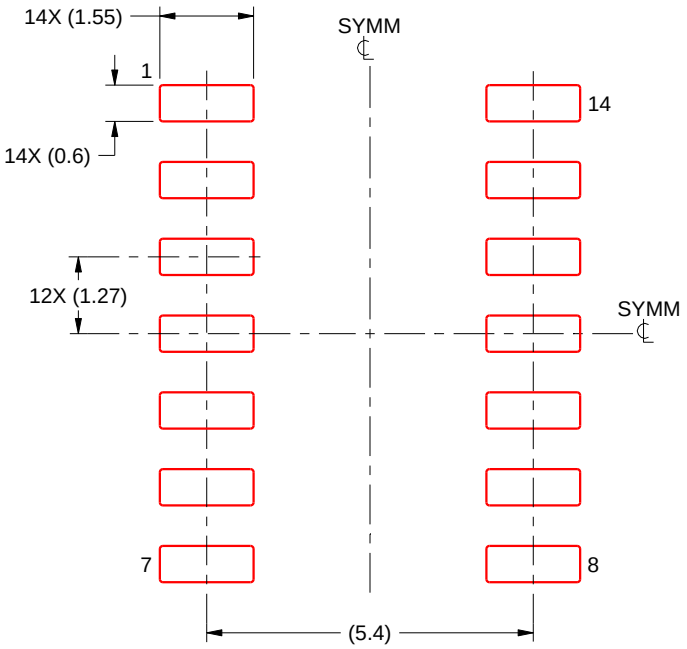
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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