THVD8010 OOK 変調付き RS-485 電力線通信用トランシーバ

1 特長

- 3V ~ 5.5V の電源電圧
- 半二重通信
  - 最大 30kbps のデータ・レート (OOK)
- オン / オフ・キーイング (OOK) 変調による RS-485 電気信号伝達
- 無極性
- 優れたノイズ耐性
- ピンで選択可能なキャリア周波数：125kHz ~ 300kHz
- 拡散スペクトラム・クロック処理による優れた EMI 性能
- スタック・バス条件を回避するための TX タイムアウト
- 動作同相範囲：–7V ~ 12V
- バス I/O 保護
  - ±18V の DC フォルト保護
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 接触放電
  - ±15kV IEC 61000-4-2 エアギャップ放電
  - ±4kV IEC 61000-4-4 高速過渡バースト
- 拡張温度範囲：-40℃ ~ 125℃
- スペースに制約のあるアプリケーションに適した 8 ピン SOT-23 パッケージ

2 アプリケーション

- HVAC システム
- ビル・オートメーション
- ファクトリ・オートメーション / 制御
- 家電製品
- ライティング
- グリッド・インフラストラクチャ

3 概要

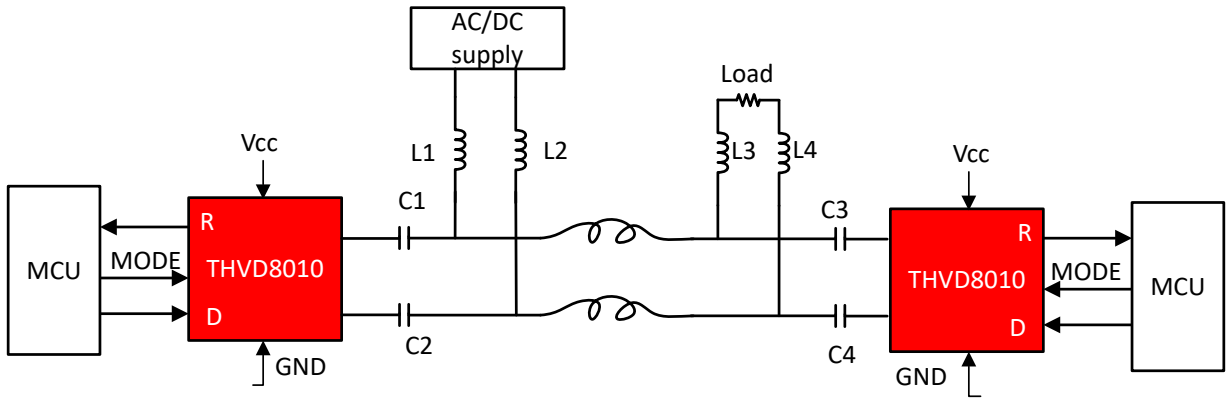
THVD8010 は、オン / オフ・キーイング (OOK) 変調および復調機能を備えた RS-485 電力線通信用トランシーバです。既存の電力線上でデータを変調することで、電力伝送とデータ通信が共通の 1 対の配線を共有できるため、システム・コストを大幅に低減できます。

ピンで設定可能なインターフェイスを採用しているため、システム設計が簡単です。キャリア周波数は、F_SET ピンの外付け抵抗を変更することで調整できます。キャリア周波数の可変範囲が広いため、システム設計者は外付けのインダクタとコンデンサを柔軟に選択できます。また、OOK 変調はデータの極性に影響されないで動作するため、システムの設置が簡単です。

製品情報

型番	パッケージ(1)	本体サイズ (公称)
THVD8010	SOT-23 (8)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2020	*	Initial release.

5 Pin Configuration and Functions

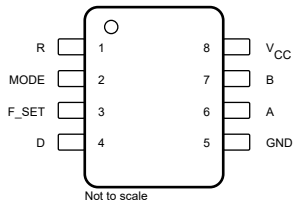


図 5-1. DRL Package, 8-Pin SOT-23, Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
MODE	2	Digital input	Transmit/receive mode selection. Low = receive mode; High = transmit mode. Has an internal 2-MΩ pull-down to GND
F_SET	3	Analog input	Carrier frequency selection. Use a resistor to GND to select a frequency.
D	4	Digital input	Driver data input, 2-MΩ pull-up to V_{CC}
GND	5	Ground	Device ground
A	6	Bus input/output	Bus I/O port A (complementary to B)
B	7	Bus input/output	Bus I/O port B (complementary to A)
V_{CC}	8	Power	3.3-V to 5-V device supply

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, MODE or F_SET)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs (differential or with respect to GND)	–18	18	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *セクション 6.4* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A and B pins to GND	±16,000	V
			All pins	±4,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD contact discharge, A and B pins to GND	±8	kV
		IEC 61000-4-2 ESD air gap discharge, A and B pins to GND	±15	
		IEC 61000-4-4 electrical fast transient, A and B pins to GND	±4	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{ID}	Input differential voltage (A and B pins)		–7		12	V
V_{CM}	Operational common mode voltage (A and B pins)		–7		12	V
V_{IH}	High-level input voltage (D and MODE pins)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D and MODE pins)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–4		4	
R_{F_SET}	Carrier frequency selection resistor		32		80	kΩ
ΔR_{F_SET}	Carrier frequency selection resistor tolerance		–2		2	%
$1/t_{UI}$	Data rate	Modulation mode(1)			f_0 / 10	bps
C_{F_SET}	Recommended load capacitance on F_SET pin				100	pF
T_A	Operating ambient temperature		–40		125	°C

(1) f_0 is the carrier frequency (in Hz) set by the external resistor between F_SET and GND pins.

6.5 Thermal Information

THERMAL METRIC[1]		THVD8010 DDF (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-top characterization parameter	29.5	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and ICPackage Thermal Metrics application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	OOK mode, R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V, Measured at 2nd pulse	See 図 7-1	1.5	2		V
		OOK mode, R_L = 100 Ω, C_L = 50 pF, Measured at 2nd pulse	See 図 7-1	2	2.5		
		OOK mode, R_L = 54 Ω, C_L = 50 pF, Measured at 2nd pulse	See 図 7-1	1.5	2		
V_{OC}	Steady state common-mode output voltage	OOK mode, R_L = 60 Ω, C_L = 50 pF	See 図 7-2	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage	OOK mode, R_L = 60 Ω, C_L = 50 pF	See 図 7-2	-160		160	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	OOK mode, R_L = 60 Ω, C_L = 50 pF, V_{CC} = 3.3 V and V_{CC} = 5V	See 図 7-2		450		mV
I_{OS}	Driver short-circuit output current	OOK mode, MODE = V_{CC}, –7 V ≤ [V_A or V_B] ≤ 12 V		–250		250	mA
f_0	Minimum carrier frequency[1]	R_{F_SET} = 77 kΩ	See 図 7-3		125		kHz
f_0	Maximum carrier frequency[1]	R_{F_SET} = 31.9 kΩ	See 図 7-3		300		kHz
DCD_{f0}	Carrier frequency duty cycle distortion	Measured over the full range of f_0		–2		2	%
Δf_0	Carrier frequency tolerance	Measured with a ±2% tolerant R_{F_SET}		–25		25	%
Δf_{SSC}	Variation of the carrier frequency for spread spectrum clocking	Measured across the full carrier frequency range			±5		%
f_{SSC}	Spread spectrum clock rate				30		kHz

6.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Receiver							
I_I	Bus input current in receive mode	MODE = GND, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–97	–70		
V_{MAG_ZERO}	OOK signal differential swing (magnitude) to detect a zero at the R output	MODE = GND, over full common mode range, OOK mode	125 kHz			1200	mV
V_{MAG_ZERO}	OOK signal differential swing (magnitude) to detect a zero at the R output		200 kHz			1200	mV
V_{MAG_ZERO}	OOK signal differential swing (magnitude) to detect a zero at the R output	MODE = GND, over full common mode range, OOK mode	300 kHz			1300	mV
V_{MAG_ONE}	OOK signal differential swing (magnitude) to detect an one at the R output	MODE = GND, over full common mode range, OOK mode	125 kHz	400			mV
V_{MAG_ONE}	OOK signal differential swing (magnitude) to detect an one at the R output		200 kHz	400			mV
V_{MAG_ONE}	OOK signal differential swing (magnitude) to detect an one at the R output		300 kHz	400			mV
V_{MAG_HYS}	Receiver differential input voltage threshold hysteresis		125 kHz	350			mV
V_{MAG_HYS}	Receiver differential input voltage threshold hysteresis		200 kHz	350			mV
V_{MAG_HYS}	Receiver differential input voltage threshold hysteresis	MODE = GND, over full common mode range, OOK mode	300 kHz	350			mV
Logic / Control Pins							
I_{IN}	Input current (D, MODE)	V_O = 0 V or V_{CC}	V_O = 0 V or V_{CC}	–5		5	µA
I_{IN}	Input current (F_SET)	V_O = V_{CC}	V_O = V_{CC}			55	µA
V_O	Output voltage (F_SET)	I_O = 0 mA			1.4		V
		32 kΩ ≤ R_{PD} ≤ 78 kΩ			785		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –4 mA	I_{OH} = –4 mA	V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 4 mA			0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, MODE = 0		–1		1	µA
Device							
I_{CC}	Supply current (quiescent)	OOK transmit mode	D = V_{CC}, MODE = V_{CC}, resistor between F_SET and GND, no load		3	5	mA
I_{CC}	Supply current (quiescent)	OOK receive mode	D = V_{CC}, MODE = GND, resistor between F_SET and GND, no load		3.8	6	mA

6.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown temperature		160	170	185	℃
T_{HYS}	Thermal shutdown hysteresis			11	15	℃

(1) See OOK modulation section for the complete carrier frequency range

6.7 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

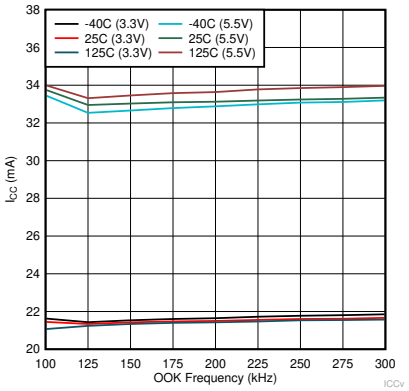
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PD_{OOK}	Chip power dissipation in OOK mode	MODE = V_{CC}, R_L = 60 Ω, no C_L, see Figure 2	f_0 = 125 kHz, 12.5 kHz (25 kbps) clock pattern as data		60	85	mW
			f_0 = 300 kHz, 30 kHz (60 Kbps) clock pattern as data		90	130	mW

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t_r, t_f	Driver differential output rise and fall times	R_L = 60 Ω, C_L = 50 pF, See 図 7-4		8	30	ns
t_{PHL}, t_{PLH}	Driver propagation delay			1	3.5	Clocks
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$			1	2.5	Clocks
Receiver						
t_r, t_f	Receiver output rise and fall times	C_L = 15 pF, See 図 7-5		2	8	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			4.5	6	Clocks
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$			0.4	3	
Device						
t_{TX-RX_OOK}	Transmit to receive mode change delay, OOK mode	Max of $t_{TX-RX\_OOK\_ZERO}$ and $t_{TX-RX\_OOK\_ONE}$. See 図 7-6 and 図 7-7			14	clocks
t_{RX-TX_OOK}	Receive to transmit mode change delay, OOK mode	See 図 7-8			3	clocks
$t_{TX\_TIMEOUT}$	Transmit timeout delay		60	110		s

6.9 Typical Characteristics



R_L = 60Ω Data rate = f_0/10 TX Enabled

図 6-1. ICC vs OOK Frequency

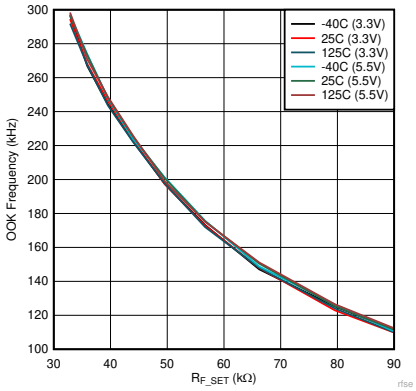


図 6-2. R_{F_SET} vs OOK Frequency

7 Parameter Measurement Information

Note

The number of pulses shown is reduced for simplicity of waveform. Please see the "OOK Modulation with F_SET pin" section for more information.

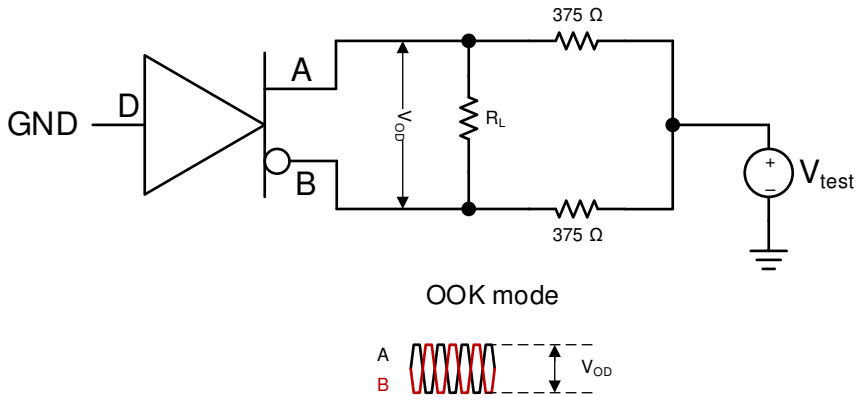


図 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

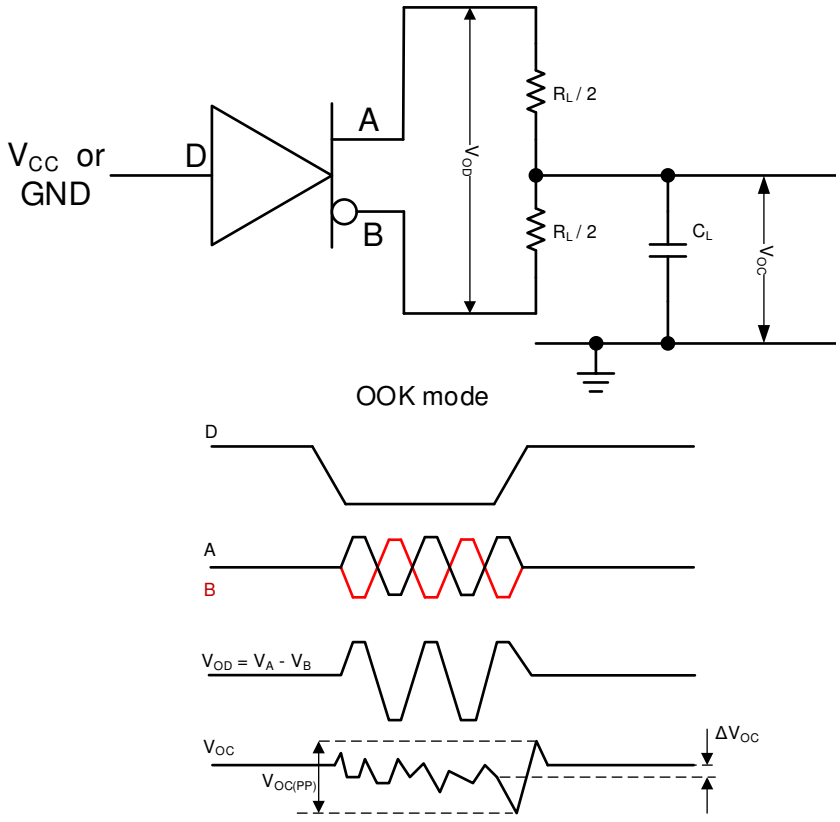


図 7-2. Measurement of Driver Differential and Common-Mode Outputs

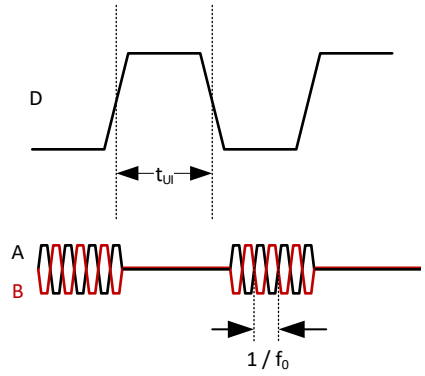


図 7-3. Measurement of Carrier Frequency

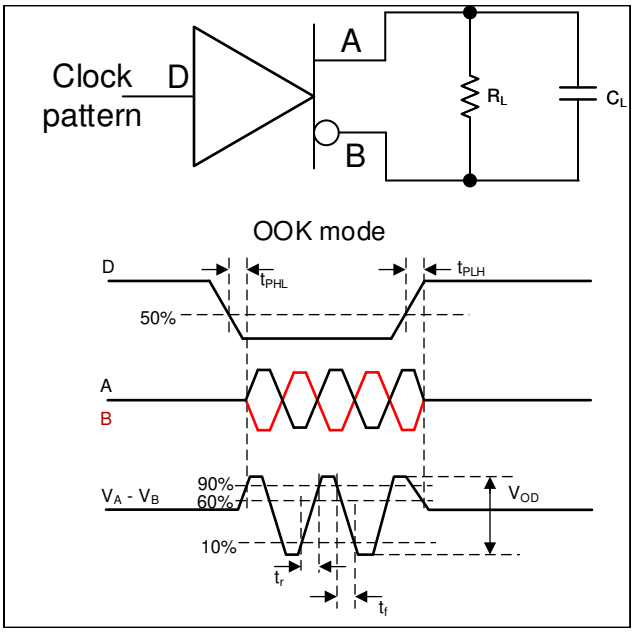


図 7-4. Measurement of Driver Switching Characteristics

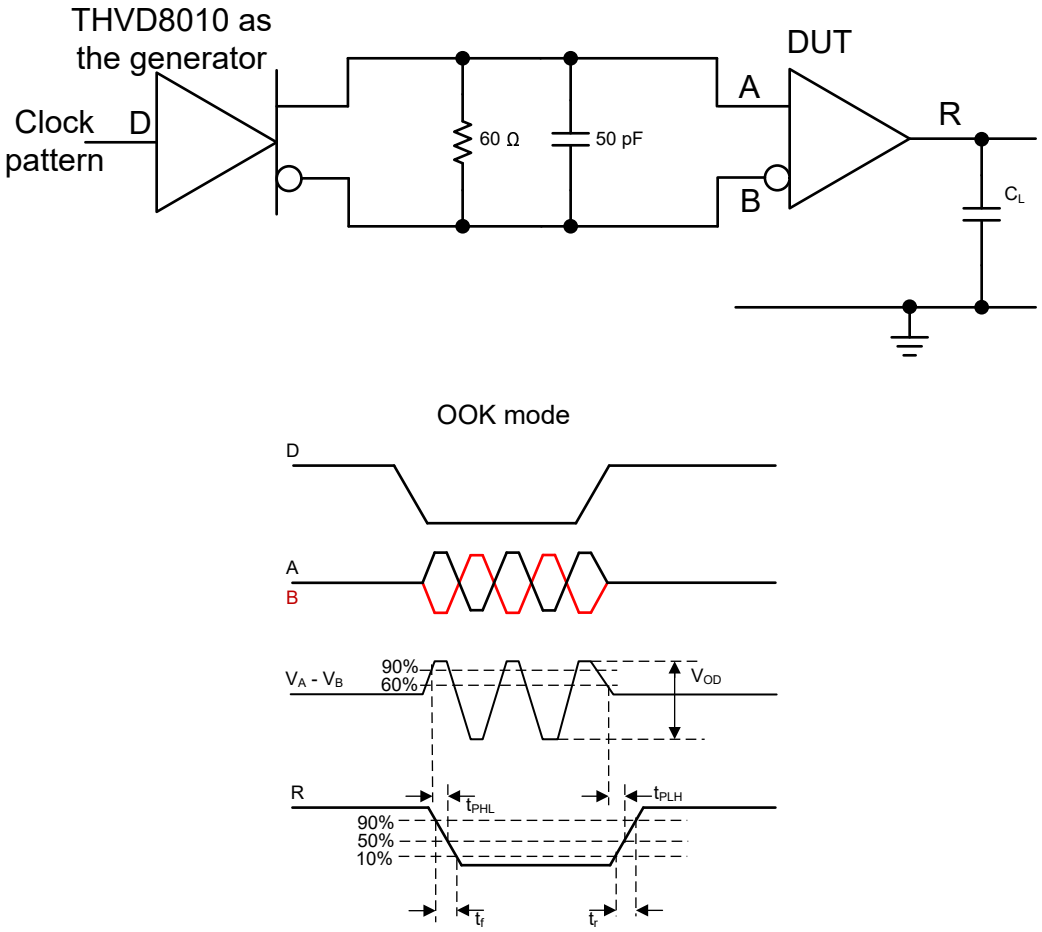


図 7-5. Measurement of Receiver Characteristics

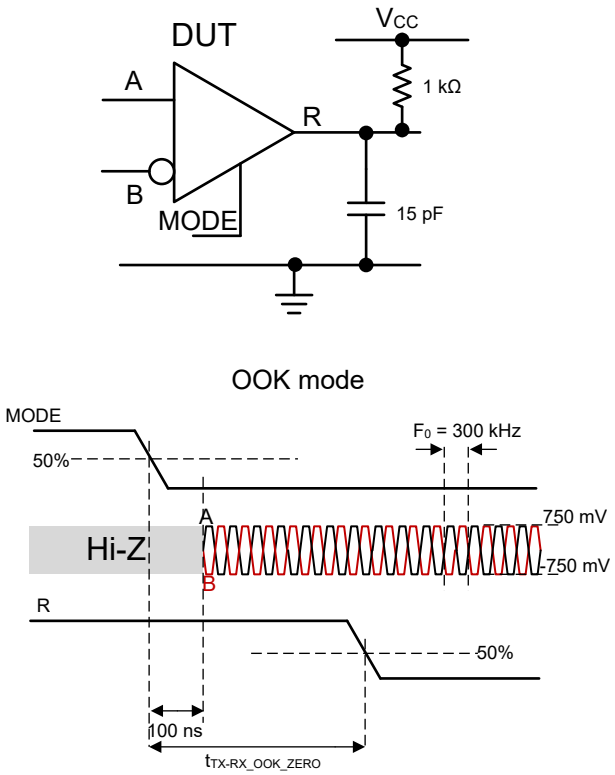


図 7-6. Transmit to Receive Mode Change with Low Output

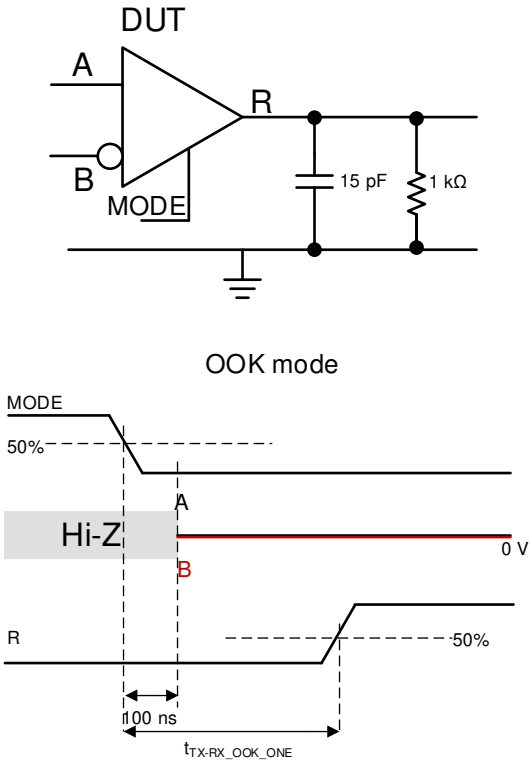


図 7-7. Transmit to Receive Mode Change with High Output

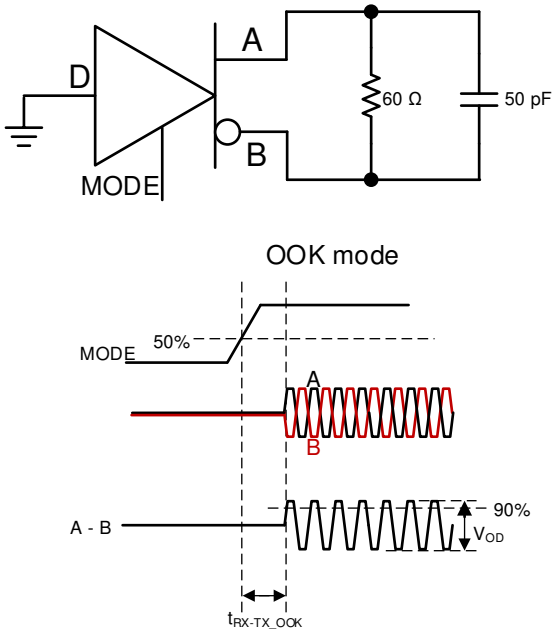


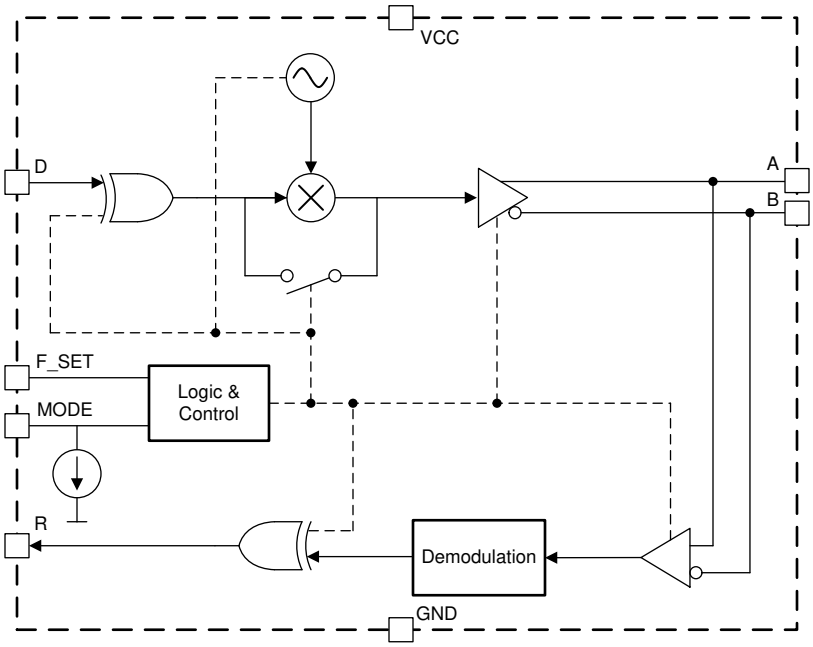
図 7-8. Receive to Transmit Mode Change

8 Detailed Description

8.1 Overview

THVD8010 enables power line communication using RS-485 physical layer signaling. An integrated OOK modulator enables RS-485 data to be directly coupled onto existing power cables via series capacitors without any updates to the MCU or the controller. The THVD8010 receiver extracts the data from the power cables through series capacitors by using a precise bandpass filter and a demodulator.

8.2 Functional Block Diagrams



8.3 Feature Description

8.3.1 OOK Modulation with F_SET pin

Data at the D input is modulated with the carrier frequency (f_0) which is set via the F_SET pin. 図 8-1 illustrates the modulation scheme. A high level at the D input is driven to the mid-level with zero differential voltage (V_{OD}). A low level at the D input is modulated at the carrier frequency. It is recommended to use a carrier frequency that is 10x higher than the data rate. Higher data rates are possible at the expense of increased pulse width distortion with the use of lower ratios.

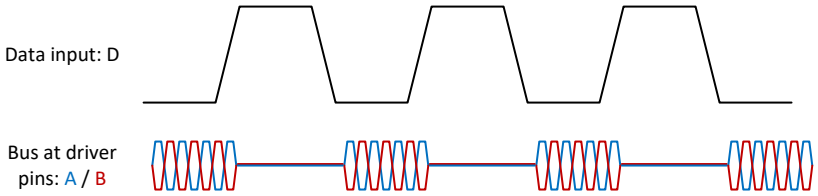


図 8-1. OOK Modulation Scheme

f_0 is programmable by changing the external resistor (R_{F_SET}) value connected to ground. 表 8-1 shows the carrier frequency for the each recommended resistor value.

表 8-1. OOK f_0 versus R_{F_SET}

R_{F_SET} (kΩ)	OOK f_0 (kHz)
77	125
50	187.5
31.9	300

The oscillator used to generate the carrier frequency features spread spectrum clocking to reduce emissions.

8.3.2 OOK Demodulation

The OOK signal received at the A and B inputs go through a bandpass filter and a peak detector to regenerate the original data stream. 図 8-2 shows the OOK input and the R output waveforms. The bandpass filter characteristics will adapt to optimal settings automatically based on the carrier frequency, set via R_{F_SET}.

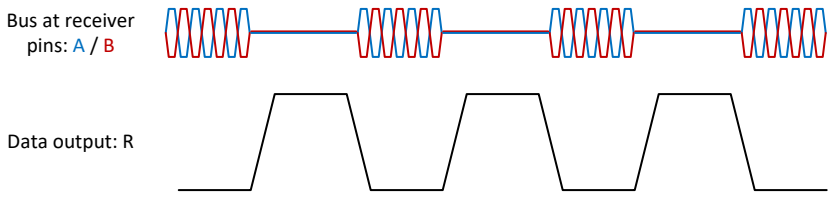


図 8-2. OOK Demodulation

8.3.3 Transmitter Timeout

The driver path incorporates a timeout feature to prevent a faulty node from occupying the bus indefinitely in a multi-drop application.

The driver stops transmitting and the outputs go high impedance if the D input doesn't detect an edge (either rising or falling) for longer than $t_{TX\_TIMEOUT}$. One of the following events brings the device back to normal operation.

- Any edge at D input
- Toggle MODE pin

The transmit path resumes operation within t_{MODE}.

8.3.4 Polarity Free Operation

THVD8010 is immune to A and B polarity at the receiver input in OOK mode. The receiver data comparator only checks for the receive input signal magnitude, ignoring the polarity, to determine its logic level. Note that reversing the polarity does result in degraded pulse width distortion.

8.3.5 Glitch Free Mode Change

The device incorporates a delay of up to t_{MODE} when changing the state of the MODE pin. This feature ensures that there are no glitches at the A, B and R outputs when transitioning between transmit and receive modes.

8.3.6 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV contact and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. This integrated protection eliminates the need of external components reducing the system BOM.

8.4 Device Functional Modes

表 8-2. Functional Modes

F_SET Configuration	Device Functional Mode
R_{F_SET} between F_SET and GND	OOK mode, f_0 set by the R_{F_SET} value
F_SET at high impedance	Invalid, not recommended for normal operation
F_SET at V_{CC}	
F_SET short to GND	

8.4.1 OOK Mode

Data at the D input is modulated with the carrier frequency set by the R_{F_SET} value when the device is transmitting (MODE = V_{CC}). See セクション 8.3.1 section for more details. In receiving (MODE = GND), the device expects an OOK modulated signal at the A and B inputs. The data is demodulated and sent out via R pin. See セクション 8.3.2 section for more details.

表 8-3. Driver function table for OOK mode

INPUTS			OUTPUTS		FUNCTION
F_SET	MODE	D	A	B	
R_{F_SET} (See 表 8-1)	H	H or Z	Bias to V_{CM}	Bias to V_{CM}	Driver is actively biased to V_{CM} on the bus
	H	L	Oscillating	Oscillating	Bus actively driven at carrier frequency
	L or Z	X	Z	Z	Driver disabled, device in receive mode

表 8-4. Receiver function table for OOK mode

INPUTS			OUTPUT	FUNCTION
F_SET	MODE	Input	R	
R_{F_SET} (See 表 8-1)	L or Z	Oscillating at F_SET and $V_{ID} > V_{MAG\_ZERO}$	L	Receive valid bus low
	L or Z	Oscillating at F_SET and $V_{MAG\_ONE} < V_{ID} < V_{MAG\_ZERO}$	?	Receive invalid bus, output indeterminate
	L or Z	Oscillating at F_SET and $V_{ID} < V_{MAG\_ONE}$	H	Receive valid bus high
	L or Z	Z / not oscillating	H	Receive valid bus high
	L or Z	OPEN, SHORT, IDLE (V_{ID} = 0 V)	H	Failsafe high output
	H	X	Z	Receiver disabled, device in transmit mode

8.4.2 Thermal shutdown (TSD)

The THVD8010 has a protection feature called thermal shutdown. When the junction temperature reaches T_{SD}, the device enters thermal shutdown protection mode. This mode disables the driver and receiver outputs, which will halt all communication through the device. Normal operation resume once the junction temperature drops out of thermal shutdown, which is typically T_{SD} - T_{HYS}.

9 Application and implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application information

The THVD8010 is able to transmit data over an AC coupled power line pair using On-Off Keying (OOK).

9.2 Typical application (OOK mode)

In order to combine data and power over a single pair of wires, capacitors and inductors are used in a bias-tee configuration. High-frequency differential data is AC-coupled onto the bus lines via series capacitances while power is DC-coupled via series inductances. The values of these components will depend on the carrier frequency, number of nodes on the bus, and the power delivery requirements (i.e., voltage and total current sourced or consumed by a given node).

In 図 9-1, there is an optional rectifier network pictured on the bus lines. This network of diodes can ensure that the node is receives power correctly from the bus wires, even if the lines get swapped.

A termination resistance, R_T, is not required for device functionality but can be useful in improving signal integrity in some applications by reducing reflections that can occur at cable ends.

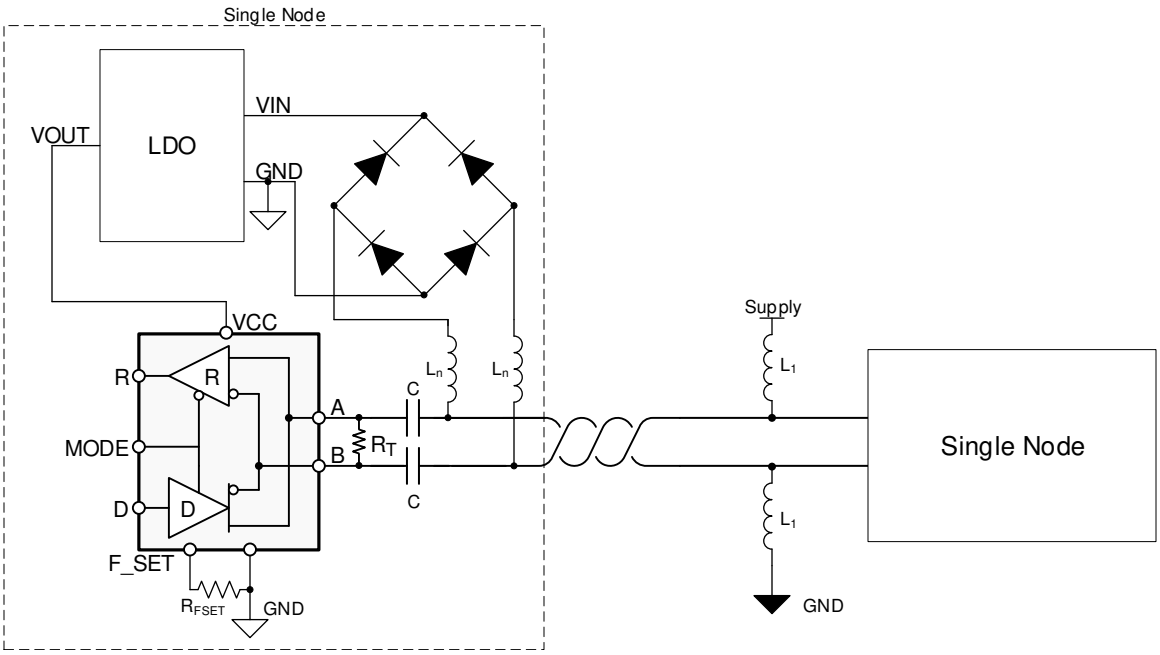


図 9-1. Typical power line network with 2 nodes

9.2.1 Design requirements

The main requirements are the values of the bus capacitors and the power inductors. Both of these values are dependant upon the carrier frequency selected.

9.2.1.1 Carrier frequency

This device uses on-off-keying to transmit binary data on the bus. Please read セクション 8.3.1 for detailed information. The modulation and demodulation of the data can result in pulse width distortion due to asymmetries in low-to-high and high-to-low transition times. These asymmetries are due to factors like

synchronization of the data to the internal carrier oscillator in the transmit path and the response time of the band-pass filter in the receive path. The impact of these factors can be minimized by choosing a carrier frequency much higher than the data rate required. A frequency ratio of at least 10:1 is recommended.

9.2.2 Detailed design procedure

9.2.2.1 Inductor value selection

It is important to note that the inductor selected must also take power consumption into consideration. The inductor should be sized to handle the maximum anticipated current in addition to the inductance value.

The parallel aggregate impedance should be selected so that the total equivalent impedance at the carrier frequency is Z ≥ 375 Ω. This assumes RS-485 loading with 60 Ω termination. If no termination is used in the application, then the total equivalent impedance at the carrier frequency could be reduced to Z ≥ 60 Ω. These examples assume that termination is used. 式 1 shows the parallel aggregate impedance equation for inductors L_1 to L_n. Since the inductance value for each node should be the same, it's simple to determine that each node's impedance should be n times the total equivalent impedance. For example, if there are 4 nodes connected to the bus and the equivalent impedance is 375 Ω, then each node impedance should be 1,500 Ω.

$$Z = Z_1 \,||Z_2\,||\,..||\,Z_n \tag{1}$$

To determine the suggested inductance value, 式 2 can be rearranged to determine L_n, as shown in 式 3.

$$Z_n = 2\pi f_0 L_n \tag{2}$$

$$L_n = \frac{Z_n}{2\pi f_0} \tag{3}$$

f_0 is the carrier frequency (OOK frequency) used. If the previous 1.5 kΩ impedance per node is assumed with a carrier frequency of 300 kHz, the resulting inductance limit is ~800 µH per node. Be aware that this is the minimum suggested value per node. Refer to 図 9-2 as a quick reference on the minimum inductance value to achieve 375 Ω of total aggregate impedance. This value can be multiplied by the number of nodes on the bus to get the minimum inductance per node. Referring to the previous example, if there are 4 nodes and a carrier frequency of 300 kHz, then the minimum aggregate inductance is about 200 µH, which is 800 µH when multiplied by 4.

9.2.2.2 Capacitor value selection

Capacitor selection is easier than inductor selection, primarily because capacitance impedance is important to allow higher frequency signals through. However, the capacitor ratings for voltage must be carefully selected to meet the application requirements. Special considerations for hot plug nodes should be made to ensure that voltage transients during hot plugging do not exceed the absolute maximum values. See セクション 6.1.

The number of nodes on the bus does not play into the capacitance calculation. The impedance of a capacitor is shown in 式 4.

$$Z = \frac{1}{2\pi f_0 C} \tag{4}$$

Maintaining Z ≤ 5 Ω keeps the impedance low enough at the carrier frequency to allow data to pass through. If the equation is rearranged to calculate C, the result is shown in 式 5.

$$C = \frac{1}{2\pi f_0 Z} \tag{5}$$

If the previous example of a 300 kHz carrier frequency is used, then a minimum capacitance value of about 106 nF. For a quick reference, refer to 図 9-3.

9.2.3 Application Curves

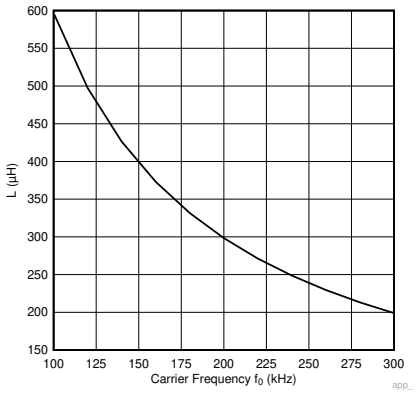


図 9-2. Inductor selection (select values above the line)

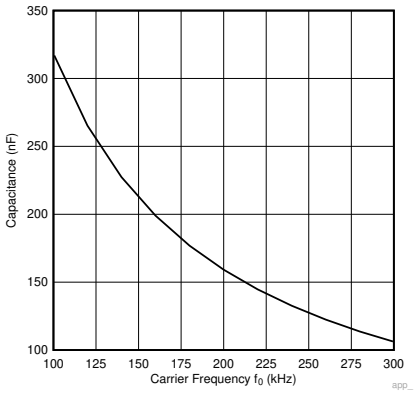


図 9-3. Capacitor selection (select values above the line)

10 Power supply recommendations

To ensure reliable operation at all data rates and supply voltages, the supply should be decoupled with a 100 nF ceramic capacitor and a 1 µF capacitor (for ESD sensitive designs) located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Place F_SET components near the pin to keep capacitance load below recommended value
4. Use a pull up or down resistor on mode to set a default state
5. Apply 100-nF to 220-nF and a 1-uF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
6. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
7. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
8. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
9. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

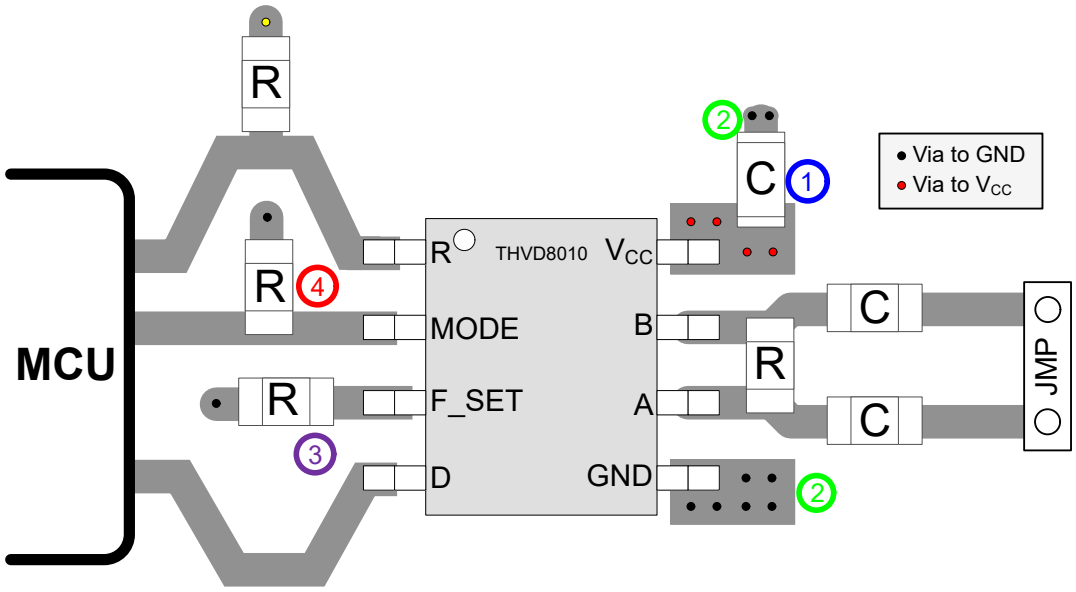


図 11-1. Layout Example (OOK)

12 Device and Documentation Support

12.1 Device Support

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD8010DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8010
THVD8010DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8010

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

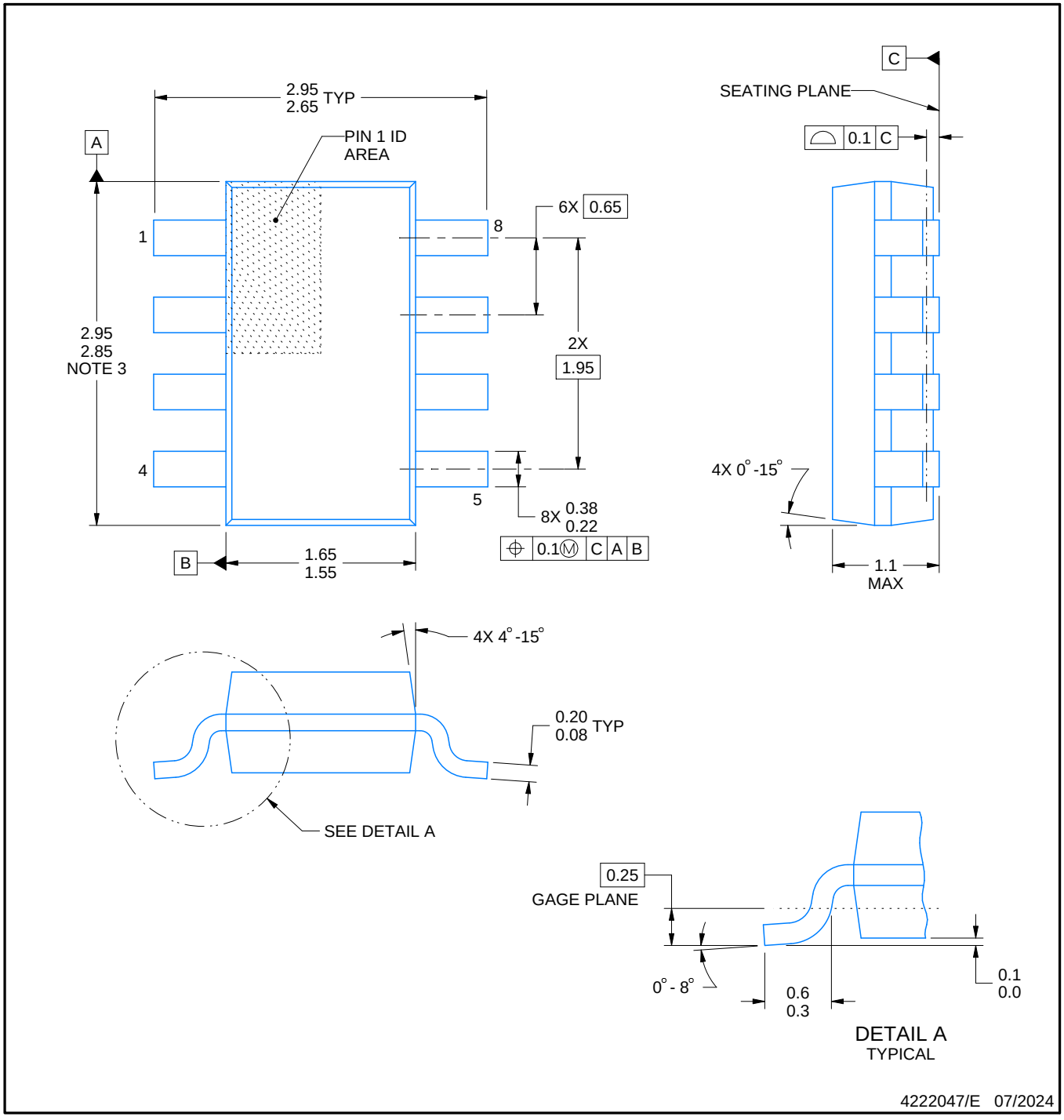
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DDF0008A

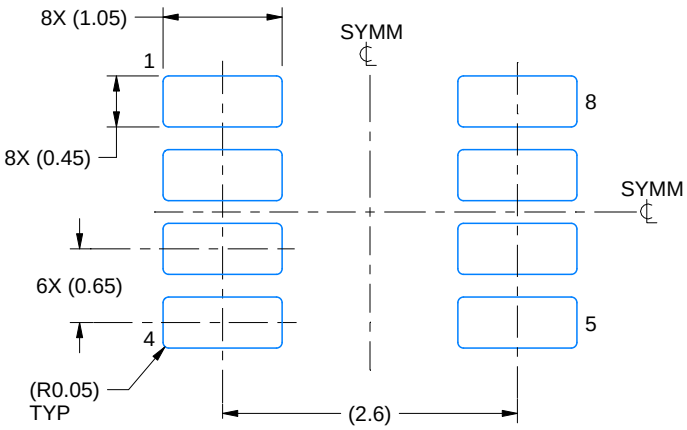
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

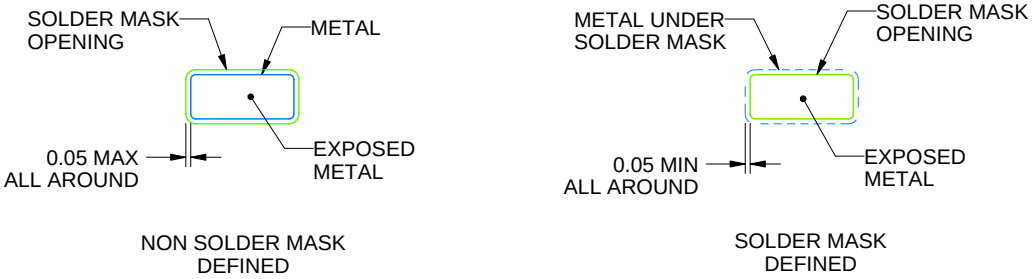


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

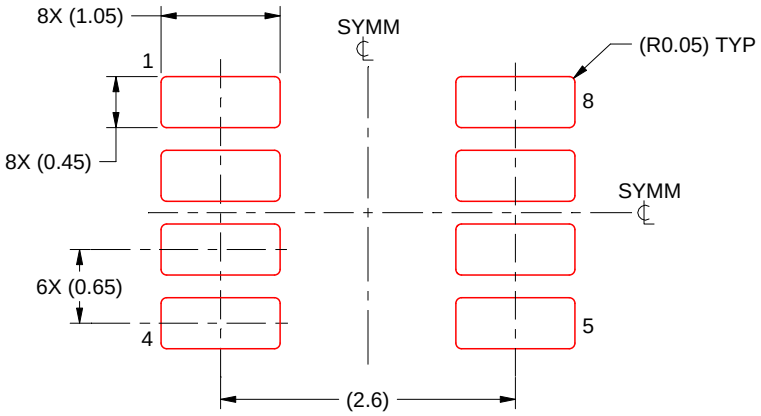
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月