THVD1520 ±8kV IEC ESD 保護の 10Mbps RS-485 トランシーバ

1 特長

- TIA/EIA-485A 規格の要件を満たすか、それを上回る性能
- 電源電圧：4.5V～5.5V
- 10Mbps、半二重 RS-422/RS-485
- バス I/O 保護
  - ± 16kV HBM ESD
  - ± 8kV IEC 61000-4-2 接触放電
  - ± 8kV IEC 61000-4-2 エアギャップ放電
  - ± 4kV IEC 61000-4-4 高速過渡バースト
- 拡張産業用温度範囲：-40℃～125℃
- レシーバの大きなヒステリシスによるノイズ除去
- 低消費電力
  - 低いスタンバイ時消費電流:1μA 未満
  - 動作時の静止電流:840μA 未満
- グリッチなしの電源オン/オフによるホット・プラグイン機能
- 開放、短絡、アイドル・バスのフェイルセーフ
- 1/8 単位負荷 (最大 256 のバス・ノード)

2 アプリケーション

- ファクトリ・オートメーション/制御
- ビルディング・オートメーション
- HVAC システム
- ビデオ監視
- スマート・メータ

3 概要

THVD1520 は、産業用アプリケーション向けの堅牢な半二重 RS-485 トランシーバです。バスのピンは高レベルの IEC 接触放電 ESD への耐性があるため、システム・レベルでの追加保護部品が不要です。

このデバイスは、単一の 5V 電源で動作します。同相電圧範囲が広く、バスのピンでの入力リークが小さいため、THVD1520 は長いケーブルを使用するマルチポイントのアプリケーションに適しています。

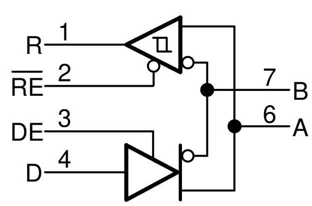
THVD1520 は、業界標準の 8 ピン SOIC パッケージで供給され、ドロップイン互換性があります。周囲温度 –40℃～125℃での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
THVD1520	SOIC (8)	4.90mm×3.91mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

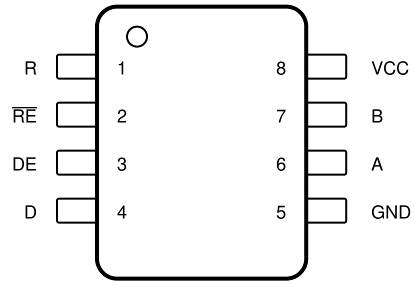
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019 年 10 月	*	初版

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low (internal 5-MΩ pull-up)
DE	3	Digital input	Driver enable, active high (internal 5-MΩ pull-down)
D	4	Digital input	Driver data input (internal 5-MΩ pull-up)
GND	5	Ground	Device ground
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
V_{CC}	8	Power	5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, DE or $\overline{RE}$)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs, as differential or common-mode with respect to GND	–18	18	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus terminals and GND	±16,000	V
			All other pins	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±8,000	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND	±8,000	
		IEC 61000-4-4 EFT (Fast transient or burst), bus terminals and GND	±4,000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate				10	Mbps
T_J	Junction temperature		–40		150	°C
T_A (2)	Operating ambient temperature		–40		125	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the device when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC(1)		THVD1520 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	V_{test} from –7 to +12 V	See 図 7	1.5	2.5		V
		R_L = 54 Ω (RS-485), C_L = 50 pF	See 図 8	1.5	2.5		
		R_L = 100 Ω (RS-422), C_L = 50 pF		2	3		
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of driver differential-output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF	See 図 8	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF	See 図 8	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				220		mV
$\lvert I_{OS} \rvert$	Driver short-circuit output current	DE = V_{CC}, -7 V ≤ [V_A or V_B] ≤ 12 V, or A pin shorted to B pin				150	mA
C_{OD}	Differential output capacitance				8		pF
Receiver							
I_I	Bus input current (driver disabled)	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	110	µA
			V_I = –7 V	–90	–70		
R_A, R_B	Bus input impedance	V_A = -7 V, V_B = 12 V and V_A = 12 V, V_B = -7 V	See 図 12	96			kΩ
V_{IT+}	Positive-going receiver differential-input voltage threshold				–90	–50	mV
$V_{IT–}$	Negative-going receiver differential-input voltage threshold			–200	–150		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		–1		1	µA
I_{OSR}	Receiver output short-circuit current	$\overline{RE}$ = 0, DE = 0	See 図 13			95	mA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)			–2.5		2.5	µA
Supply							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = 0, no load		600	840	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC}, no load		440	580	
		Driver disabled, receiver enabled	DE = 0, $\overline{RE}$ = 0, no load		530	680	
		Driver and receiver disabled	DE = 0, $\overline{RE}$ = V_{CC}, no load		0.1	1	

(1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than $V_{IT–}$.

6.7 Power Dissipation Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNIT
PD	Power dissipation, driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated	R_L = 300 Ω, C_L = 50 pF	100	mW
		RS-422 load	R_L = 100 Ω, C_L = 50 pF	135	
		RS-485 load	R_L = 54 Ω, C_L = 50 pF	190	

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		See 図 9	10	17	30	ns
t_{PHL}, t_{PLH}	Driver propagation delay		See 図 9		20	35	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} – t_{PLH}\|$		See 図 9		0.8	4	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See 図 10 and 図 11		25	100	ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled	See 図 10 and 図 11		25	100	ns
		Receiver disabled	See 図 10 and 図 11		1.5	3	µs
Receiver							
t_r, t_f	Receiver output rise and fall times		See 図 14		5	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		See 図 14		50	95	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} – t_{PLH}\|$		See 図 14		3	15	ns
t_{PHZ}, t_{PLZ}	Receiver disable time		See 図 15		15	30	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See 図 15		25	170	ns
		Driver disabled	See 図 16		1	5	µs

6.9 Typical Characteristics

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

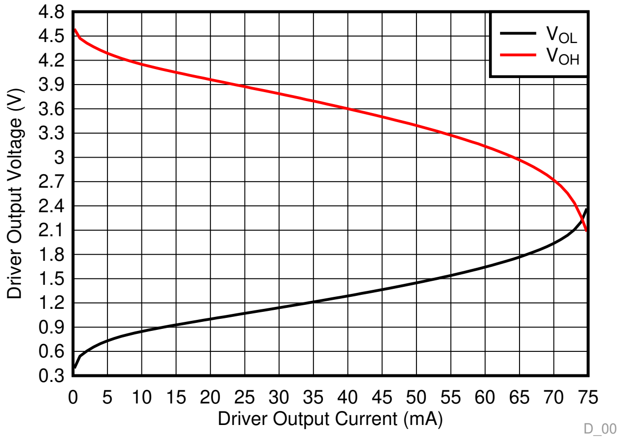


図 1. Driver Output Voltage vs Driver Output Current

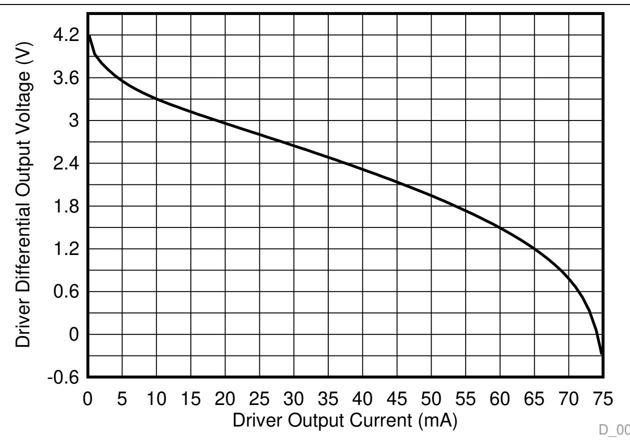


図 2. Driver Differential Output Voltage vs Driver Output Current

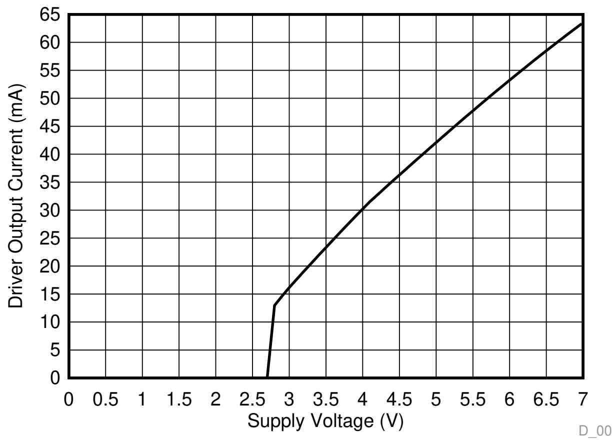


図 3. Driver Output Current vs Supply Voltage

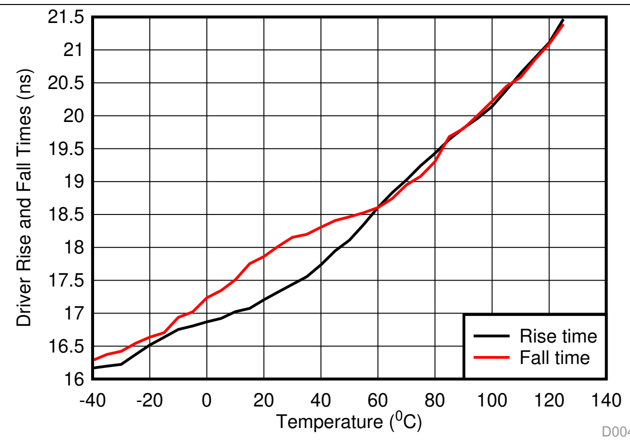


図 4. Driver Rise or Fall Time vs Temperature

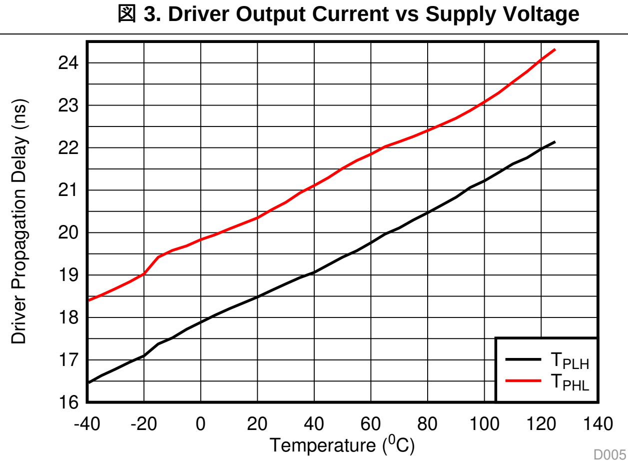
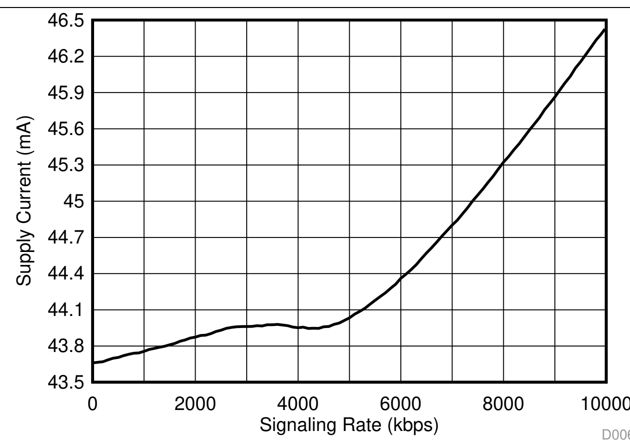


図 5. Driver Propagation Delay vs Temperature



50% duty cycle square-wave R_L = 54 Ω C_L = 50 pF   DE = V_{CC}, $\overline{RE}$ = GND

図 6. Supply Current vs Signaling Rate

7 Parameter Measurement Information

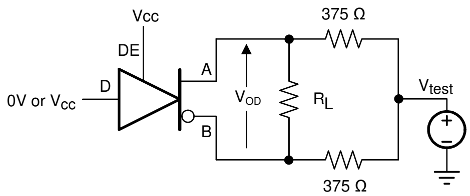


図 7. Measurement of Driver Differential Output Voltage With Common-Mode Load

図 8. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

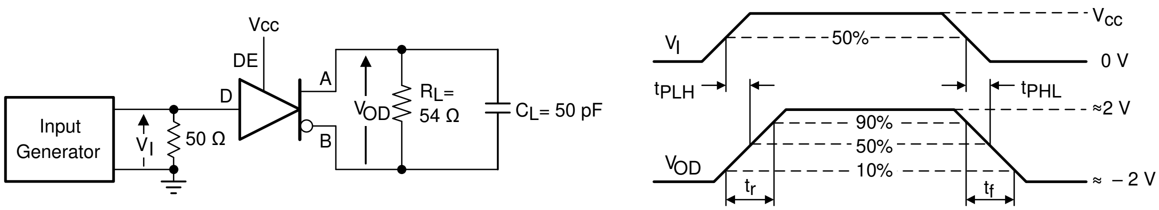


図 9. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

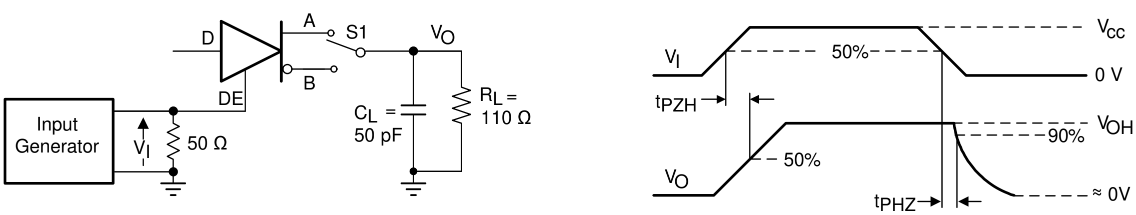


図 10. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

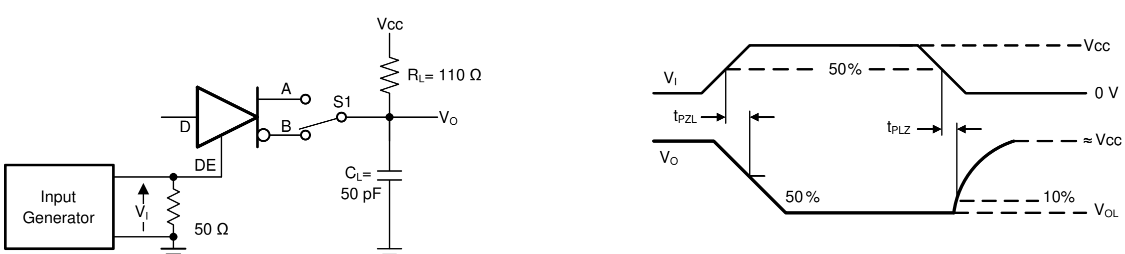


図 11. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (continued)

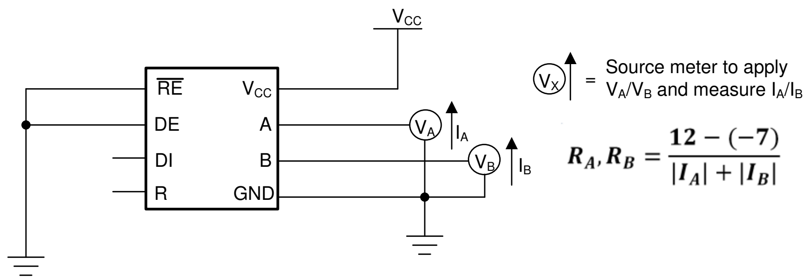


図 12. Measurement of Bus Impedance

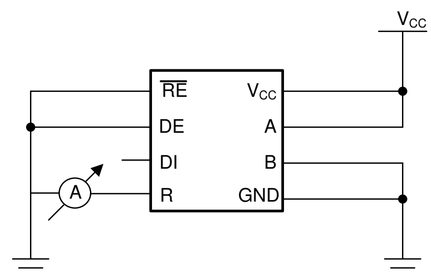


図 13. Measurement of Receiver Output Short Circuit Current

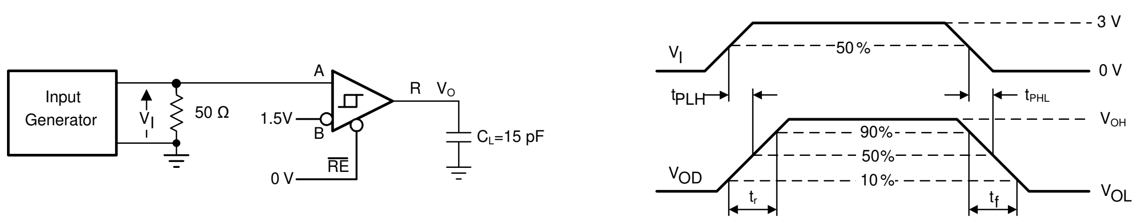


図 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

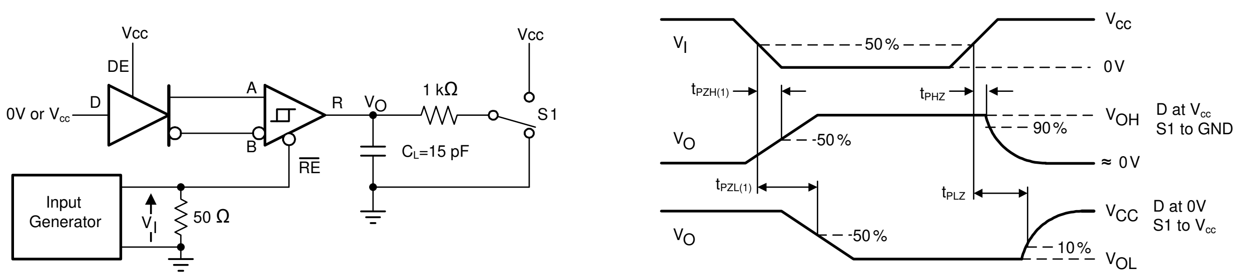


図 15. Measurement of Receiver Enable/Disable Times With Driver Enabled

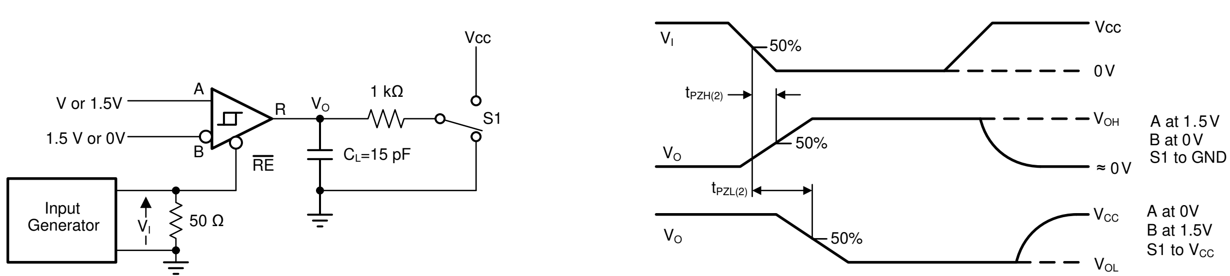


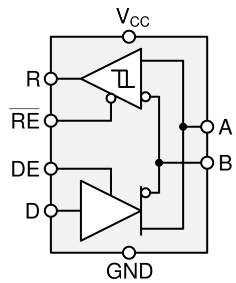
図 16. Measurement of Receiver Enable Times With Driver Disabled

8 Detailed Description

8.1 Overview

The THVD1520 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 10 Mbps.

8.2 Functional Block Diagrams



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV (contact discharge), ±8 kV (air gap discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THVD1520 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

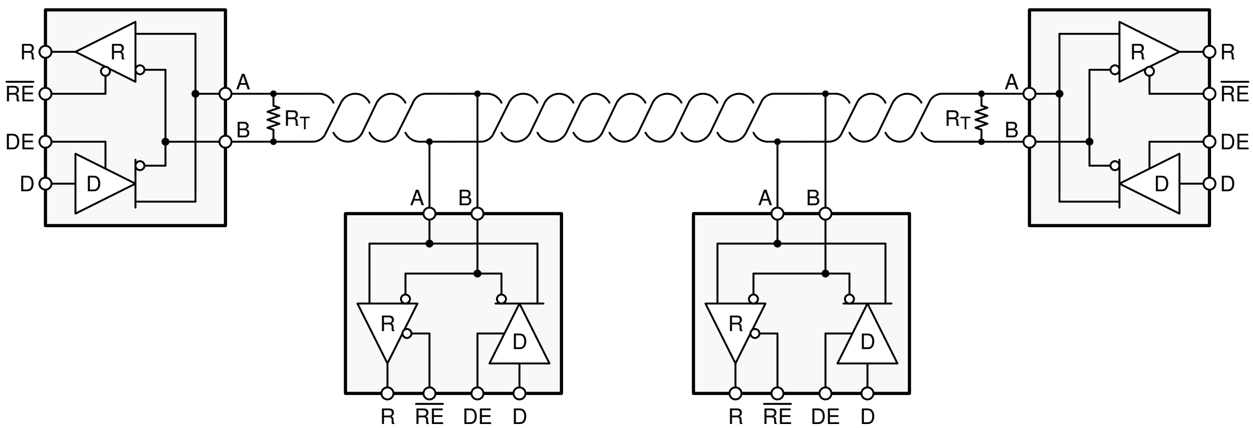


図 17. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \le 0.1 \times t_r \times v \times c$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c (1)

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1520 consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receivers of the THVD1520 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{HYS} (the separation between V_{IT+} and $V_{IT–}$). As shown in the table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

Typical Application (continued)

9.2.1.5 Transient Protection

The bus pins of the THVD1520 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

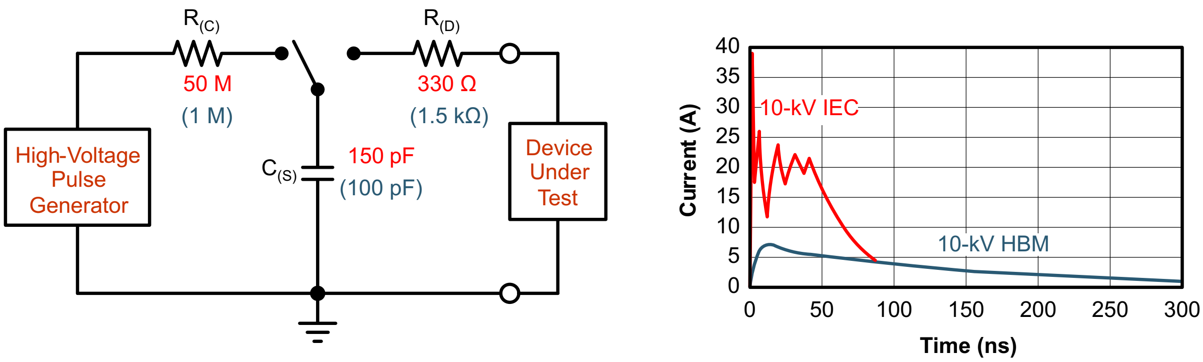


図 18. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

図 19 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

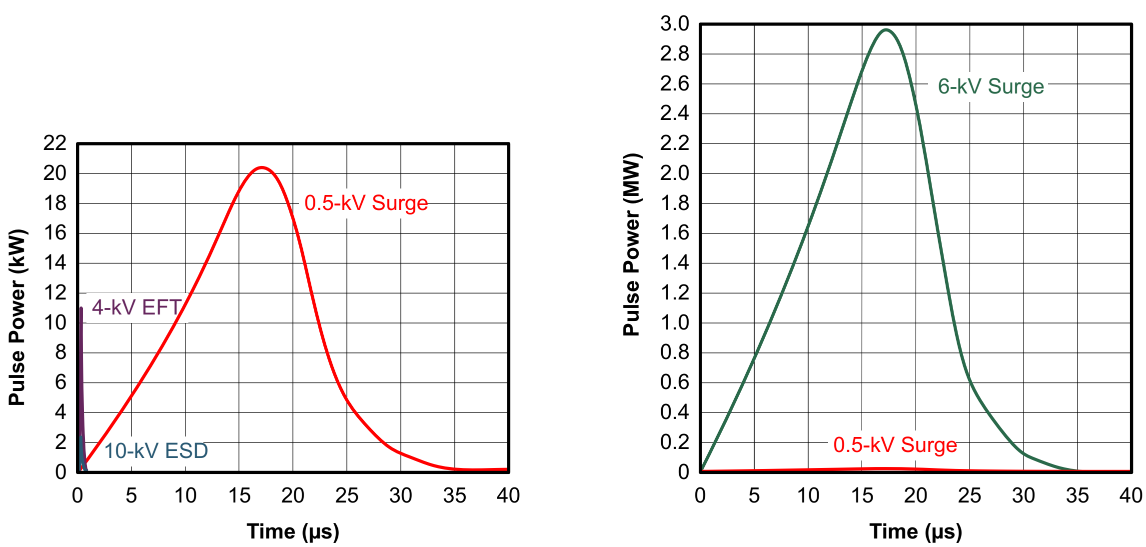


図 19. Power Comparison of ESD, EFT, and Surge Transients

Typical Application (continued)

In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 図 20 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

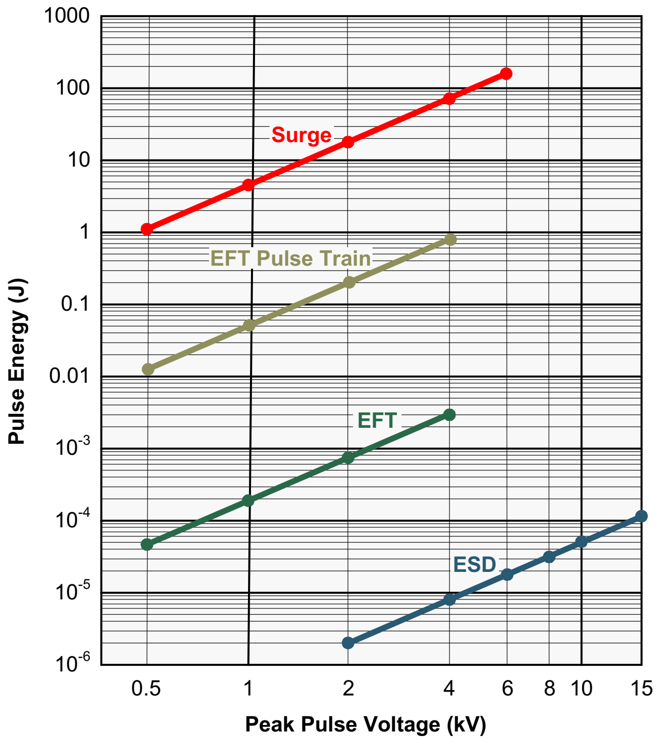


図 20. Comparison of Transient Energies

Typical Application (continued)

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. 図 21 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 3 shows the associated bill of materials.

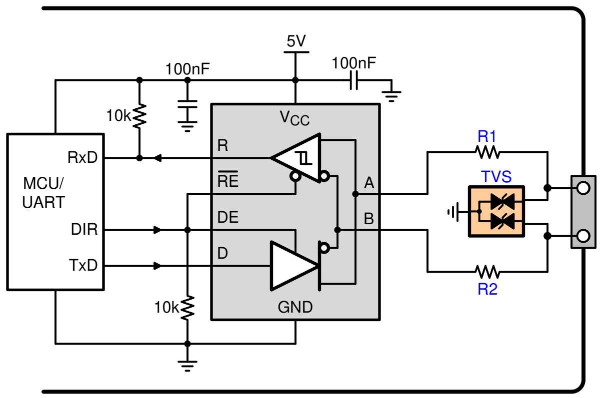


図 21. Transient Protection Against Surge Transients for Half-Duplex Devices

表 3. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD1520	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curves

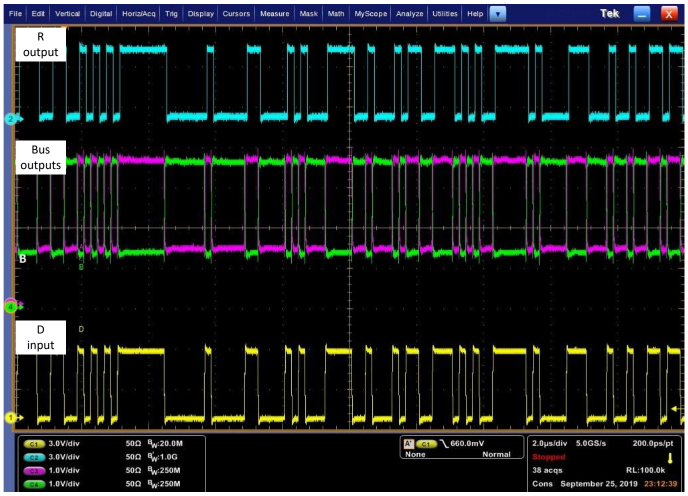


図 22. Waveforms at 10 Mbps Operation, PRBS7 Data Pattern

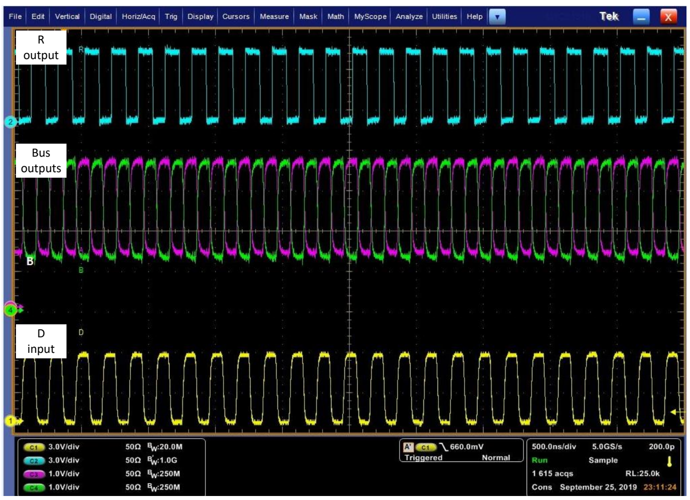


図 23. Waveforms at 10 Mbps Operation, Clock Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

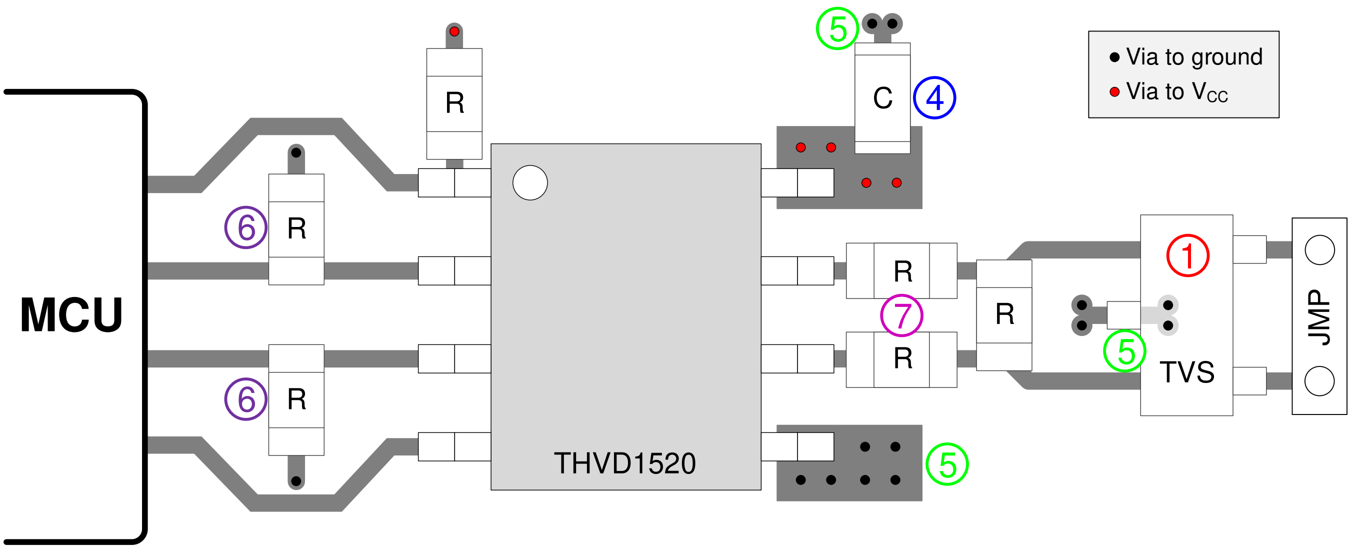


図 24. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1520DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520
THVD1520DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1520

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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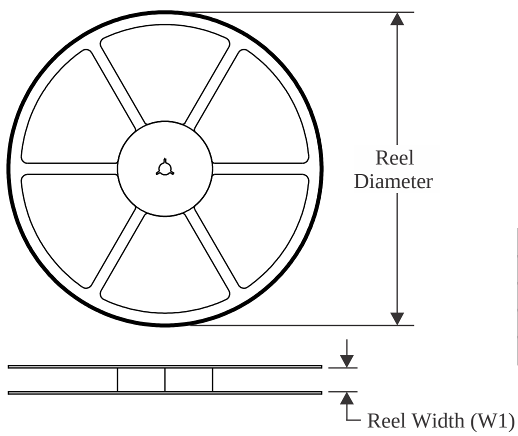
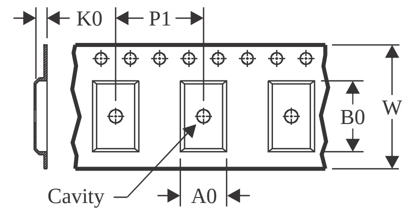
REEL DIMENSIONS

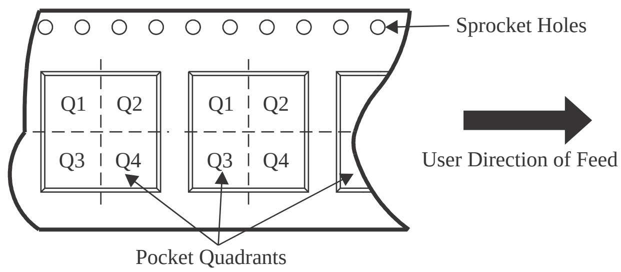


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

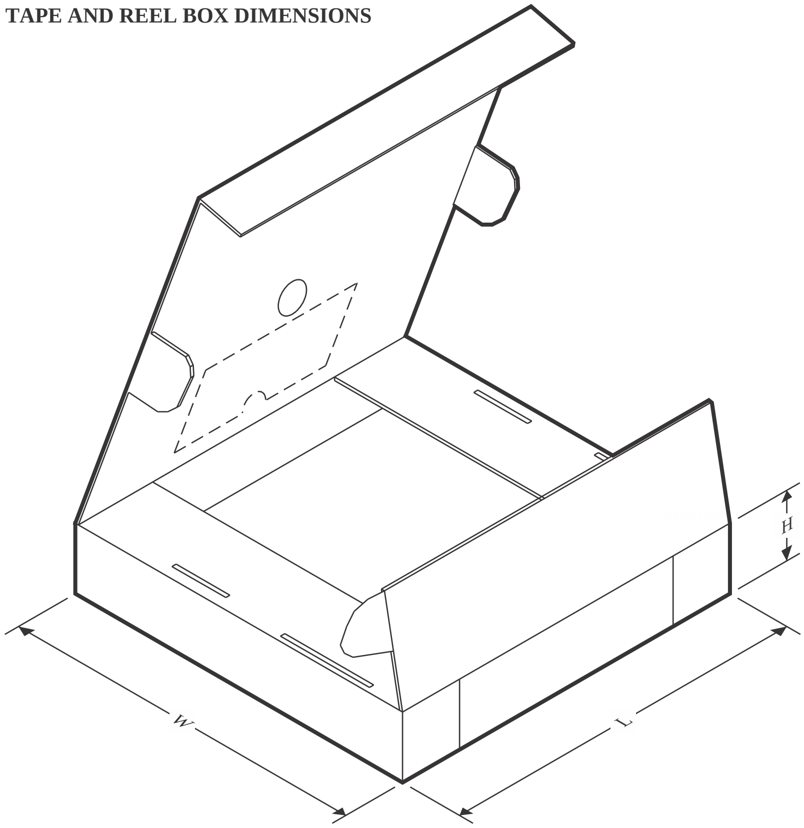
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

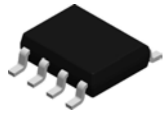
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1520DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1520DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

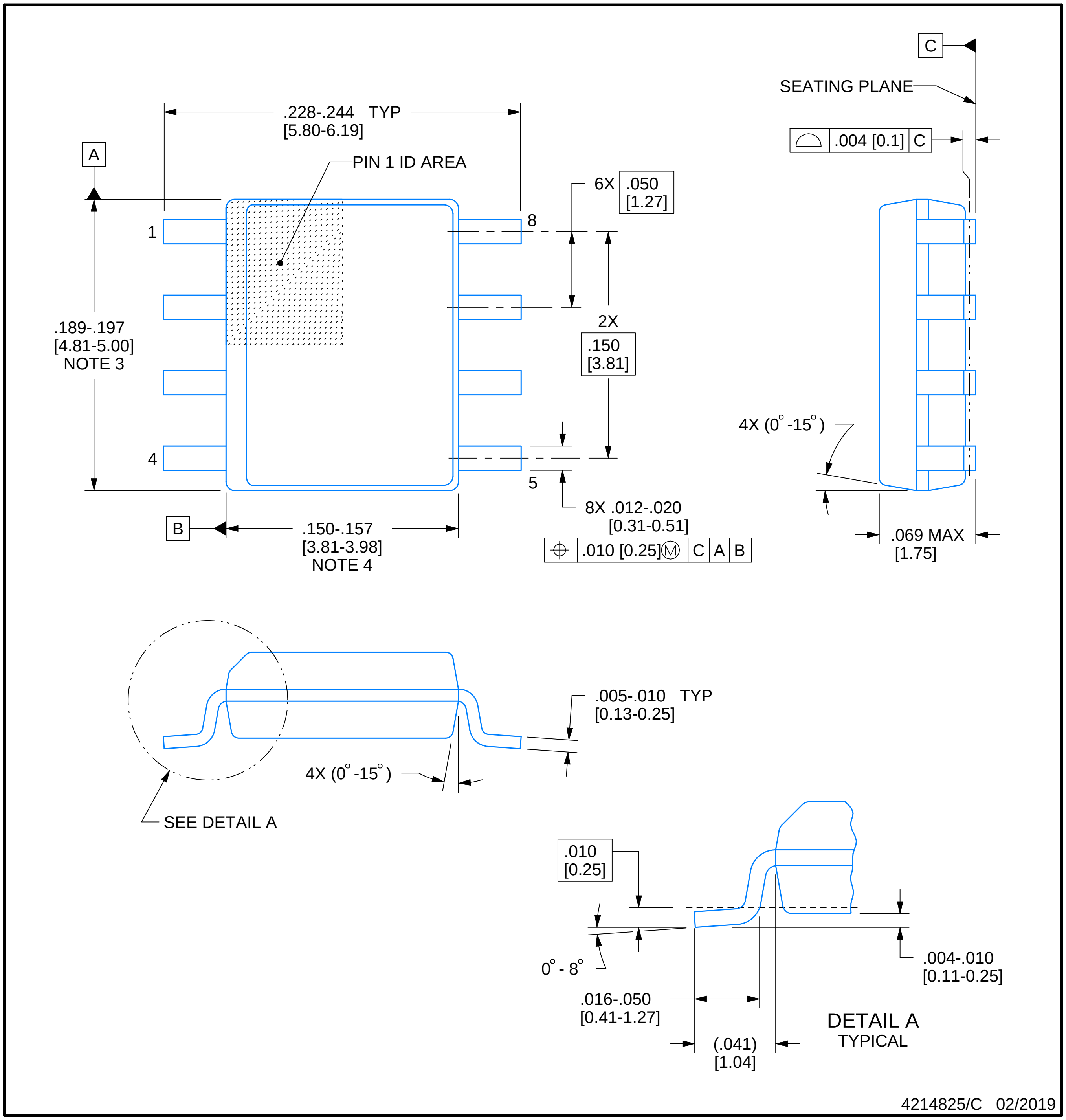
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1520DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1520DRG4	SOIC	D	8	2500	353.0	353.0	32.0



D0008A

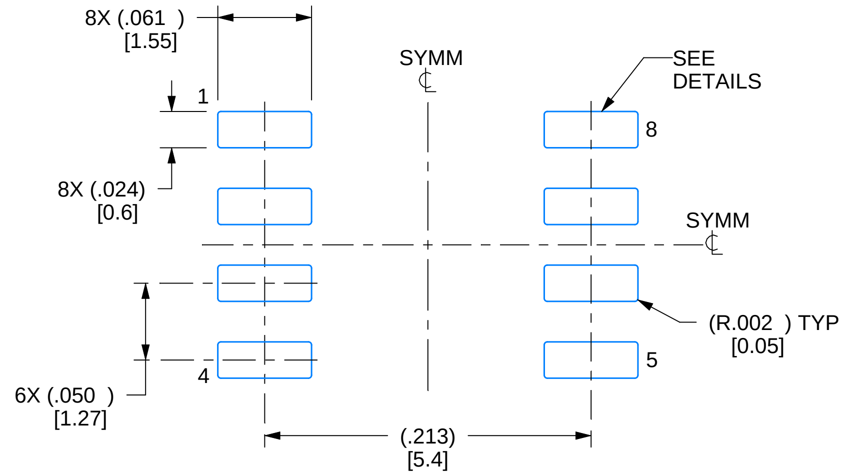
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

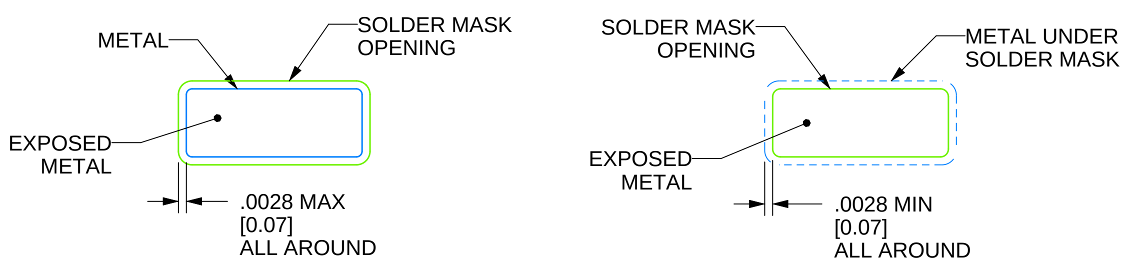


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

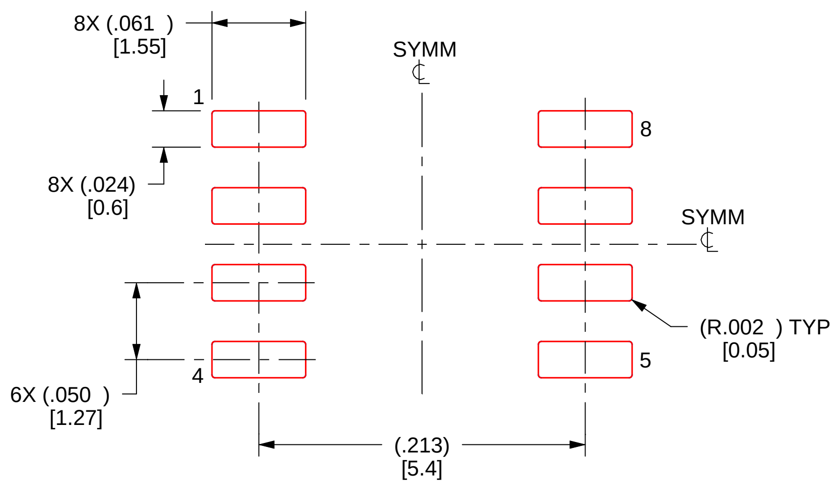
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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