THS3001 420MHz、高速、電流帰還型アンプ

1 特長

- 高速度:
  - 420MHz の帯域幅 (G = 1、-3dB)
  - スルー レート:6500V/µs
  - 40ns のセトリング タイム (0.1%)
- 高い出力駆動能力:I_O = 100 mA
- 非常に優れたビデオ性能
  - 115MHz の帯域幅 (0.1dB、G = 2)
  - 0.01% の差動ゲイン
  - 0.02° の差動位相
- 小さい入力オフセット電圧: 3mV (最大値)
- 非常に低い歪み:
  - THD = -96dBc (f = 1MHz 時)
  - THD = -80dBc (f = 10MHz 時)
- 広範な電源:
  - V_{CC} = ±4.5V～±16V
- 評価基板を提供

2 アプリケーション

- 通信
- 画像処理
- 高品質ビデオ

3 概要

THS3001 は、通信、画像処理、高品質ビデオ アプリケーション用に設計された高速の電流帰還型オペアンプです。このデバイスは、優れた過渡応答を必要とする大信号アプリケーション向けに、6500V/µs の非常に高速なスルーレート、420MHz の帯域幅、40ns のセトリング時間を実現しています。また、THS3001 は -96dBc の非常に小さい歪みで動作するため、ワイヤレス通信基地局または超高速 ADC/DAC バッファなどのアプリケーションに最適です。

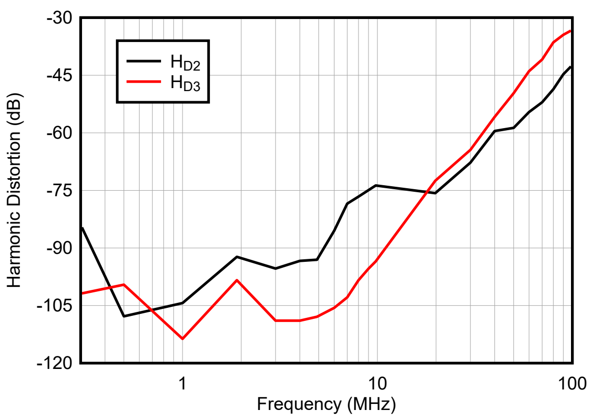
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
THS3001	D (SOIC、8)	4.9mm × 6mm
	DGN (HVSSOP、8)	3mm × 4.9mm

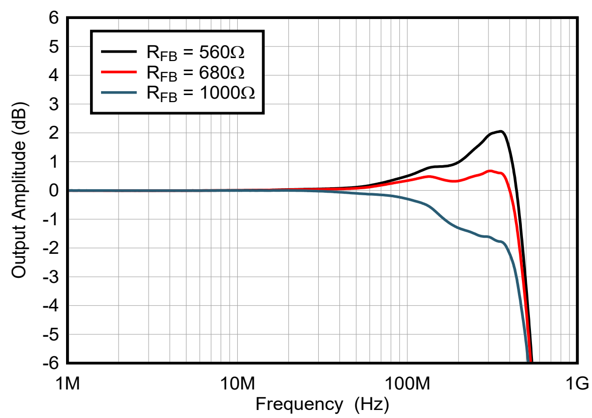
(1) 詳細は、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。

関連デバイス

THS4011 THS4012	290MHz VFB 高速アンプ
THS6012	500mA CFB 高速アンプ
THS6022	250mA CFB 高速アンプ



高調波歪みと周波数との関係



出力振幅と周波数との関係

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4 Pin Configuration and Functions

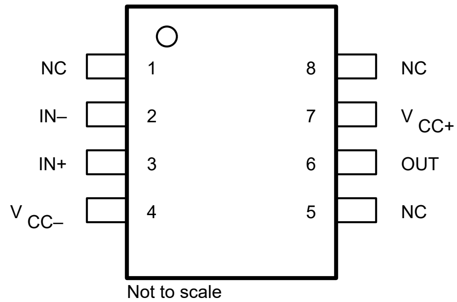


図 4-1. THS3001: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No internal connection
2	IN–	Input	Inverting input
3	IN+	Input	Noninverting input
4	V_{CC-}	Input	Negative power-supply connection
5	NC	—	No internal connection
6	OUT	Output	Amplifier output
7	V_{CC+}	Input	Positive power-supply connection
8	NC	—	No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNITS
Vcc	Supply voltage, V_{CC+} to V_{CC-}		33	V
V_I	Input voltage	$\pm V_{CC}$	$\pm V_{CC}$	V
I_O	Output current		175	mA
V_{ID}	Differential input voltage		±6	V
T_J	Maximum junction temperature		150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability[2]		125	°C
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability and/or lifetime of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual-supply	±4.5	±15	±16	V
		Single-supply	9	30	32	
T_A	Operating free-air temperature		–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC[1]		THS3001		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.5	56.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	78.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	29.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	4.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	29.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.5	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, R_L = 150Ω, and R_F = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (-3dB)	G = 1, R_F = 1kΩ	V_{CC} = ±5V		330		MHz
			V_{CC}= ±15V		420		
		G = 2	V_{CC} = ±5V, R_F = 750Ω		300		
			V_{CC} = ±15V, R_F = 680Ω		385		
		G = 5	V_{CC} = ±15V, R_F = 560Ω		350		
	Bandwidth for 0.1dB flatness	G = 2	V_{CC} = ±5V, R_F = 750Ω		65		
			V_{CC} = ±15V, R_F = 680Ω		55		
	Full power bandwidth[2]	V_{CC} = ±5V, $V_{O(PP)}$ = 4V, R_L = 500Ω	G = –5		65		
			G = 5		62		
		V_{CC} = ±15V, $V_{O(PP)}$ = 20V, R_L = 500Ω	G = –5		32		
			G = 5		31		
SR	Slew rate[1]	V_{CC} = ±5V, $V_{O(PP)}$ = 4V	G = –5		1700		V/µs
			G = 5		1300		
		V_{CC} = ±15V, $V_{O(PP)}$ = 20V	G = –5		6500		
			G = 5		6300		
t_s	Settling time to 0.1%	Gain = –1	V_{CC} = ±15V, 0V to 10V Step		40		ns
			VCC = ±5V, 0V to 2V Step,		25		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = ±15V, $V_{O(PP)}$ = 2V, G = 2, f_c = 10MHz			–80		dBc
V_n	Input voltage noise	V_{CC} = ±5V or ±15V G = 2, f = 10kHz			1.6		nV/√Hz
I_{np}	Noninverting input current noise	V_{CC} = ±5V or ±15V, f = 10kHz, G = 2			13		pA/√Hz
I_{nn}	Inverting input current noise	V_{CC} = ±5V or ±15V, f = 10kHz, G = 2			16		pA/√Hz

5.5 Electrical Characteristics (続き)

at T_A = 25°C, R_L = 150Ω, and R_F = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
V_{IO}	Input offset voltage	V_{CC} = ±5V or ±15V	T_A = 25°C		1	3	mV
			T_A = full range			4	
	Input offset voltage drift	V_{CC} = ±5V or ±15V			5		μV/°C
Z_{OL}	Open loop transresistance	V_{CC} = ±5V, V_O = ±2.5V, R_L = 1kΩ			1.3		MΩ
		V_{CC} = ±15V, V_O = ±7.5V, R_L = 1kΩ			2.4		
I_{IB+}	Noninverting input bias current	V_{CC} = ±5V or ±15V	T_A = 25°C		2	10	μA
			T_A = full range			15	
$I_{IB–}$	Inverting input bias current	V_{CC} = ±5V or ±15V	T_A = 25°C		1	10	μA
			T_A = full range			15	
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5V		±3	±3.2		V
		V_{CC} = ±15V		±12.9	±13.2		
CMRR	Common-mode rejection ratio	V_{CC} = ±5V, V_{CM} = ±2.5V		62	70		dB
		V_{CC} = ±15V, V_{CM} = ±10V		65	73		
R_{I+}	Noninverting input resistance				1.5		MΩ
$R_{I–}$	Inverting input resistance				15		Ω
C_I	Differential input capacitance				7.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±5V	R_L = 150Ω	±2.9	±3.2		V
			R_L = 1kΩ	±3	±3.3		
		V_{CC} = ±15V	R_L = 150Ω	±12.1	±12.8		
			R_L = 1kΩ	±12.8	±13.1		
I_O	Output current(2)	V_{CC} = ±5V, R_L = 20Ω			100		mA
		V_{CC} = ±15V, R_L = 75Ω		85	120		
R_O	Output resistance	Open loop at 5MHz			10		Ω
POWER SUPPLY							
I_{CC}	Quiescent current	V_{CC} = ±5V	T_A = 25°C		5.5	7.5	mA
			T_A = full range			8.5	
		V_{CC} = ±15V	T_A = 25°C		6.6	9	
			T_A = full range			10	
		V_{CC} = ±18V	T_A = 25°C		6.9	9.5	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5V	T_A = 25°C	65	76		dB
			T_A = full range	63			
		V_{CC} = ±15V	T_A = 25°C	69	76		
			T_A = full range	67			

(1) Full range = 0°C to 70°C for the THS3001C and -40°C to 85°C for the THS3001I.
(2) Observe power dissipation ratings to keep the junction temperature below absolute maximum when the output is heavily loaded or shorted. See セクション 7.4.1.2.

5.6 Typical Characteristics

表 5-1. Table of Graphs

			FIGURE
$\lvert V_O \rvert$	Output voltage swing	vs Free-air temperature	図 5-1
I_{CC}	Current supply	vs Free-air temperature	図 5-2
I_{IB}	Input bias current	vs Free-air temperature	図 5-3
V_{IO}	Input offset voltage	vs Free-air temperature	図 5-4
CMRR	Common-mode rejection ratio	vs Common-mode input voltage	図 5-5
		vs Common-mode input voltage	図 5-6
		vs Frequency	図 5-7
	Transresistance	vs Free-air temperature	図 5-8
	Closed-loop output impedance	vs Frequency	図 5-9
V_n	Voltage noise	vs Frequency	図 5-10
I_n	Current noise	vs Frequency	
PSRR	Power supply rejection ratio	vs Frequency	図 5-11
		vs Free-air temperature	図 5-12
SR	Slew rate	vs Output step peak-to-peak	図 5-13, 図 5-14
	Normalized slew rate	vs Gain	図 5-15
	Harmonic distortion	vs Peak-to-peak output voltage swing	図 5-16, 図 5-17
		vs Frequency	図 5-18, 図 5-19
	Output amplitude	vs Frequency	図 5-20 to 図 5-24
	Normalized output response	vs Frequency	図 5-25 to 図 5-28
	Small- and large-signal frequency response		図 5-29, 図 5-30
	Small-signal pulse response		図 5-31, 図 5-32
	Large-signal pulse response		図 5-33 to 図 5-40

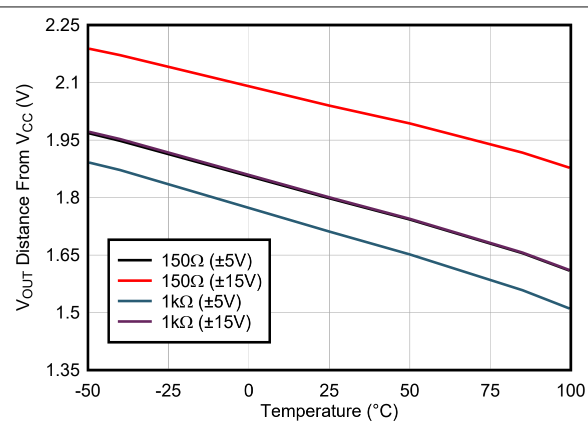


図 5-1. Output Voltage Swing vs Free-Air Temperature

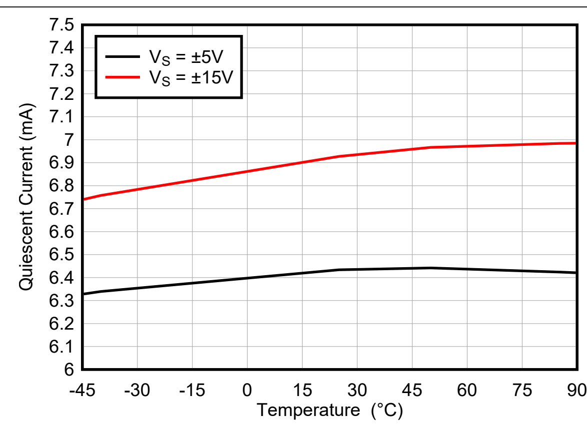


図 5-2. Current Supply vs Free-Air Temperature

5.6 Typical Characteristics (continued)

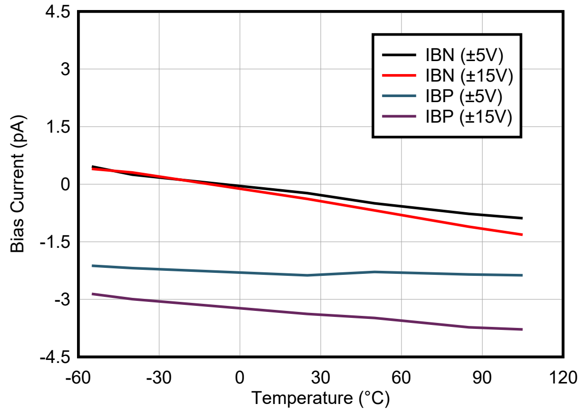


図 5-3. Input Bias Current vs Free-Air Temperature

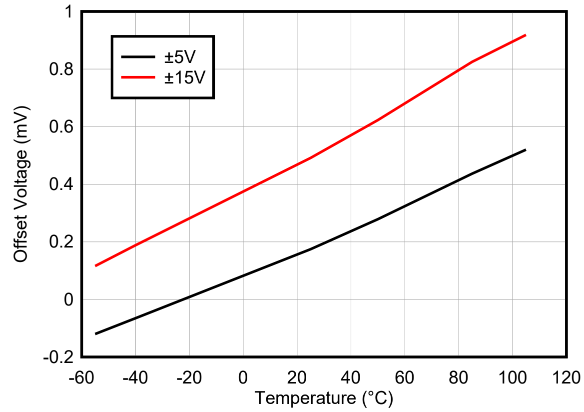
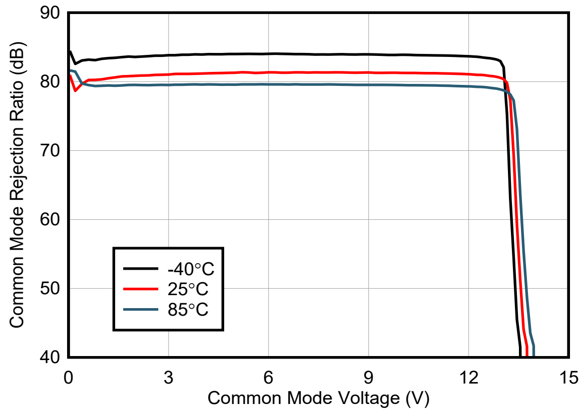
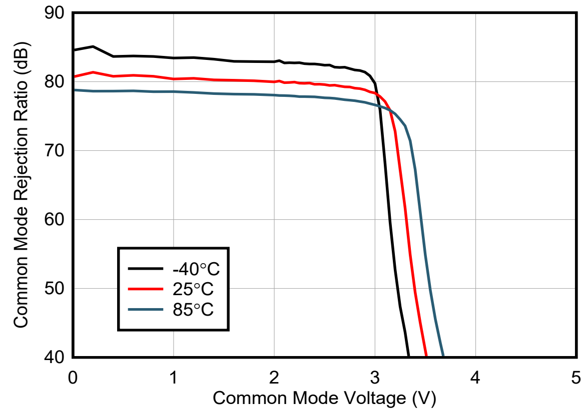


図 5-4. Input Offset Voltage vs Free-Air Temperature



V_S = ±15V

図 5-5. Common-Mode Rejection Ratio vs Common-Mode Input Voltage



V_S = ±5V

図 5-6. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

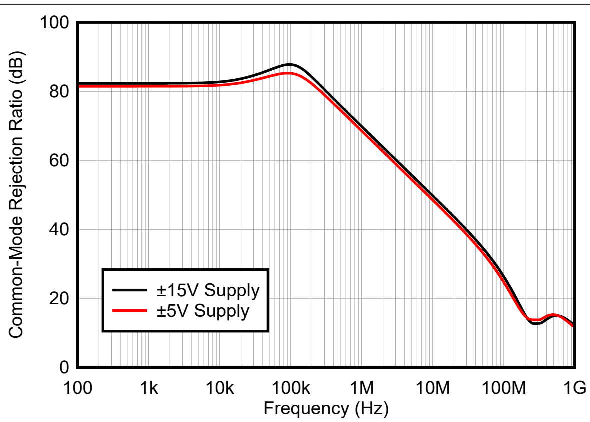


図 5-7. Common-Mode Rejection Ratio vs Frequency

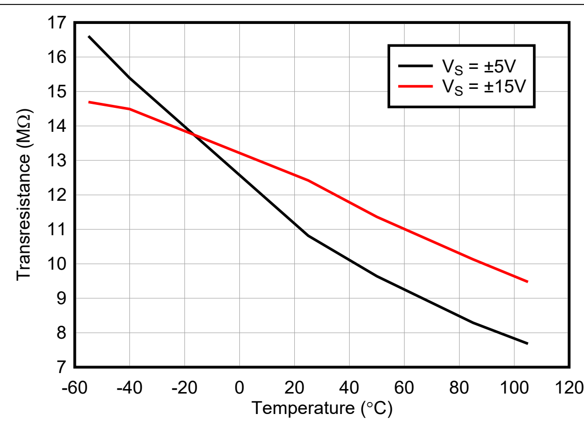
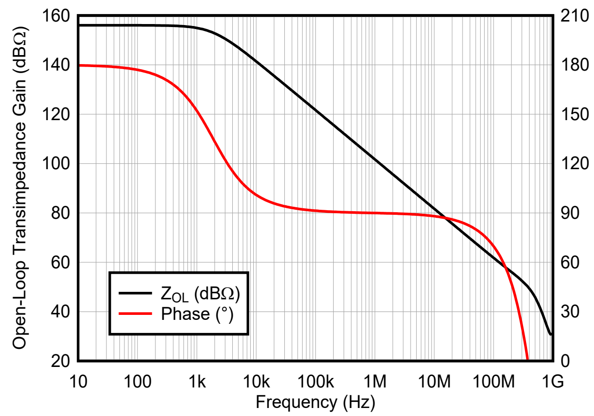


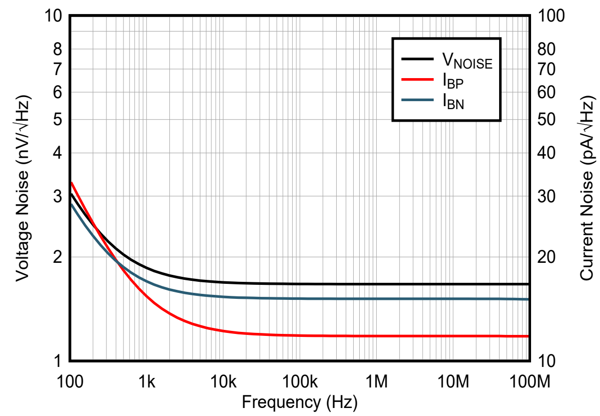
図 5-8. Transresistance vs Free-Air Temperature

5.6 Typical Characteristics (continued)



V_{CC} = ±15V, R_{FB} = 680Ω, gain = +2, V_{IN}= $2V_{PP}$

図 5-9. Closed-Loop Output Impedance vs Frequency



V_S = ±15V

図 5-10. Voltage Noise and Current Noise vs Frequency

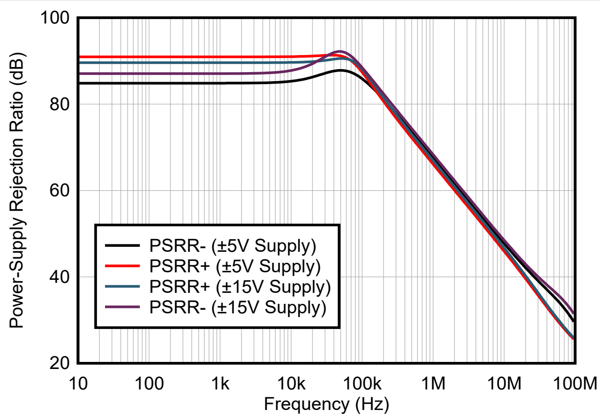


図 5-11. Power Supply Rejection Ratio vs Frequency

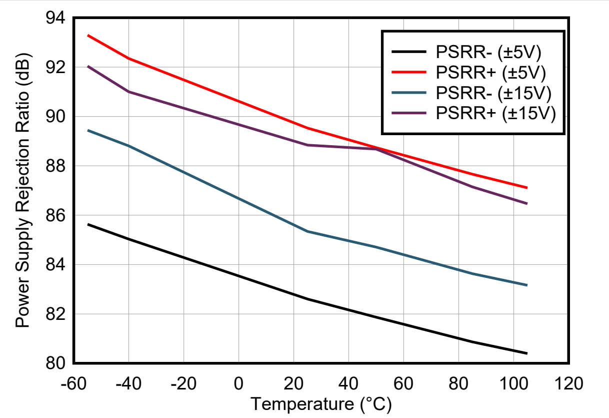
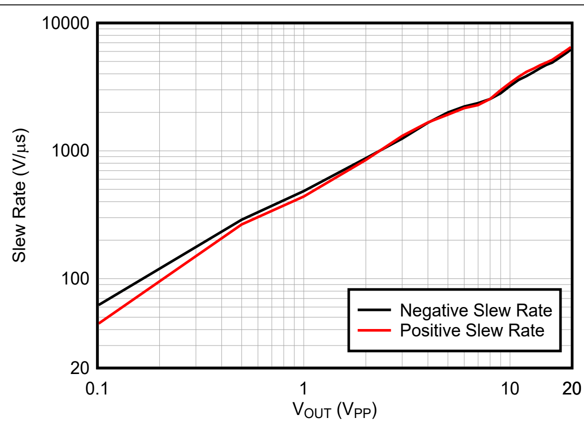
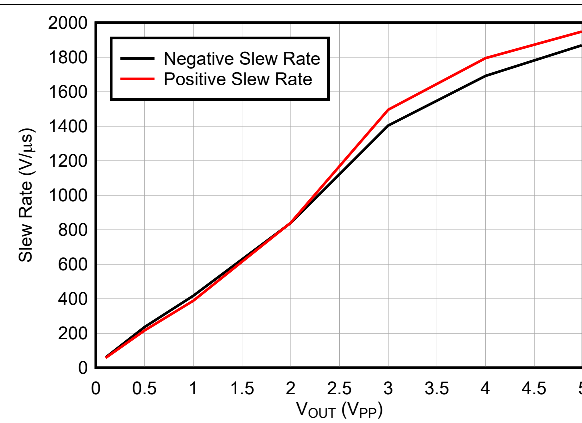


図 5-12. Power Supply Rejection Ratio vs Free-Air Temperature



V_S = ±15V, gain = +5, R_L = 150Ω, R_{FB} = 1kΩ,
$t_{RISE/FALL}$ = 300ps, V_{OUT} = $4V_{PP}$

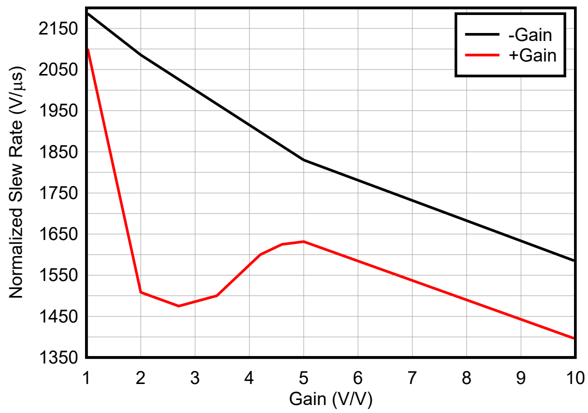
図 5-13. Slew Rate vs Output Step



V_S = ±5V, gain = +5, R_L = 150Ω, R_{FB} = 1kΩ,
$t_{RISE/FALL}$ = 300ps

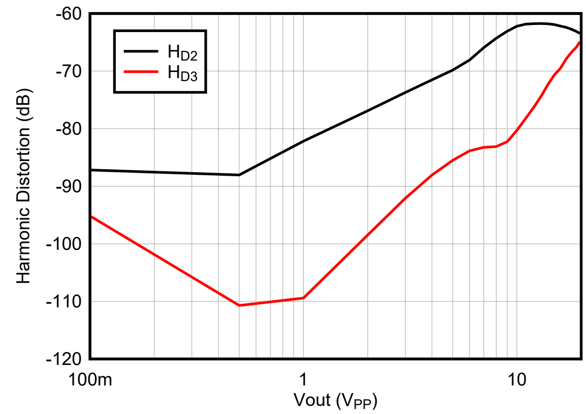
図 5-14. Slew Rate vs Output Step

5.6 Typical Characteristics (continued)



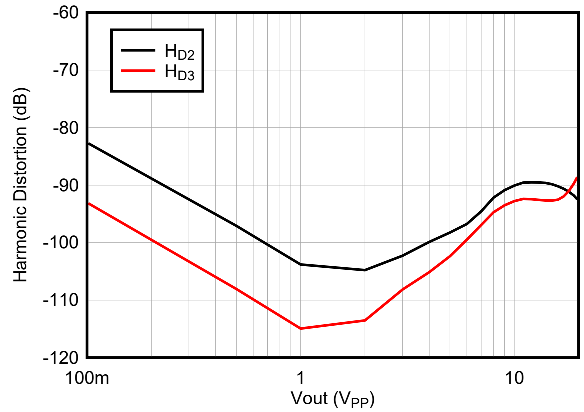
V_S = ±5V, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps, V_{OUT} = 4V_{PP}

図 5-15. Normalized Slew Rate vs Gain



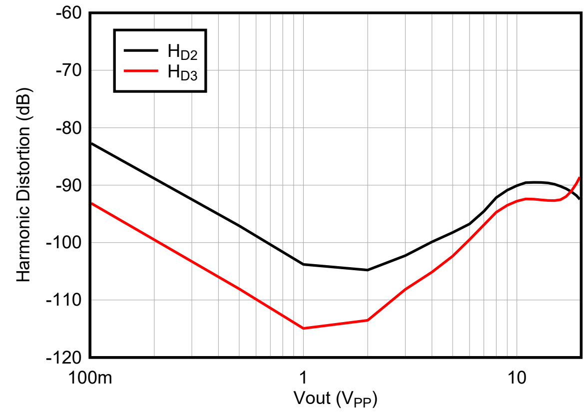
V_S = ±15V, gain = +2, R_L = 150Ω, R_{FB} = 680Ω, f_{IN} = 8MHz

図 5-16. Harmonic Distortion vs Peak-to-Peak Output Voltage Swing



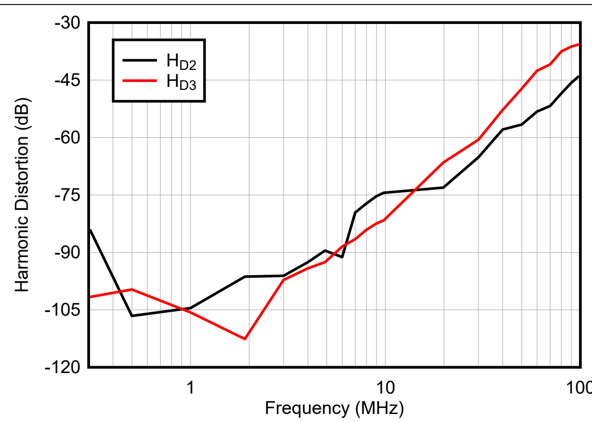
V_S = ±15V, gain = +2, R_L = 150Ω, R_{FB} = 680Ω, f_{IN} = 1MHz

図 5-17. Harmonic Distortion vs Peak-to-Peak Output Voltage Swing



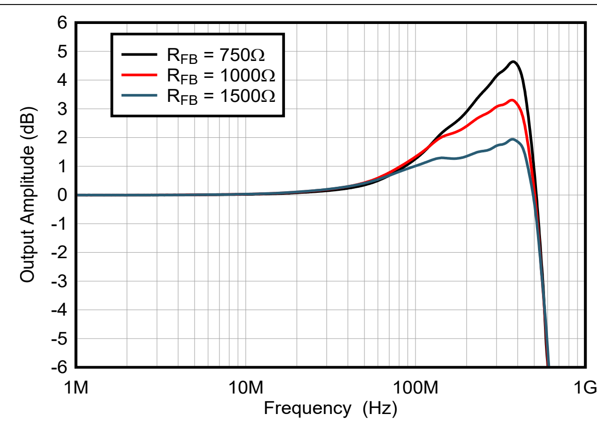
V_S = ±15V, gain = +2, R_L = 150Ω, R_{FB} = 680Ω, V_{OUT} = 2V_{PP}

図 5-18. Harmonic Distortion vs Frequency



V_S = ±5V, gain = +2, R_L = 150Ω, R_{FB} = 680Ω, V_{OUT} = 2V_{PP}

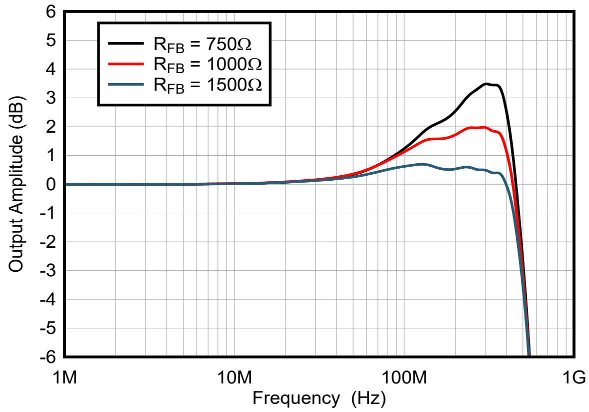
図 5-19. Harmonic Distortion vs Frequency



V_S = ±15V, gain = +1, R_L = 150Ω, V_{IN} = 200mV_{RMS}

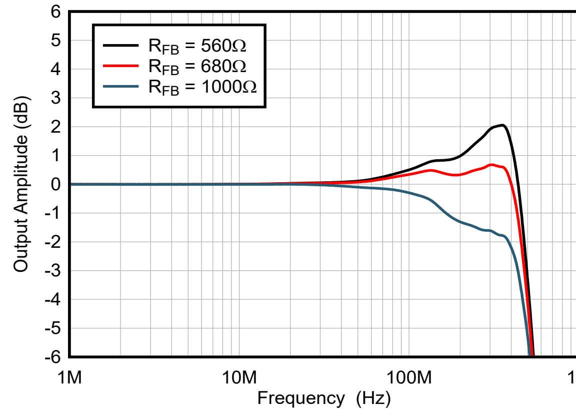
図 5-20. Output Amplitude vs Frequency

5.6 Typical Characteristics (continued)



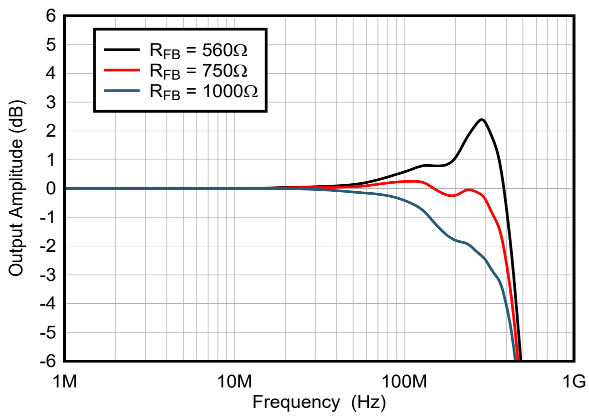
V_S = ±5V, gain = +1, R_L = 150Ω, V_{IN} = 200mV_{RMS}

図 5-21. Output Amplitude vs Frequency



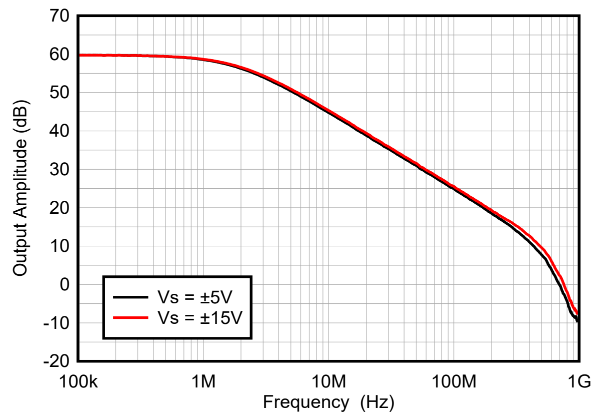
V_S = ±15V, gain = +2, R_L = 150Ω, V_{IN} = 200mV_{RMS}

図 5-22. Output Amplitude vs Frequency



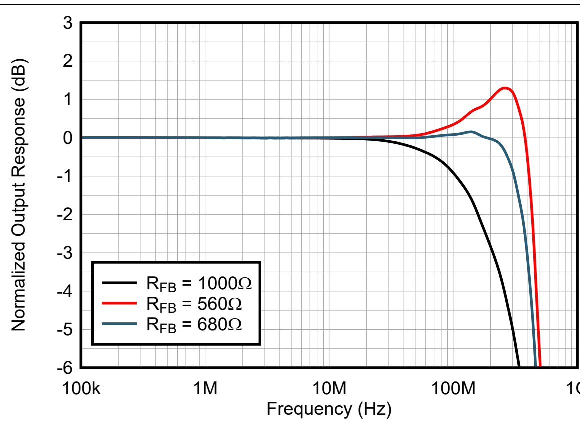
V_S = ±5V, gain = +2, R_L = 150Ω, V_{IN} = 200mV_{RMS}

図 5-23. Output Amplitude vs Frequency



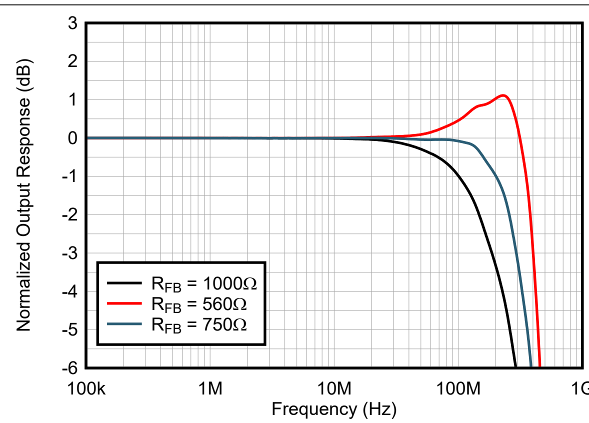
Gain = +1000, R_L = 150Ω, R_{FB} = 10kΩ, V_{OUT} = 200mV_{RMS}

図 5-24. Output Amplitude vs Frequency



V_S = ±15V, gain = –1, R_L = 150Ω, V_{IN} = 200mV_{RMS}

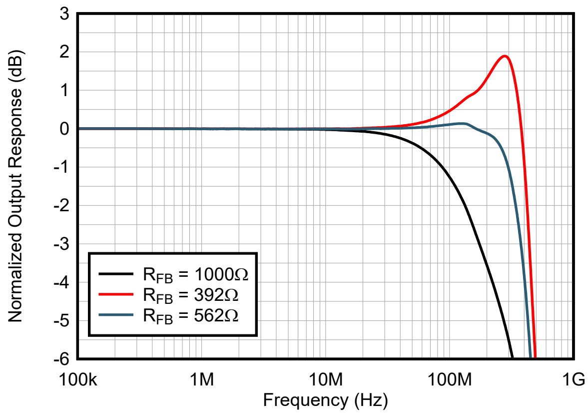
図 5-25. Normalized Output Response vs Frequency



V_S = ±5V, gain = –1, R_L = 150Ω, V_{IN} = 200mV_{RMS}

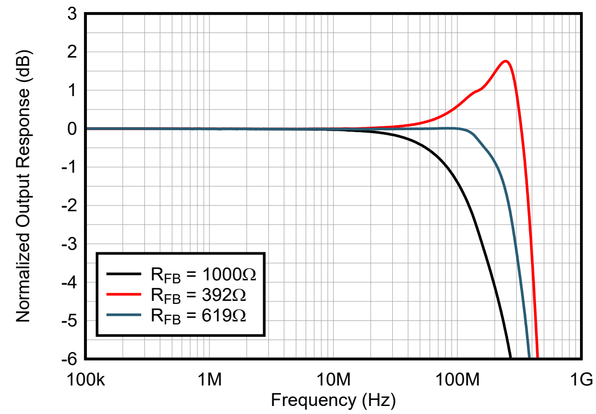
図 5-26. Normalized Output Response vs Frequency

5.6 Typical Characteristics (continued)



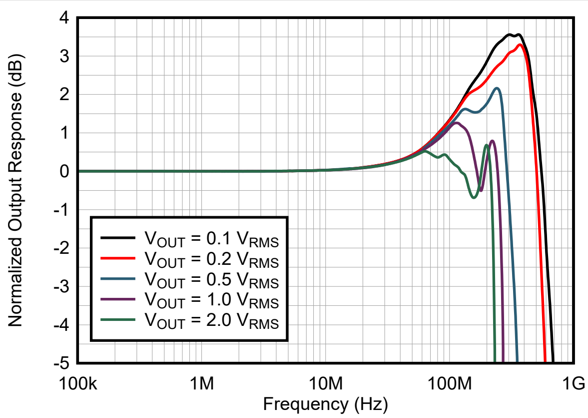
V_S = ±15V, gain = +5, R_L = 150Ω, V_{IN} = 200mV_{RMS}

図 5-27. Normalized Output Response vs Frequency



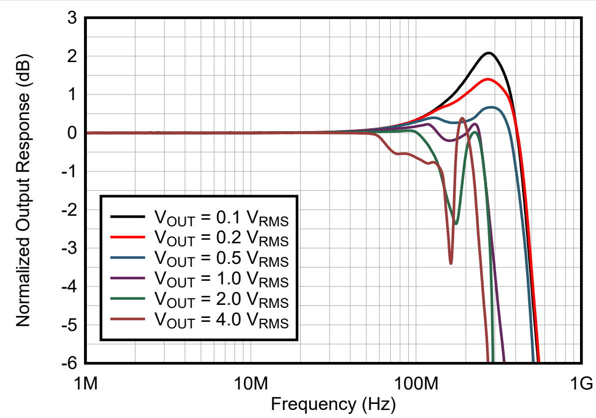
V_S = ±5V, gain = +5, R_L = 150Ω, V_{IN} = 200mV_{RMS}

図 5-28. Normalized Output Response vs Frequency



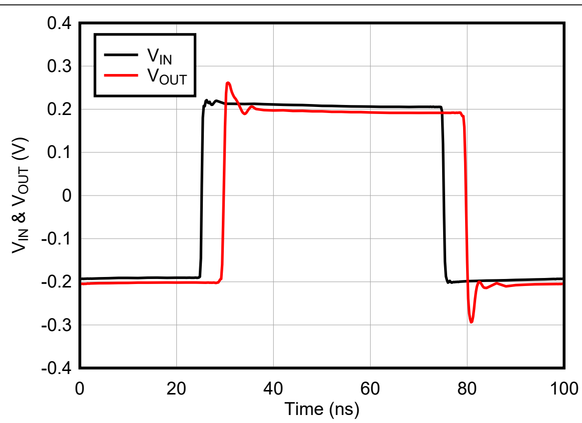
V_S = ±15V, gain = +1, R_L = 150Ω, R_{FB} = 1kΩ

図 5-29. Small- and Large-Signal Frequency Response



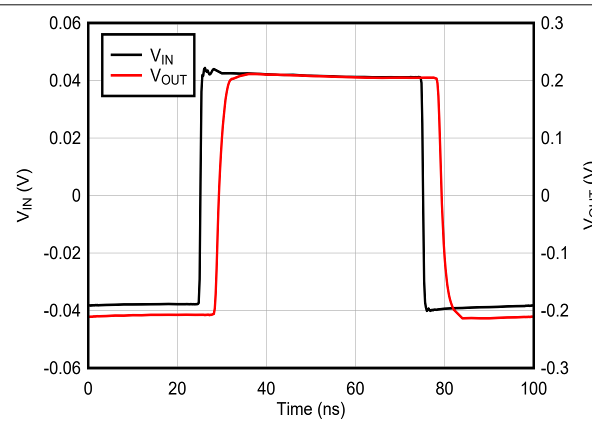
V_S = ±15V, gain = +2, R_L = 150Ω, R_{FB} = 680Ω

図 5-30. Small- and Large-Signal Frequency Response



V_S = ±5V, gain = +1, R_L = 150Ω, R_{FB} = 1kΩ,
$t_{RISE/FALL}$ = 300ps

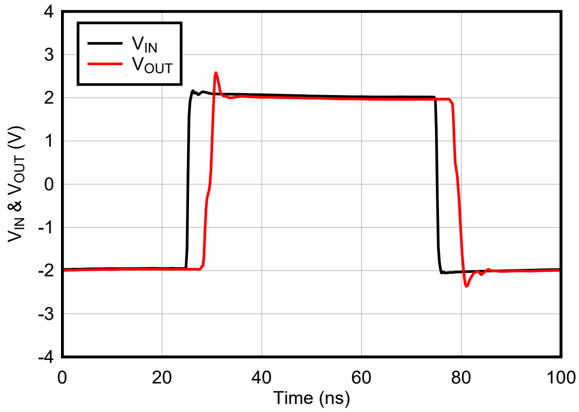
図 5-31. Small-Signal Pulse Response



V_S = ±5V, gain = +5, R_L = 150Ω, R_{FB} = 1kΩ,
$t_{RISE/FALL}$ = 300ps

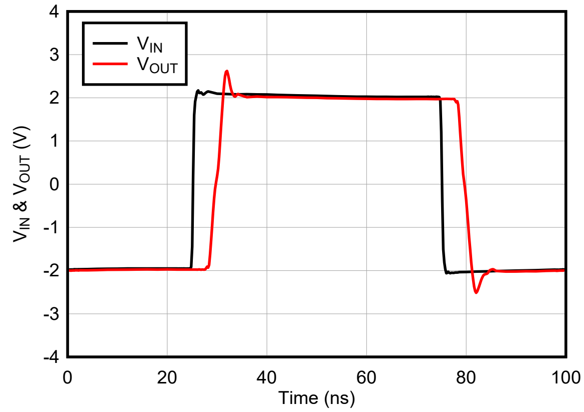
図 5-32. Small-Signal Pulse Response

5.6 Typical Characteristics (continued)



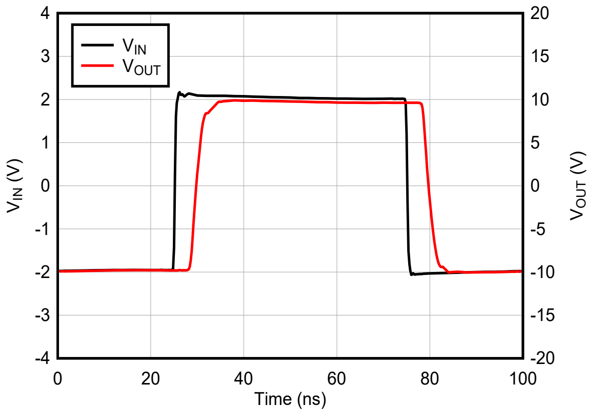
V_S = ±15V, gain = +1, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-33. Large-Signal Pulse Response



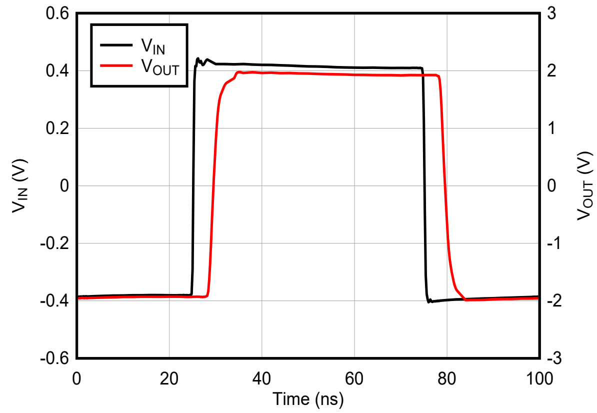
V_S = ±5V, gain = +1, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-34. Large-Signal Pulse Response



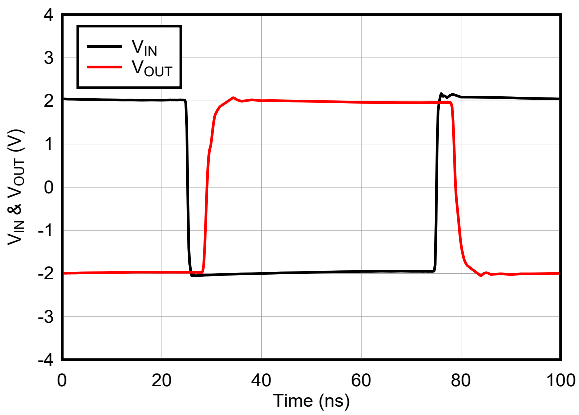
V_S = ±15V, gain = +5, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-35. Large-Signal Pulse Response



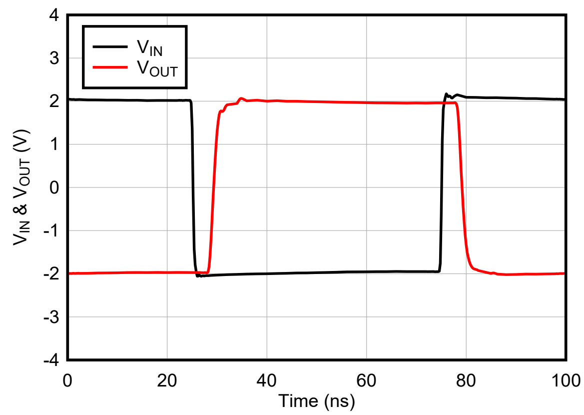
V_S = ±5V, gain = +5, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-36. Large-Signal Pulse Response



V_S = ±15V, gain = –1, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

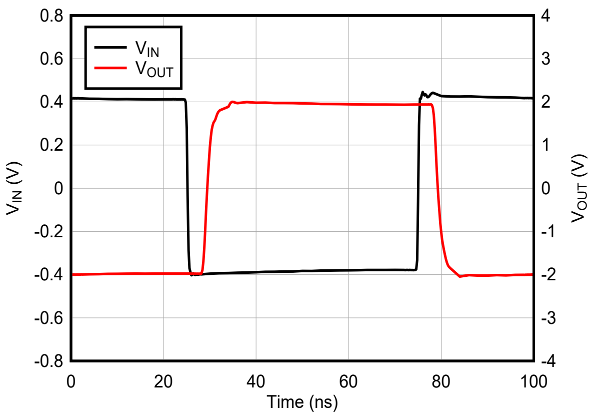
図 5-37. Large-Signal Pulse Response



V_S = ±5V, gain = –1, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

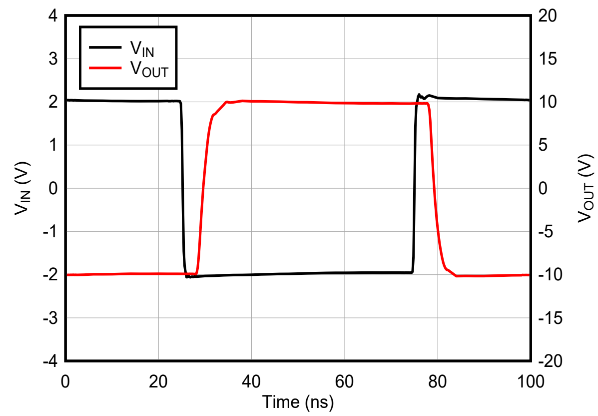
図 5-38. Large-Signal Pulse Response

5.6 Typical Characteristics (continued)



V_S = ±5V, gain = –5, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-39. Large-Signal Pulse Response



V_S = ±5V, gain = –5, R_L = 150Ω, R_{FB} = 1kΩ, $t_{RISE/FALL}$ = 300ps

図 5-40. Large-Signal Pulse Response

6 Detailed Description

6.1 Overview

The THS3001 is a high-speed operational amplifier configured in a current-feedback architecture. The device is built using a 30V, dielectrically isolated, complementary, bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. 図 6-1 shows a simplified schematic.

6.2 Functional Block Diagram

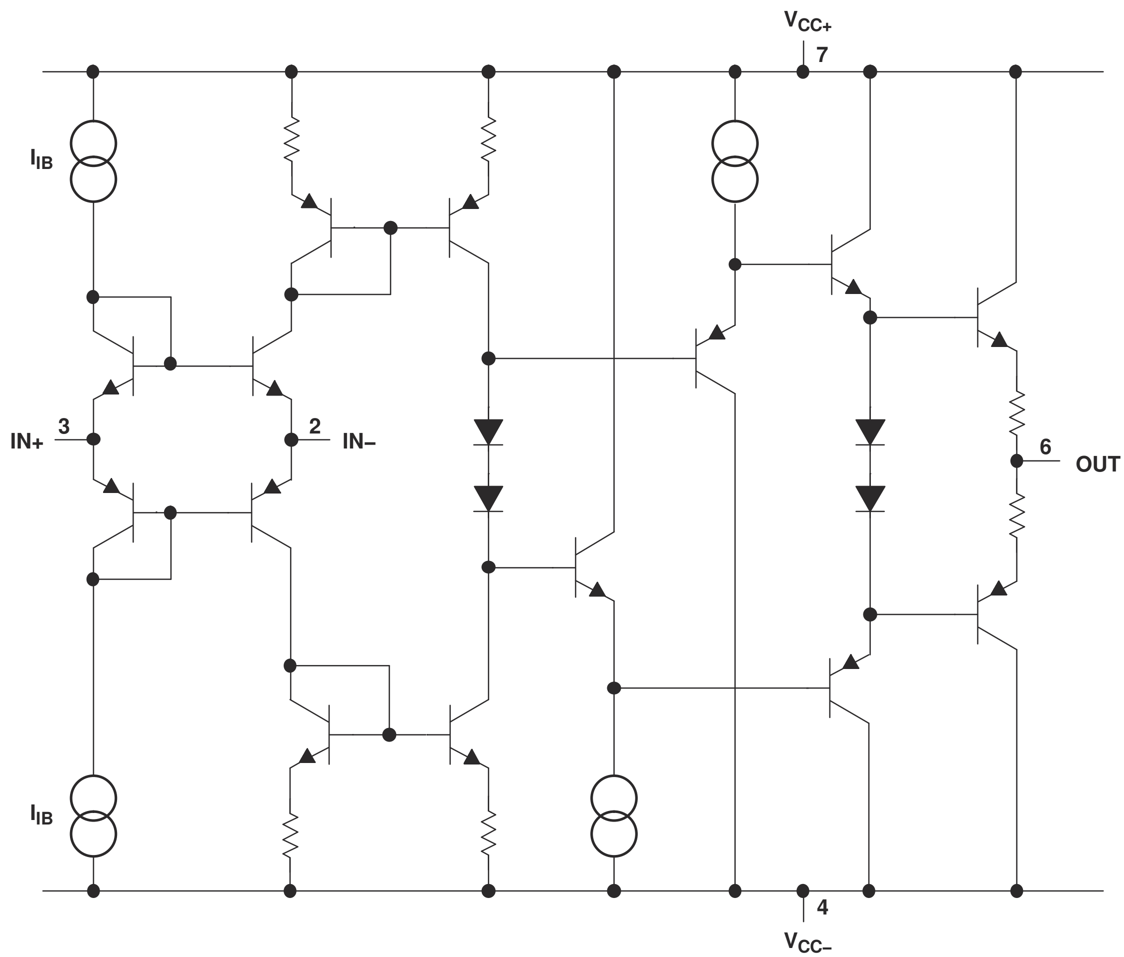


図 6-1. Simplified Schematic

6.3 Device Functional Modes

The THS3001 has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9V (±4.5V) and less than 32V (±16V).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Recommended Feedback and Gain Resistor Values

The THS3001 is fabricated using Texas Instruments 30V complementary bipolar process, HVBiCOM. This process provides the excellent isolation and extremely high slew rates that result in excellent distortion characteristics.

As with all current-feedback amplifiers, the bandwidth of the THS3001 is an inversely proportional function of the value of the feedback resistor (see Figures 26 to 34). 表 7-1 shows the recommended resistors for an optimized frequency response. Use these values as a starting point, and after optimized values are found, use a 1% tolerance resistors to maintain frequency response characteristics. For most applications, a feedback resistor value of 1kΩ is recommended, a good compromise between bandwidth and phase margin that yields a stable amplifier.

表 7-1. Recommended Resistor Values for an Optimized Frequency Response

GAIN	R_F FOR V_{CC} = ±15V	R_F FOR V_{CC} = ±5V
1	1kΩ	1kΩ
2, –1	680Ω	750Ω
2	620Ω	620Ω
5	560Ω	620Ω

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. The reason is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independent of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage-feedback amplifiers. Therefore, after a frequency response is found that is designed for a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, make sure to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. Knowing that decreasing load impedance increases total harmonic distortion (THD) is also important Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion.

7.1.2 Noise Calculations

Noise can cause errors on small signals. This problem is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback (CFB) amplifiers is the same as for voltage-feedback (VFB) amplifiers. The only difference between CFB and VFB amplifiers is that CFB amplifiers generally specify different current-noise parameters for each input, whereas VFB amplifiers usually only specify one noise-current parameter. 図 7-1 shows the noise model. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/√Hz)
- IN+ = Noninverting current noise (pA/√Hz)
- IN– = Inverting current noise (pA/√Hz)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR$_x$)

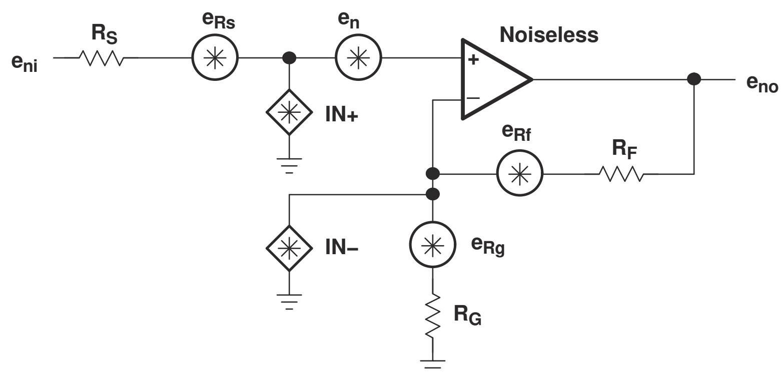


図 7-1. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)} \tag{1}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)} \tag{2}$$

The previous equations show that to keep noise at a minimum, use small-value resistors. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This result leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Noise is summed in a root-mean-squares method; therefore, noise sources smaller than 25% of the largest noise source can be effectively ignored. This threshold can greatly simplify the formula and make noise calculations much easier.

7.1.3 Slew Rate

The slew rate performance of a current-feedback amplifier, like the THS3001, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors can help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS3001 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. As can be seen from the specification tables as well as some of the figures in this data sheet, slew-rate performance in the inverting configuration is faster than in the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. Also, if the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes.

Internally, the THS3001 has other factors that impact the slew rate. The amplifiers behavior during the slew-rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1500V/µs are processed by the input stage in a linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in 図 7-2. For slew rates greater than 1500V/µs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew-rate capabilities. 図 7-2 and 図 7-3 show waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster-slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input-signal slew rate reduces the effect.

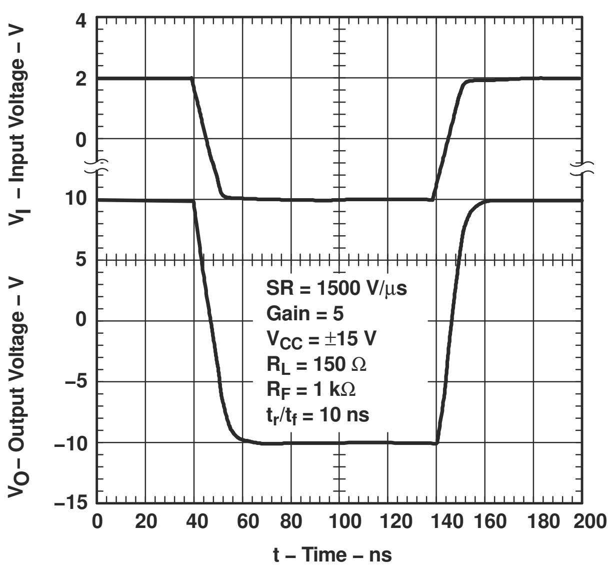


図 7-2. Slew Rate

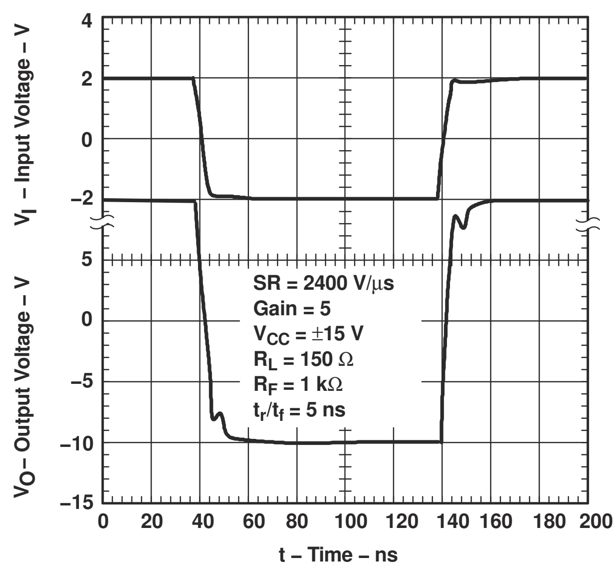
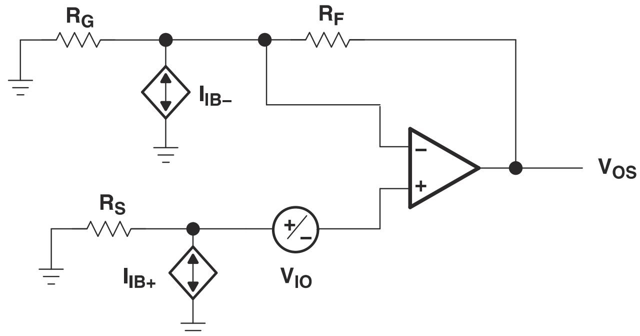


図 7-3. Slew Rate

7.1.4 Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



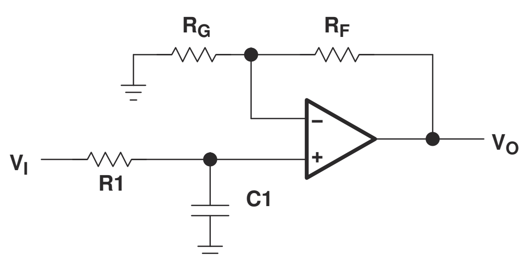
$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

図 7-4. Output Offset Voltage Model

7.2 Typical Applications

7.2.1 General Configurations

A common error for the first-time CFB user is the creation of a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration can oscillate and is *not* recommended. The THS3001, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a low impedance. This results in an unstable amplifier when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see 図 7-5).



$$f_{-3\ dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

図 7-5. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. A CFB amplifier high slew rate and bandwidth can create accurate signals and help minimize distortion. An example is shown in 図 7-6.

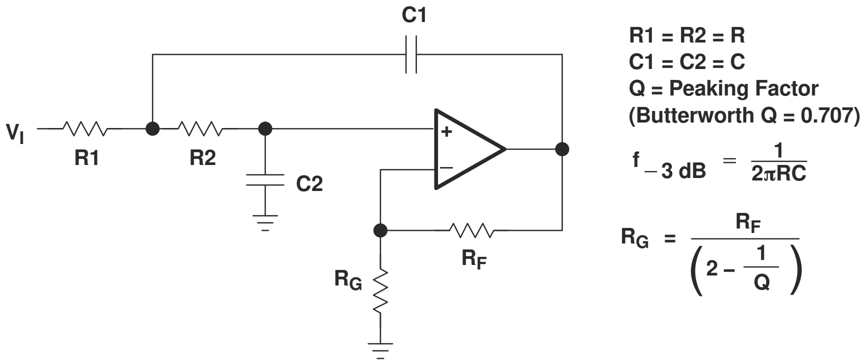


図 7-6. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in 図 7-7, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in 図 7-8, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.

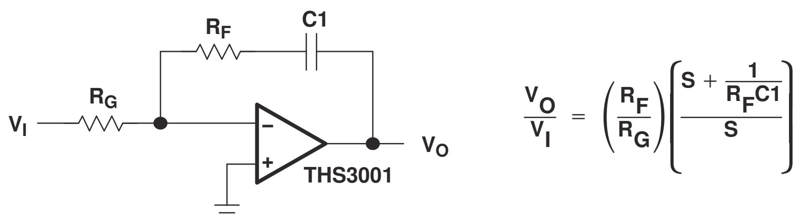


図 7-7. Inverting CFB Integrator

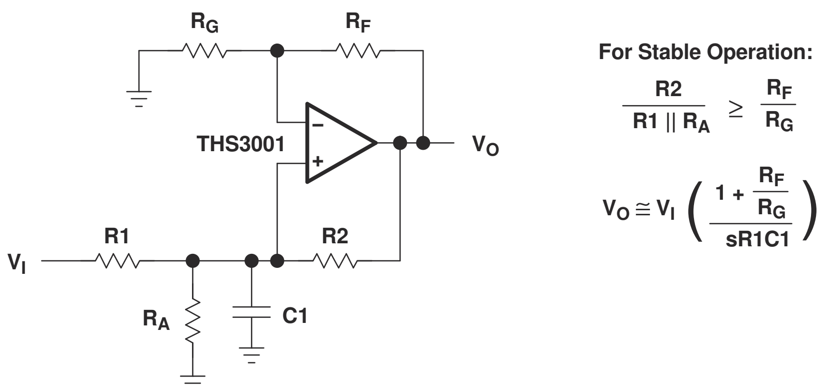


図 7-8. Noninverting CFB Integrator

The THS3001 can also be employed as a good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases (see Figures 22 to 25 for more information). Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

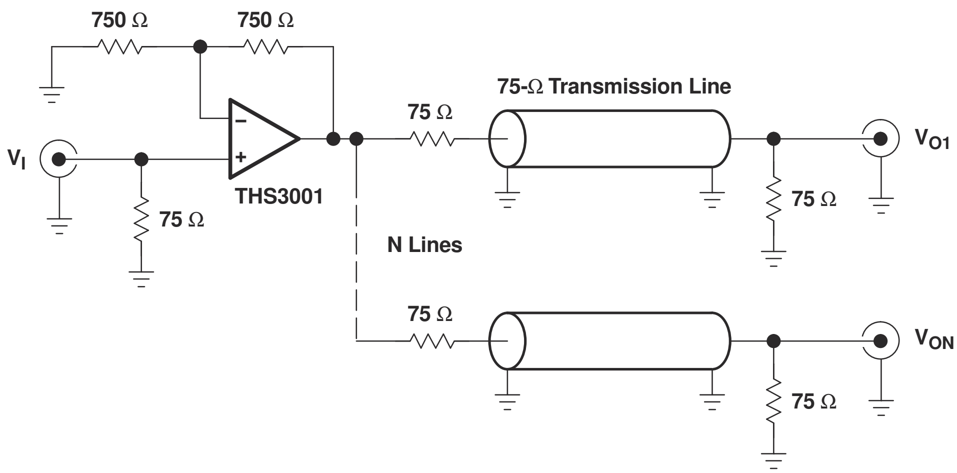


図 7-9. Video Distribution Amplifier Application

7.2.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS3001 has been internally compensated to maximize the bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10pF, a resistor needs to be placed in series with the output of the amplifier, as shown in 図 7-10. A minimum value of 20Ω can work adequately for most applications. For example, in 75Ω transmission systems, setting the series resistor value to 75Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

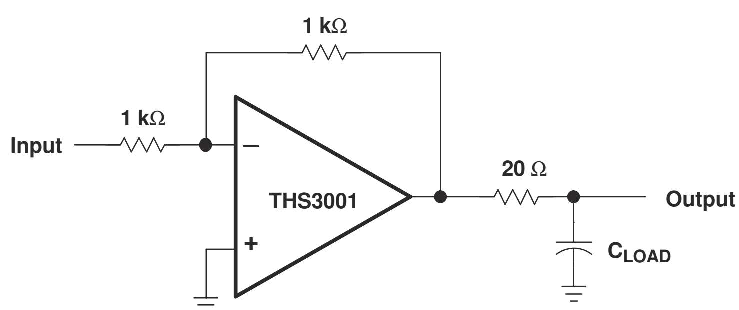


図 7-10. Driving a Capacitive Load

7.3 Power Supply Recommendations

The THS3001 family operates off a single supply or with dual supplies. Choose supplies that provide for the required headroom to supply rails as specified by the common-mode range (CMR). Operating from a single supply has numerous advantages. With the negative supply at ground, the dc errors due to the –PSRR term are minimized. Decouple supplies with low inductance capacitors to ground as close to the amplifier as possible. When operating on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. When using a ground plane, remove the ground plane close to input sensitive pins to reduce stray parasitics that adversely impact device performance. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 PCB Design Considerations

Proper PCB design techniques in two areas are important for best performance with the THS3001. These areas are high-speed layout techniques and thermal-management techniques. Because the THS3001 is a high-speed part, the following guidelines are recommended.

- Ground plane: The ground plane needs be used on the board to provide all components with a low inductive ground connection, but needs to be removed from below the output and negative input pins as noted below.
- The DGN package option includes a thermal pad for increased thermal performance. When using this package, the PCB designer needs to distribute the negative supply as a power plane, and tie the thermal pad to this supply with multiple vias for proper power dissipation. Do not tie the thermal pad to ground when using split supply (±V) as this can cause worse distortion performance than shown in this data sheet.
- Input stray capacitance: To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components need to be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in 図 7-11, which shows what happens when a 1pF capacitor is added to the inverting input terminal. The bandwidth increases at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, while the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in 図 7-12, where a 10pF capacitor adds only 0.35dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially look like a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So proper analysis of adding a capacitor to the inverting input node needs to be performed for stable operation.

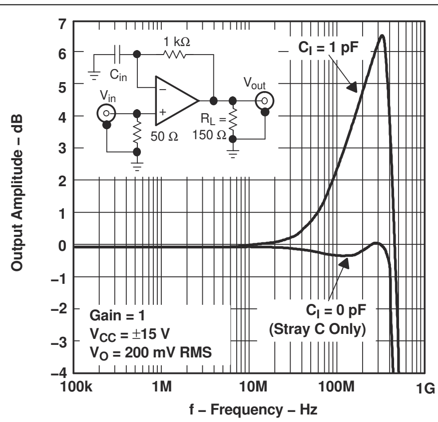


図 7-11. Output Amplitude vs Frequency

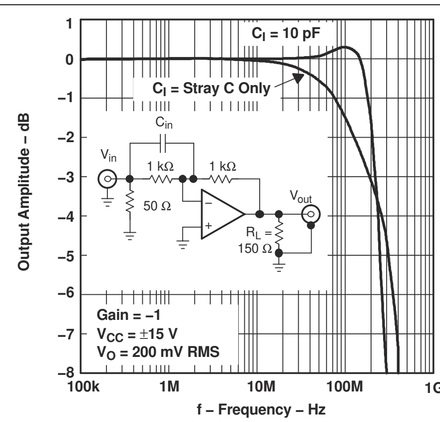


図 7-12. Output Amplitude vs Frequency

- Proper power-supply decoupling: Use a minimum 6.8μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor on each supply terminal. The tantalum capacitor can be shared among several amplifiers depending on the application, but use a 0.1μF ceramic capacitor on the supply terminal of every amplifier. In addition, place the 0.1μF capacitor as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. In addition, distances of less than 0.1 inch between the device power terminal and the ceramic capacitors are recommended.

7.4.1.2 Thermal Considerations

The THS3001 incorporates output-current-limiting protection. If the output is ever shorted to ground, the output current is automatically limited to the value given in the data sheet. While the output-current-limiting protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors.

> 注意
> Continuous output shorts are not recommended and can damage the device. Additionally, connection of the amplifier output to one of the supply rails (V_{CC} or V_{EE}) is not recommended and can result in device failure. In addition, the THS3001 does not incorporate thermal-shutdown protection. Because of this limitation, pay special attention to the device power dissipation, or failure can result.

The thermal coefficient θ_{JA} is approximately 169°C/W for the SOIC 8-pin D package. For a given θ_{JA}, the maximum power dissipation shown in 図 7-13 is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS3001 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = Thermal coefficient from die junction to ambient air (°C/W)

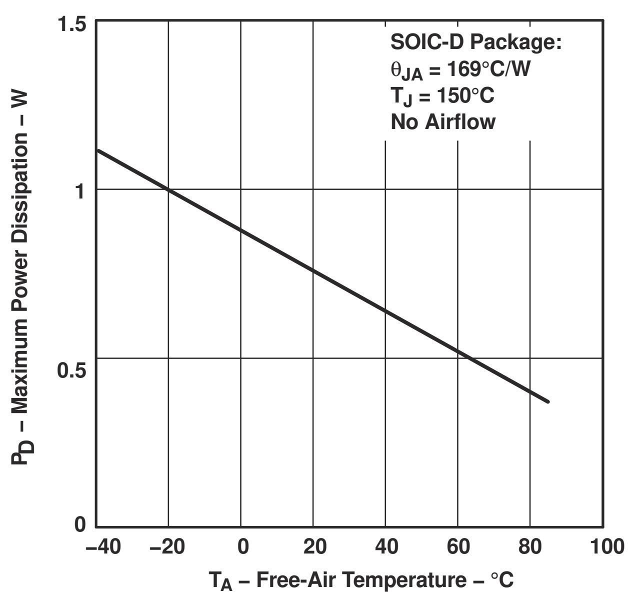


図 7-13. Maximum Power Dissipation vs Free-Air Temperature

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Evaluation Board

An evaluation board is available for the THS3001 (THS3001EVM). The board has been configured for low parasitic capacitance to optimize for the full performance of the amplifier. A schematic of the evaluation board is shown in 図 8-1. The circuitry has been designed so that the amplifier can be used in either an inverting or noninverting configuration. For more detailed information, see the *THS3001 EVM User's Guide*. Order the evaluation board online through the TI web site, or through your local TI sales office or distributor.

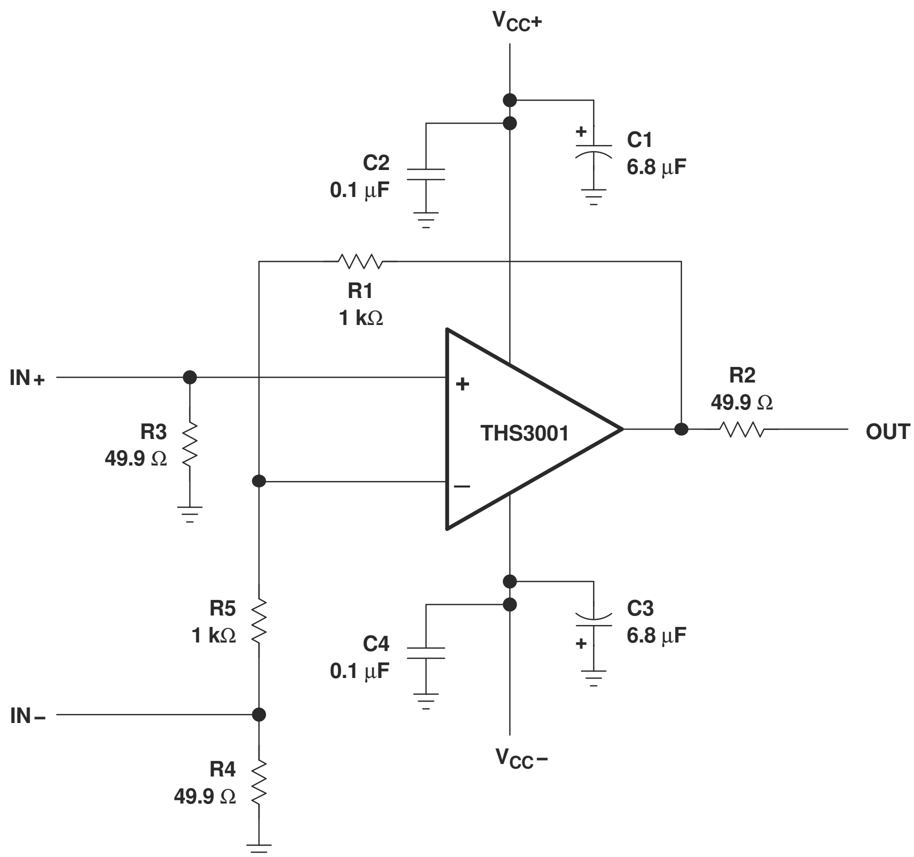


図 8-1. THS3001 Evaluation Board Schematic

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (September 2009) to Revision I (December 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 「ピン構成および機能」、「仕様」、「ESD 定格」、「推奨動作条件」、「熱に関する情報」、「詳細説明」、「概要」、「機能ブロック図」、「デバイスの機能モード」、「アプリケーションと実装」、「代表的なアプリケーション」、「電源に関する推奨事項」、「レイアウト」、「レイアウトのガイドライン」、「熱に関する考慮事項」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- Updated table note 1 on *Absolute Maximum Ratings* to add additional clarification 4
- Deleted THS3001HV from *Absolute Maximum Ratings* 4
- Deleted THS3001HV from *Recommended Operating Conditions* 4
- Updated *Recommended Operating Conditions* with nominal values 4
- Changed Vss to Vcc in *Recommended Operating Conditions* to maintain consistency with *Absolute Maximum Ratings* 4
- Moved *Operating Characteristics* to be included in *Electrical Characteristics* 5
- Changed bandwidth for 0.1dB flatness in *Electrical Characteristics* from 85MHz (5V) and 115MHz (15V) to 65MHz (5V) and 55MHz (15V) 5
- Deleted differential gain and phase from *Electrical Characteristics* 5
- Deleted power supply operating range from from *Electrical Characteristics* 5
- Deleted *Slew Rate vs Supply Voltage* from *Typical Characteristics* 7
- Deleted *Differential Gain and Phase Loading* from *Typical Characteristics* 7

Changes from Revision G (March 2008) to Revision H (September 2009) **Page**

- 現行基準に合わせ文書形式を更新 1
- Updated information about THS3001EVM availability 24

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3001CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3001C
THS3001CDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	ADP
THS3001CDGNR	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	ADP
THS3001CDR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3001C
THS3001HVCDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	BNK
THS3001HVIDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	BNJ
THS3001ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-	3001I
THS3001IDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-	ADQ
THS3001IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-	ADQ
THS3001IDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADQ
THS3001IDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADQ
THS3001IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-	3001I
THS3001IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3001I
THS3001IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3001I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

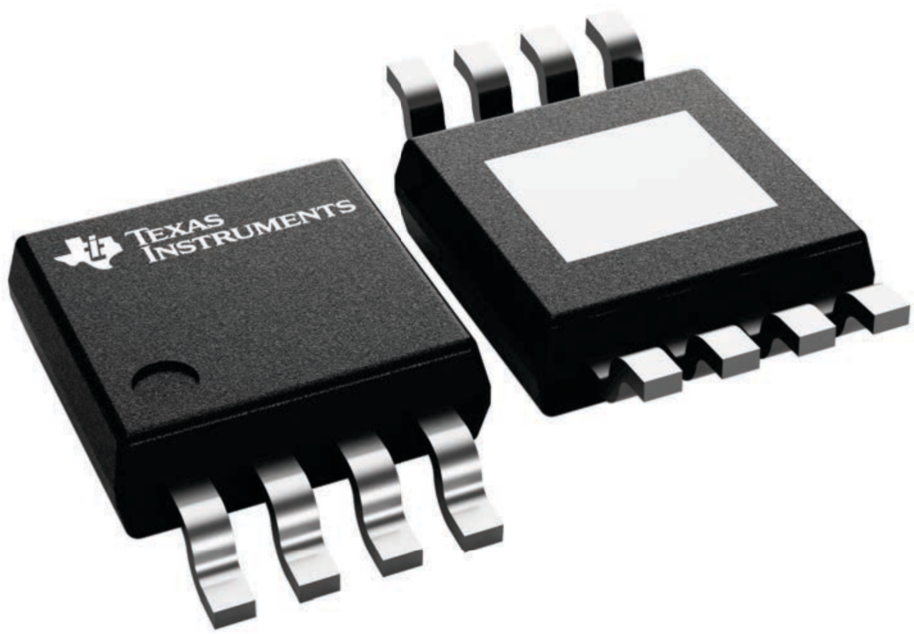
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

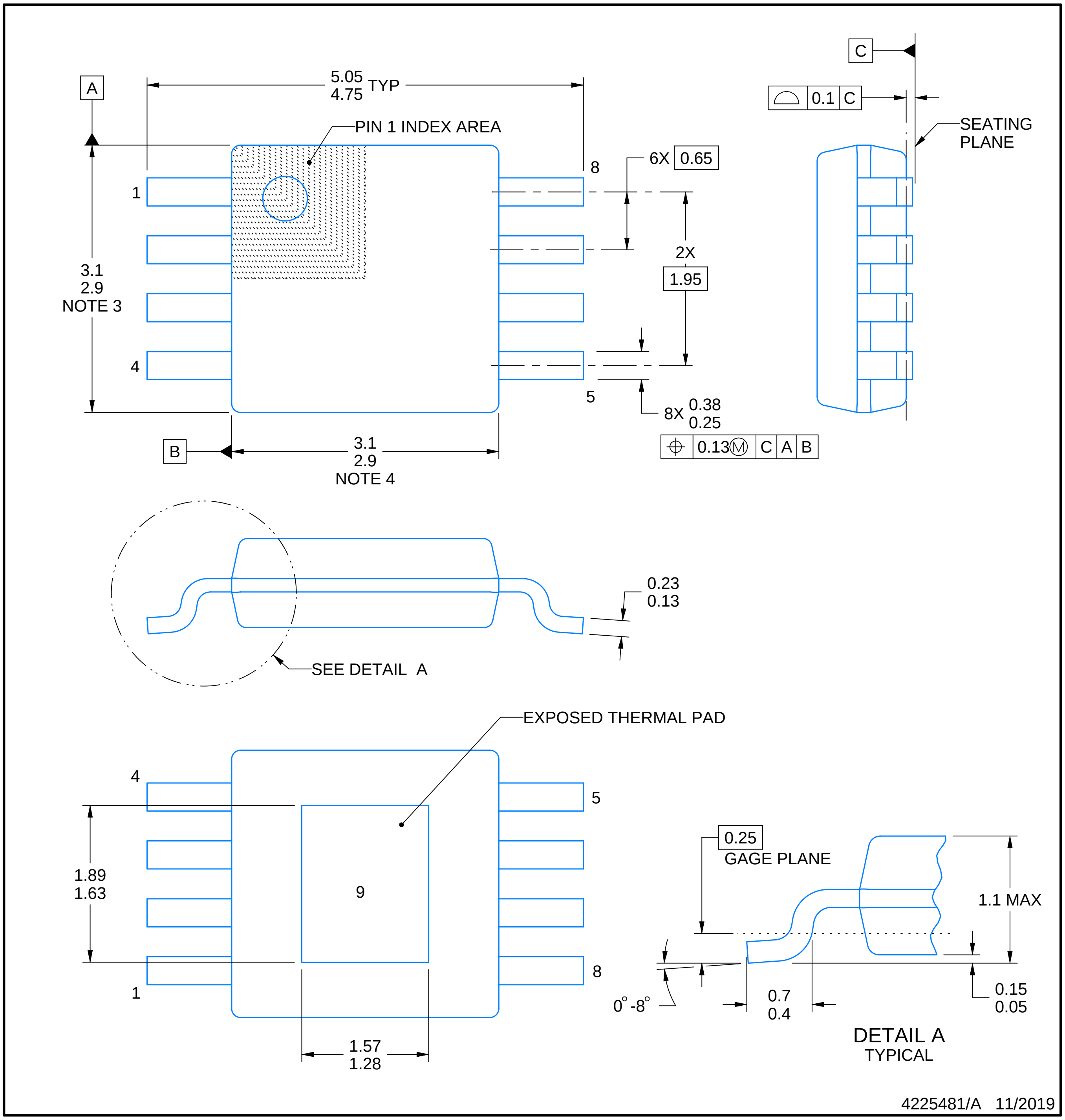
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



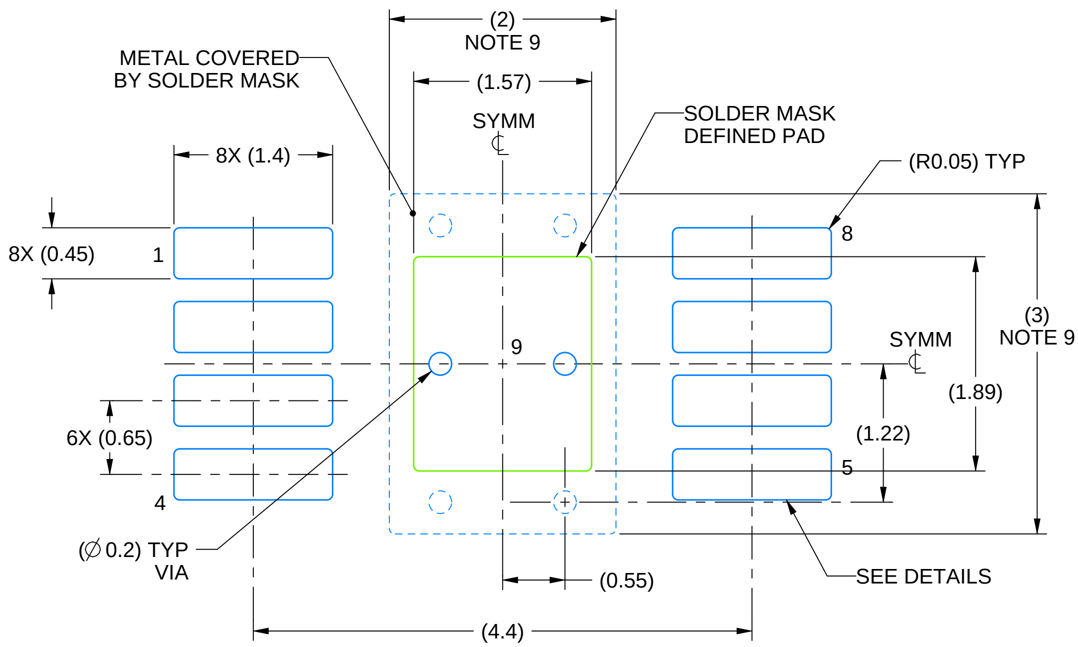
4225482/B



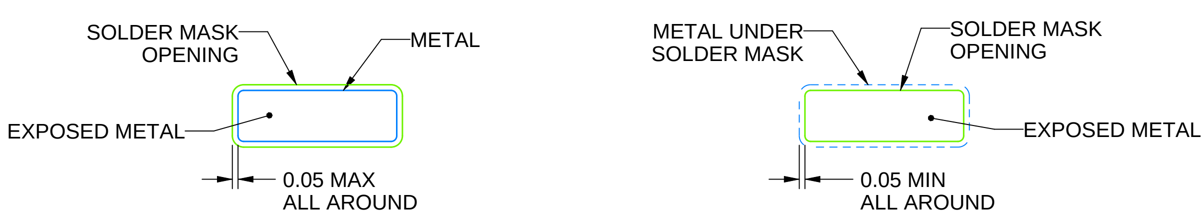
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

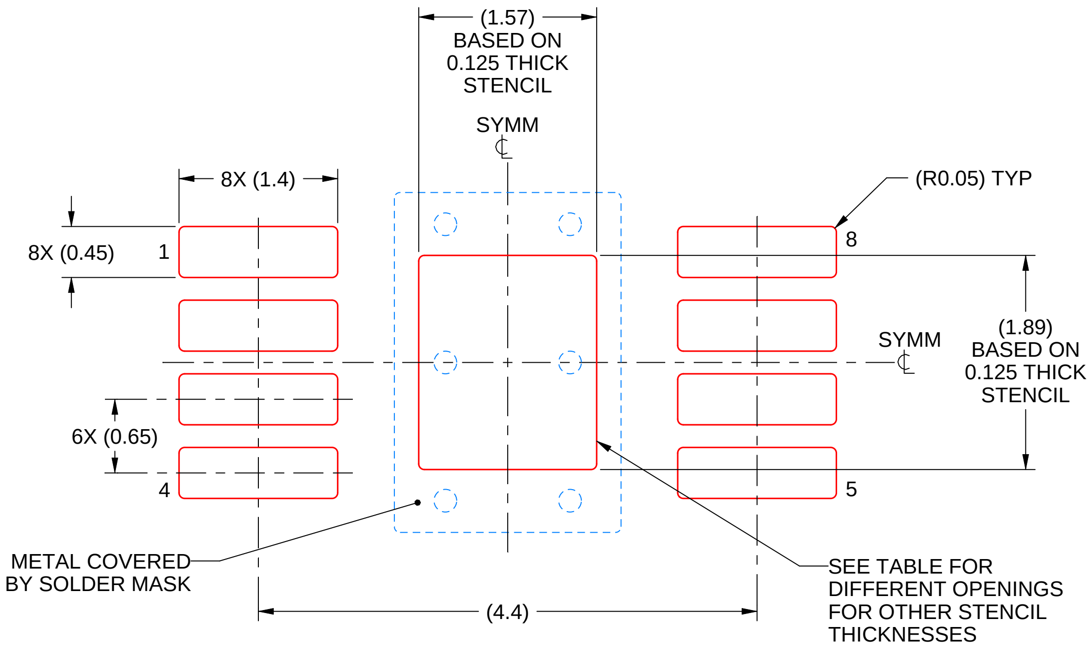
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



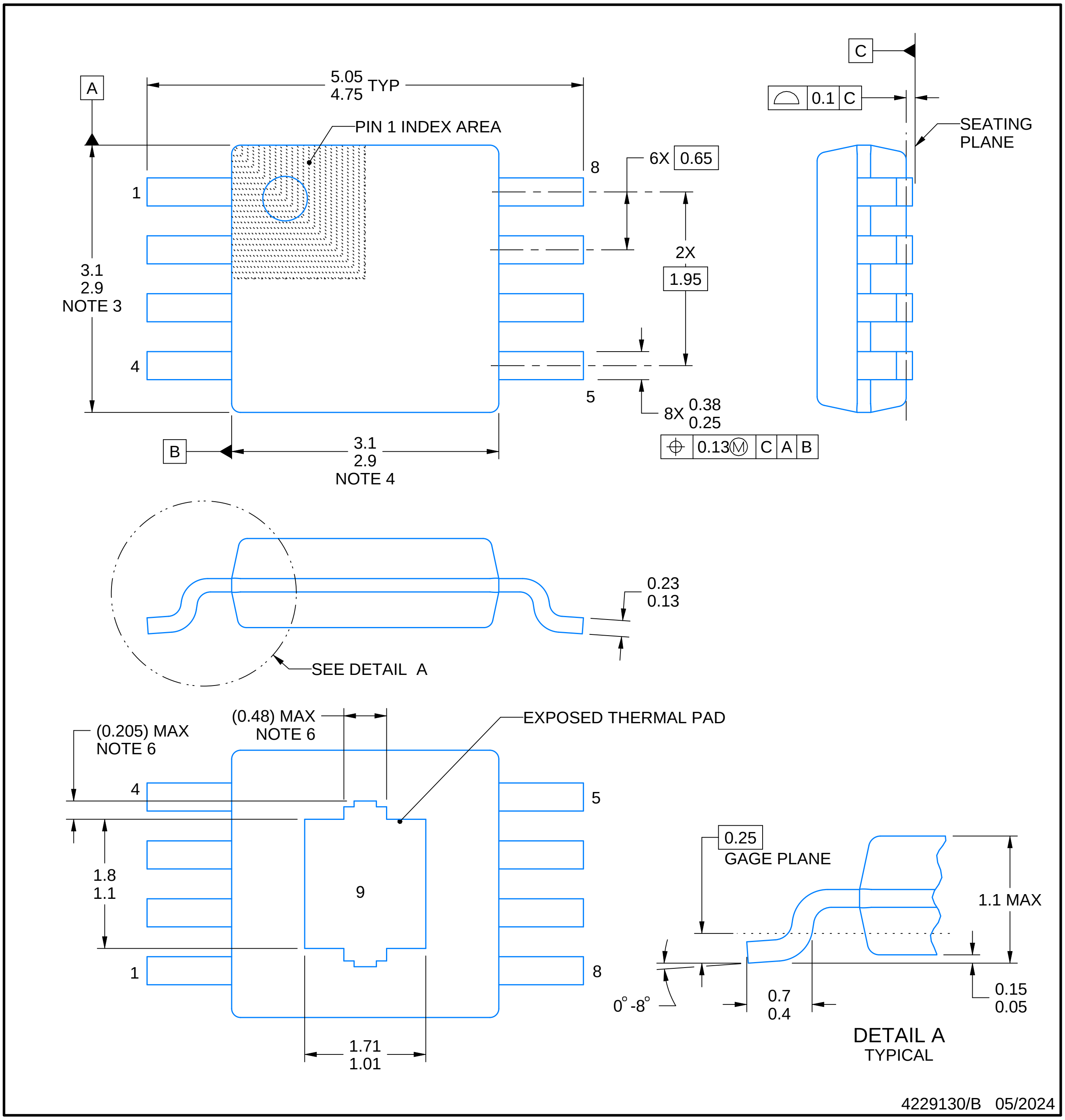
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

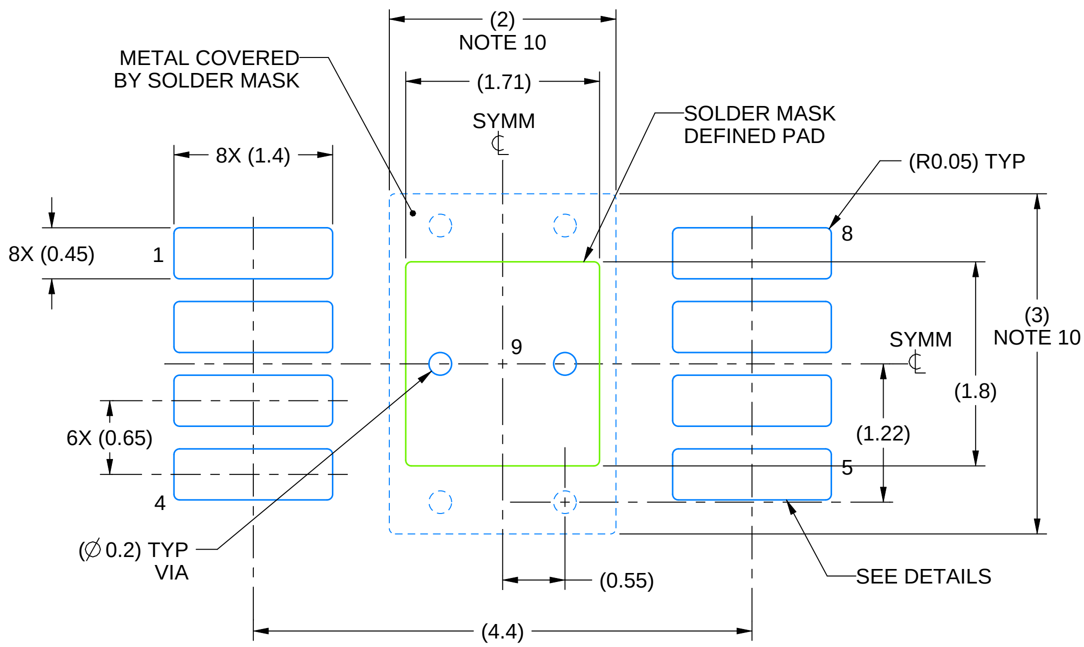
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



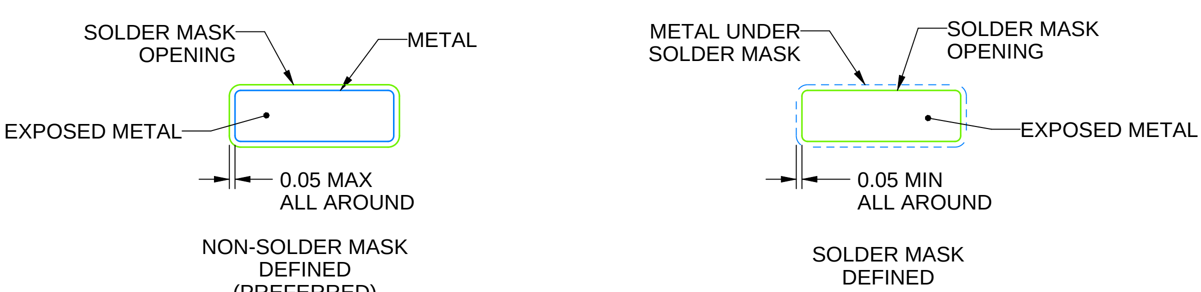
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

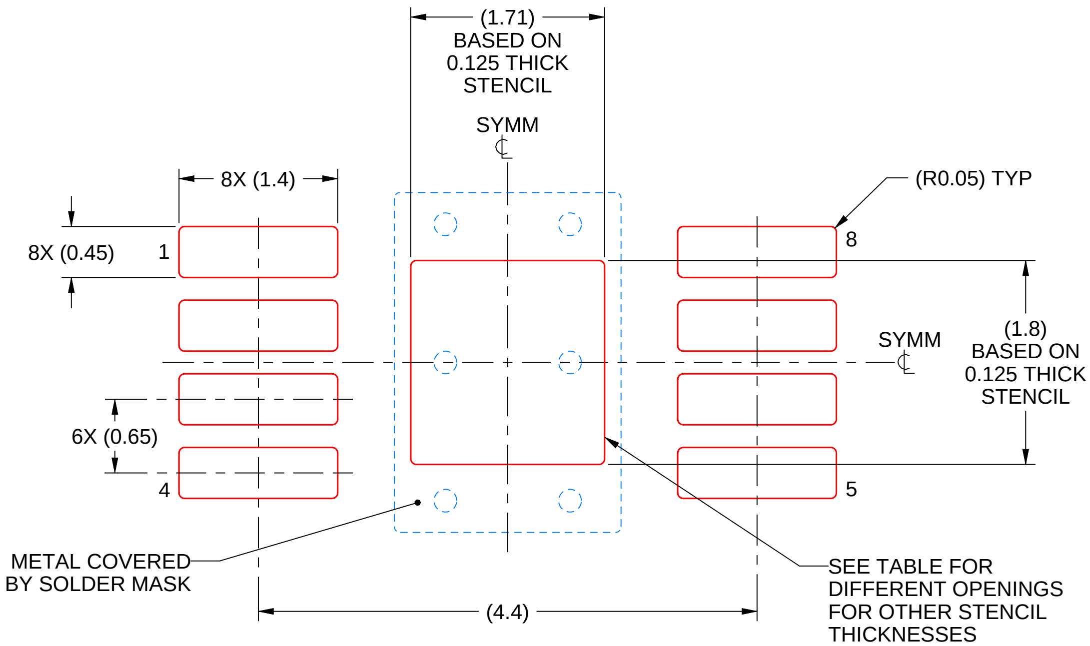


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



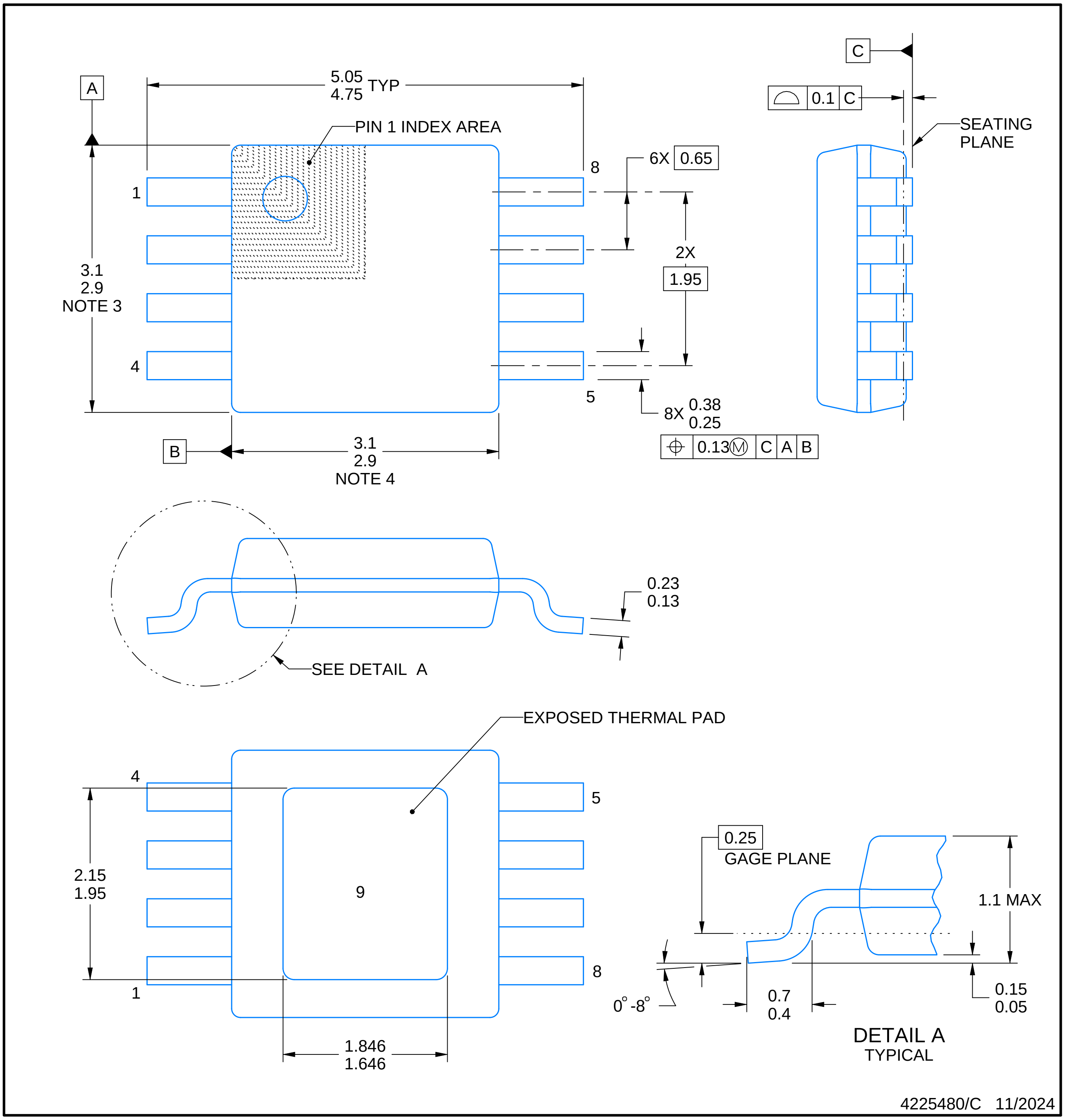
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

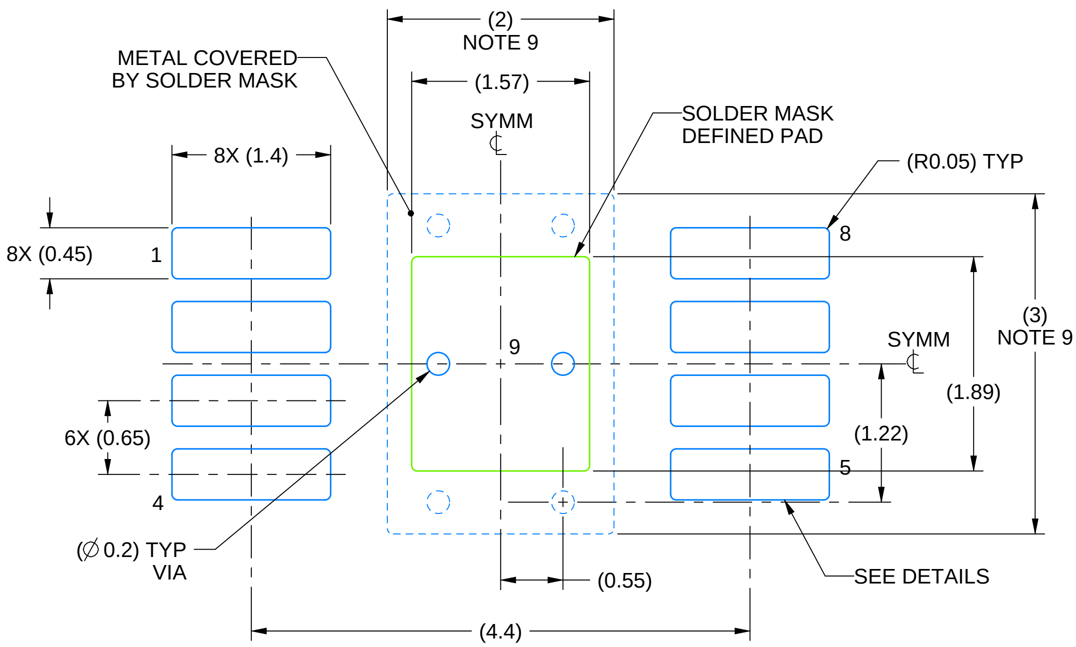
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



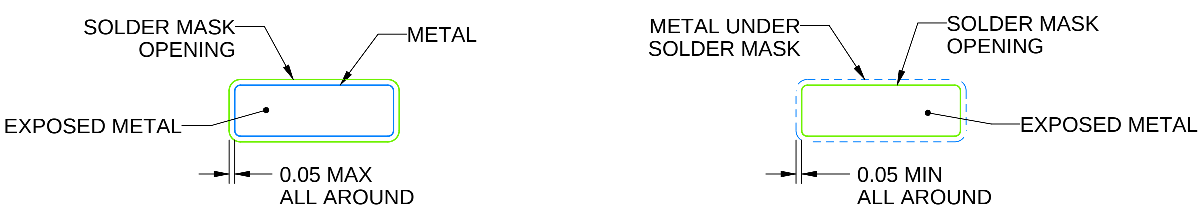
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

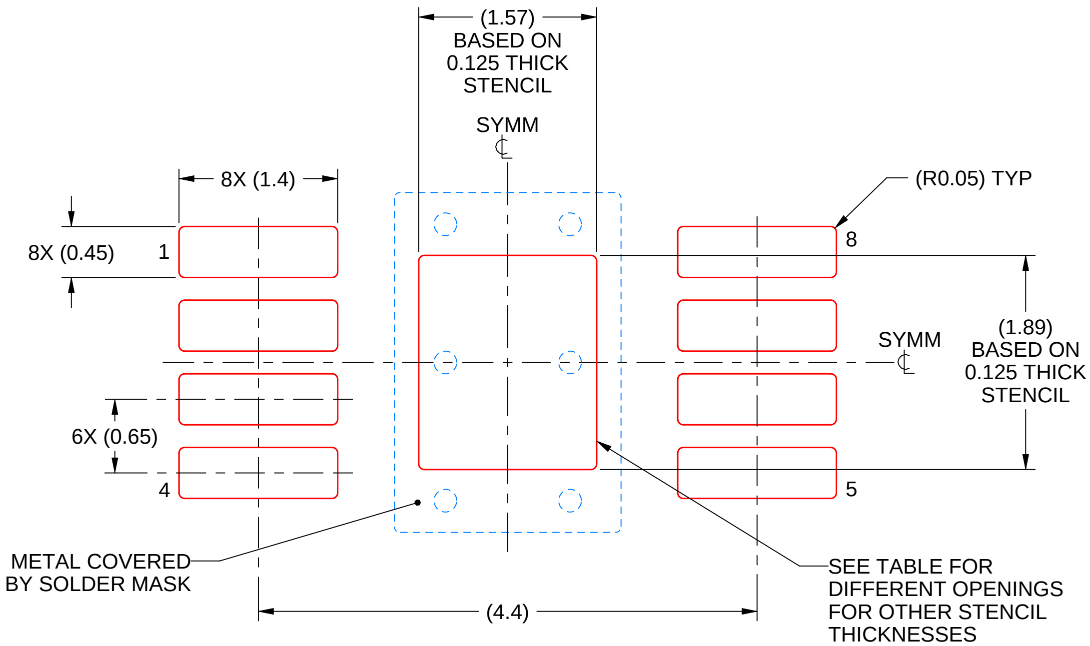
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



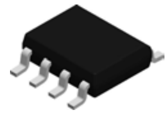
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

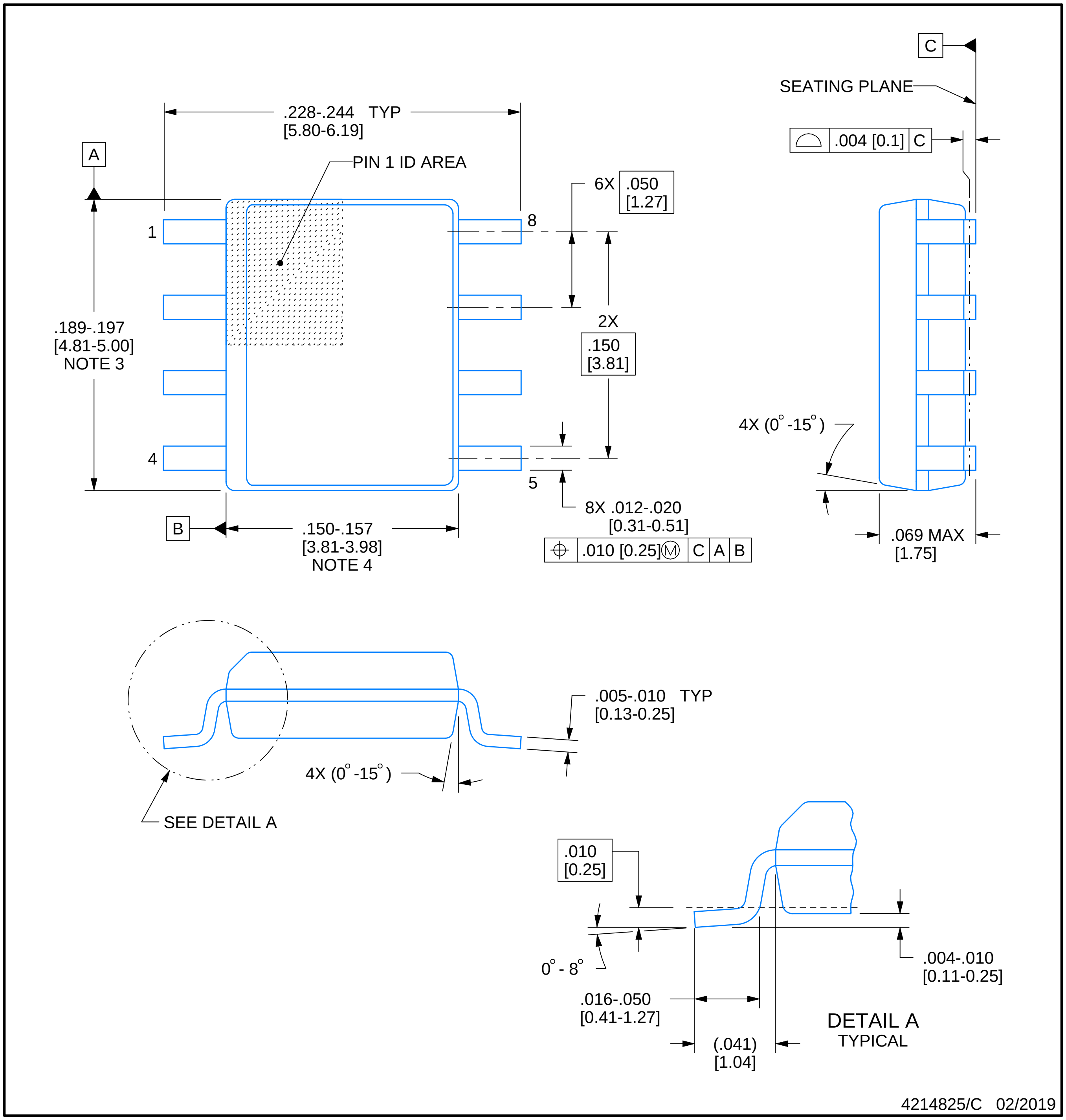


PACKAGE OUTLINE

D0008A

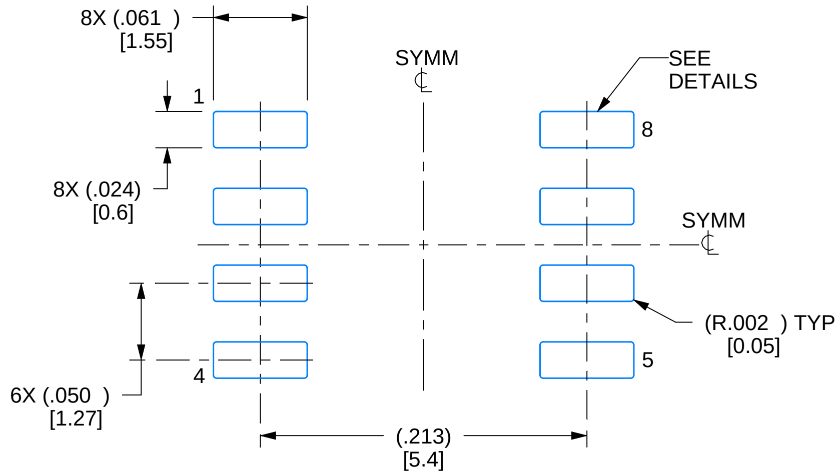
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

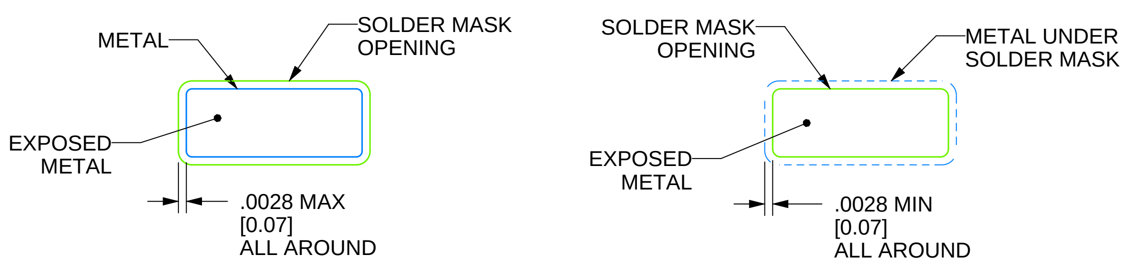


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

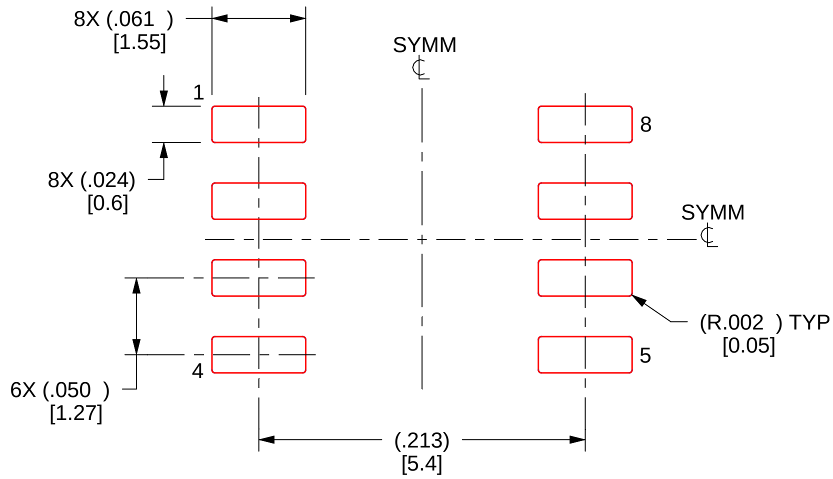
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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