TCAN844-Q1 車載用、フォルト保護機能搭載、スタンバイ モード付き CAN FD トランシーバ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 人体モデル (HBM) ESD 保護：AEC Q100-002 準拠、
    CANH および CANL ピンで ±12kV
  - デバイス帯電モデル (CDM) ESD 保護：AEC Q100-011 準拠、±500V
  - IEC 61000-4-2 接触放電：±8kV (電源供給なし)
- ISO 11898-2:2024 の物理層規格に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5Mbps)
  - 短く対称的な伝搬遅延時間によりタイミング マージンを強化
- TCAN844V-Q1 の I/O 電圧範囲：2.9V～5.25V
- 12V バッテリ アプリケーションをサポート
- レシーバの同相入力電圧：±12V
- 保護機能：
  - バス フォルト保護：±40V
  - 低電圧保護
  - TXD ドミナント タイムアウト (DTO)
    - 最小 9.2kbps のデータ レート
  - サーマル シャットダウン保護 (TSD)
- 動作モード：
  - 通常モード
  - リモート ウェイクアップ要求をサポートする、低消費電力スタンバイ モード
- 電源非接続時の最適化された挙動
  - バスおよびロジック ピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
  - ホットプラグ対応：電源オン / オフ時のバスおよび RXD 出力のグリッチ フリー動作
- 8 ピン SOIC、小型フットプリント SOT-23、自動光学検査 (AOI) に適したリードレス VSON-8 パッケージ

2 アプリケーション

- 自動車および輸送システム
  - 車体制御モジュール
  - 車載ゲートウェイ
  - 先進運転支援システム (ADAS)
  - インフォテインメント

3 概要

TCAN844-Q1 は高速 CAN (Controller Area Network) トランシーバであり、ISO 11898-2:2024 高速 CAN 仕様の物理層要件に適合しています。

本デバイスは V_{IO} ピンによる内部ロジック レベル変換機能を備えているため、トランシーバの I/O を 3.3V または、5V のロジック レベルに直接接続できます。このトランシーバは、低消費電力スタンバイ モードと、ISO 11898-2:2024 に規定されたウェイクアップ パターン (WUP) に適合した「CAN によるウェイク」をサポートしています。

このトランシーバは、サーマル シャットダウン (TSD)、TXD ドミナント タイムアウト (DTO)、電源低電圧検出、±40V バス フォルト保護も備えています。これらのデバイスには、電源電圧低下またはフローティング ピン発生時のフェイルセーフ動作が定義されています。これらのトランシーバは、業界標準の SOIC-8 および VSON-8 パッケージで供給されるだけでなく、省スペースの小型 SOT-23 パッケージ オプションもあります。

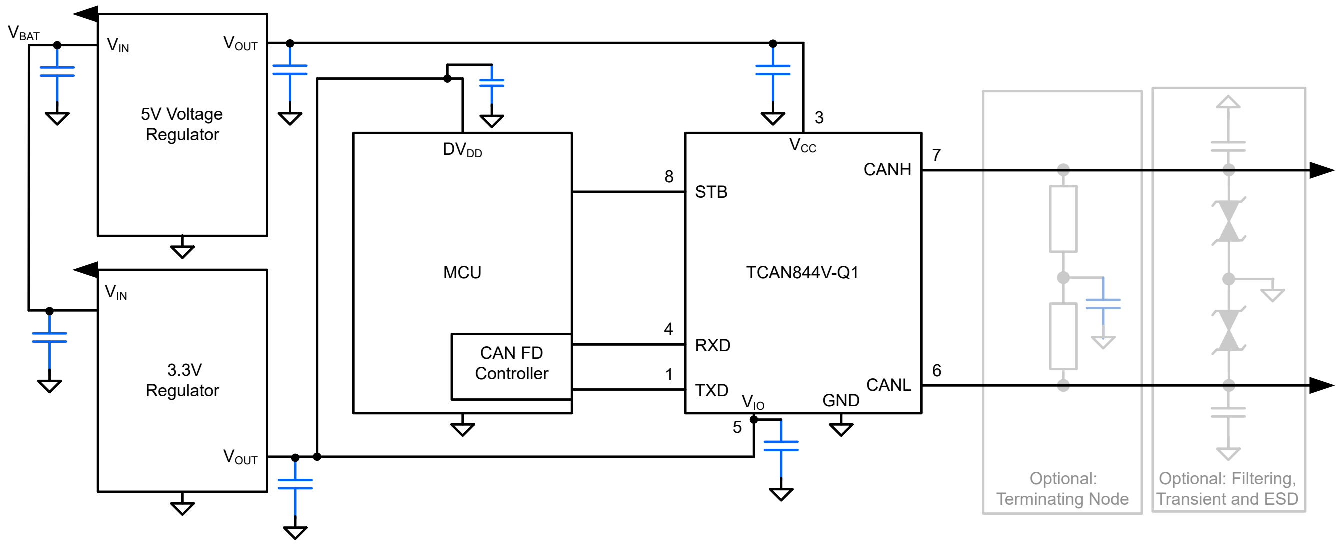
パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
TCAN844-Q1	SOIC (D)	4.9 mm × 6mm
	VSON (DRB)	3 mm × 3mm
	SOT-23 (DDF)	2.9 mm × 2.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

表 3-1. デバイス比較表

部品番号	ピン 5 で低電圧 I/O ロジックをサポート	ピン 8 のモード選択
TCAN844-Q1	なし	リモート ウェイクアップ機能付き低消費電力スタンバイ モード
TCAN844V-Q1	あり	



概略回路図

Table of Contents

4 Pin Configuration and Functions

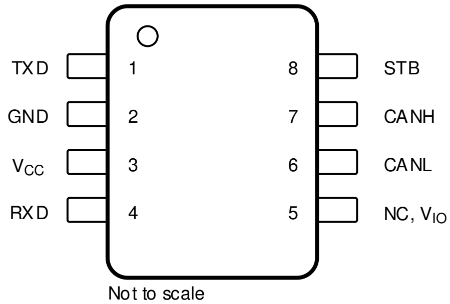


図 4-1. DDF Package, 8-Pin SOT (Top View)

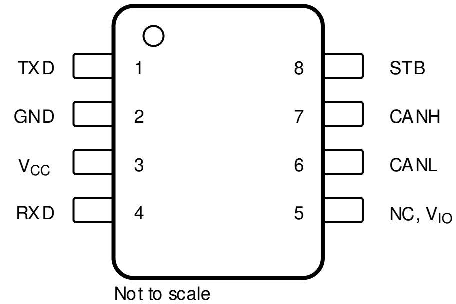


図 4-2. D Package, 8-Pin SOIC (Top View)

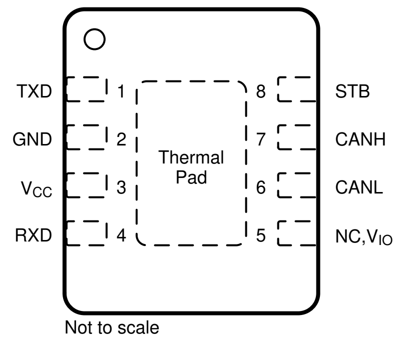


図 4-3. DRB Package, 8-Pin VSON (Top View)

表 4-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input; integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-stated when device powered off
NC	5	—	Not internally connected; Devices without V_{IO}
V_{IO}		Supply	I/O supply voltage for devices with suffix 'V'
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control; integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for improved thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage (CANH, CANL)	–40	40	V
V_{DIFF}	Max differential voltage range between CANH and CANL	–12	12	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Operating virtual junction temperature range	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			CANH and CANL	±12000	V
		Charged-device model (CDM), per AEC Q100-011		±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings, IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)(1)	CAN bus terminals (CANH CANL) to GND	IEC 61000-4-2 (150pF, 330Ω): Unpowered contact discharge	±8000	V

(1) Tested according to IEC 62228-3 CAN Transceivers (2019), Section 6.4; DIN EN 61000-4.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IO}	Supply voltage for I/O level shifter	2.9		5.25	V
$I_{OH(RXD)}$	RXD terminal high level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_J	Operational free-air temperature (see thermal characteristics table)	–40		150	°C
T_{SDR}	Thermal shutdown	160			°C
T_{SDF}	Thermal shutdown release			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

5.5 Thermal Characteristics

THERMAL METRIC		TCAN844(V)-Q1			UNIT
		D (SOIC)	DRB (VSON)	DDF (SOT23)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.1	67.7	180.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.3	77.2	94.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	40.3	93.3	°C/W

5.5 Thermal Characteristics (続き)

THERMAL METRIC		TCAN844(V)-Q1			UNIT
		D (SOIC)	DRB (VSON)	DDF (SOT23)	
Ψ_{JT}	Junction-to-top characterization parameter	21.1	6.8	8.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.5	40.1	93.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	23.7	–	°C/W

5.6 Power Supply Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	TXD = 0V, R_L = 60Ω, C_L = open		44	70	mA
	Supply current normal mode	Dominant	TXD = 0V, R_L = 50Ω, C_L = open		48	80	mA
	Supply current normal mode	Recessive	TXD = V_{CC}, R_L = 50Ω, C_L = open, RCM = open		5.6	10	mA
	Supply current normal mode	Dominant with bus fault	TXD = 0V, CANH = CANL = ±25V, R_L = open, C_L = open			130	mA
	Supply current standby mode	TCAN844V	TXD = V_{IO}, R_L = 50Ω, C_L = open			5	µA
	Supply current standby mode	TCAN844	TXD = V_{CC}, R_L = 50Ω, C_L = open			30	µA
I_{IO}	I/O supply current normal mode	Dominant	RXD floating, TXD = 0V		135	400	µA
	I/O supply current normal mode	Recessive	RXD floating, TXD = V_{IO}		28	150	µA
	I/O supply current standby mode		RXD floating, TXD = V_{IO}		20	28	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.6	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.5	V
UV_{VIO}	Rising under voltage detection on V_{IO}				2.5	2.9	V
UV_{VIO}	Falling under voltage detection on V_{IO}			2.1	2.4		V
TSD	Thermal shutdown temperature			165	180	195	
TSD_HYS	Thermal shutdown hysteresis				10		

5.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60 Ω, C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave		90		mW
		V_{CC} = 5.25 V, V_{IO} = 3.3 V, T_J = 150°C, R_L = 60 Ω, C_{L_RXD} = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		110		mW

5.8 Electrical Characteristics

Over recommended operating conditions with TJ = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics						
$V_{CANH(D)}$	Bus output voltage (dominant) CANH	V_{TXD} = 0V, R_L =50Ω to 65Ω, C_L = open, R_{CM} = open	2.75		4.5	V
$V_{CANL(D)}$	Bus output voltage (dominant) CANL	V_{TXD} = 0V, R_L =50Ω to 65Ω, C_L = open, R_{CM} = open	0.5		2.25	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Bus output voltage (recessive)	V_{TXD} = V_{CC}, R_L = open (no load), R_{CM} = open	2		3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}	R_{TERM} = 60Ω, C_L = open, C_{SPLIT} = 4.7 nF	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)	R_L = 60Ω, C_L = open	–400		400	mV
$V_{DIFF(D)}$	Differential output voltage normal mode Dominant	TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open	1.5		3	V
		TXD = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open	1.4		3.3	V
		TXD = 0V, R_L = 2240Ω, C_L = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage normal mode Recessive	TXD = V_{CC} or V_{IO}, R_L = 60Ω, C_L = open	–120		12	mV
		Normal mode, TXD = V_{CC} or V_{IO}, R_L = open, C_L = open	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage on CANH with bus biasing inactive	V_{TXD} = V_{CC} or V_{IO}, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
$V_{CANL(INACT)}$	Bus output voltage on CANL with bus biasing inactive	V_{TXD} = V_{CC} or V_{IO}, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
$V_{DIFF(INACT)}$	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive	V_{TXD} = V_{CC} or V_{IO}, R_L = open, C_L = open, R_{CM} = open	–0.2		0.2	V
$I_{CANH(OS)}$	Short-circuit steady-state output current, Dominant	–3.0V ≤ V_{CANH} ≤ +18.0V, CANL = open, V_{TXD} = 0V	–115			mA
$I_{CANL(OS)}$		–3.0V ≤ V_{CANL} ≤ +18.0V, CANH = open, V_{TXD} = 0V			115	mA
I_{OS_REC}	Short-circuit steady-state output current; Recessive	–40V ≤ V_{BUS} ≤ +40V, V_{BUS} = CANH = CANL	–5		5	mA
Receiver Electrical Characteristics						
$V_{DIFF\_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	0.9		8	V
$V_{DIFF\_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	-3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes	-12V ≤ V_{CM} ≤ 12V		80		mV
$V_{DIFF\_RX(D\_INACT)}$	Receiver dominant state differential input voltage range, bus biasing in-active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	1.15		8	V
$V_{DIFF\_RX(R\_INACT)}$	Receiver recessive state differential input voltage range, bus biasing in-active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	–3		0.4	V
V_{CM}	Common mode range:		–12		12	V
$I_{LKG(IOFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V			5	μA
CI powered Normal	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, V_{IO} = V_{CC}			20	pF
C_{ID} powered Normal	Differential input capacitance	TXD = V_{CC}, V_{IO} = V_{CC}			10	pF
R_{DIFF}	Differential input resistance during passive recessive state	V_{TXD} = V_{CC} or V_{IO}, normal mode: –2.0V ≤ V_{CANH} ≤ +7.0V; –2.0V ≤ V_{CANL} ≤ +7.0V	18		90	kΩ

5.8 Electrical Characteristics (続き)

Over recommended operating conditions with TJ = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{SE_CANH} R_{SE_CANL}	Single ended Input resistance during passive recessive state	$-2V \le V_{CANH} \le +7V$ $-2V \le V_{CANL} \le +7V$	9		45	kΩ
m_R	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	$V_{CANH} = V_{CANL} = 5V$	–2%		2%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	TCAN844	0.7 × V_{CC}			V
V_{IH}	High-level input voltage	TCAN844V	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	TCAN844			0.3 × V_{CC}	V
V_{IL}	Low-level input voltage	TCAN844V			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.25V	–2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC} = V_{IO} = 5.25V	–200		–20	μA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	μA
C_I	Input Capacitance	$V_{IN} = 0.4 \times \sin(2 \times \pi \times 2 \times 10^6 \times t) + 2.5V$		2		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level input voltage	I_O = –2mA, TCAN844	0.8 × V_{CC}			V
V_{OH}	High-level input voltage	I_O = –2mA, TCAN844V	0.8 × V_{IO}			V
V_{OL}	Low-level input voltage	I_O = 2 mA, TCAN844			0.2 × V_{CC}	V
V_{OL}	Low-level input voltage	I_O = 2mA, TCAN844V			0.2 × V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	μA
STB Terminal						
V_{IH}	High-level input voltage	TCAN844	0.7 × V_{CC}			V
V_{IH}	High-level input voltage	TCAN844V	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	TCAN844			0.3 × V_{CC}	V
V_{IL}	Low-level input voltage	TCAN844V			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current STB	V_{CC} = V_{IO} = STB = 5.25V	–2		2	μA
I_{IL}	Low-level input leakage current STB	V_{CC} = V_{IO} = 5.25V, STB = 0V	–20		–2	μA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	μA

5.9 Switching Characteristics

Over recommended operating conditions with TJ = -40℃ to 150℃ (unless otherwise noted)

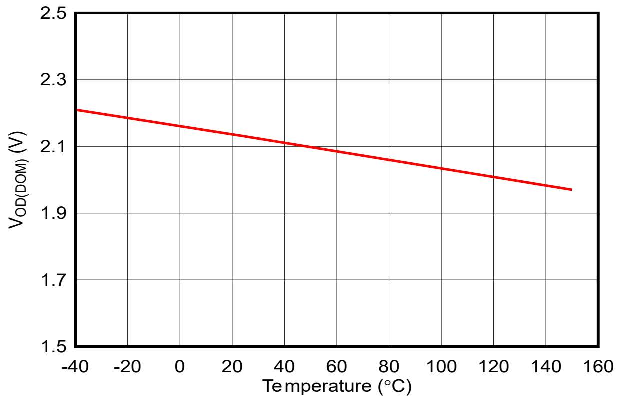
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF		100	220	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF		110	220	ns
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal				45	μs
t_{WK_FILTER}	Filter time for a valid wake-up pattern		0.5		1.8	μs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value		0.8		6	ms
Driver Switching Characteristics						

5.9 Switching Characteristics (続き)

Over recommended operating conditions with TJ = -40℃ to 150℃ (unless otherwise noted)

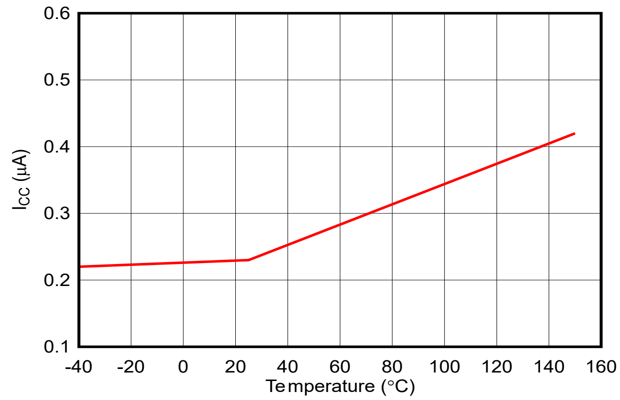
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	R_L = 60Ω, C_L = 100pF, R_{CM} = open		50		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			45		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			4		ns
t_R	Differential output signal rise time			32		ns
t_F	Differential output signal fall time			27		ns
t_{TXD_DTO}	Dominant timeout	R_L = 60Ω, C_L = 100pF	0.8		6.5	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	C_{L_RXD} = 15pF		75		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			70		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation: $t_{BIT(TXD)}$ = 500 ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	-65		30	ns
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation: $t_{BIT(TXD)}$ = 200 ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	-45		10	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)}$ = 500 ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(RXD)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-100		50	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)}$ = 200 ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(RXD)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-80		20	ns
$t_{\Delta REC}$	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-65		40	ns
$t_{\Delta REC}$	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

5.10 Typical Characteristics



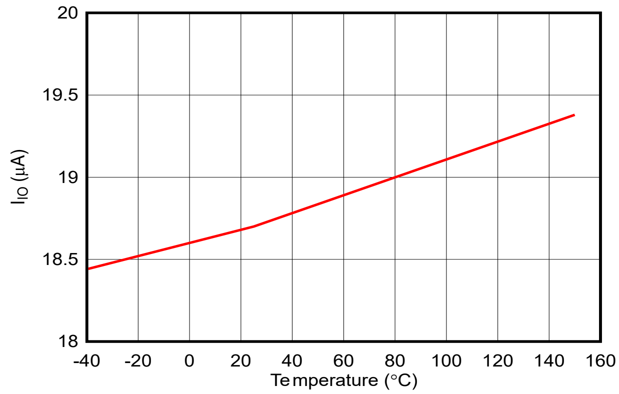
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-1. $V_{OD(DOM)}$ vs Temperature



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-2. I_{CC} Standby vs Temperature



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-3. I_{IO} Standby vs Temperature

6 Parameter Measurement Information

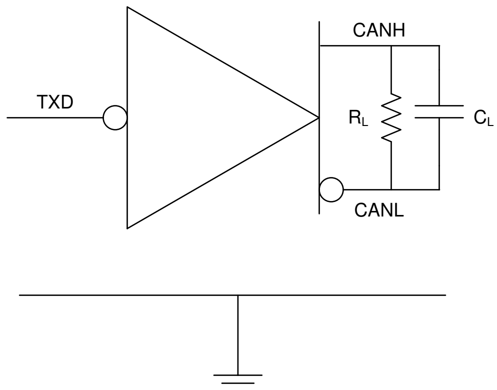


図 6-1. I_{CC} Test Circuit

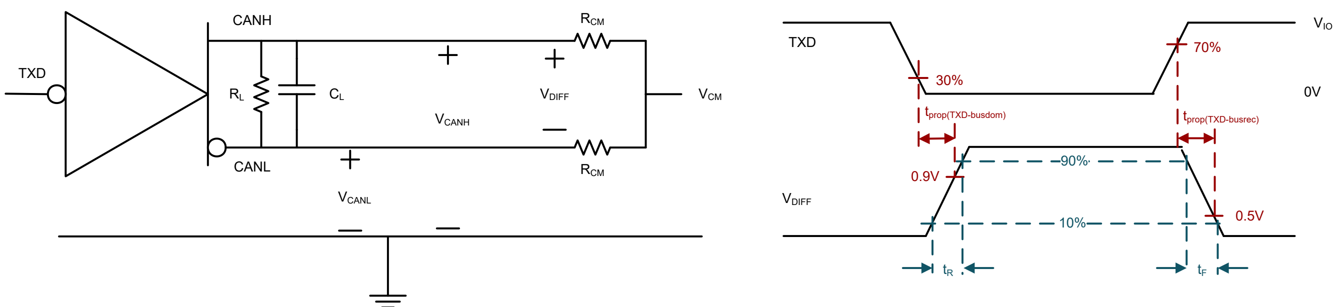


図 6-2. Driver Test Circuit and Measurement

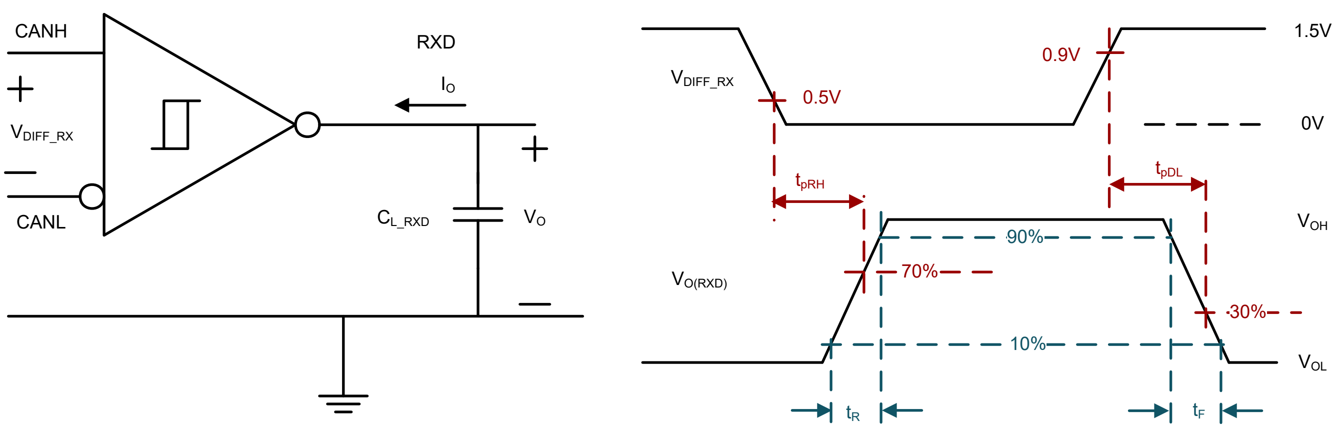


図 6-3. Receiver Test Circuit and Measurement

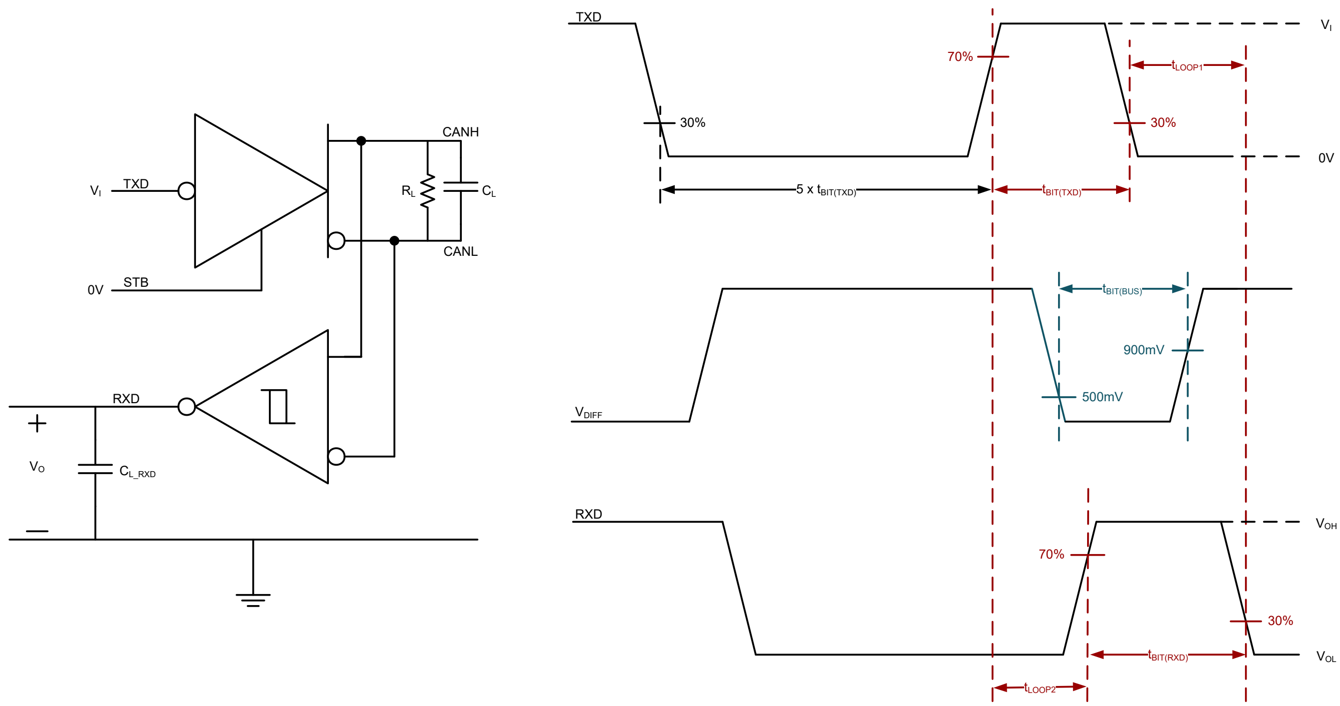


図 6-4. Transmitter and Receiver Timing Test Circuit and Measurement

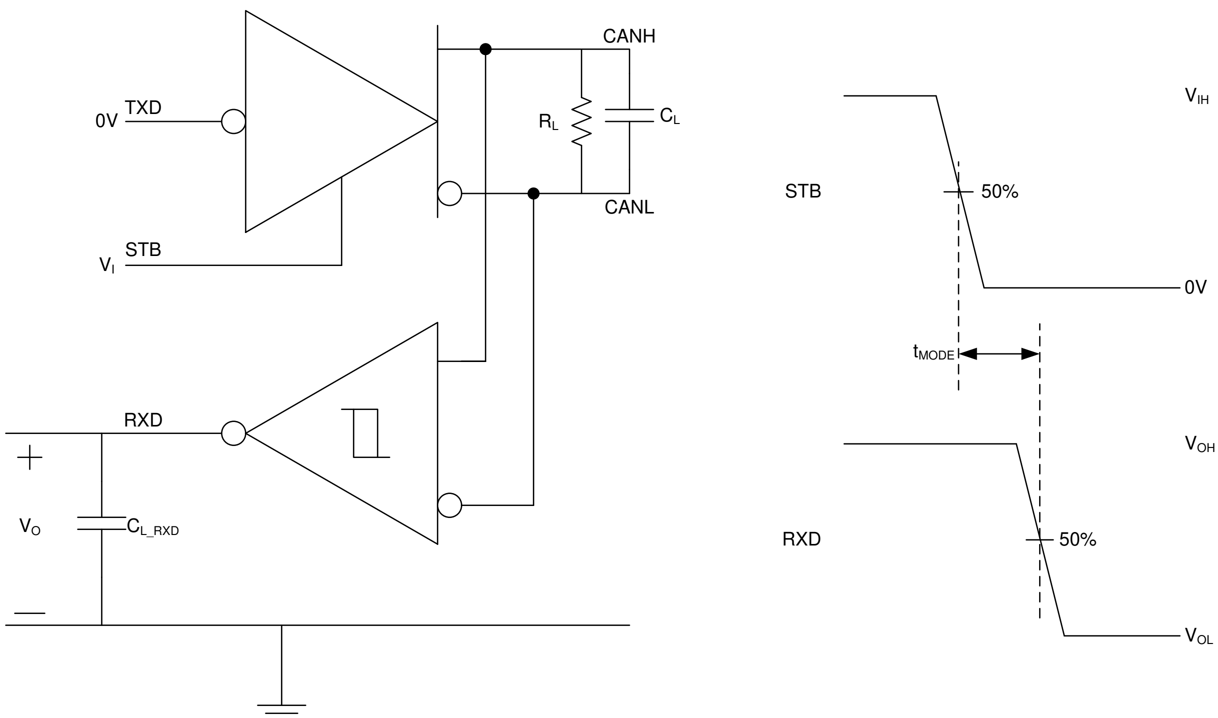


図 6-5. t_{MODE} Test Circuit and Measurement

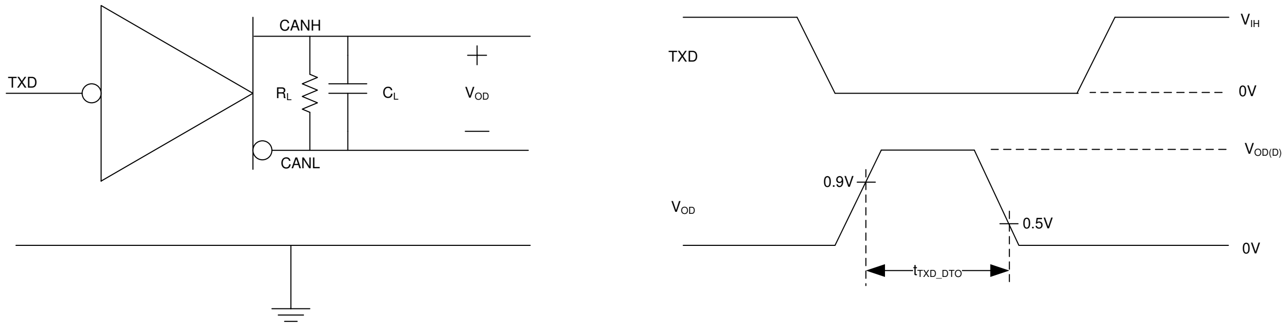


図 6-6. TXD Dominant Timeout Test Circuit and Measurement

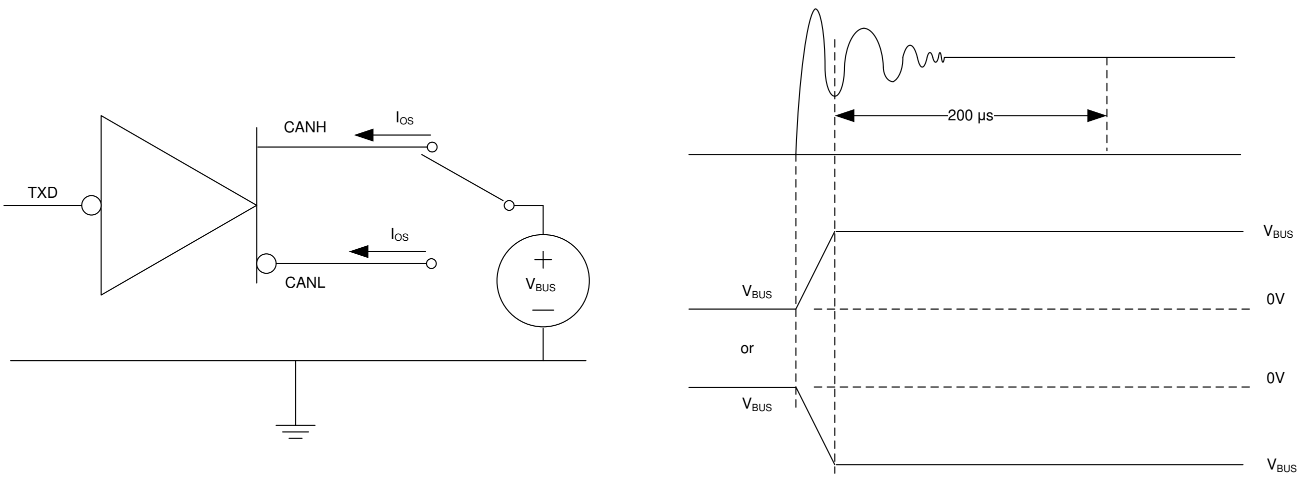


図 6-7. Driver Short-Circuit Current Test and Measurement

7 Detailed Description

7.1 Overview

The device is compatible with the specifications of the ISO 11898-2:2024 high speed CAN (Controller Area Network) physical layer standard. The transceivers provide a number of different protection features for the stringent automotive system requirements while also supporting CAN FD data rates up to 5Mbps.

The device supports the following CAN and CAN FD standards:

- Physical layer compatibility:
  - ISO 11898-2:2024 High speed medium access unit
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps

7.2 Functional Block Diagram

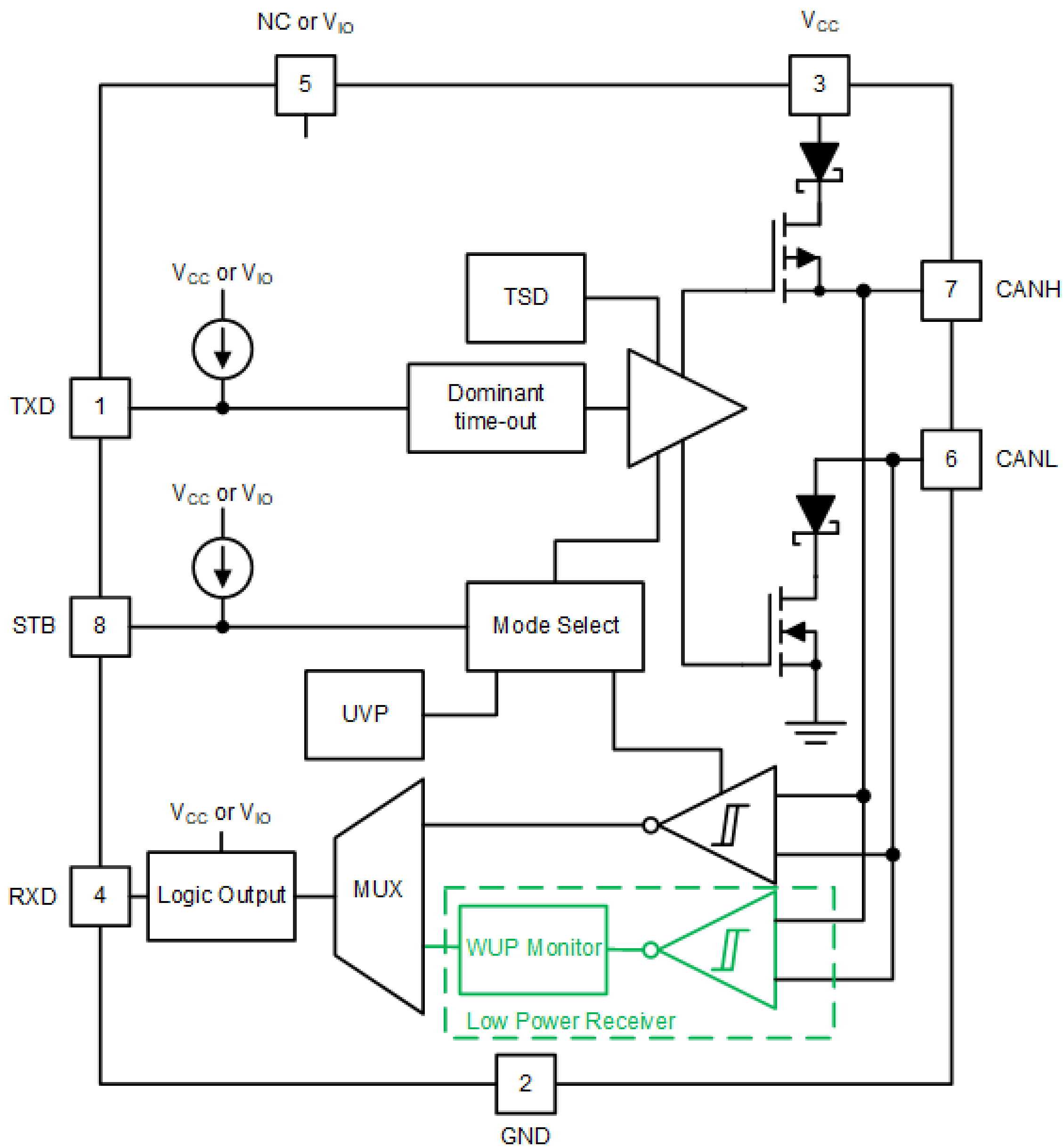


図 7-1. Block Diagram

7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the transceiver.

7.3.1.2 GND

GND is the ground pin of the transceiver. The pin must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.1.4 RXD

RXD is the logic-level signal, referenced to either V_{CC} or V_{IO}, from the TCAN844-Q1 to a CAN controller. This pin is only driven once V_{IO} is present.

7.3.1.5 V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage which avoids the requirement for a level shifter. V_{IO} supports voltages from 2.9V to 5.25V providing the widest range of controller support.

7.3.1.6 CANH and CANL

The CANH and CANL pins are the CAN high and CAN low differential bus pins. These pins are internally connected to the CAN transmitter, receiver and the low-power wake-up receiver.

7.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

7.3.2 CAN Bus States

The CAN bus has two logical states during operation, recessive and dominant. See 図 7-2 and 図 7-3.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN844(V)-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See 図 7-2 and 図 7-3.

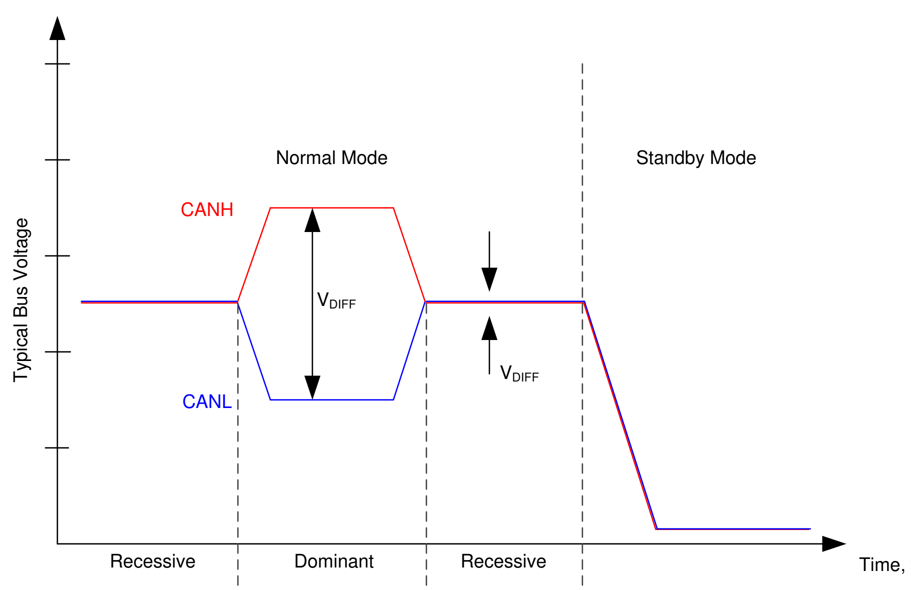
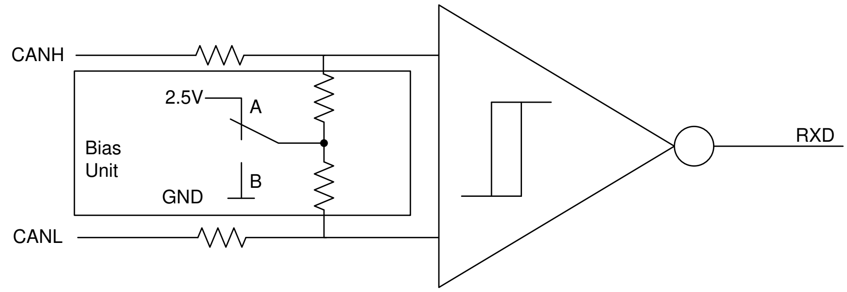


図 7-2. Bus States



A - Normal Mode B - Standby Mode

図 7-3. Simplified Recessive Common Mode Bias Unit and Receiver

7.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate can be calculated using 式 1.

$$\text{Minimum Data Rate} = 11\text{bits} / t_{TXD\_DTO} = 11\text{bits} / 1.2\text{ms} = 9.2\text{kbps} \quad (1)$$

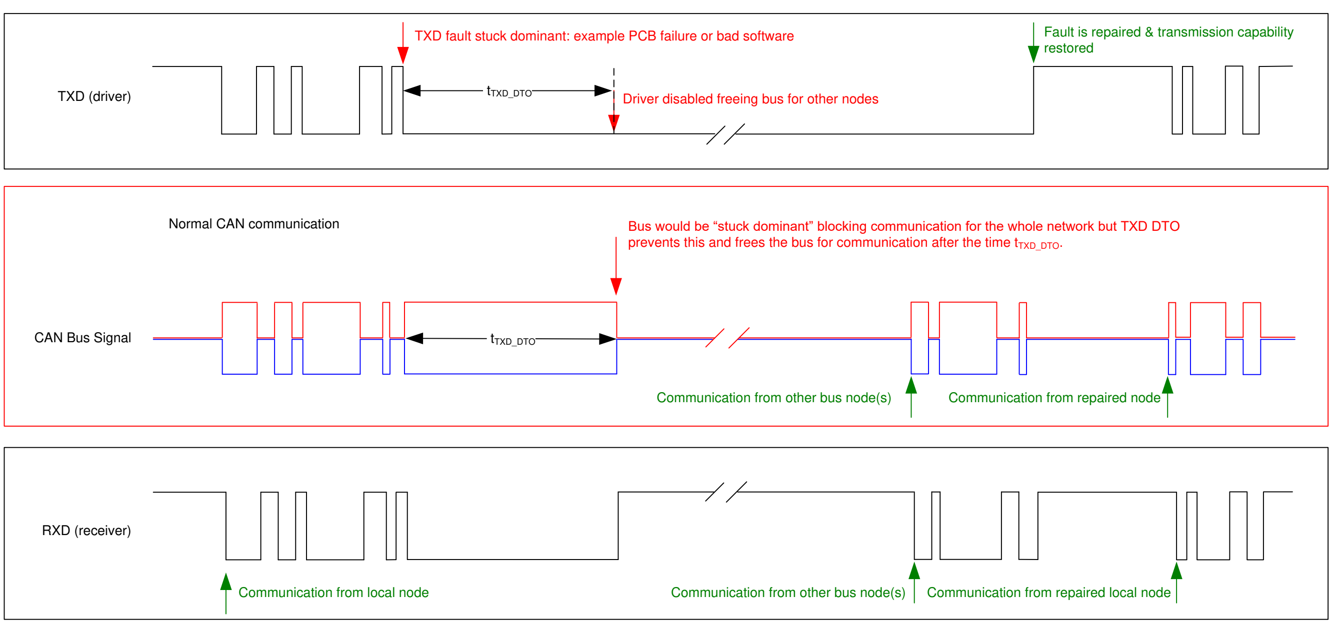


図 7-4. Example Timing Diagram for TXD Dominant Timeout

7.3.4 CAN Bus Short-Circuit Current Limiting

The TCAN844(V)-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout. Which prevents permanently having the higher short-circuit current of a dominant state in a system fault. During CAN communication, the bus switches between the dominant and recessive states. The short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design, the average power rating, $I_{OS(AVG)}$, are used. The percentage dominant is limited by the TXD DTO and the CAN protocol. Which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. Providing a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \%\ Transmit \times [(\%\ REC\_Bits \times I_{OS(SS)\_REC}) + (\%\ DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%\ Receive \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short circuit current and the possible fault cases of the network are taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

7.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN844(V)-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN844(V)-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 7-1. Undervoltage Lockout - TCAN844-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance	High impedance

表 7-2. Undervoltage Lockout - TCAN844V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = High: Standby Mode	Weak biased to GND	V_{IO}: Remote wake request See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
		STB =Low: Protected Mode	High impedance	Recessive
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN844-Q1 transitions to normal mode. The host controller can again send and receive CAN traffic.

7.3.7 Unpowered Device

The TCAN844(V)-Q1 is designed to be a passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the device does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so the pins do not load other circuits which may remain powered.

7.3.8 Floating pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias cannot be relied upon by design though, especially in noisy environments. Instead internal bias should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See 表 7-3 for details on pin bias conditions.

表 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

7.4 Device Functional Modes

7.4.1 Operating Modes

The TCAN844(V)-Q1 has two main operating modes, normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin.

表 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

7.4.2 Normal Mode

This is the normal operating mode of the TCAN844(V)-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional.

The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins.

The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

7.4.3 Standby Mode

This is the low-power mode of the TCAN844(V)-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in 図 7-5. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see 図 7-2 and 図 7-3.

In standby mode, only the V_{IO} supply is required; therefore, the V_{CC} may be switched off for additional system level current savings.

7.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN844(V)-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node needs to return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2024 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN844(V)-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP; thus, no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ can be detected as part of a WUP and a wake-up request can be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP; thus, a wake request is always generated. See 図 7-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2024 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less can contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See 図 7-5 for the timing diagram of the wake-up pattern with wake timeout feature.

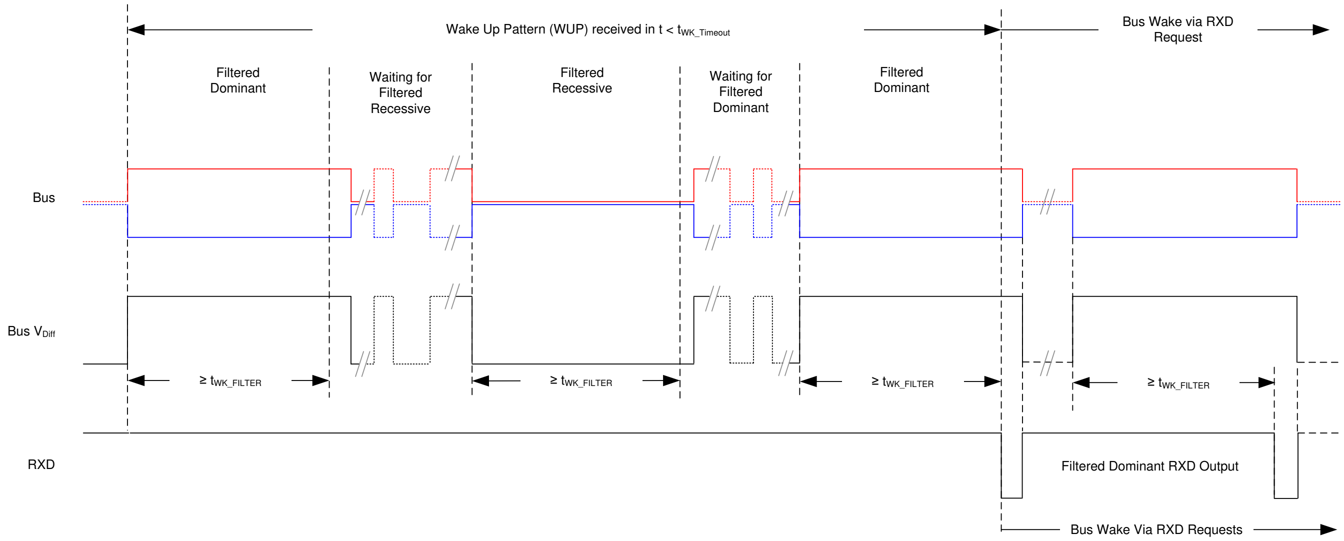


図 7-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

7.4.4 Driver and Receiver Function

The TCAN844-Q1 logic I/Os support CMOS levels with respect to either V_{CC} for 5V systems (TCAN844-Q1) or V_{IO} for compatibility with MCUs that support 3.3V or 5V systems (TCAN844V-Q1).

表 7-5. Driver Function Table

Device Mode	TXD Input[(1)]	Bus Outputs		Driven Bus State[(2)]
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see 図 7-2 and 図 7-3

表 7-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} – V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred See 図 7-5
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

8 Application Information Disclaimer

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TCAN844(V)-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. 図 8-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

8.2 Typical Application

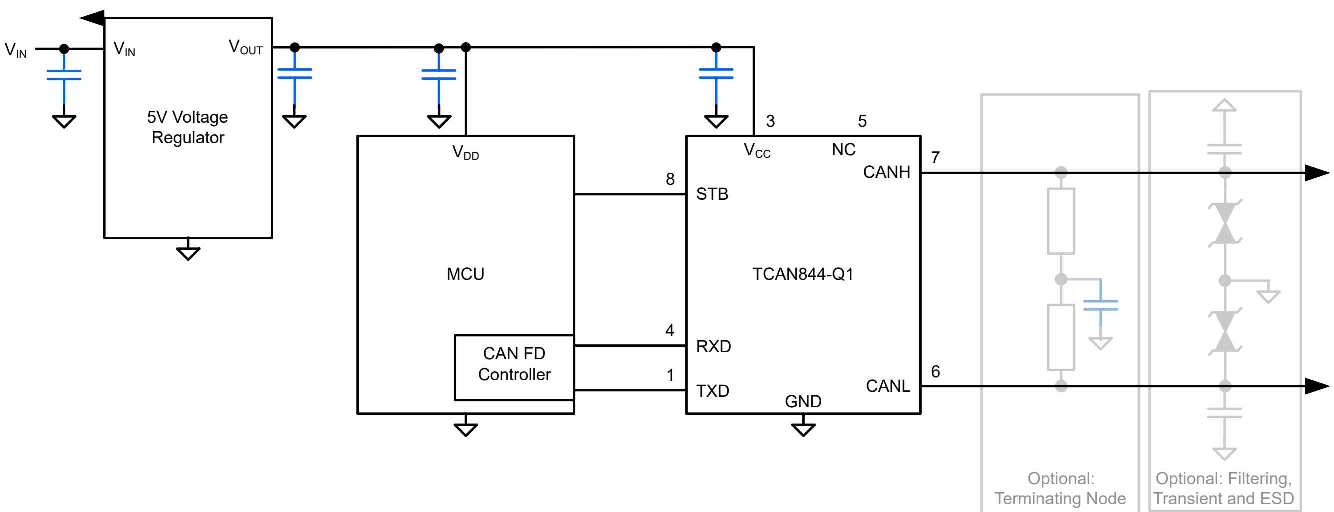


図 8-1. Transceiver Application Using 5V IO Connections

8.2.1 Design Requirements

8.2.1.1 CAN Termination

Termination can be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used, see 図 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that can be present on the differential signal lines.

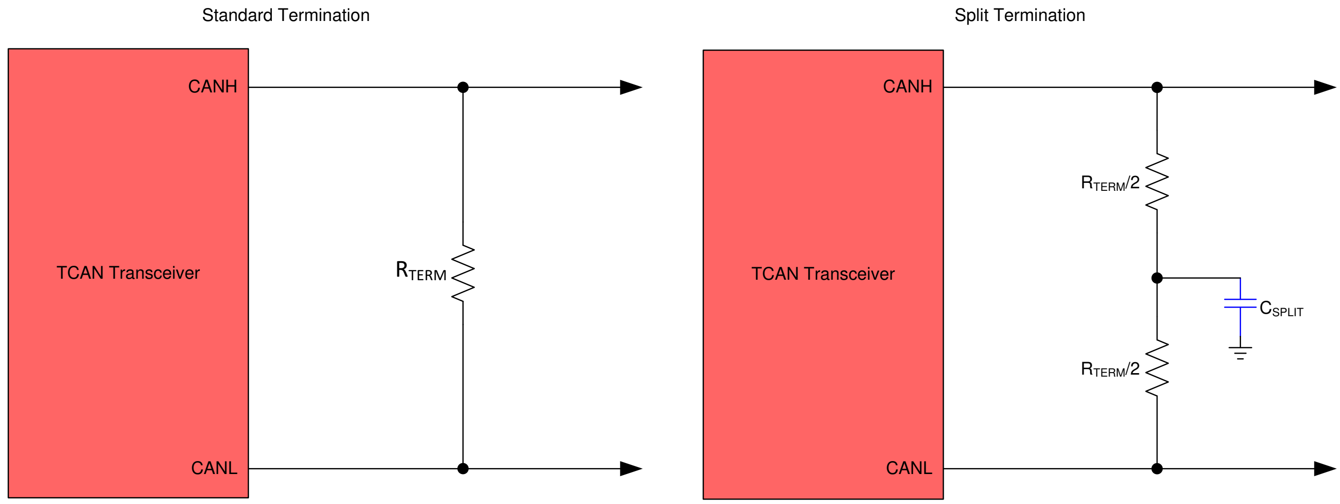


図 8-2. CAN Bus Termination Concepts

8.2.2 Detailed Design Procedures

8.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN844V-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. Various CAN standards made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN844(V)-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the device is a minimum of 40kΩ. If 100 TCAN844V-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN844(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets, and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length can also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to develop robust network operation.

See the application report Controller Area Network Physical layer requirements (SLLA270). The document discusses in detail all system design physical layer parameters.

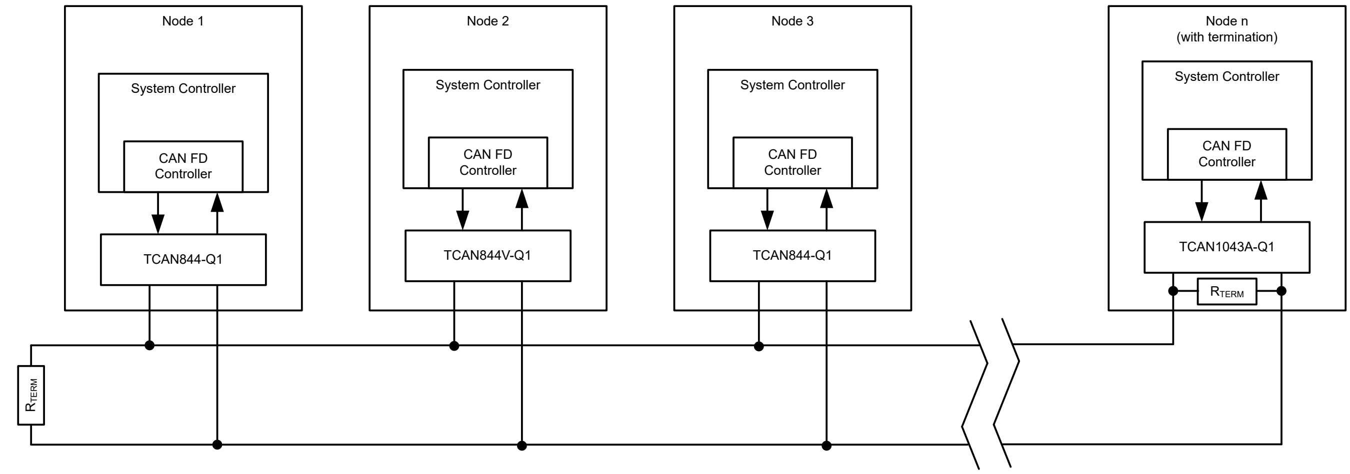


図 8-3. Typical CAN Bus

8.2.3 Application Curve

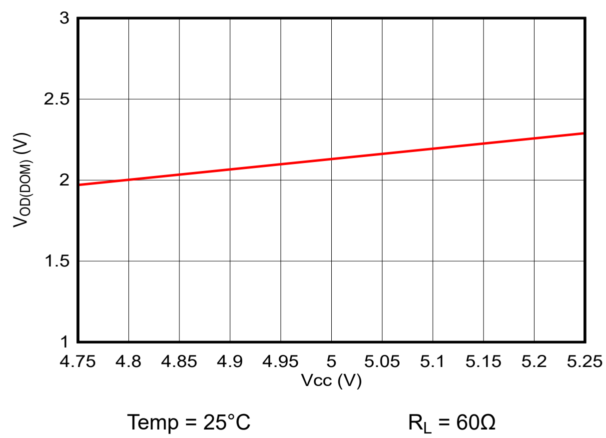


図 8-4. $V_{OD(DOM)}$ vs V_{CC}

8.3 System Examples

The TCAN844V-Q1 transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 3.3V application is shown in 図 8-5. The bus termination is shown for illustrative purposes.

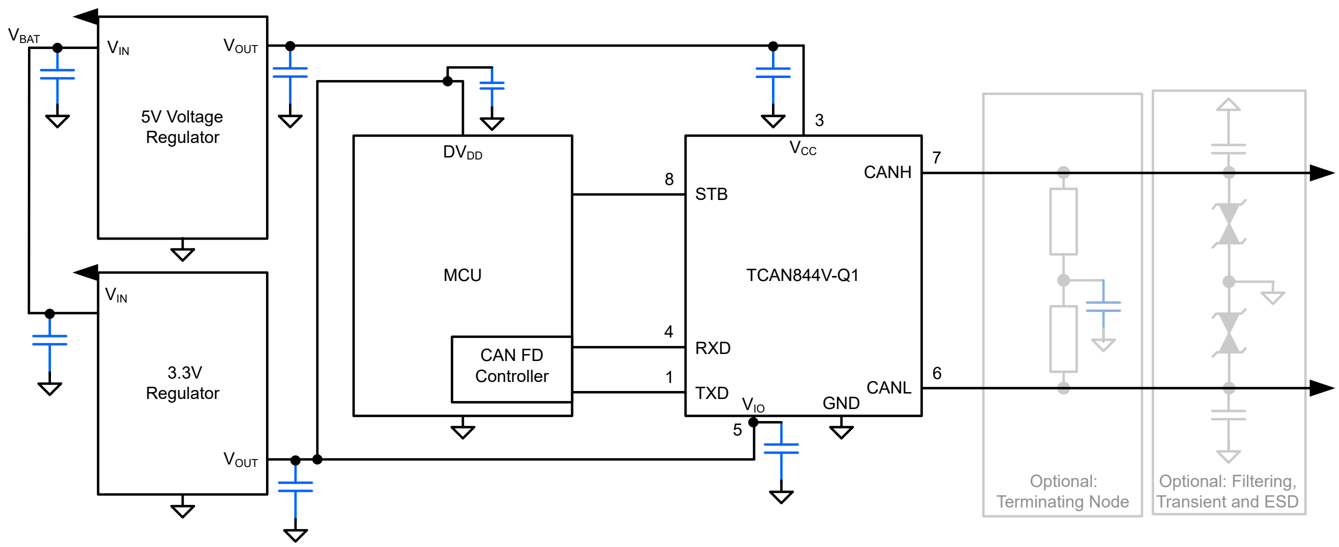


図 8-5. Typical Transceiver Application Using 3.3V IO Connections

8.4 Power Supply Recommendations

The TCAN844-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.75V and 5.25V.

The TCAN844V-Q1 implements an IO level shifting supply input, V_{IO}, designed for a range between 2.9V and 5.25V.

Both the V_{CC} and V_{IO} inputs must be well regulated. In addition to the power supply filtering a decoupling capacitance, typically 100nF, can be placed near the CAN transceiver main V_{CC} and V_{IO} supply pins.

8.5 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

8.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors are placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

注

High-frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R2 and R3, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See セクション 8.2.1.1, セクション 7.3.4, and 式 2 for information on termination concepts and power ratings needed for the termination resistor(s).

8.5.2 Layout Example

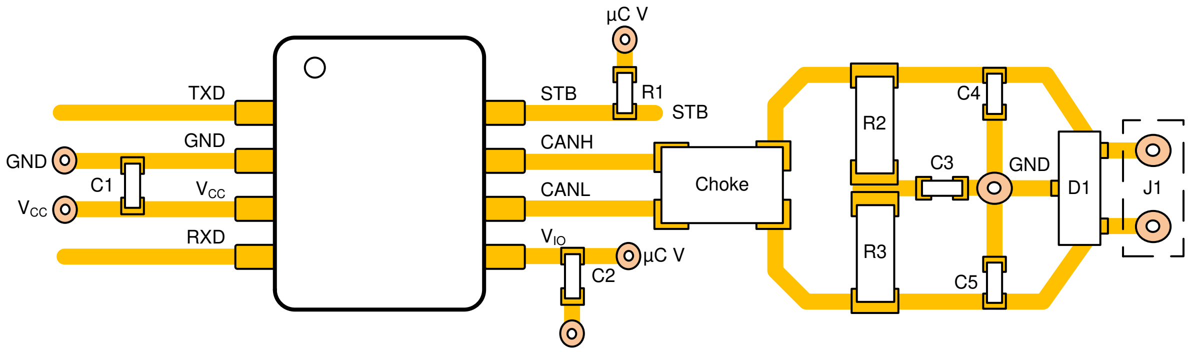


図 8-6. Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2024) to Revision A (October 2024) **Page**

- リビジョン A は、本データシートの最初の公開リリースです......1
- 「特長」の一覧に HBM、CDM、接触放電の情報を追加......1
- Added the *Dissipation Rating* table......5
- Changed the operating conditions from: T_J = -40℃ to 125℃ to: T*J* = -40℃ to 150℃ in the *Electrical Characteristics* and *Switching Characteristics* tables......5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN844VDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T844V
TCAN844VDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T844V
TCAN844VDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T844V
TCAN844VDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T844V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

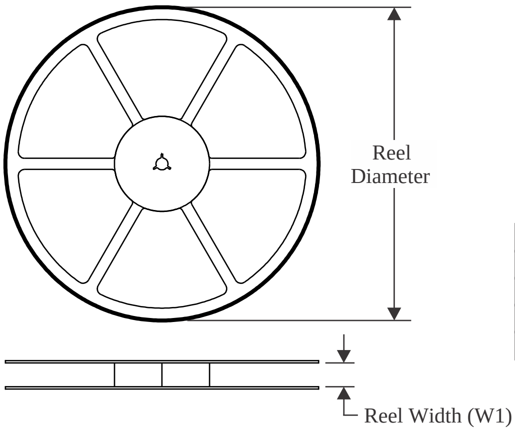
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

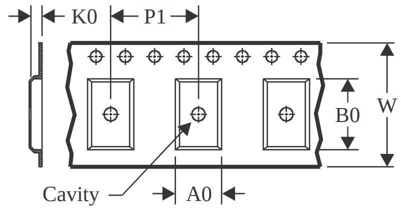
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

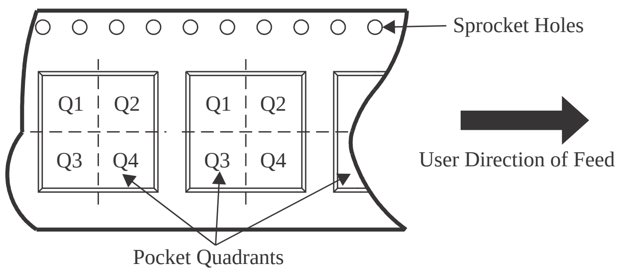


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

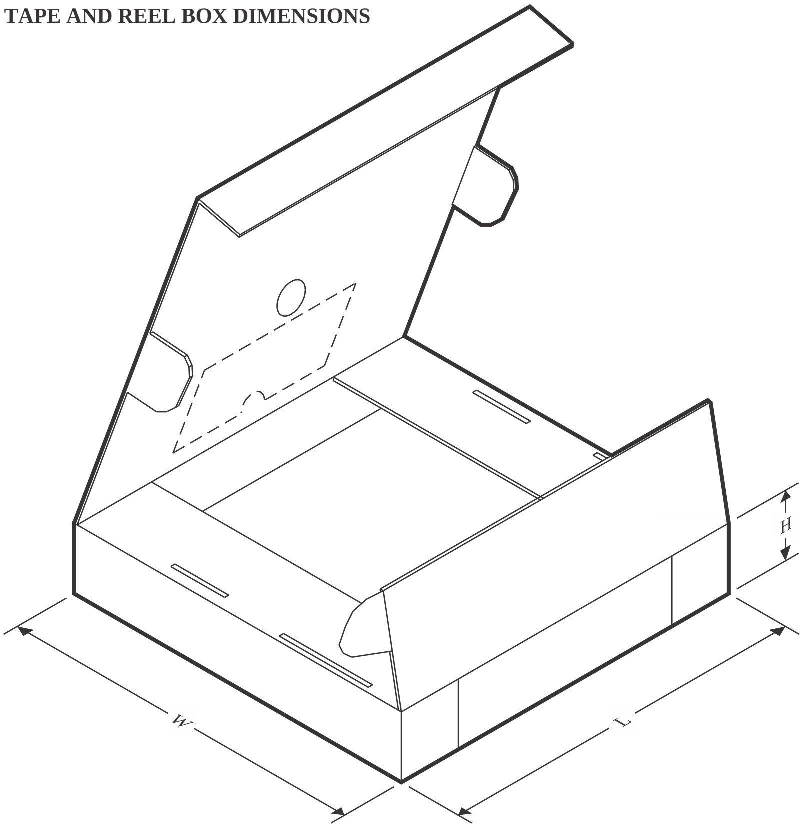
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN844VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN844VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

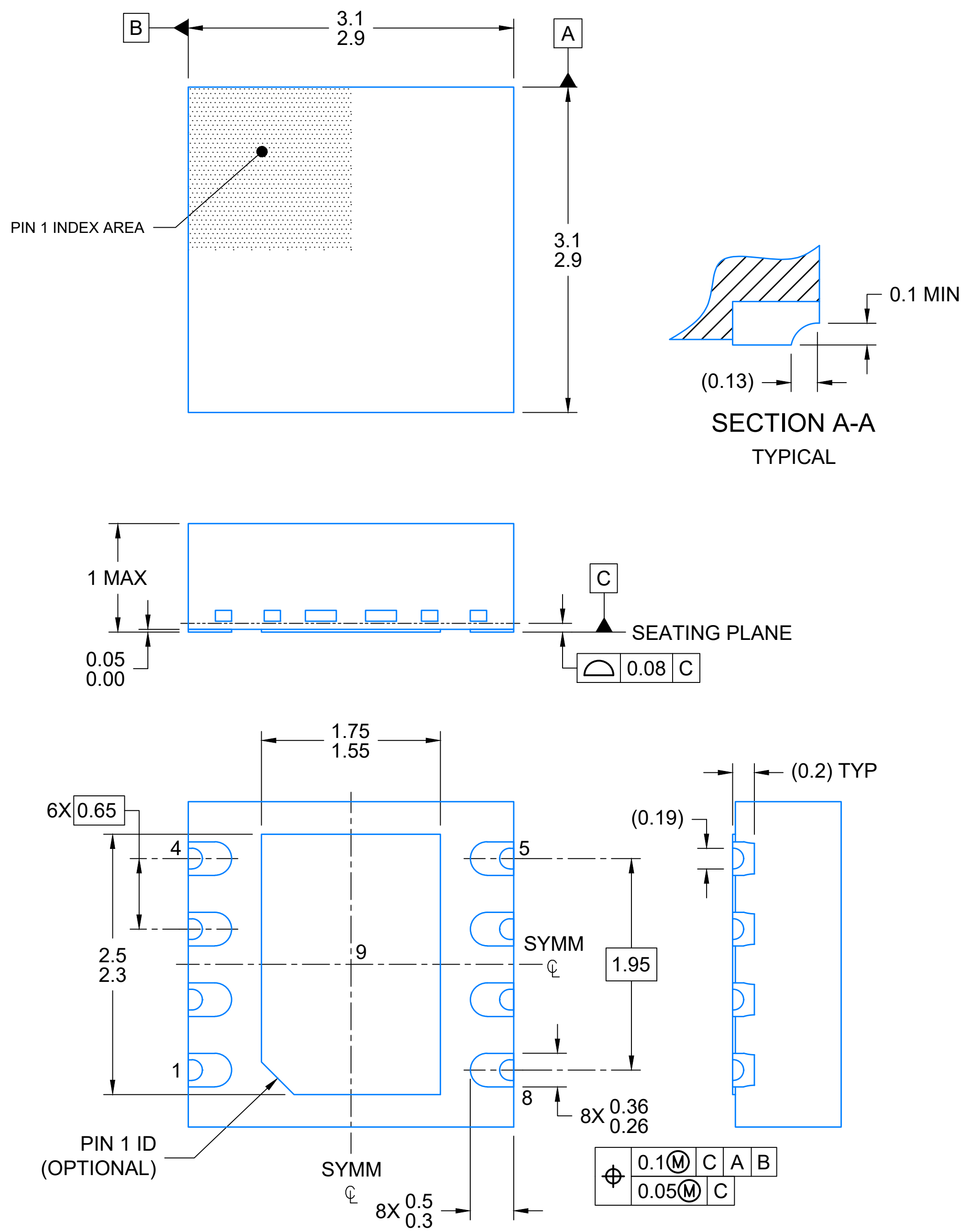
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN844VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN844VDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

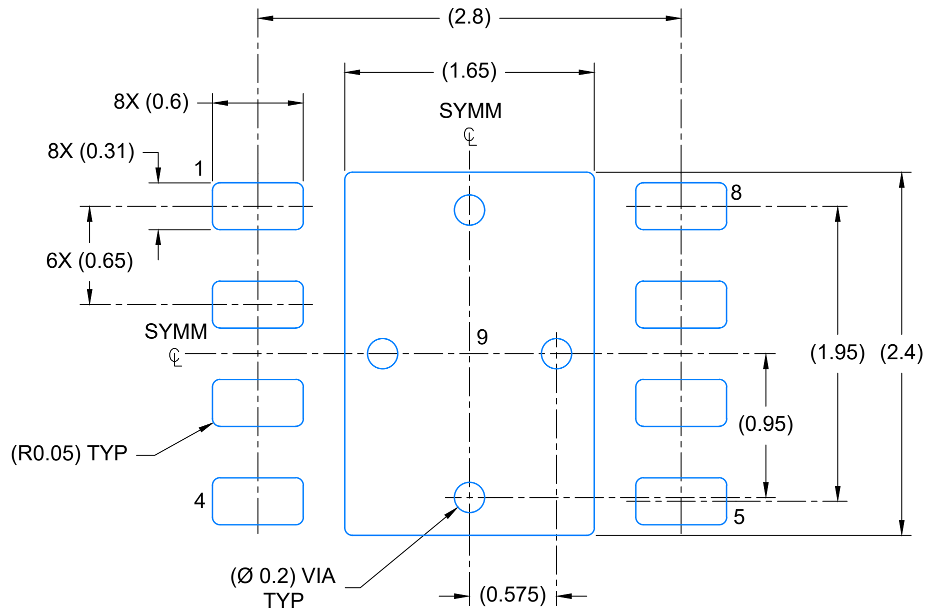
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



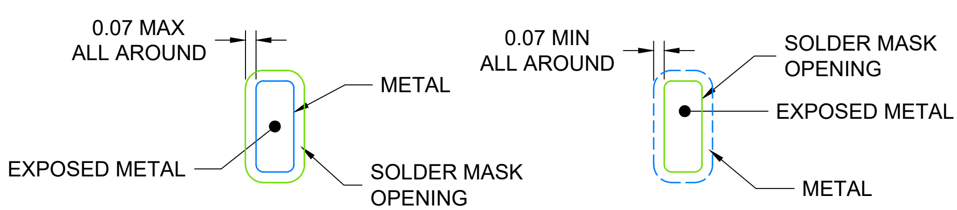
4225036/A 06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

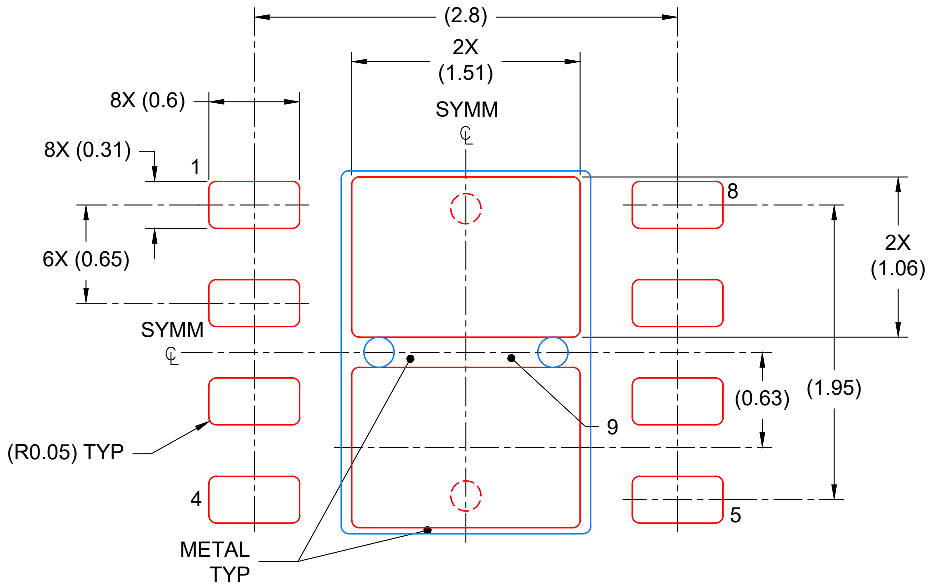
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



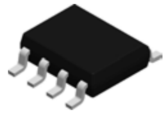
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

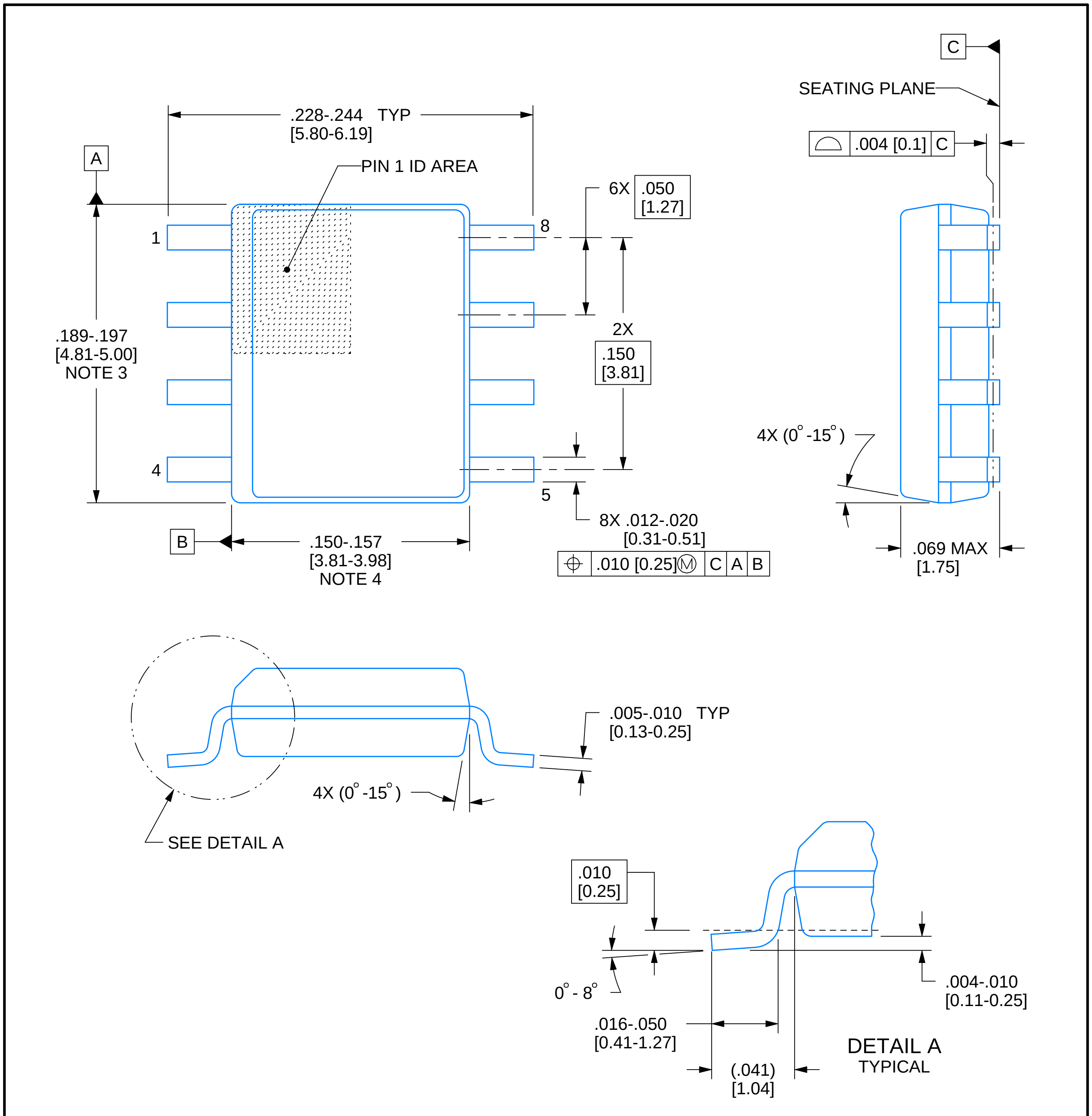


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

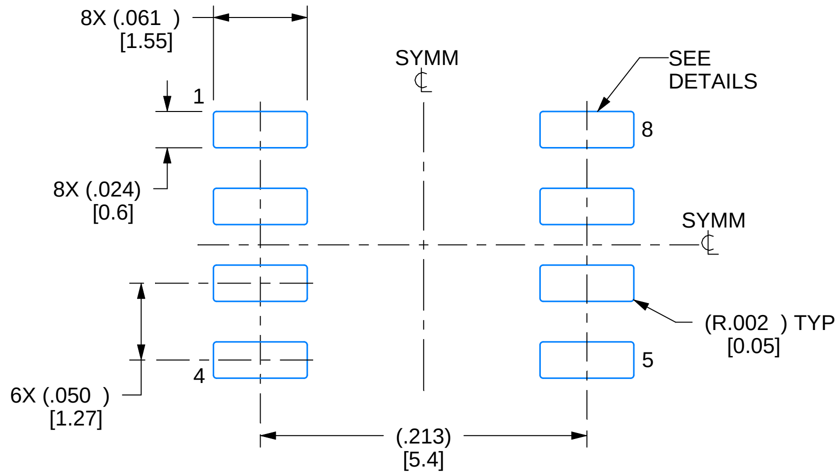
SMALL OUTLINE INTEGRATED CIRCUIT



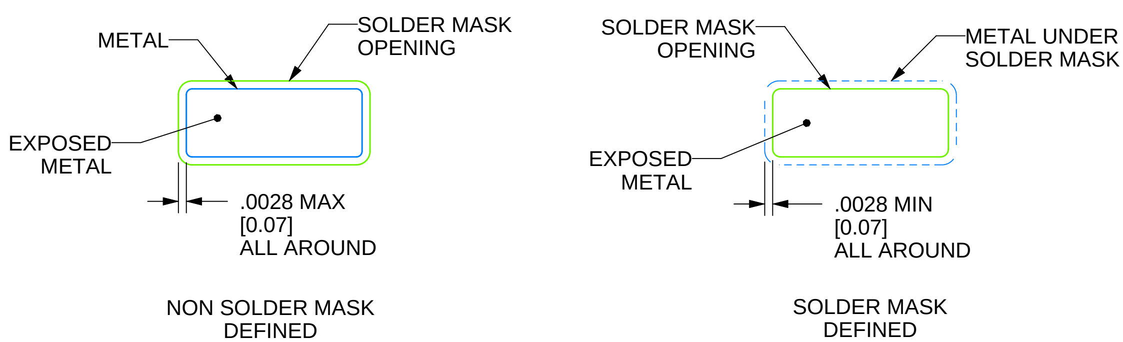
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

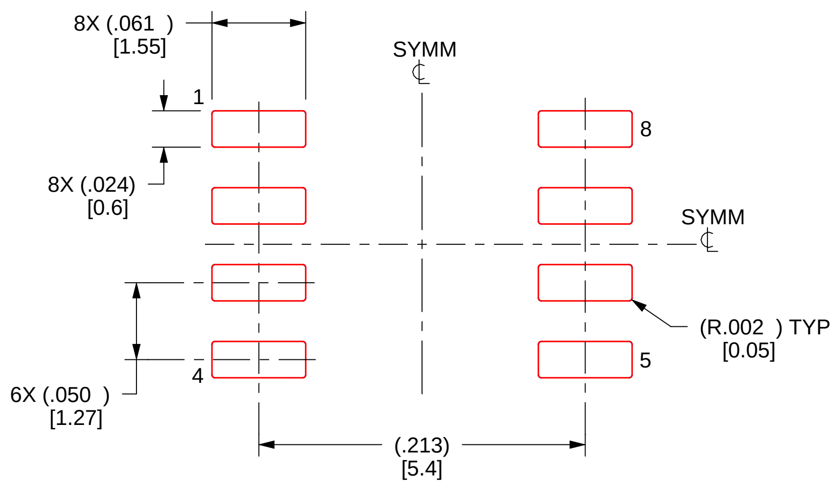


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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