参考資料

TCAN1057A-Q1 車載用、フォルト保護機能搭載、CAN FD トランシーバ

1 特長

- 車載アプリケーション用に AEC-Q100 (グレード 1) 認定済み
- ISO 11898-2:2016 物理層規格要件に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
  - 短く対称的な伝搬遅延時間によりタイミング マージンを強化
- TCAN1057AV の I/O 電圧範囲: 1.7V～5.5V
- 12V および 24V バッテリ アプリケーションをサポート
- レシーバの同相入力電圧:±12 V
- 保護機能:
  - バス フォルト保護:±58 V
  - 低電圧保護
  - TXD ドミナント タイムアウト (DTO)
    - 最小 9.2kbps のデータ レート
  - サーマル シャットダウン保護 (TSD)
- 動作モード:
  - 通常モード
  - サイレント モード
- 電源非接続時の最適化された挙動
  - バスおよびロジック ピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
  - ホットプラグ対応:バスおよび RXD 出力での電源オン/オフ時のグリッチ フリー動作
- 接合部温度範囲:-40℃～150℃
- SOIC (8)、小型フットプリント SOT23 (8)、自動光学検査 (AOI) 性能を向上させたリードレス VSON (8) パッケージで供給

2 アプリケーション

- 自動車および輸送システム
  - 車体制御モジュール
  - 車載ゲートウェイ
  - 先進運転支援システム (ADAS)
  - インフォテインメント

3 概要

TCAN1057A-Q1 は、ISO 11898-2:2016 高速 CAN (Controller Area Network) 仕様の物理層要件を満たす高速 CAN トランシーバです。

このトランシーバは、電磁両立性 (EMC) 認証済みであり、最高 5 メガビット/秒 (Mbps) の Classical CAN および CAN FD ネットワークに最適です。これらのデバイスを使用すると、シンプルなネットワークで最大 8Mbps の動作を実現できます。デバイスは、通常モードとサイレント モードという 2 つの動作モードをサポートしています。このトランシーバは、サーマル シャットダウン (TSD)、TXD ドミナント タイムアウト (DTO)、最高 ±58V のバス フォルト保護を含む多くの保護および診断機能も備えています。本デバイスには、電源電圧低下またはフローティング ピン発生時のフェイルセーフ動作が定義されています。

本トランシーバは V_{IO} ピンによるレベル シフト機能を内蔵しているため、トランシーバの I/O を 1.8V、2.5V、3.3V、5V のロジック レベルに直接接続できます。

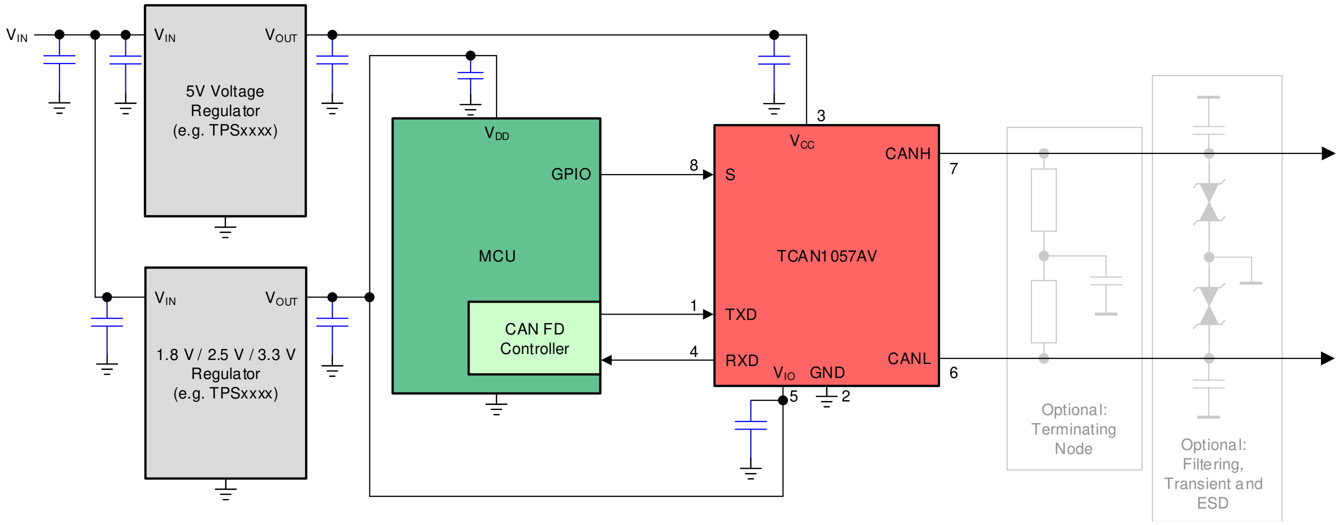
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TCAN1057A-Q1	SOT-23 (DDF) (8)	2.9 mm × 2.8mm
	VSON (DRB) (8)	3 mm × 3mm
	SOIC (D) (8)	4.9 mm × 6mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

表 3-1. デバイス比較表

デバイスの型番	ピン 5 で低電圧 I/O ロジックをサポート	ピン 8 でモード選択
TCAN1057A-Q1	なし	サイレント モード
TCAN1057AV-Q1	あり	サイレント モード


VIN
VIN
VOUT
5V Voltage Regulator (e.g. TPSxxxx)
VIN
VOUT
1.8 V / 2.5 V / 3.3 V Regulator (e.g. TPSxxxx)
VDD
GPIO
MCU
CAN FD Controller
3
VCC
CANH
7
8
S
TCAN1057AV
1
TXD
4
RXD
VIO
GND
CANL
6
5
2
Optional: Terminating Node
Optional: Filtering, Transient and ESD

概略回路図

Table of Contents

1 特長.......... 1
2 アプリケーション.......... 1
3 概要.......... 1
4 Pin Configuration and Functions.......... 4
5 Specifications.......... 5
  5.1 Absolute Maximum Ratings 5
  5.2 ESD Ratings 5
  5.3 ESD Ratings Table — IEC Specifications 5
  5.4 Recommended Operating Conditions 5
  5.5 Thermal Characteristics 6
  5.6 Supply Characteristics 6
  5.7 Dissipation Ratings 7
  5.8 Electrical Characteristics 7
  5.9 Switching Characteristics 9
6 Parameter Measurement Information.......... 11
7 Detailed Description.......... 14
  7.1 Overview.......... 14
  7.2 Functional Block Diagram.......... 15
  7.3 Feature Description.......... 15
  7.4 Device Functional Modes.......... 19
8 Application Information Disclaimer.......... 20
  8.1 Application Information.......... 20
  8.2 Typical Application.......... 20
  8.3 Power Supply Recommendations.......... 23
  8.4 Layout.......... 24
9 Device and Documentation Support.......... 25
  9.1 Documentation Support.......... 25
  9.2 ドキュメントの更新通知を受け取る方法.......... 25
  9.3 サポート・リソース.......... 25
  9.4 Trademarks.......... 25
  9.5 静電気放電に関する注意事項.......... 25
  9.6 用語集.......... 25
10 Revision History.......... 25
11 Mechanical, Packaging, and Orderable Information.......... 26

4 Pin Configuration and Functions

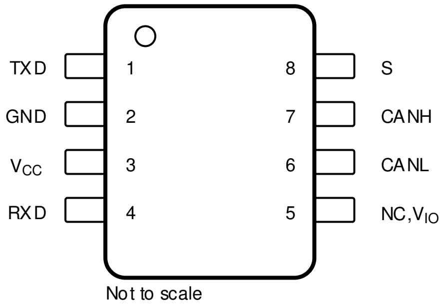


図 4-1. DDF Package, 8-Pin SOT (Top View)

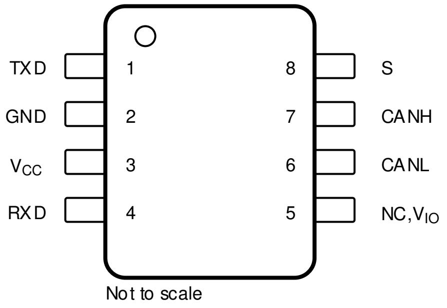


図 4-2. D Package, 8-Pin SOIC (Top View)

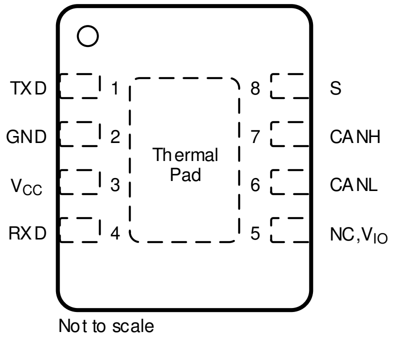


図 4-3. DRB Package, 8-Pin VSON (Top View)

表 4-1. Pin Functions

Pins		Type	Description
Name	**No.**		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
NC	5	—	No connect (not internally connected); devices without V_{IO}
V_{IO}		Supply	I/O supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
S	8	Digital Input	Silent mode control input, integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings Table — IEC Specifications

				VALUE	UNIT
V_{ESD}	System level Electrostatic discharge(1)	CAN bus terminals (CANH and CANL) to GND	Unpowered contact discharge per ISO10605 (1)	±8000	V
			SAE J2962-2 per ISO 10605 Powered Contact Discharge (2)	±8000	V
			SAE J2962-2 per ISO 10605 Powered Air Discharge (2)	±15000	V
V_{Tran}	Transient voltage per ISO 7637-2(3)		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Transient voltage per ISO 7637-3(4)		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers.

(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.

(3) Tested according to IEC 62228-3:2019 CAN Transceivers.

(4) Tested according to SAE J2962-2.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V

5.4 Recommended Operating Conditions (続き)

		MIN	NOM	MAX	UNIT
$I_{OH(RXD)}$	RXD terminal high-level output current, Devices with V_{IO}	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current, Devices with V_{IO}			1.5	mA
$I_{OH(RXD)}$	RXD terminal high-level output current, Devices without V_{IO}	–2			mA
$I_{OL(RXD)}$	RXD terminal low-level output current, Devices without V_{IO}			2	mA
T_J	Operating junction temperature	-40		150	℃

5.5 Thermal Characteristics

THERMAL METRIC[1]		TCAN1057Ax-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.5	122	55.2	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	63	62.4	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	42.4	27.5	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	19.3	2.4	2.3	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	70.2	42.2	27.4	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	--	11.5	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Supply Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	TXD = 0 V, S = 0 V, R_L = 60 Ω, C_L = open; See 図 6-1		45	70	mA
			TXD = 0 V, S = 0 V, R_L = 50 Ω, C_L = open; See 図 6-1		49	80	mA
		Recessive	TXD = V_{CC} or V_{IO}, S = 0 V, R_L = 50 Ω, C_L = open; See 図 6-1		4.5	7.5	mA
		Dominant with bus fault	TXD = 0 V, S = 0 V, CANH = CANL = ±25 V, R_L = open, C_L = open; See 図 6-1			130	mA
	Supply current Silent mode		TXD = S = V_{CC} or V_{IO}, R_L = 50 Ω, C_L = open; See 図 6-1			2.1	mA
I_{IO}	I/O supply current Normal mode, Devices with V_{IO}	Dominant	S = 0 V, TXD = 0 V RXD floating		125	300	μA
		Recessive	TXD = V_{IO} , S = 0 V RXD floating		25	48	μA
UV_{CC}	Rising undervoltage detection on V_{CC} for protected mode				4.2	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.5	4	4.25	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				200		mV
UV_{VIO}	Rising undervoltage detection on V_{IO} (Devices with V_{IO})				1.56	1.65	V
	Falling undervoltage detection on V_{IO} (Devices with V_{IO})			1.4	1.51	1.59	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				40		mV

5.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_A= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_A= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 5 V, T_A= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
T_{TSD}	Thermal shutdown temperature		175	195	210	°C
$T_{TSD(HYS)}$	Thermal shutdown hysteresis			12		

5.8 Electrical Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	S = 0 V, TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open; See 図 6-2	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal or silent mode	CANH and CANL	S = 0 V, TXD = V_{IO} R_L = open (no load), R_{CM} = open See 図 6-2	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		S = 0 V, TXD = 250 kHz, 1 MHz, 2.5 MHz R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_{CM} = open; See 図 6-2 and 図 8-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		S = 0 V R_L = 60 Ω, C_L = open; See 図 6-2	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	S = 0 V, TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open; See 図 6-2	1.5		3	V
			S = 0 V, TXD = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open; See 図 6-2	1.4		3.3	V
			S = 0 V, TXD = 0 V R_L = 2240 Ω, C_L = open; See 図 6-2	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	S = 0 V, TXD = V_{IO} R_L = 60 Ω, C_L = open; See 図 6-2	–120		12	mV
			S = 0 V, TXD = V_{IO} R_L = open, C_L = open; See 図 6-2	–50		50	mV
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		S = 0 V, TXD = 0 V $V_{(CANH)}$ = -15 V to 40 V, CANL = open; See 図 6-7	–115			mA
			S = 0 V, TXD = 0 V $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open; See 図 6-7			115	mA

5.8 Electrical Characteristics (続き)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode	S = 0 V, TXD = V_{IO} –27 V ≤ V_{BUS} ≤ 32 V, where V_{BUS} = CANH = CANL; See 図 6-7	–5		5	mA
Receiver Electrical Characteristics						
V_{IT}	Input threshold voltage Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 図 6-3 and 表 7-6	500		900	mV
V_{DOM}	Dominant state differential input voltage range Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 図 6-3 and 表 7-6	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 図 6-3 and 表 7-6	-4		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 図 6-3 and 表 7-6		115		mV
V_{CM}	Common-mode range Normal and silent mode	See 図 6-3 and 表 7-6	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	μA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO} (1)			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	TXD = V_{IO} (1), S = 0 V, -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single-ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0 V V_{CC}= V_{IO} = 5.5 V	–200	-100	–20	μA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V V_{CC}= V_{IO} = 0 V	–1	0	1	μA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –2 mA Devices without V_{IO}; See 図 6-3	0.8 V_{CC}			V
V_{OH}	High-level output voltage	I_O = –1.5 mA Devices with V_{IO}; See 図 6-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 2mA Devices without V_{IO}; See 図 6-3			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 1.5mA Devices with V_{IO}; See 図 6-3			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V V_{CC} = V_{IO} = 0 V	–1	0	1	μA
S Terminal (Silent Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V

5.8 Electrical Characteristics (続き)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input leakage current	$V_{CC} = V_{IO}$ = S = 5.5 V	–2		2	μA
I_{IL}	Low-level input leakage current	S = 0 V $V_{CC} = V_{IO}$ = 5.5 V,	–20		–2	μA
$I_{LKG(OFF)}$	Unpowered leakage current	S = 5.5V $V_{CC} = V_{IO}$ = 0 V	–1	0	1	μA

(1) $V_{IO} = V_{CC}$ in non-V variants of device

5.9 Switching Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	S = 0 V, V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 図 6-4		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	S = 0 V, V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 図 6-4		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	S = 0 V, V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 図 6-4		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	S = 0 V, V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 図 6-4		180	255	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See 図 6-5			20	μs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	S = 0 V R_L = 60 Ω, C_L = 100 pF; See 図 6-2		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			14		ns
t_R	Differential output signal rise time			25		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout	S = 0 V R_L = 60 Ω, C_L = 100 pF; See 図 6-6	1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	S = 0 V $C_{L(RXD)}$ = 15 pF; See 図 6-3		81		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			66		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						

5.9 Switching Characteristics (続き)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500 ns	S = 0 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$; See 図 6-4	450		525	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200 ns		160		205	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 125 ns(1)		85		130	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500 ns		410		540	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200 ns		130		210	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 125 ns(1)		75		135	ns
Δt_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500 ns		-50		20	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 200 ns		-40		10	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 125 ns(1)		-40		10	ns

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

6 Parameter Measurement Information

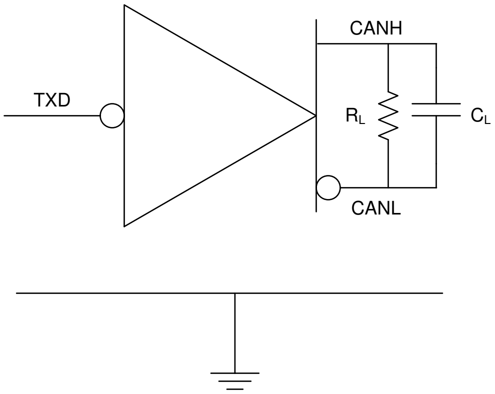


図 6-1. I_{CC} Test Circuit

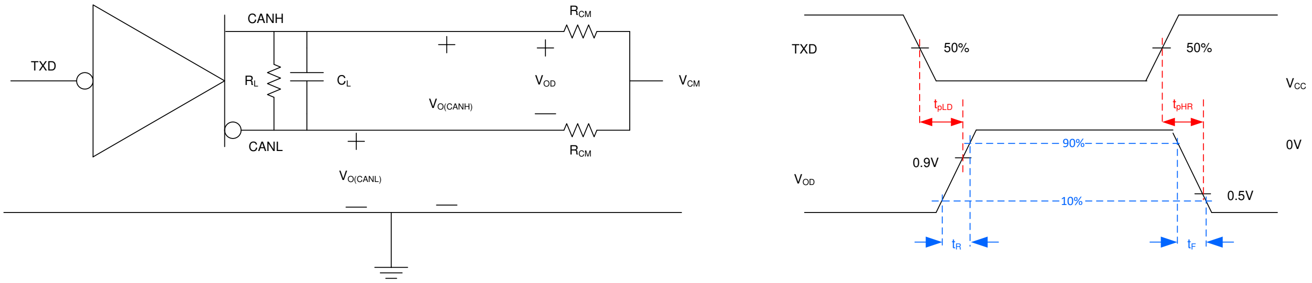


図 6-2. Driver Test Circuit and Measurement

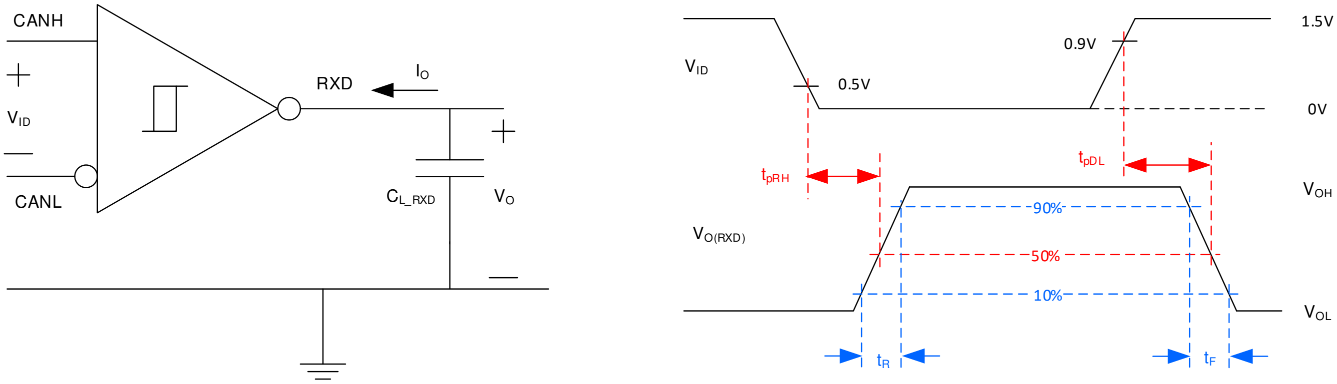


図 6-3. Receiver Test Circuit and Measurement

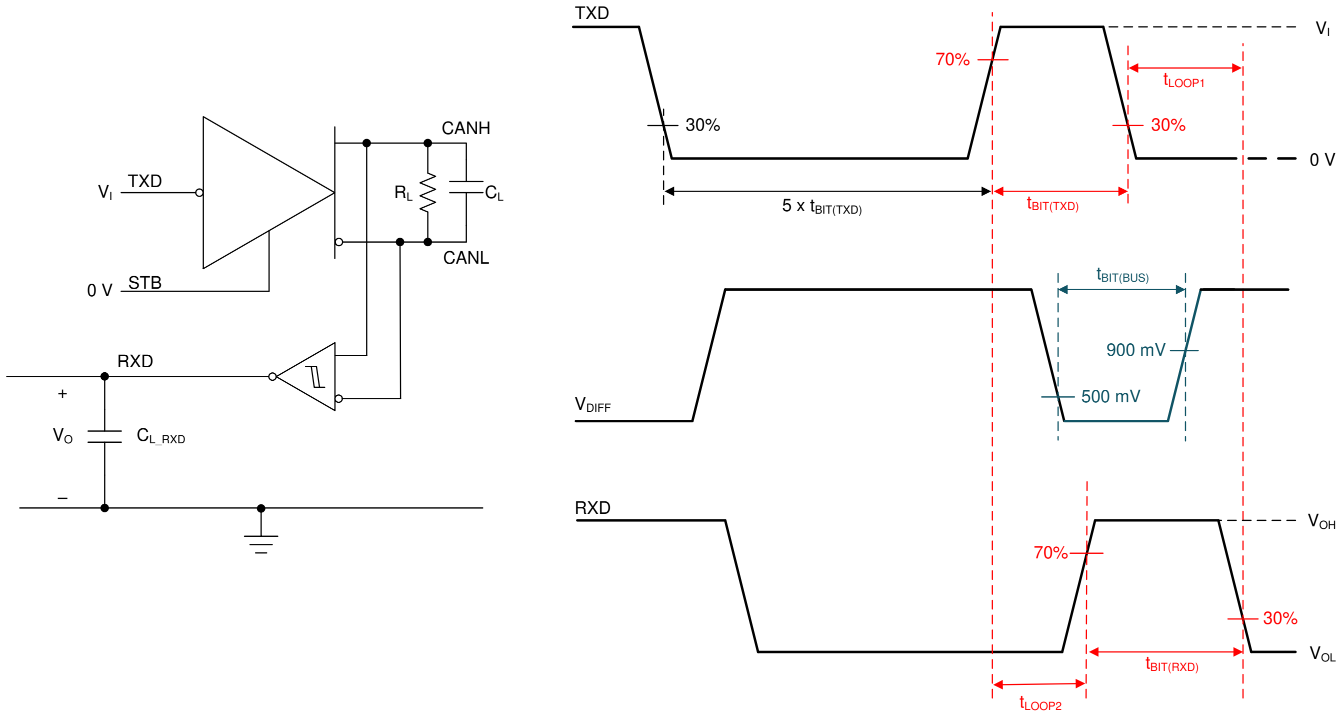


図 6-4. Transmitter and Receiver Timing Test Circuit and Measurement

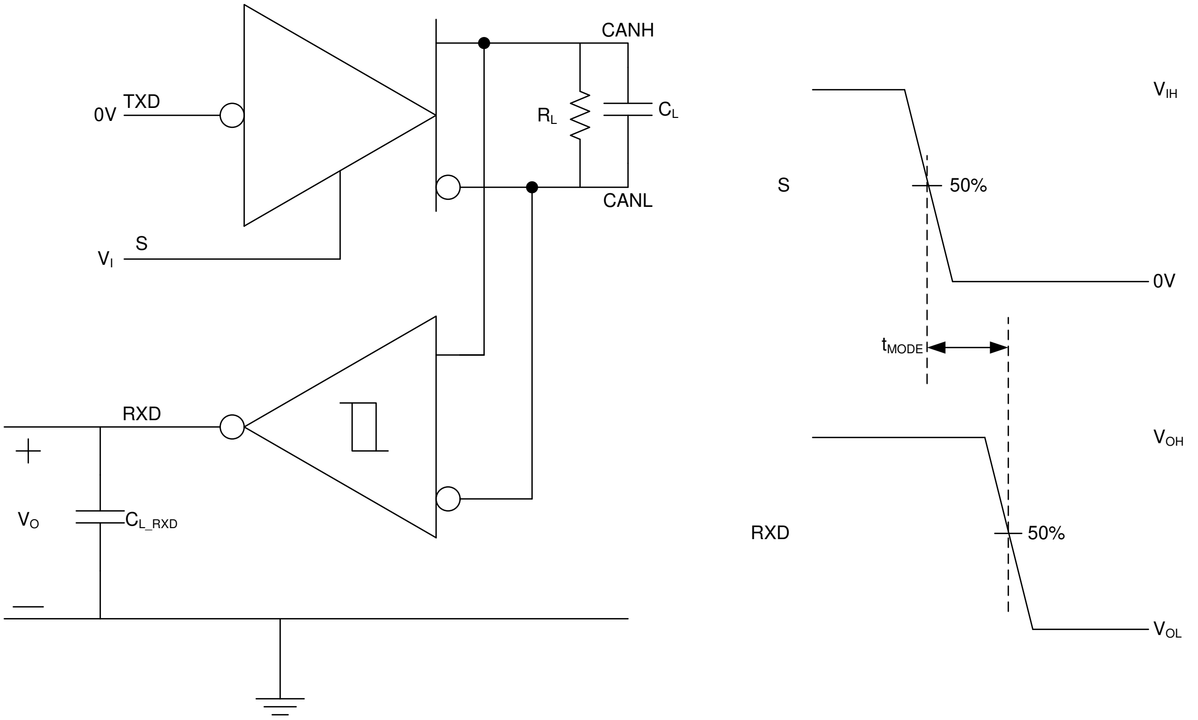


図 6-5. t_{MODE} Test Circuit and Measurement

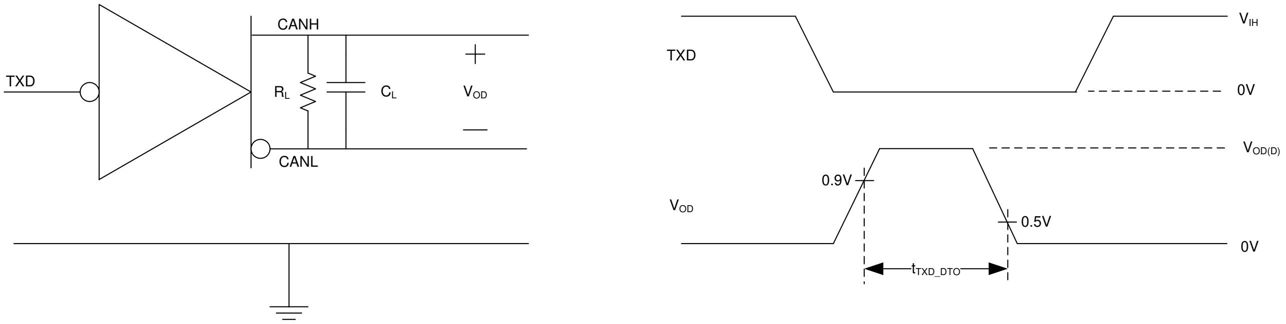


図 6-6. TXD Dominant Timeout Test Circuit and Measurement

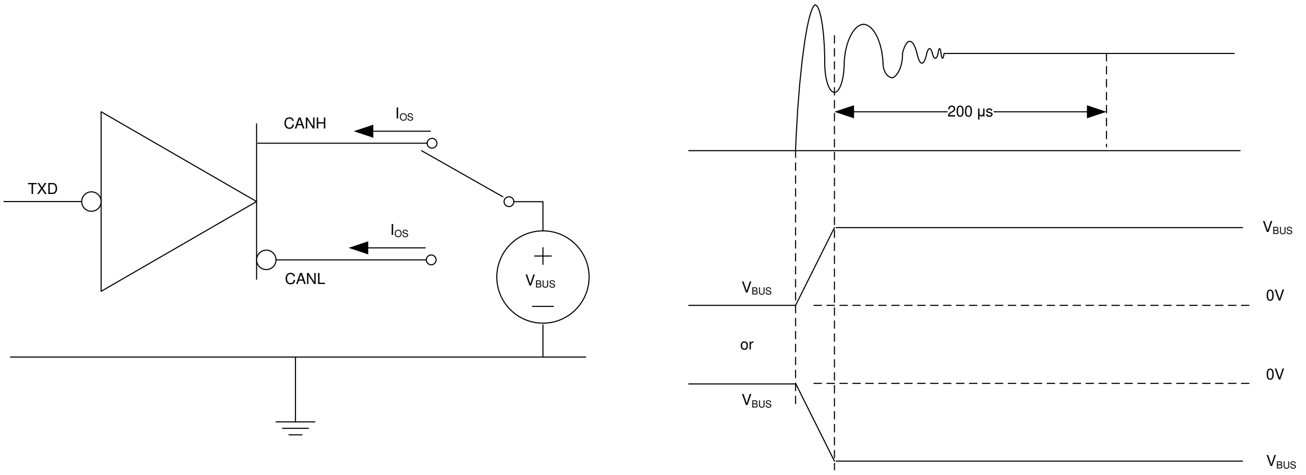


図 6-7. Driver Short-Circuit Current Test and Measurement

7 Detailed Description

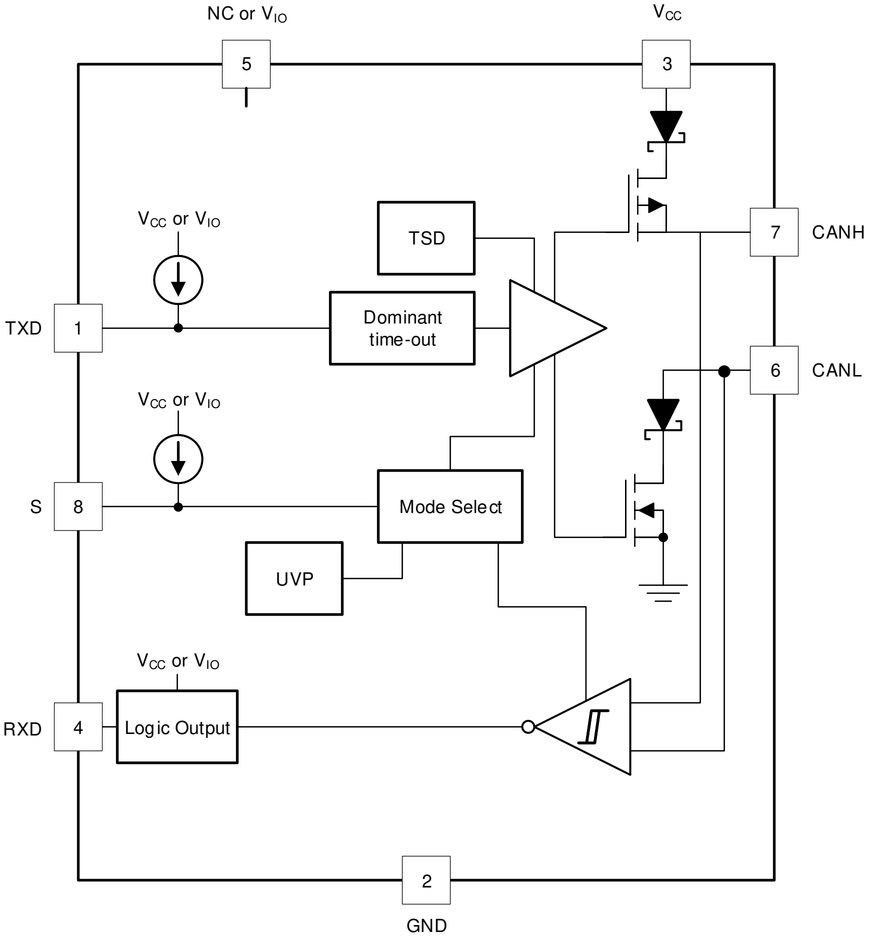
7.1 Overview

The TCAN1057A(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features for the stringent automotive system requirements while also supporting CAN FD data rates up to 8Mbps.

The devices support the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance Test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the transceivers.

7.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5-V power supply to the CAN transceiver.

7.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either V_{CC} or V_{IO} , from the transceivers to the CAN controller. RXD is only driven once V_{IO} is present.

7.3.1.5 V_{IO}

The V_{IO} pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. The V_{IO} pin should be connected to the controller's I/O voltage source.

7.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

7.3.1.7 S (Silent)

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation than the S pin can be tied directly to system GND using a pull-down resistor. If silent mode is the only intended mode of operation than the S pin can be tied directly to a static system voltage source using a pull-up resistor.

7.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 図 7-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

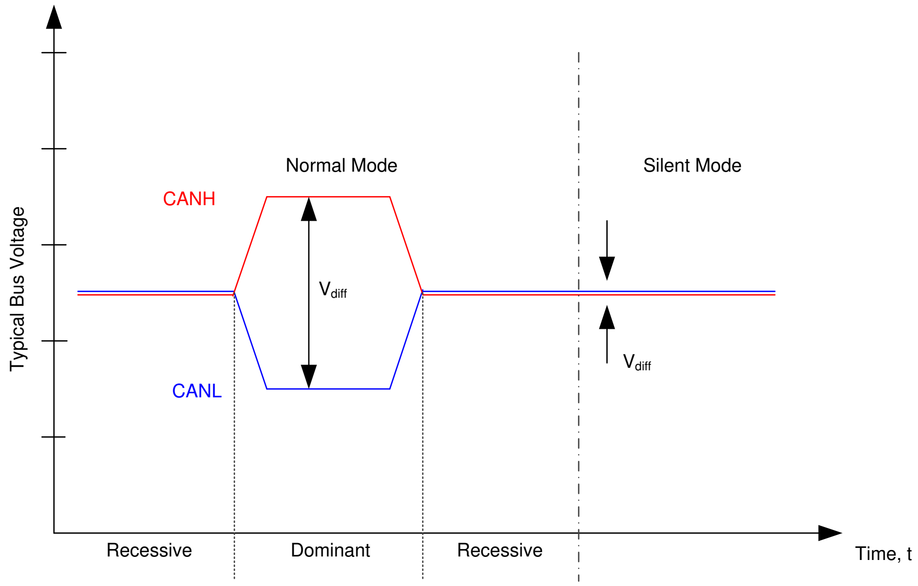


図 7-1. Bus States

7.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

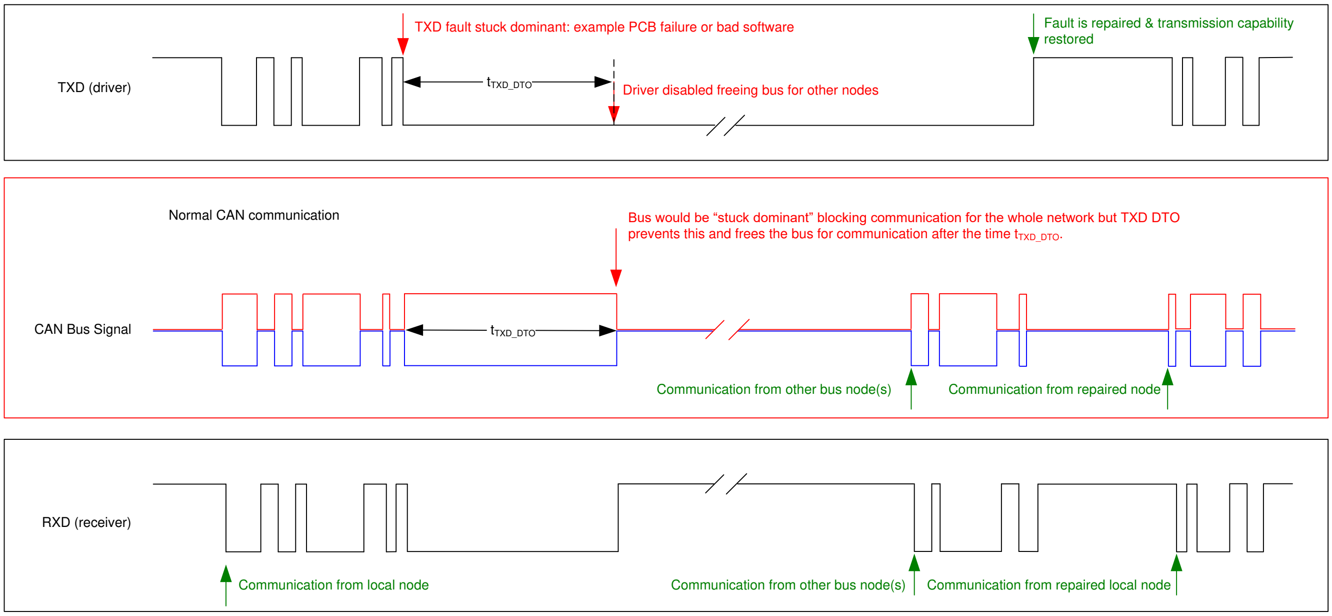


図 7-2. Example Timing Diagram for TXD Dominant Timeout

7.3.4 CAN Bus short-circuit current limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

7.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 7-1. Undervoltage Lockout - TCAN1057A-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance Weak pull-down to ground(1)	High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

表 7-2. V_{IO} Undervoltage Lockout - TCAN1057AV-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	S = V_{IO}: Silent mode	High impedance Weak pull-down to ground(1)	Recessive
		S = GND: Protected mode		
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and t_{MODE} has expired the device transitions to normal mode and the host controller can send and receive CAN traffic again.

7.3.7 Unpowered Device

The device is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the pins do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so the pins do not load other circuits which may remain powered.

7.3.8 Floating pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See 表 7-3 for details on pin bias conditions.

表 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
S	Pull-up	Weakly biases S towards low-power silent mode to prevent excessive system power

7.4 Device Functional Modes

7.4.1 Operating Modes

The device has two main operating modes; normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

表 7-4. Operating Modes

S	Device Mode	Driver	Receiver	RXD Pin
High	Silent mode	Disabled	Enabled	Mirrors bus state
Low	Normal Mode	Enabled	Enabled	

7.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

7.4.3 Silent Mode

In silent mode the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN1057A(V)-Q1 is reduced in silent mode due to the CAN driver being disabled.

7.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to either V_{CC} or V_{IO}.

表 7-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Silent	X	High impedance	High impedance	Biased recessive

(1) X = irrelevant
(2) For bus state see 図 7-1

表 7-6. Receiver Function Table Normal and Silent Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal or Silent	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Any	Open ($V_{ID} \approx 0V$)	Open	High

8 Application Information Disclaimer

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.2 Typical Application

図 8-1 shows a typical configuration for 5V system using the device. The bus termination is shown for illustrative purposes.

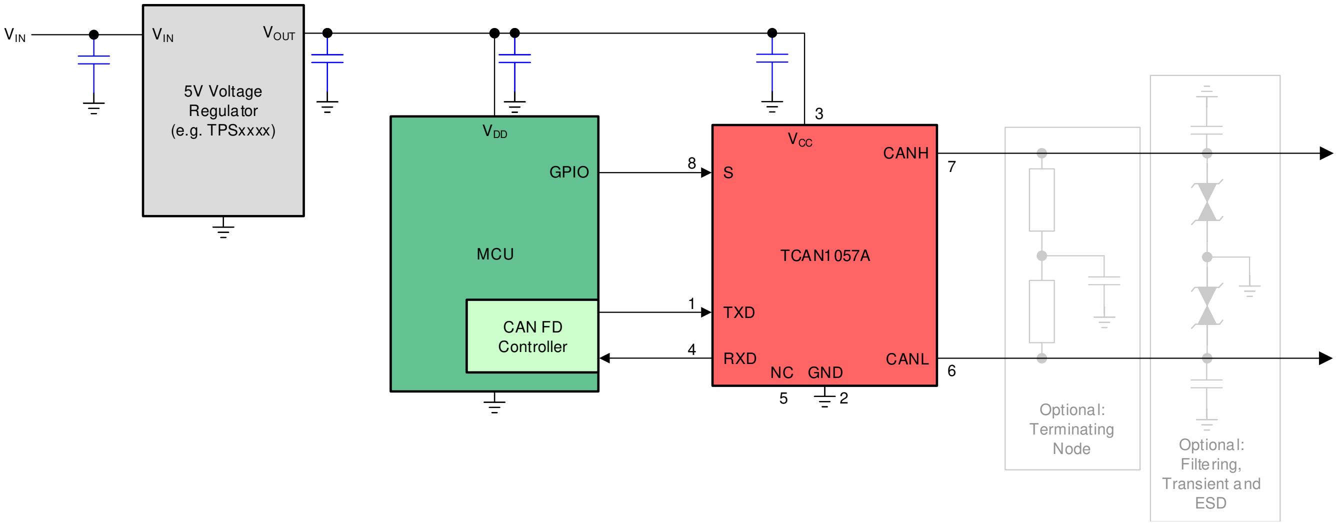


図 8-1. Transceiver Application Using 5V I/O Connections

8.2.1 Design Requirements

8.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see 図 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

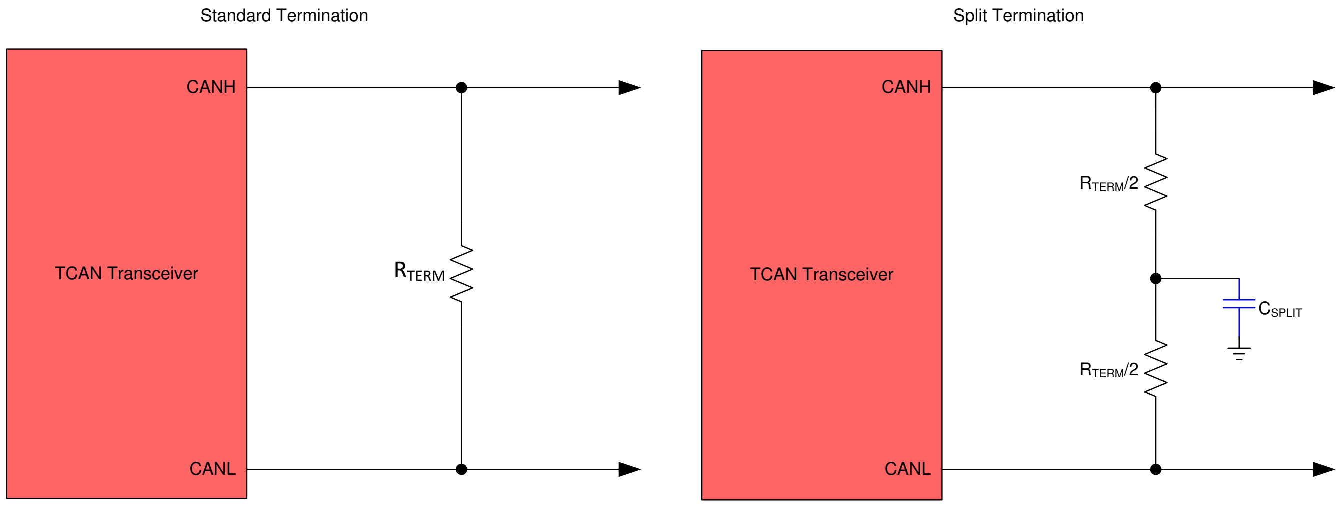


図 8-2. CAN Bus Termination Concepts

8.2.2 Detailed Design Procedures

8.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1057A(V)-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1057A(V)-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the transceiver is a minimum of 40kΩ. If 100 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN1057A(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity. Thus, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design for robust network operation.

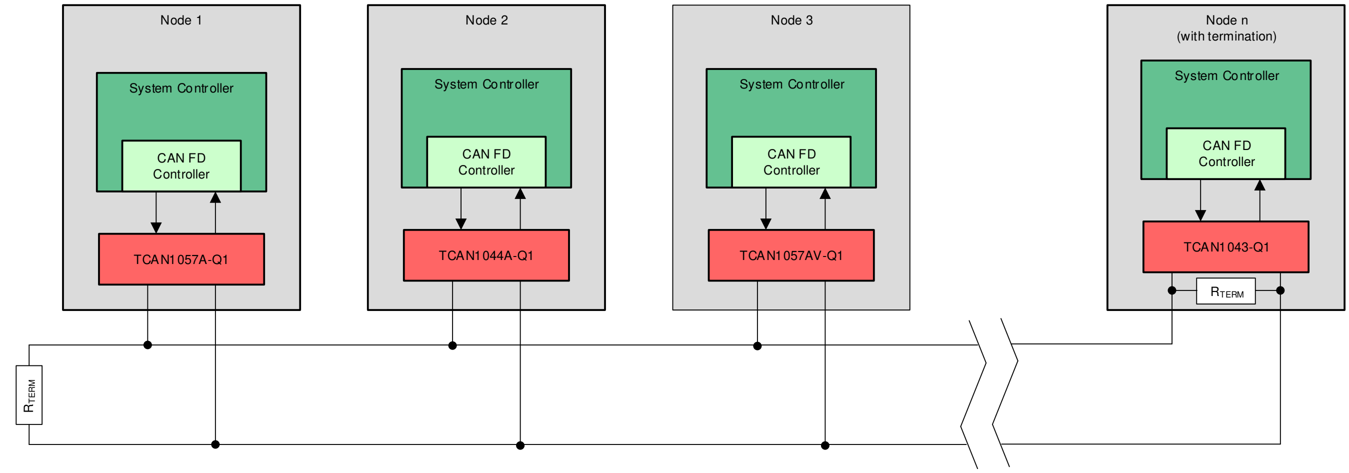
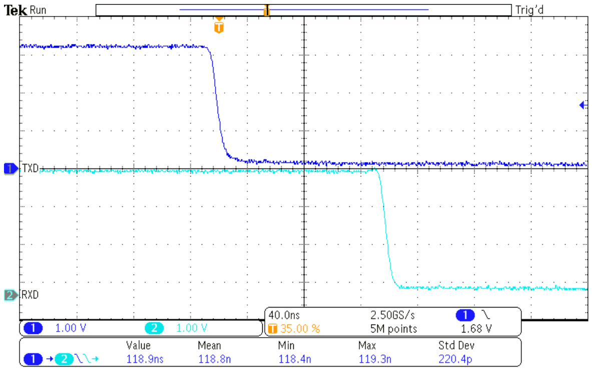


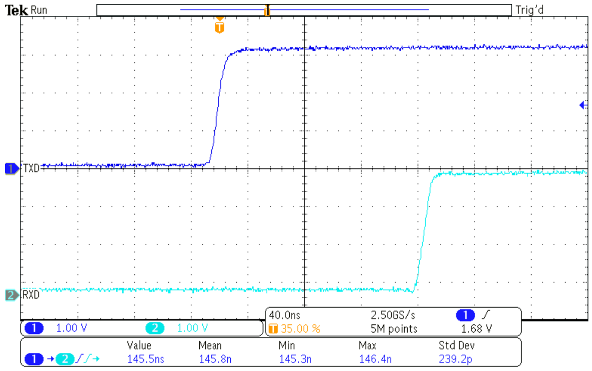
図 8-3. Typical CAN Bus

8.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 8-4. $t_{PROP(LOOP1)}$



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 8-5. $t_{PROP(LOOP2)}$

8.2.4 System Examples

図 8-6 shows a typical configuration for 1.8V, 2.5V, or 3.3V systems using the TCAN1057AV. The bus termination is shown for illustrative purposes.

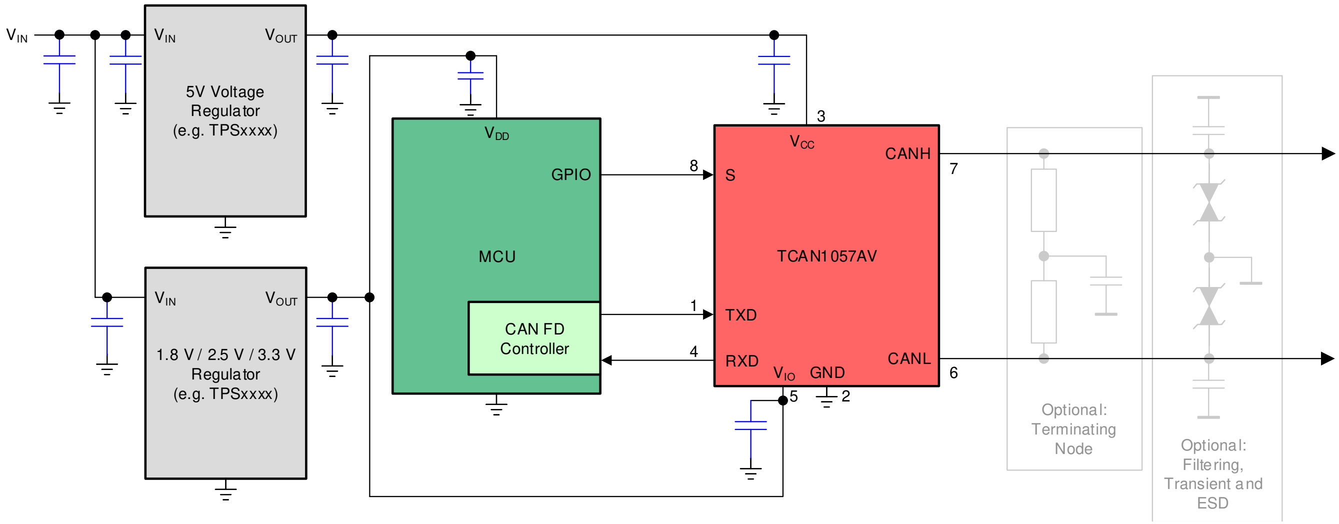


図 8-6. Typical Transceiver Application Using 1.8V, 2.5V, 3.3V IO Connections

8.3 Power Supply Recommendations

The TCAN1057A transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TCAN1057AV implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.7V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, should be placed near the CAN transceiver's main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

8.4 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

8.4.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter 0.1µF capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling 0.1µF capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

注

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two 60Ω resistors, R4 and R5, with the center or split tap of the termination connected to ground via a 1-100nF capacitor C3. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and 式 2 for information on termination concepts and power ratings needed for the termination resistor(s).

8.4.2 Layout Example

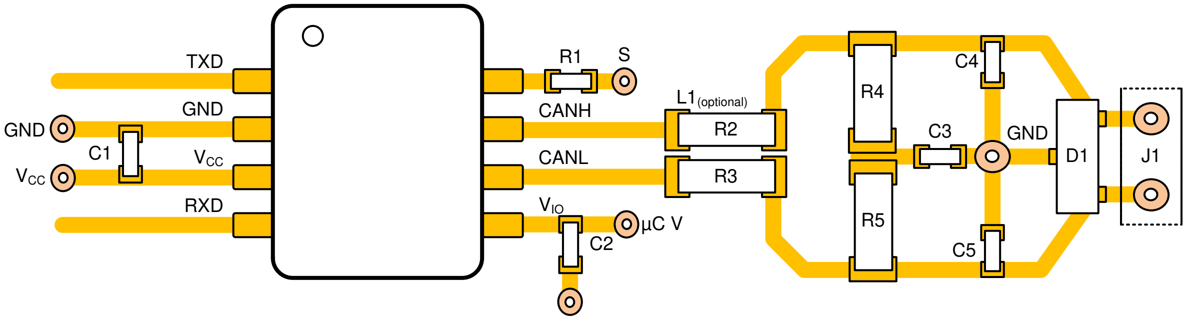


図 8-7. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (November 2021) to Revision C (October 2024) **Page**

- データシートのタイトルとヘッダー情報から部品番号 TCAN1057AV-Q1 を削除。 1
- 「製品情報」表を「パッケージ情報」表に変更 1

Changes from Revision A (May 2021) to Revision B (November 2021) **Page**

- 「製品情報」表の DFF および D パッケージから製品プレビューを削除 1

Changes from Revision * (February 2021) to Revision A (May 2021) **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1057ADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HEF
TCAN1057ADDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HEF
TCAN1057ADRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057A
TCAN1057ADRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057A
TCAN1057ADRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057A
TCAN1057ADRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057A
TCAN1057AVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HFF
TCAN1057AVDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HFF
TCAN1057AVDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057AV
TCAN1057AVDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1057AV
TCAN1057AVDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057AV
TCAN1057AVDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1057AV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

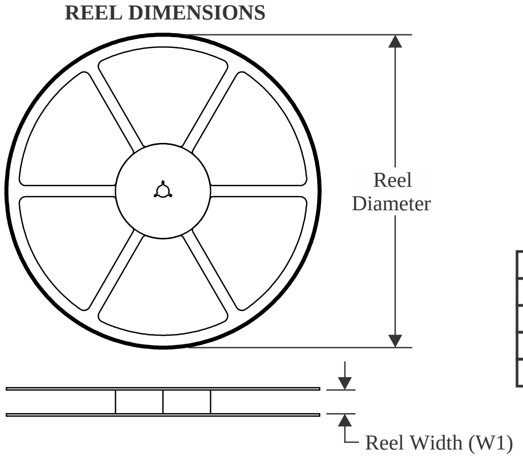
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

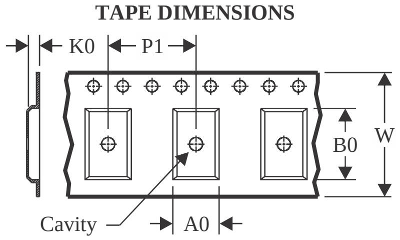
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

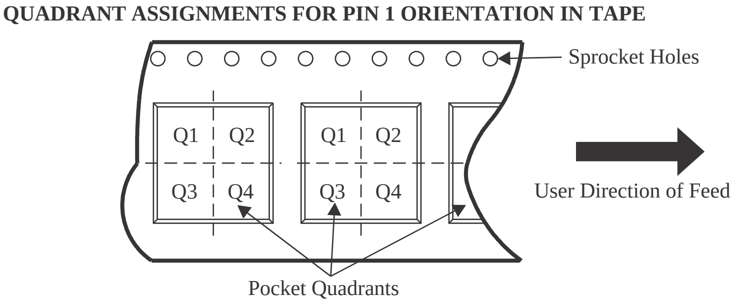
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





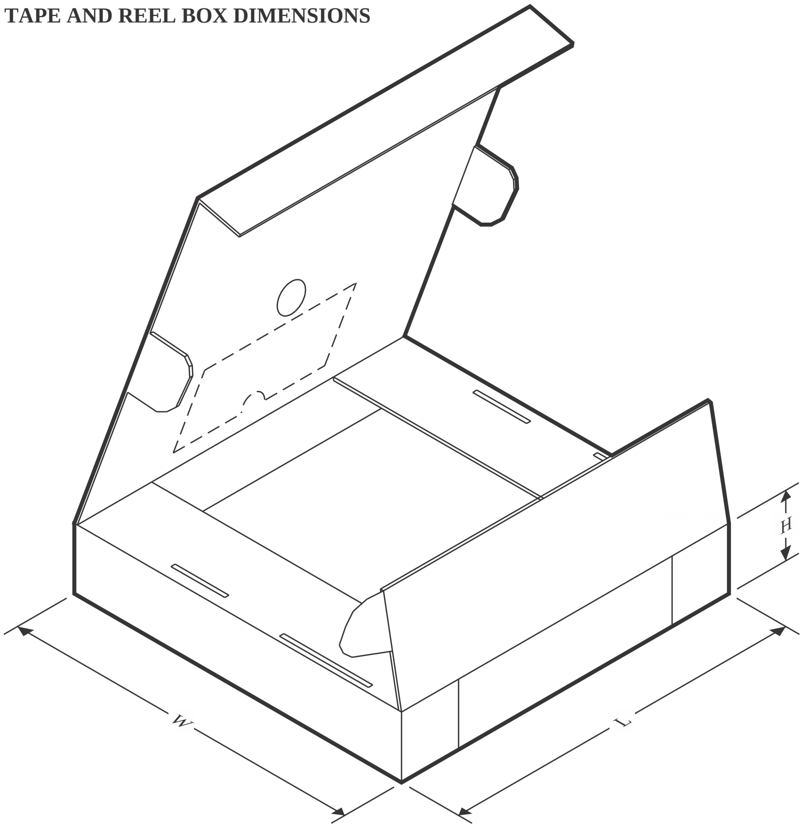
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

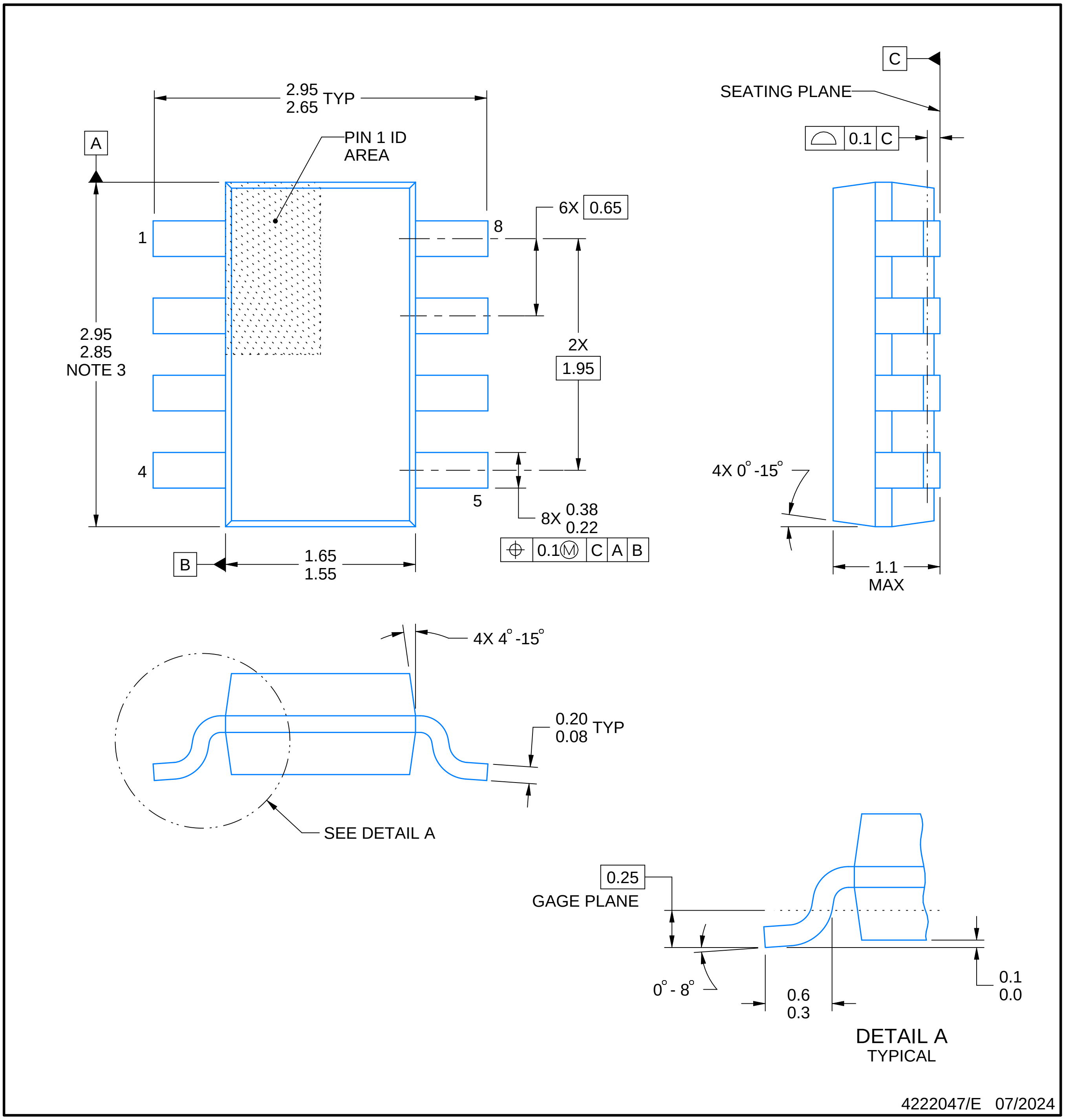
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1057ADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1057ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1057ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1057ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1057AVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1057AVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1057AVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1057AVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

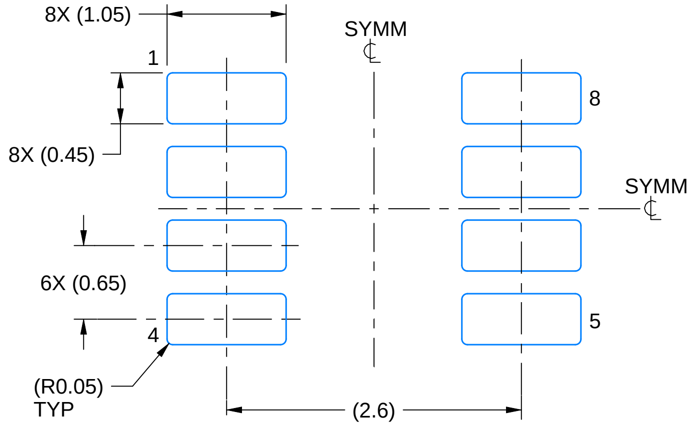
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1057ADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1057ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1057ADRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1057ADRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TCAN1057AVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1057AVDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1057AVDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TCAN1057AVDRQ1	SOIC	D	8	2500	356.0	356.0	35.0



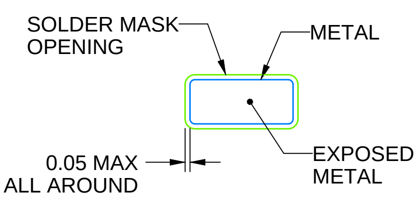
4222047/E 07/2024

NOTES:

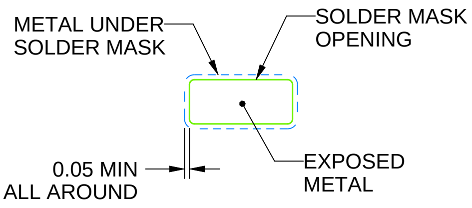
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

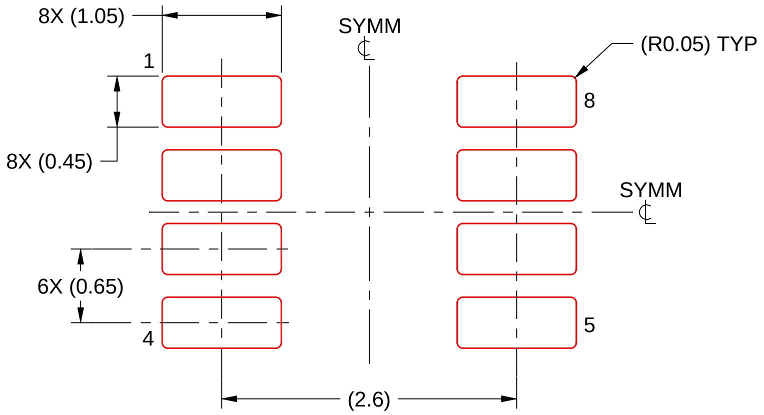


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

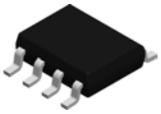


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

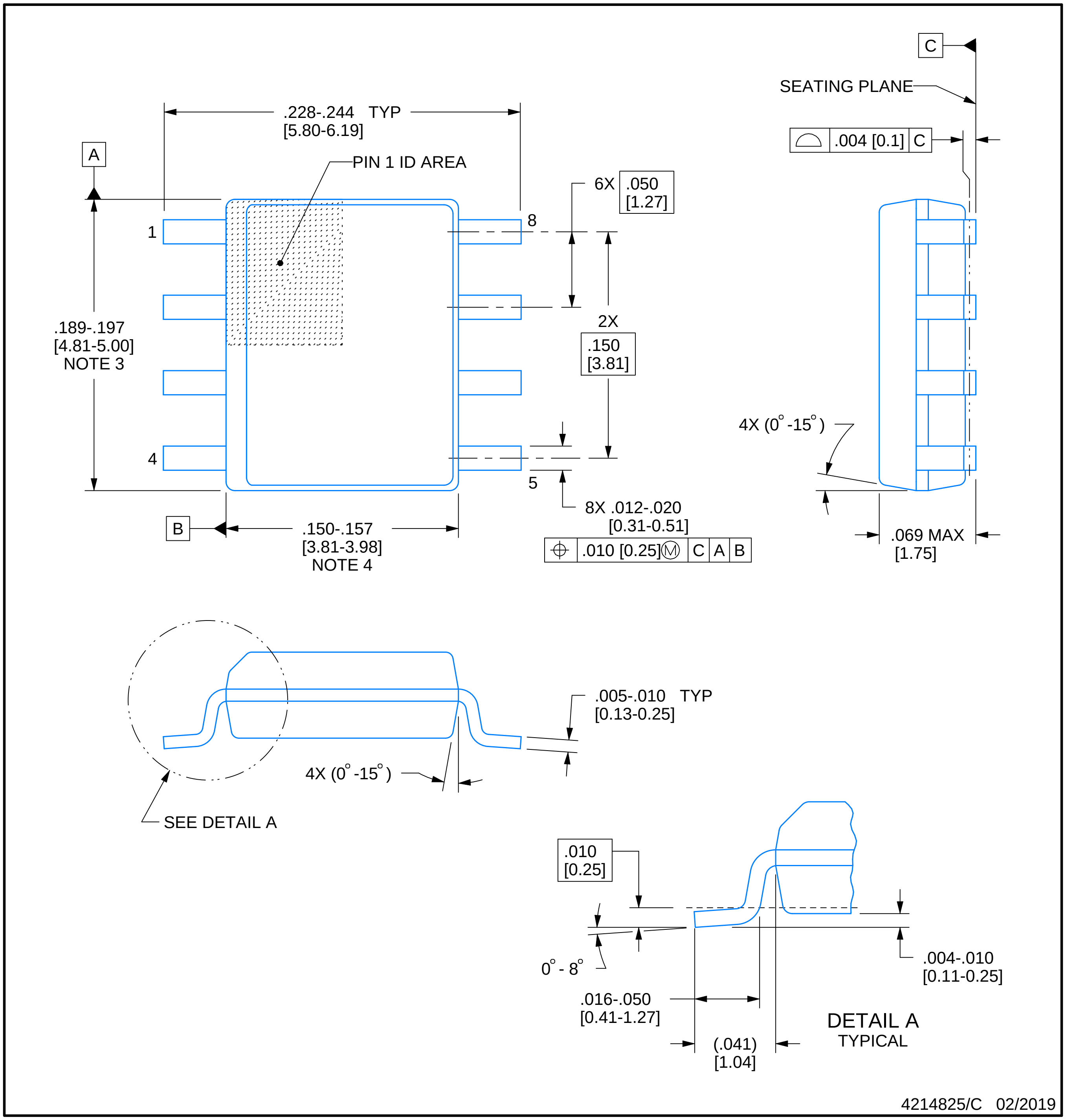


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

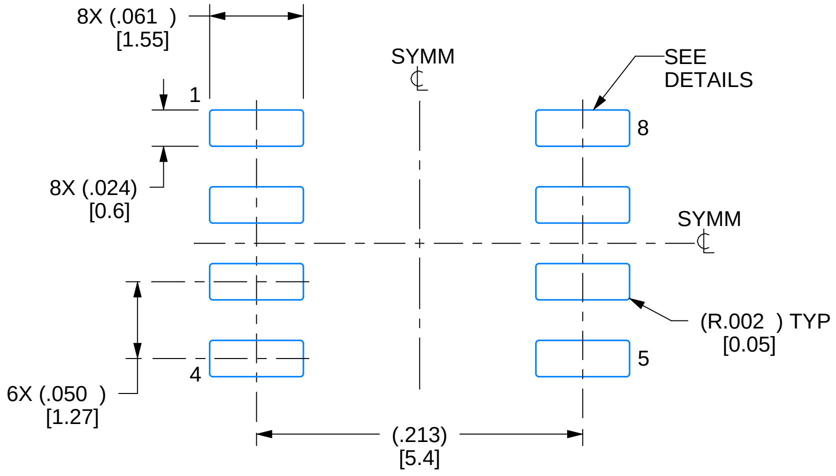
SMALL OUTLINE INTEGRATED CIRCUIT



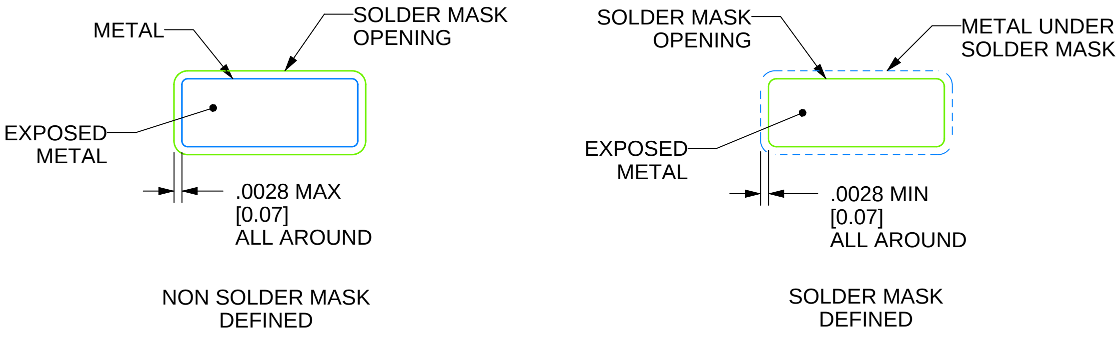
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



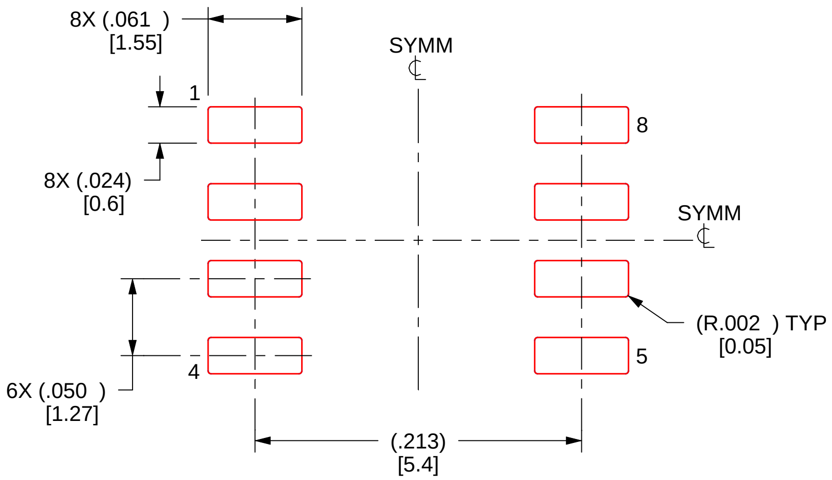
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

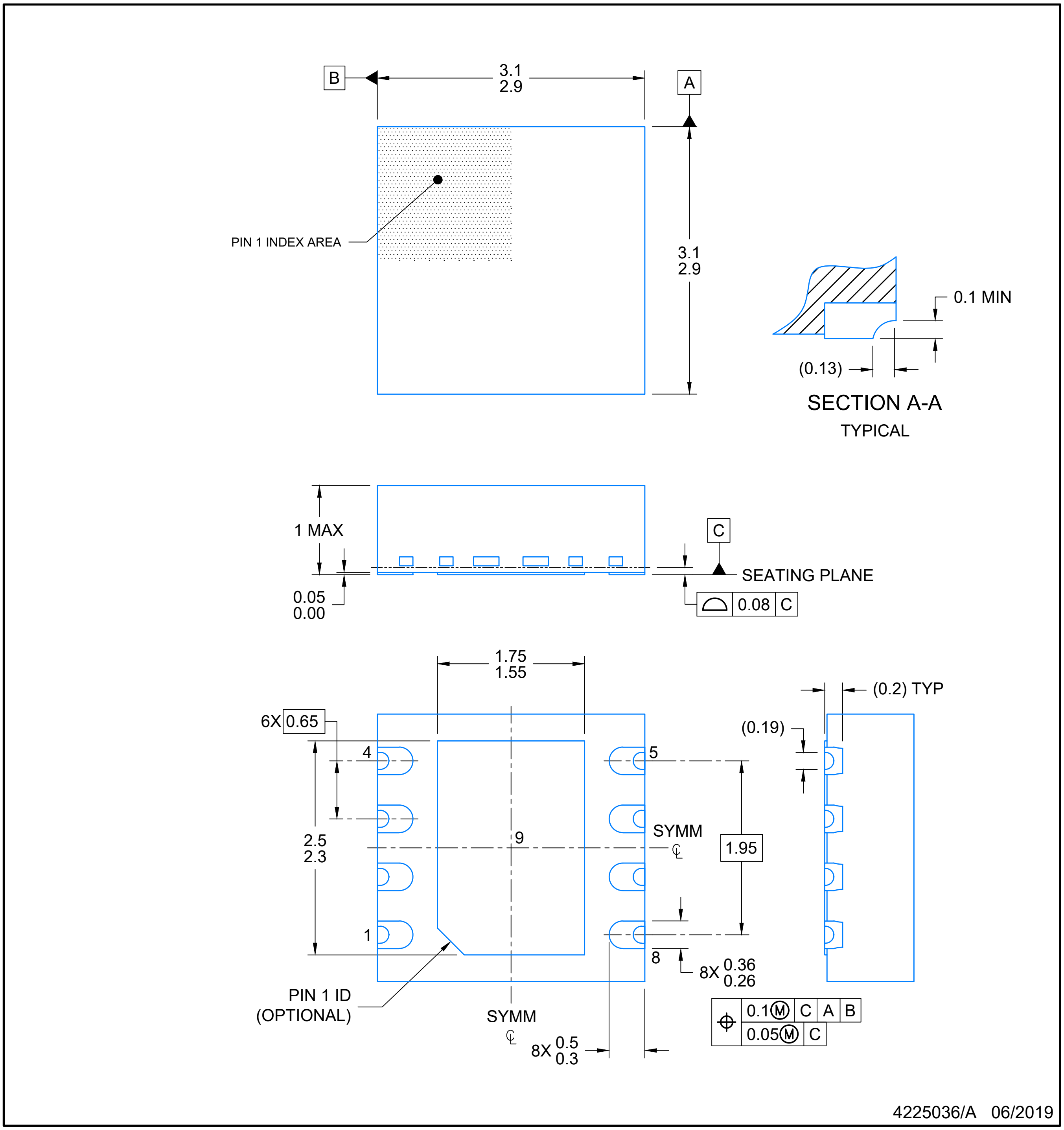
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

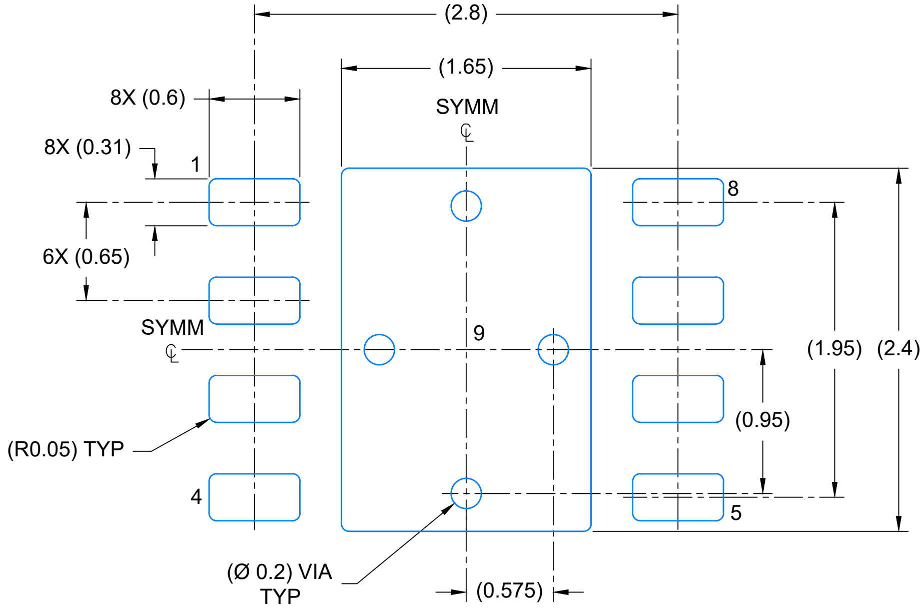
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



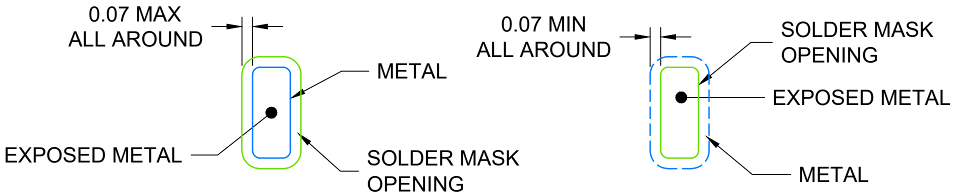
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

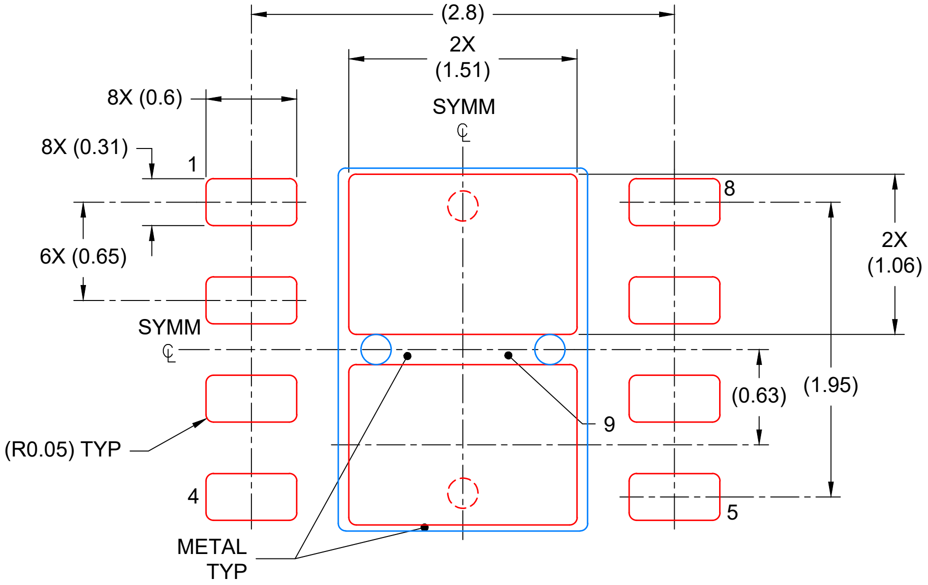
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス･インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス･インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス･インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス･インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス･インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス･インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス･インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス･インスツルメンツは一切の責任を拒否します。

テキサス･インスツルメンツの製品は、 テキサス･インスツルメンツの販売条件、または ti.com やかかる テキサス･インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス･インスツルメンツがこれらのリソースを提供することは、適用される テキサス･インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス･インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265