

TCAN1044-Q1 車載用、フォルト保護機能搭載、1.8V I/O 対応、CAN FD トランシーバ

1 特長

- AEC-Q100: 車載アプリケーション認定済み
 - 温度グレード 1: -40°C ~ 125°C T_A
- ISO 11898-2:2016 および ISO 11898-5:2007 物理層規格の要件に適合
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
 - 短く対称的な伝搬遅延時間によりタイミング マージンを強化
 - 負荷のある CAN ネットワークでより高いデータレートを実現
- I/O 電圧範囲: 1.7 V ~ 5.5 V
 - 1.8V、2.5V、3.3V、5V アプリケーションをサポート
- 保護機能:
 - バスフォルト保護: ±58 V
 - 低電圧保護
 - TXD ドミナント タイムアウト (DTO)
 - 最小 9.2kbps のデータレート
 - サーマル シャットダウン保護 (TSD)
- 動作モード:
 - 通常モード
 - リモート ウェイクアップ要求をサポートする、低消費電力スタンバイ モード
- 電源非接続時の最適化された挙動
 - バスおよびロジックピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
 - ホットプラグ対応: バスおよび RXD 出力での電源オン/オフ時のグリッチ フリー動作
- 接合部温度範囲: -40°C ~ 150°C
- レシーバの同相入力電圧: ±12 V

- SOIC (8)、SOT23 (8) パッケージ、自動光学検査 (AOI) 性能を向上させたリードレス VSON (8) パッケージで供給

2 アプリケーション

- 車両および輸送システム
 - 車体制御モジュール
 - 車載ゲートウェイ
 - 先進運転支援システム (ADAS)
 - インフォテインメント

3 概要

TCAN1044-Q1 は、ISO 11898-2:2016 高速 CAN (Controller Area Network) 仕様の物理層要件を満たす高速 CAN トランシーバです。

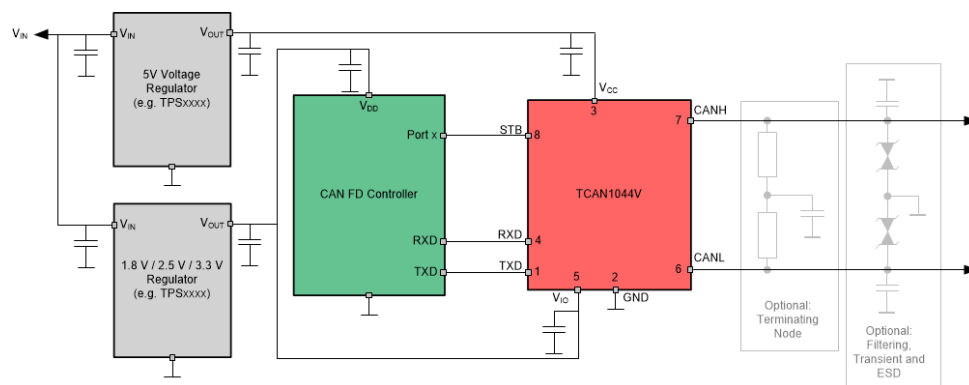
TCAN1044-Q1 トランシーバは Classical CAN ネットワークおよび最高 8 メガビット/秒 (Mbps) の CAN FD ネットワークの両方に対応しています。TCAN1044V-Q1 は V_{IO} ピンによるロジックレベル変換機能を備えているため、トランシーバの I/O を 1.8V、2.5V、3.3V、5V のロジックレベルに直接接続できます。このトランシーバは低消費電力スタンバイ モードと、ISO 11898-2:2016 に定義されたウェイクアップ パターン (WUP) に準拠した「CAN によるウェイク」をサポートしています。TCAN1044-Q1 トランシーバは、サーマル シャットダウン (TSD)、TXD ドミナント タイムアウト (DTO)、電源低電圧検出、最高 ±58V のバスフォルト保護に対応する保護および診断機能も備えています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
TCAN1044-Q1	SOT (DDF, 8)	2.9 mm × 2.8mm
	VSON (DRB, 8)	3 mm × 3mm
	SOIC (D, 8)	4.9 mm × 6mm

- (1) 詳細については、[セクション 12](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。





概略回路図

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4 Device Comparison

表 4-1. Device Comparison Table

Part Number	Low Voltage I/O Logic Support on Pin 5	Pin 8 Mode Selection
TCAN1044-Q1	No	Low Power Standby Mode with Remote Wake
TCAN1044V-Q1	Yes	

5 Pin Configuration and Functions

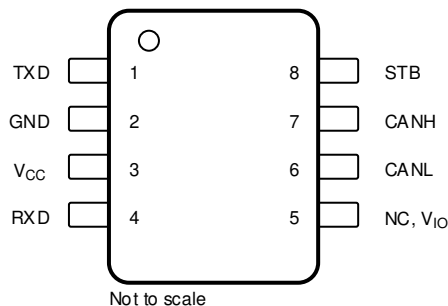


図 5-1. DDF Package, 8-Pin SOT
(Top View)

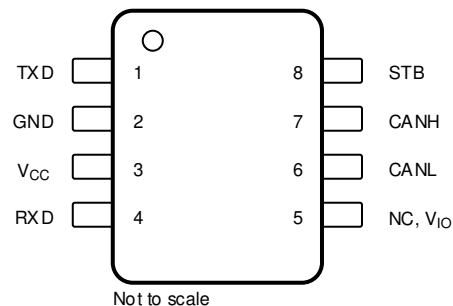


図 5-2. D Package, 8-Pin SOIC
(Top View)

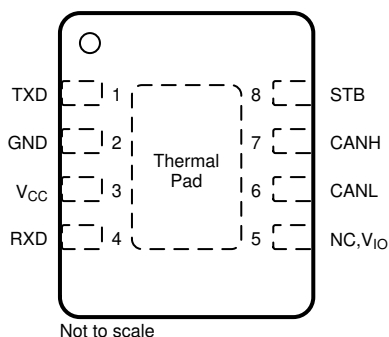


図 5-3. DRB Package, 8-Pin VSON
(Top View)

表 5-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input
GND	2	GND	Ground connection
V _{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
NC	5	—	No Connect (not internally connected); Devices without V _{IO}
V _{IO}		Supply	I/O supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control, integrated pull up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.3	6	V
V _{IO}	Supply voltage I/O level shifter	−0.3	6	V
V _{BUS}	CAN Bus IO voltage CANH and CANL	−58	58	V
V _{DIFF}	Max differential voltage between CANH and CANL	−45	45	V
V _{Logic_Input}	Logic input terminal voltage	−0.3	6	V
V _{RXD}	RXD output terminal voltage range	−0.3	6	V
I _{O(RXD)}	RXD output current	−8	8	mA
T _J	Operating virtual junction temperature range	−40	150	°C
T _{STG}	Storage temperature	−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values, except differential IO bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	HBM classification level 3A for all pins	±3000	V
			HBM classification level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings

				VALUE	UNIT
V _{ESD}	System Level Electro-Static Discharge (ESD) ⁽³⁾	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10650 Powered Contact Discharge	±8000	V
			SAE J2962-2 per ISO 10650 Powered Air Discharge	±15000	V
V _{Tran}	ISO 7637 ISO Pulse Transients ⁽¹⁾	CAN bus terminals (CANH, CANL)	Pulse 1	−100	V
			Pulse 2a	75	V
			Pulse 3a	−150	V
			Pulse 3b	100	V
	ISO 7637 Slow transients pulse ⁽²⁾	CAN bus terminals (CANH, CANL) to GND	DCC slow transient pulse	±85	V

- (1) Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
- (2) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- (3) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
I _{OH(RXD)}	RXD terminal high level output current	−2			mA
I _{OL(RXD)}	RXD terminal low level output current			2	mA

6.4 Recommended Operating Conditions (続き)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		125	°C

6.5 Thermal Characteristics

THERMAL METRIC ⁽¹⁾		TCAN1044x-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	119.9	49.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	61.8	58.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.6	39.7	23.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	2.1	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	39.5	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	–	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Supply Characteristics

Over recommended operating conditions with $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	TXD = 0 V, STB = 0 V, $R_L = 60\ \Omega$, $C_L = \text{open}$ See Figure 7-1		45	70	mA
			TXD = 0 V, STB = 0 V, $R_L = 50\ \Omega$, $C_L = \text{open}$ See Figure 7-1		49	80	mA
		Recessive	TXD = V_{CC} , STB = 0 V, $R_L = 50\ \Omega$, $C_L = \text{open}$ See Figure 7-1		4.5	7.5	mA
		Dominant with bus fault	TXD = 0 V, STB = 0 V, CANH = CANL = $\pm 25\ \text{V}$, $R_L = \text{open}$, $C_L = \text{open}$ See Figure 7-1			130	mA
I_{CC}	Supply current Standby mode Devices with V_{IO}		TXD = STB = V_{IO} , $R_L = 50\ \Omega$, $C_L = \text{open}$ See Figure 7-1		0.2	1	μA
I_{CC}	Supply current Standby mode Devices without V_{IO}		TXD = STB = V_{CC} , $R_L = 50\ \Omega$, $C_L = \text{open}$ See Figure 7-1			14.5	μA
I_{IO}	I/O supply current Normal mode	Dominant	TXD = 0 V, STB = 0 V RXD floating		125	300	μA
I_{IO}	I/O supply current Normal mode	Recessive	TXD = 0 V, STB = 0 V RXD floating		25	48	μA
I_{IO}	I/O supply current Standby mode		TXD = 0 V, STB = V_{IO} RXD floating		8.5	13.5	μA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.25	V
UV_{VIO}	Rising under voltage detection on V_{IO} (Devices with V_{IO})				1.56	1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO} (Devices with V_{IO})			1.4	1.51	1.59	V

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D	Average power dissipation Normal mode	V _{CC} = 5 V, V _{IO} = 1.8 V, T _J = 27°C, R _L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		110		mW
		V _{CC} = 5 V, V _{IO} = 3.3 V, T _J = 27°C, R _L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		110		mW
		V _{CC} = 5 V, V _{IO} = 5 V, T _J = 27°C, R _L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		110		mW
		V _{CC} = 5.5 V, V _{IO} = 1.8 V, T _A = 125°C, R _L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		120		mW
		V _{CC} = 5.5 V, V _{IO} = 3.3 V, T _A = 125°C, R _L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		120		mW
		V _{CC} = 5.5 V, V _{IO} = 5 V, T _A = 125°C, R _L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C _{L_RXD} = 15 pF		120		mW
T _{TSD}	Thermal shutdown temperature			192		°C
T _{TSD_HYS}	Thermal shutdown hysteresis			10		

6.8 Electrical Characteristics

Over recommended operating conditions with $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	TXD = 0 V, STB = 0 V, $50\ \Omega \leq R_L \leq 65\ \Omega$, C_L = open, R_{CM} = open See 図 7-2 and 図 8-3 ,	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	TXD = V_{IO} , STB = 0 V, R_L = open (no load), R_{CM} = open See 図 7-2 and 図 8-3	2	$0.5\ V_{CC}$	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)} + V_{O(CANL)}$)/ V_{CC}		STB = 0 V, R_L = $60\ \Omega$, $C_{SPLIT} = 4.7\ \text{nF}$, C_L = open, R_{CM} = open, TXD = 250 kHz, 1 MHz, 2.5 MHz See 図 7-2 and 図 9-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry ($V_{CC} - V_{O(CANH)} - V_{O(CANL)}$)		STB = 0 V, R_L = $60\ \Omega$, C_L = open See 図 7-2 and 図 8-3	-400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	TXD = 0 V, STB = 0 V, $50\ \Omega \leq R_L \leq 65\ \Omega$, C_L = open See 図 7-2 and 図 8-3	1.5		3	V
			TXD = 0 V, STB = 0 V, $45\ \Omega \leq R_L \leq 70\ \Omega$, C_L = open See 図 7-2 and 図 8-3	1.4		3.3	V
			TXD = 0 V, STB = 0 V, $R_L = 2240\ \Omega$, C_L = open See 図 7-2 and 図 8-3	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	TXD = V_{IO} , STB = 0 V, $R_L = 60\ \Omega$, C_L = open See 図 7-2 and 図 8-3	-120		12	mV
			TXD = V_{IO} , STB = 0 V, R_L = open, C_L = open See 図 7-2 and 図 8-3	-50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO} , R_L = open (no load) See 図 7-2 and 図 8-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0 V, $V_{(CANH)} = -15\ \text{V}$ to $40\ \text{V}$, CANL = open, TXD = 0 V See 図 7-7 and 図 8-3	-115			mA
			STB = 0 V, $V_{(CANL)} = -15\ \text{V}$ to $40\ \text{V}$, CANH = open, TXD = 0 V See 図 7-7 and 図 8-3			115	mA
$I_{OS(SS_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0 V, $-27\ \text{V} \leq V_{BUS} \leq 32\ \text{V}$, where $V_{BUS} = \text{CANH} = \text{CANL}$, TXD = V_{IO} See 図 7-7 and 図 8-3	-5		5	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage Normal mode		STB = 0 V, $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	500		900	mV
$V_{IT(STB)}$	Input threshold Standby mode		STB = V_{IO} , $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	400		1150	mV
V_{DOM}	Dominant state differential input voltage range Normal mode		STB = 0 V, $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode		STB = 0 V, $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	-4		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode		STB = V_{IO} , $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode		STB = V_{IO} , $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode		STB = 0 V, $-12\ \text{V} \leq V_{CM} \leq 12\ \text{V}$ See 図 7-3, 表 7-1, and 表 8-6		100		mV
V_{CM}	Common mode range Normal and standby modes		See 図 7-3 and 表 8-6 表 8-6	-12		12	V

6.8 Electrical Characteristics (続き)

Over recommended operating conditions with $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{LKG(OFF)}	Unpowered bus input leakage current	CANH = CANL = 5 V, V _{CC} = V _{IO} = GND				5	μA
C _I	Input capacitance to ground (CANH or CANL)	TXD = V _{IO} ⁽¹⁾				20	pF
C _{ID}	Differential input capacitance					10	pF
R _{ID}	Differential input resistance	TXD = V _{IO} ⁽¹⁾ , STB = 0 V, -12 V ≤ V _{CM} ≤ 12 V		40		90	kΩ
R _{IN}	Single ended input resistance (CANH or CANL)			20		45	kΩ
R _{IN(M)}	Input resistance matching [1 – (R _{IN(CANH)} / R _{IN(CANL)})] × 100 %	V _(CAN_H) = V _(CAN_L) = 5 V		–1%		1%	
TXD Terminal (CAN Transmit Data Input)							
V _{IH}	High-level input voltage	Devices without V _{IO}		0.7 V _{CC}			V
V _{IH}	High-level input voltage	Devices with V _{IO}		0.7 V _{IO}			V
V _{IL}	Low-level input voltage	Devices without V _{IO}		0.3 V _{CC}			V
V _{IL}	Low-level input voltage	Devices with V _{IO}		0.3 V _{IO}			V
I _{IH}	High-level input leakage current	TXD = V _{CC} = V _{IO} = 5.5 V		–2.5	0	1	μA
I _{IL}	Low-level input leakage current	TXD = 0 V, V _{CC} = V _{IO} = 5.5 V		–200	-100	–20	μA
I _{LKG(OFF)}	Unpowered leakage current	TXD = 5.5 V, V _{CC} = V _{IO} = 0 V		–1	0	1	μA
C _I	Input Capacitance	V _{IN} = 0.4×sin(2×π×2×10 ⁶ ×t)+2.5 V			5		pF
RXD Terminal (CAN Receive Data Output)							
V _{OH}	High-level output voltage	I _O = –2 mA, Devices without V _{IO} See Figure 7-3		0.8 V _{CC}			V
V _{OH}	High-level output voltage	I _O = –2 mA, Devices with V _{IO} See Figure 7-3		0.8 V _{IO}			V
V _{OL}	Low-level output voltage	I _O = 2 mA, Devices without V _{IO} See Figure 7-3		0.2 V _{CC}			V
V _{OL}	Low-level output voltage	I _O = –2 mA, Devices with V _{IO} See Figure 7-3		0.2 V _{IO}			V
I _{LKG(OFF)}	Unpowered leakage current	RXD = 5.5 V, V _{CC} = V _{IO} = 0 V		–1	0	1	μA
STB Terminal (Standby Mode Input)							
V _{IH}	High-level input voltage	Devices without V _{IO}		0.7 V _{CC}			V
V _{IH}	High-level input voltage	Devices with V _{IO}		0.7 V _{IO}			V
V _{IL}	Low-level input voltage	Devices without V _{IO}		0.3 V _{CC}			V
V _{IL}	Low-level input voltage	Devices with V _{IO}		0.3 V _{IO}			V
I _{LKG(OFF)}	Unpowered leakage current	STB = 5.5V, V _{CC} = V _{IO} = 0 V		–1	0	1	μA

(1) $V_{IO} = V_{CC}$ in non-V variants of device

6.9 Switching Characteristics

Over recommended operating conditions with $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics					
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_L(RXD) = 15\text{ pF}$ $V_{IO} = 2.8\text{ V to } 5.5\text{ V}$ See Figure 7-4			125 to 210 ns
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_L(RXD) = 15\text{ pF}$ $V_{IO} = 1.7\text{ V}$ See Figure 7-4			165 to 255 ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_L(RXD) = 15\text{ pF}$ $V_{IO} = 2.8\text{ V to } 5.5\text{ V}$ See Figure 7-4			150 to 210 ns

6.9 Switching Characteristics (続き)

Over recommended operating conditions with $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PROP(LOOP2)}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF V _{IO} = 1.7 V See Figure 7-4		180	255	ns
t _{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure 7-5			20	μs
t _{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 8-5	0.5		1.8	μs
t _{WK_TIMEOUT}	Bus wake-up timeout	See Figure 8-5	0.8		6	ms
Driver Switching Characteristics						
t _{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	STB = 0 V, R _L = 60 Ω, C _L = 100 pF See Figure 7-2 and Figure 7-6		80		ns
t _{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
t _{sk(p)}	Pulse skew (t _{pHR} - t _{pLD})			20		ns
t _R	Differential output signal rise time			30		ns
t _F	Differential output signal fall time			50		ns
t _{TXD.DTO}	Dominant timeout			1.2		4.0
Receiver Switching Characteristics						
t _{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	STB = 0 V, C _{L(RXD)} = 15 pF See Figure 7-3		90		ns
t _{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			65		ns
t _R	RXD output signal rise time			10		ns
t _F	RXD output signal fall time			10		ns
FD Timing Characteristics						
t _{BIT(BUS)}	Bit time on CAN bus output pins t _{BIT(TXD)} = 500 ns	STB = 0 V, R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF Δt _{REC} = t _{BIT(RXD)} - t _{BIT(BUS)} See Figure 7-4	450		530	ns
t _{BIT(BUS)}	Bit time on CAN bus output pins t _{BIT(TXD)} = 200 ns		155		210	ns
t _{BIT(RXD)}	Bit time on RXD output pins t _{BIT(TXD)} = 500 ns		400		550	ns
t _{BIT(RXD)}	Bit time on RXD output pins t _{BIT(TXD)} = 200 ns		120		220	ns
t _{REC}	Receiver timing symmetry t _{BIT(TXD)} = 500 ns		-50		20	ns
t _{REC}	Receiver timing symmetry t _{BIT(TXD)} = 200 ns		-45		15	ns

6.10 Typical Characteristics

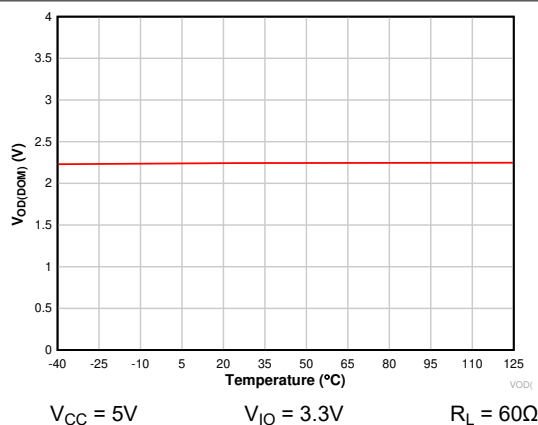


図 6-1. $V_{OD(DOM)}$ vs Temperature

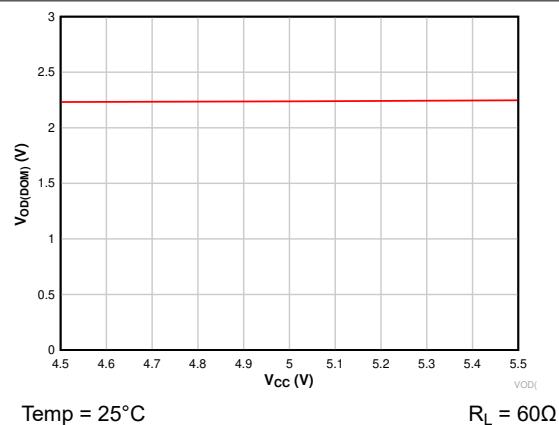


図 6-2. $V_{OD(DOM)}$ vs V_{CC}

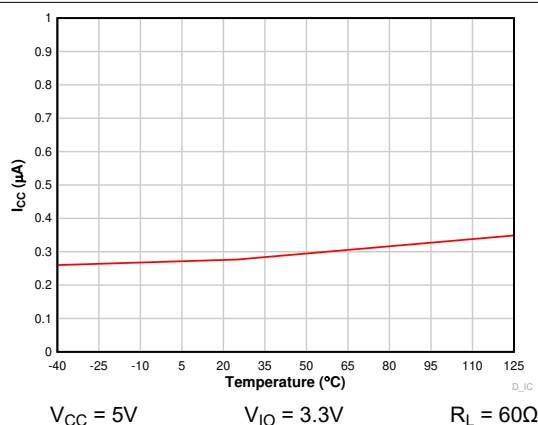


図 6-3. I_{CC} Standby vs Temperature

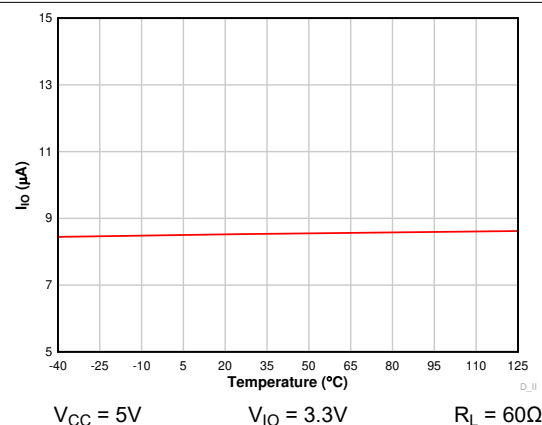


図 6-4. I_{IO} Standby vs Temperature

7 Parameter Measurement Information

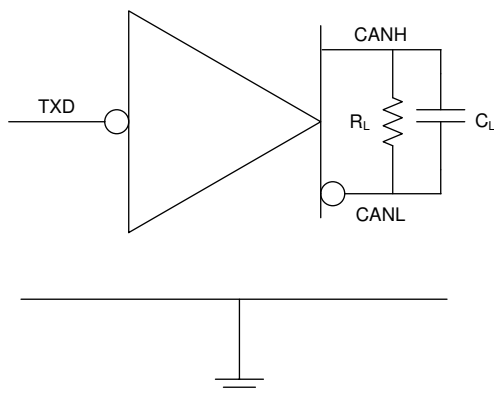


図 7-1. I_{CC} Test Circuit

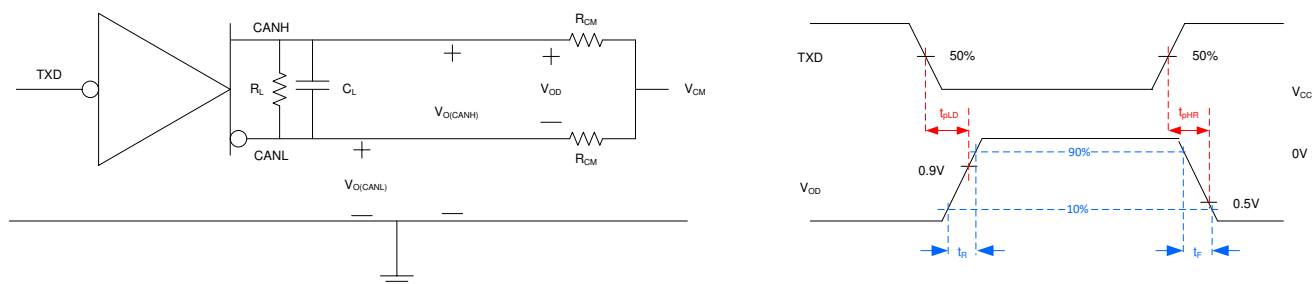


図 7-2. Driver Test Circuit and Measurement

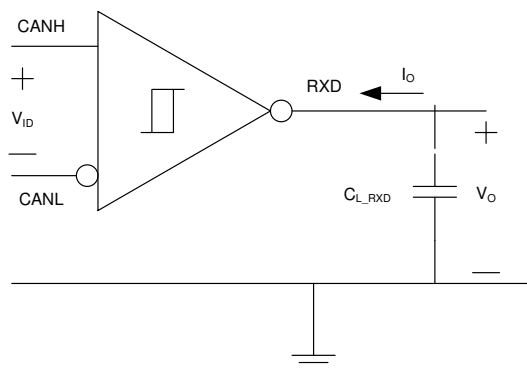


図 7-3. Receiver Test Circuit and Measurement

表 7-1. Receiver Differential Input Voltage Threshold Test

Input (See 図 7-3)			Output	
V_{CANH}	V_{CANL}	$ V_{ID} $	RXD	
-11.5V	-12.5V	1000mV	Low	V_{OL}
12.5V	11.5V	1000mV		
-8.55V	-9.45V	900mV		
9.45 V	8.55V	900mV		
-8.75V	-9.25V	500mV	High	V_{OH}
9.25V	8.75V	500mV		
-11.8 V	-12.2V	400mV		
12.2V	11.8V	400mV		
Open	Open	X		

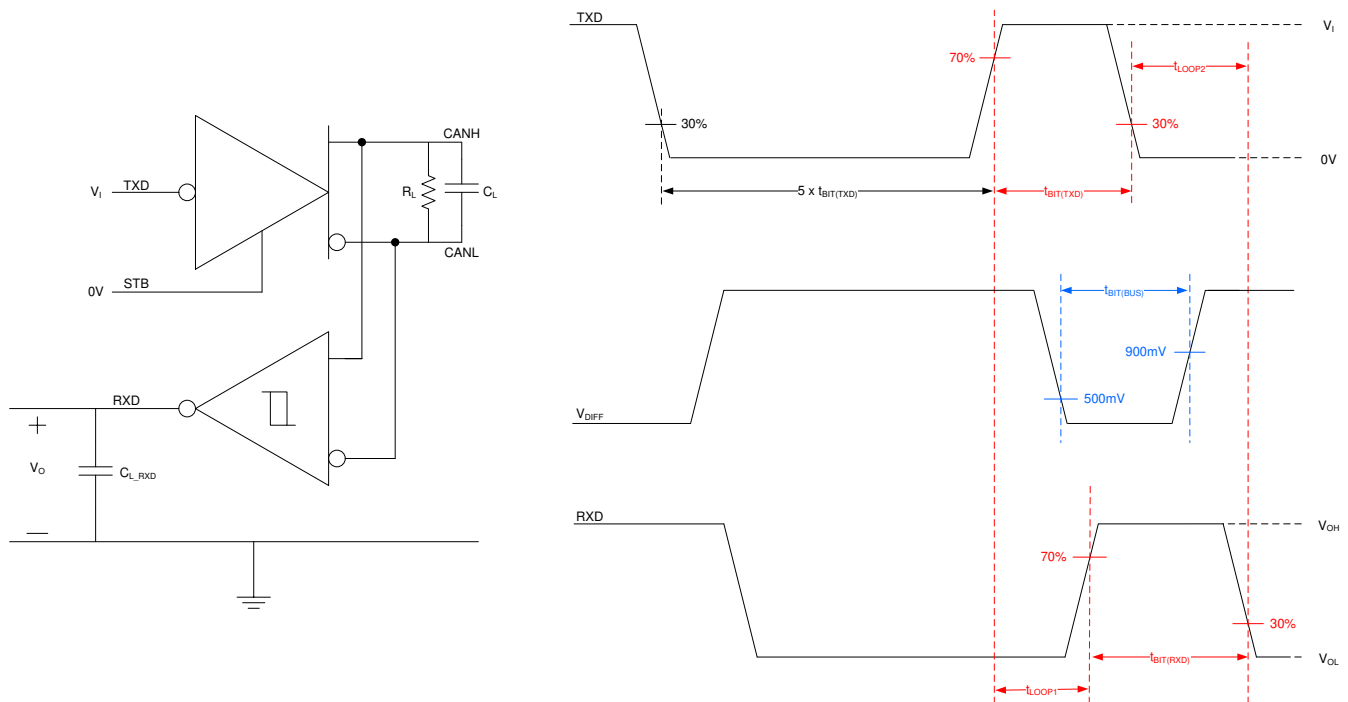


図 7-4. Transmitter and Receiver Timing Test Circuit and Measurement

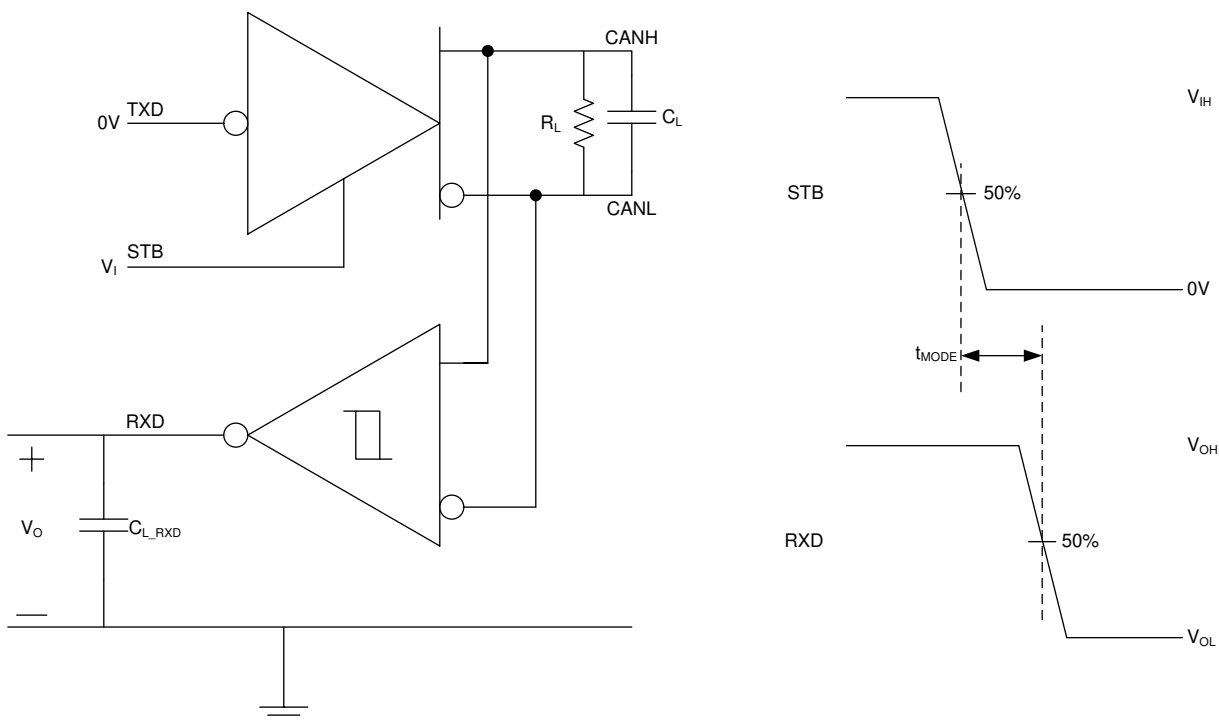


Figure 7-5. t_{MODE} Test Circuit and Measurement

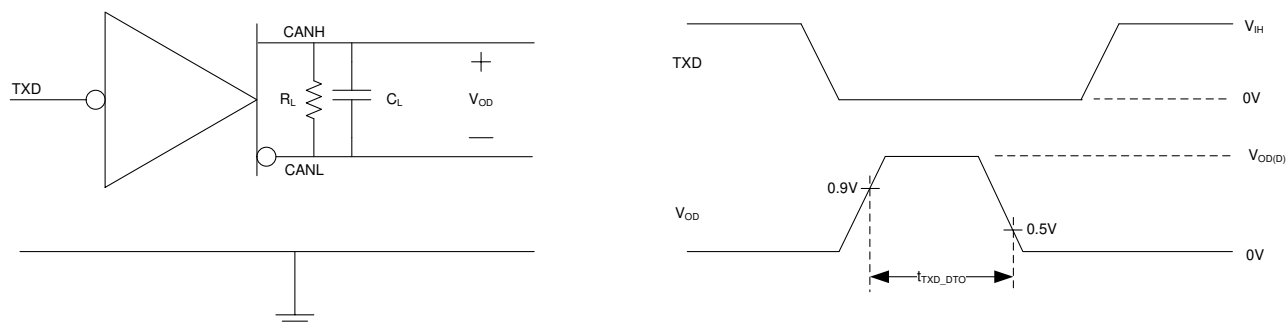
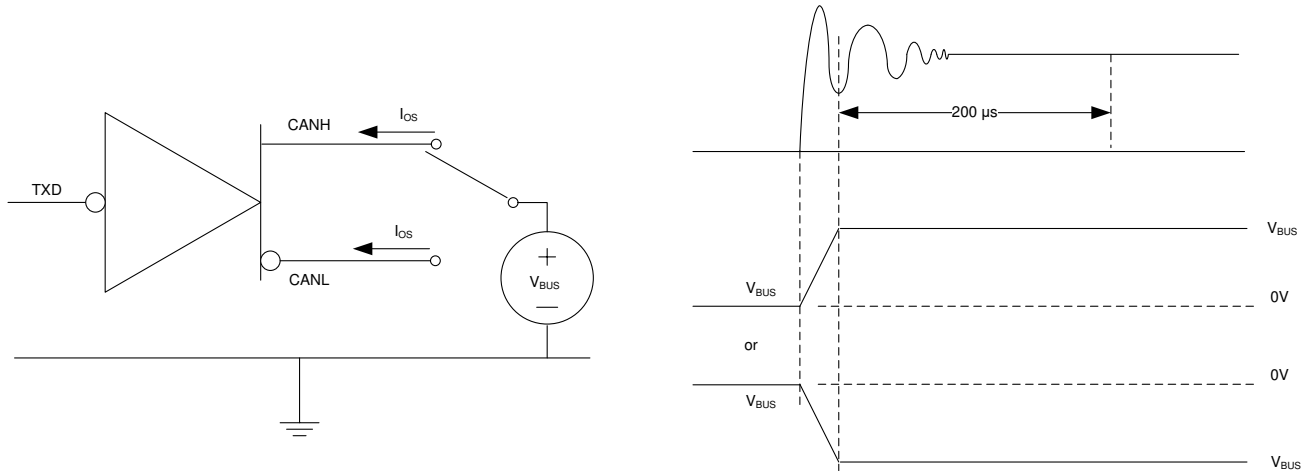


Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement



7-7. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

The TCAN1044-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8Mbps.

The TCAN1044-Q1 conforms to the following CAN standards:

- CAN transceiver physical layer standards:
 - ISO 11898-2:2016 High speed medium access unit
 - ISO 11898-5:2007 High speed medium access unit with low-power mode
 - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
 - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
 - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
 - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
 - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
 - ARINC 825-4 General Standardization of CAN (Controller Area Network) Bus Protocol For Airborne Use
- EMC requirements:
 - VeLIO (Vehicle LAN Interoperability and Optimization) CAN and CAN-FD Transceiver Requirements
 - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance test requirements:
 - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

8.2 Functional Block Diagram

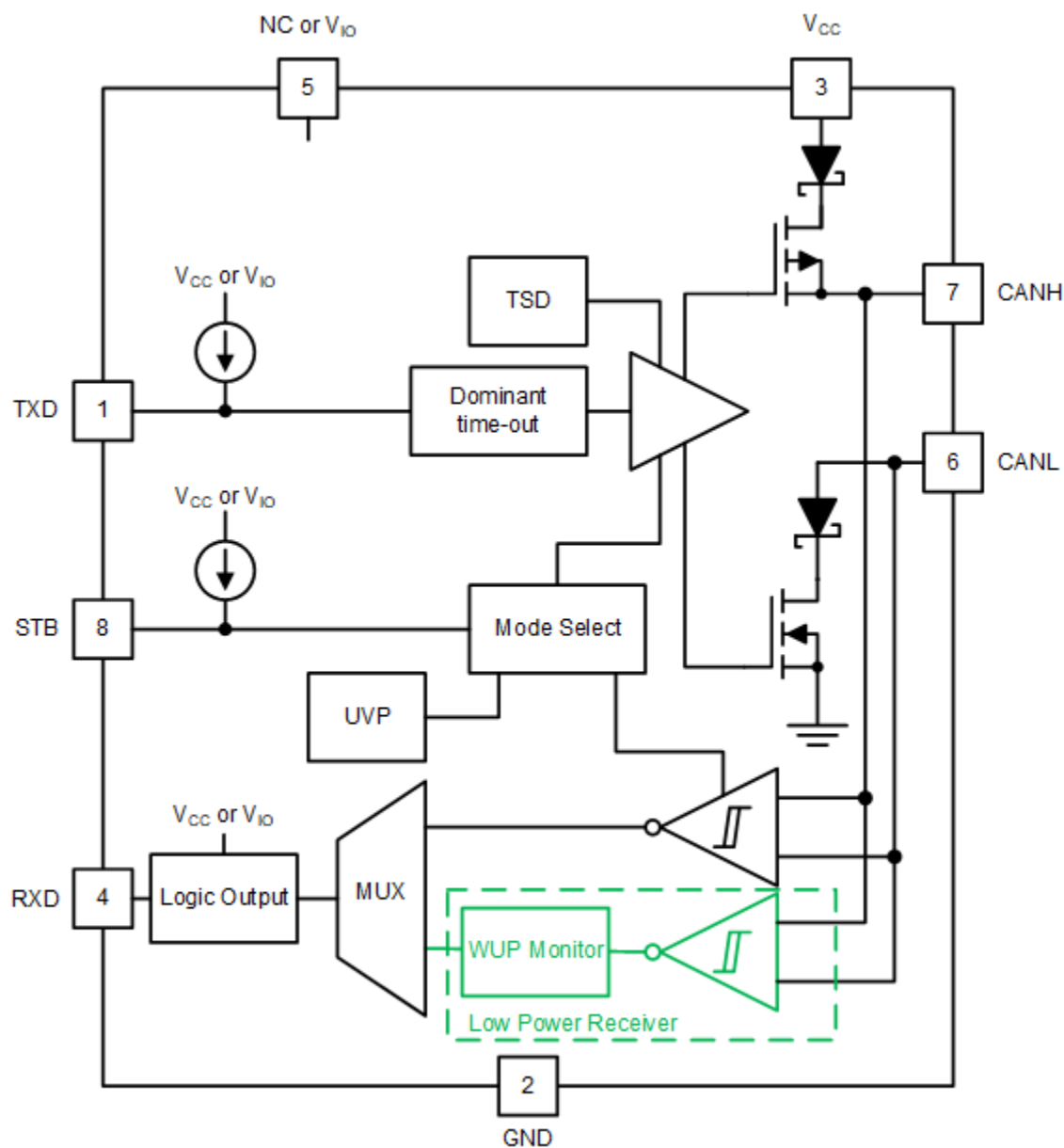


図 8-1. Block Diagram

8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the TCAN1044-Q1 transceivers.

8.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

8.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either V_{CC} or V_{IO} , from the TCAN1044-Q1 transceivers to the CAN controller. RXD is only driven once V_{IO} is present.

When a wake event takes place RXD is driven low.

8.3.1.5 V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7V to 5.5V providing the widest range of controller support.

8.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

8.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, then the STB pin can be tied directly to GND.

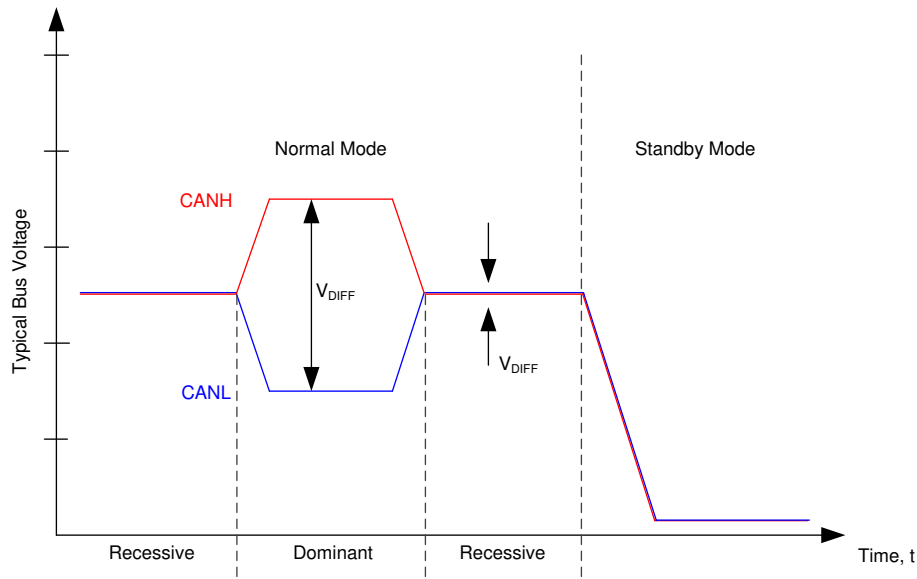
8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See [Figure 8-2](#) and [Figure 8-3](#).

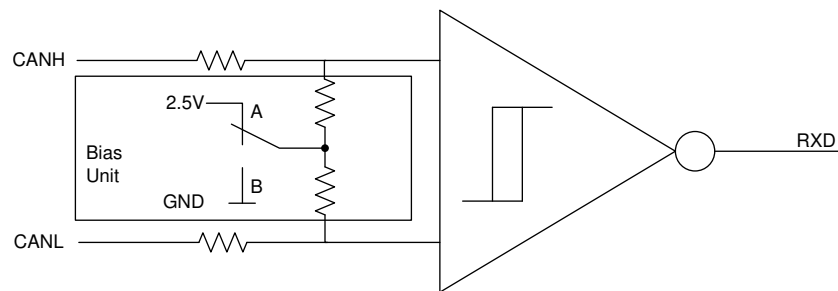
A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1044-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See [Figure 8-2](#) and [Figure 8-3](#).



8-2. Bus States



- A. Normal Mode
- B. Standby Mode

8-3. Simplified Recessive Common Mode Bias Unit and Receiver

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO} . The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO} , the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant timeout. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

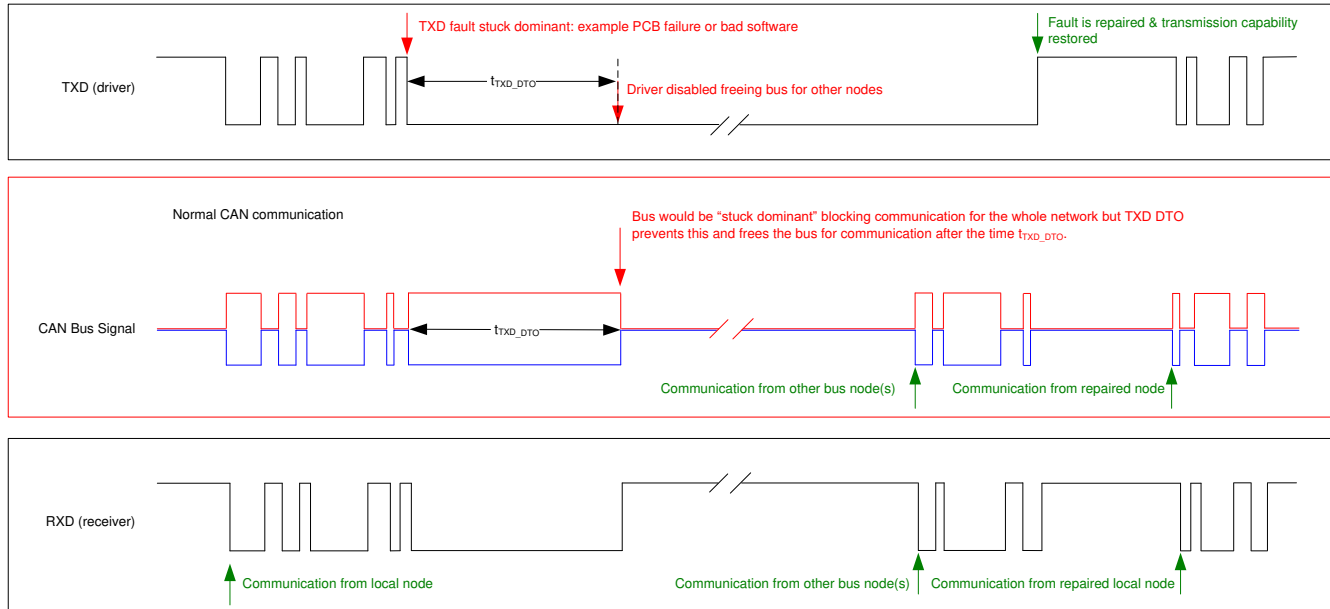


図 8-4. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short Circuit Current Limiting

The TCAN1044-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \% \text{ Transmit} \times [(\% \text{ REC_Bits} \times I_{OS(SS_REC)} + (\% \text{ DOM_Bits} \times I_{OS(SS_DOM)})] + [\% \text{ Receive} \times I_{OS(SS_REC)}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS_REC)}$ is the recessive steady state short circuit current
- $I_{OS(SS_DOM)}$ is the dominant steady state short circuit current

This short circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1044-Q1 exceeds the thermal shutdown threshold, T_{TSD} , the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD} . The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN1044-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO} , have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 8-1. Undervoltage Lockout - TCAN1044-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
$> UV_{VCC}$	Normal	Per TXD	Mirrors bus
$< UV_{VCC}$	Protected	High impedance Weak pull-down to ground ⁽¹⁾	High impedance

(1) $V_{CC} = GND$, see $I_{LKG(OFF)}$

表 8-2. Undervoltage Lockout - TCAN1044V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
$> UV_{VCC}$	$> UV_{VIO}$	Normal	Per TXD	Mirrors bus
$< UV_{VCC}$	$> UV_{VIO}$	STB = V_{IO} : standby mode	High impedance Weak pull-down to ground ⁽¹⁾	V_{IO} : Remote wake request ⁽²⁾
		STB = GND: Protected		Recessive
$> UV_{VCC}$	$< UV_{VIO}$	Protected		High impedance
$< UV_{VCC}$	$< UV_{VIO}$	Protected		High impedance

(1) $V_{CC} = GND$, see $I_{LKG(OFF)}$

(2) See [セクション 8.4.3.1](#)

Once the undervoltage condition is cleared and t_{MODE} has expired the TCAN1044-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

8.3.7 Unpowered Device

The TCAN1044-Q1 is designed to be a suitable passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the pins do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so the pins do not load other circuits which may remain powered.

8.3.8 Floating pins

The TCAN1044-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See [表 8-3](#) for details on pin bias conditions.

表 8-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering

表 8-3. Pin Bias (続き)

Pin	Pull-up or Pull-down	Comment
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

8.4 Device Functional Modes

8.4.1 Operating Modes

The TCAN1044-Q1 has two main operating modes: normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the TCAN1044-Q1.

表 8-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See セクション 8.4.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.4.2 Normal Mode

This is the normal operating mode of the TCAN1044-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

8.4.3 Standby Mode

This is the low-power mode of the TCAN1044-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in [図 8-5](#). The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see [図 8-2](#) and [図 8-3](#).

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1044-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1044-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK_FILTER(MIN)}$ and $t_{WK_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be

generated. Bus state times greater than $t_{WK_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 8-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 8-5 for the timing diagram of the wake-up pattern with wake timeout feature.

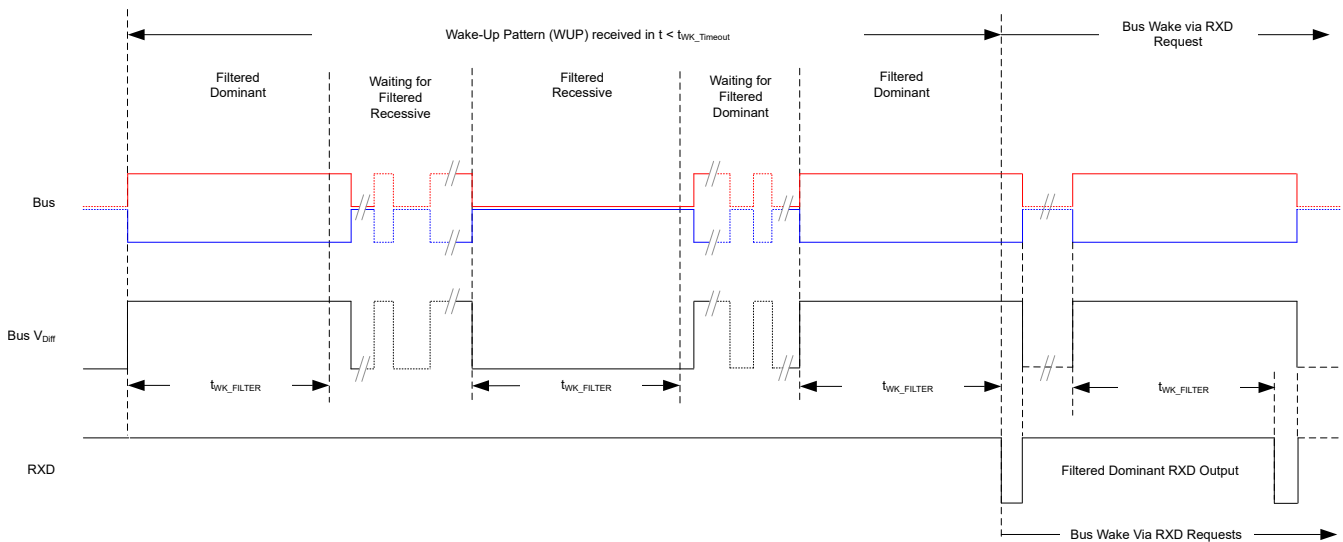


Figure 8-5. Wake-Up Pattern (WUP) with $t_{WK_TIMEOUT}$

8.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1044-Q1 are CMOS levels with respect to either V_{CC} for 5V systems or V_{IO} for compatible with MCUs having 1.8V, 2.5V, 3.3V, or 5V systems.

表 8-5. Driver Function Table

Device Mode	TXD Input ⁽¹⁾	Bus Outputs		Driven Bus State ⁽²⁾
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant

(2) For bus state and bias see [図 8-2](#) and [図 8-3](#)

表 8-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred See 図 8-5
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

9 Application and Implementation

注

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9.1 Application Information

9.2 Typical Application

The TCAN1044-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. 図 9-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

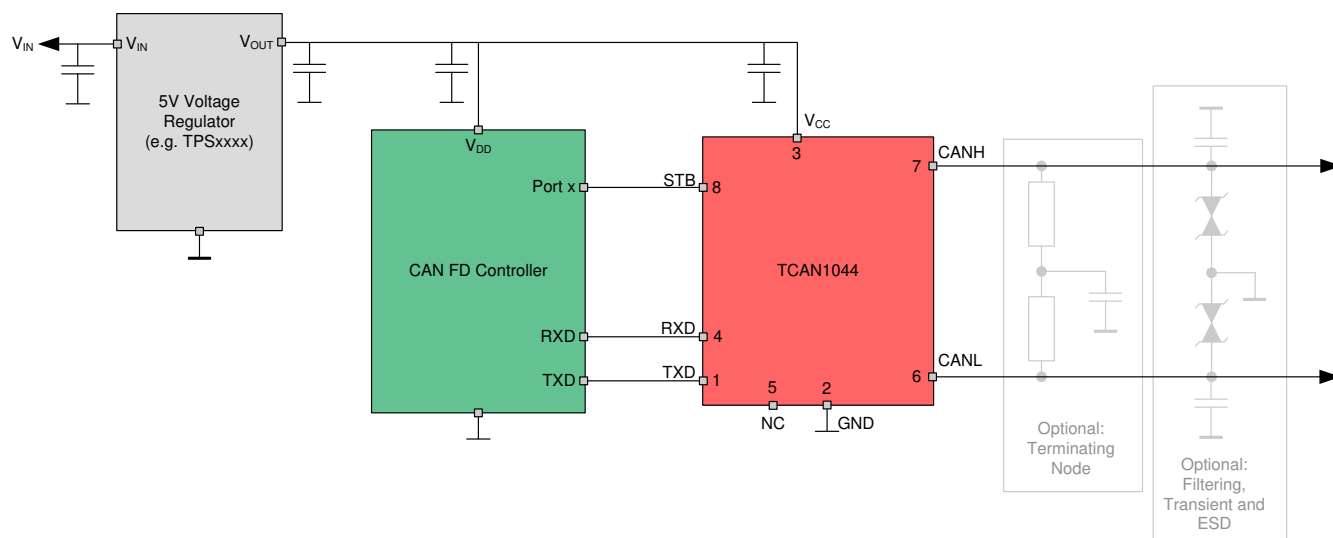


図 9-1. Transceiver Application Using 5V I/O Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see [Figure 9-2](#). Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

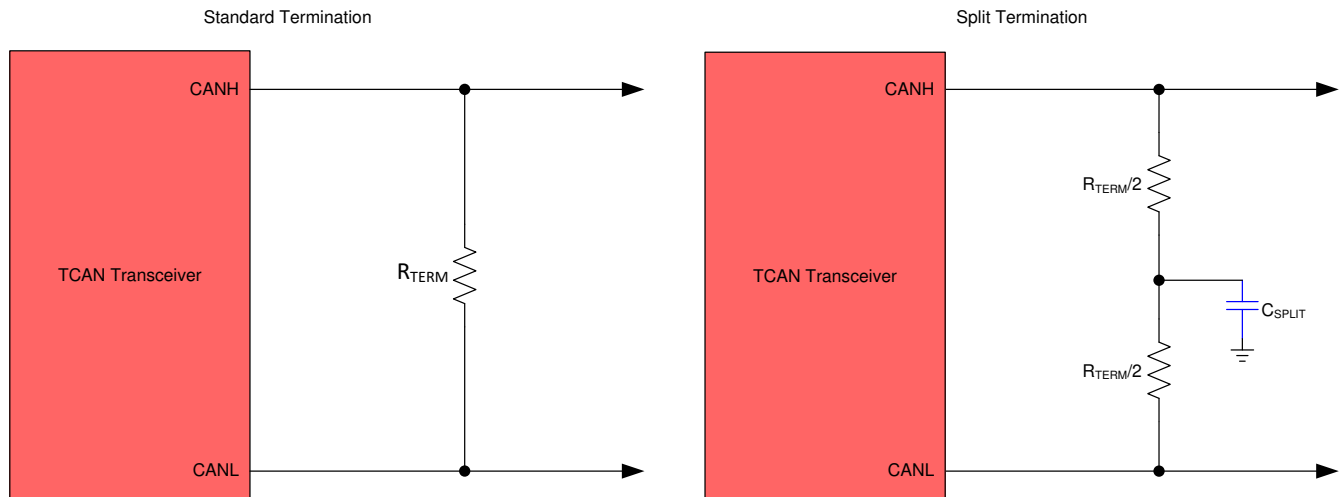


Figure 9-2. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1044-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1044-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the TCAN1044-Q1 is a minimum of $40k\Omega$. If 100 TCAN1044-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω . Therefore, the TCAN1044-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

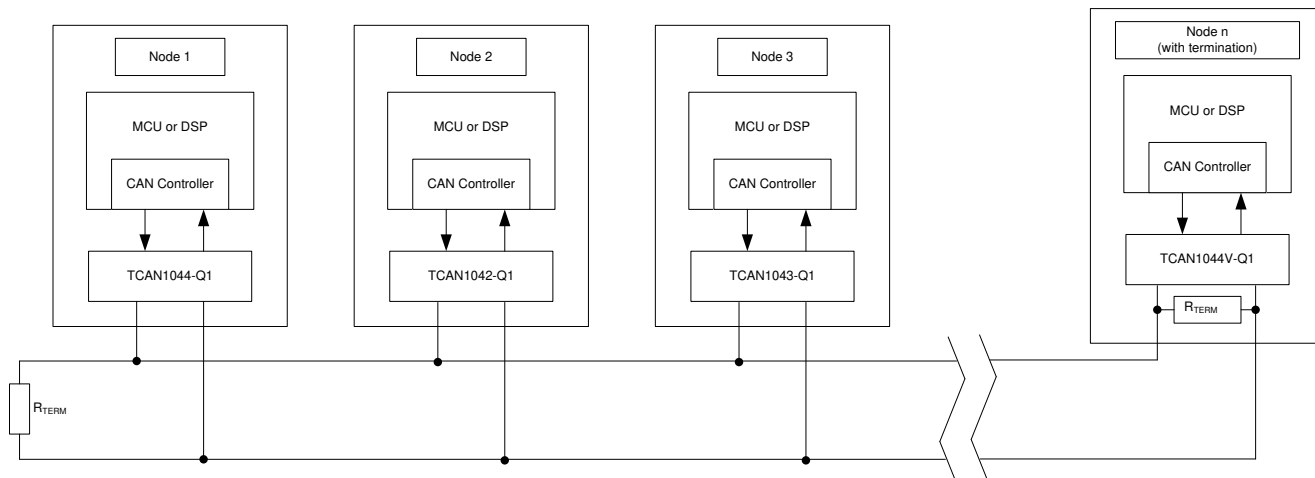


図 9-3. Typical CAN Bus

9.2.3 Application Curves

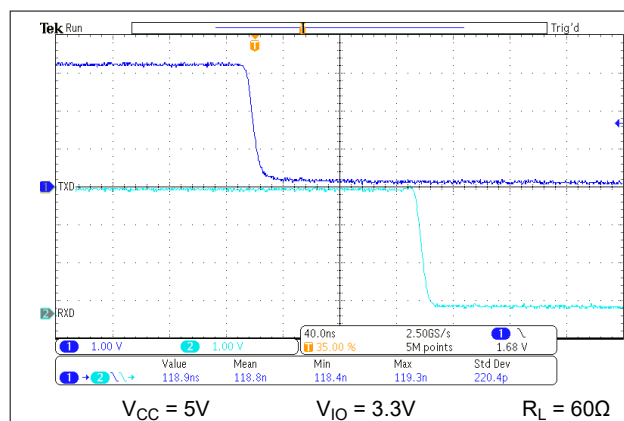


図 9-4. $t_{PROP(LOOP1)}$

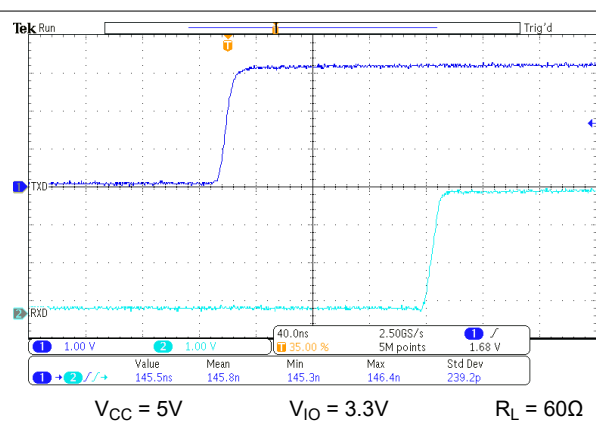


図 9-5. $t_{PROP(LOOP2)}$

9.3 System Examples

The TCAN1044-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V, 2.5V, or 3.3V application is shown in [Figure 9-6](#). The bus termination is shown for illustrative purposes.

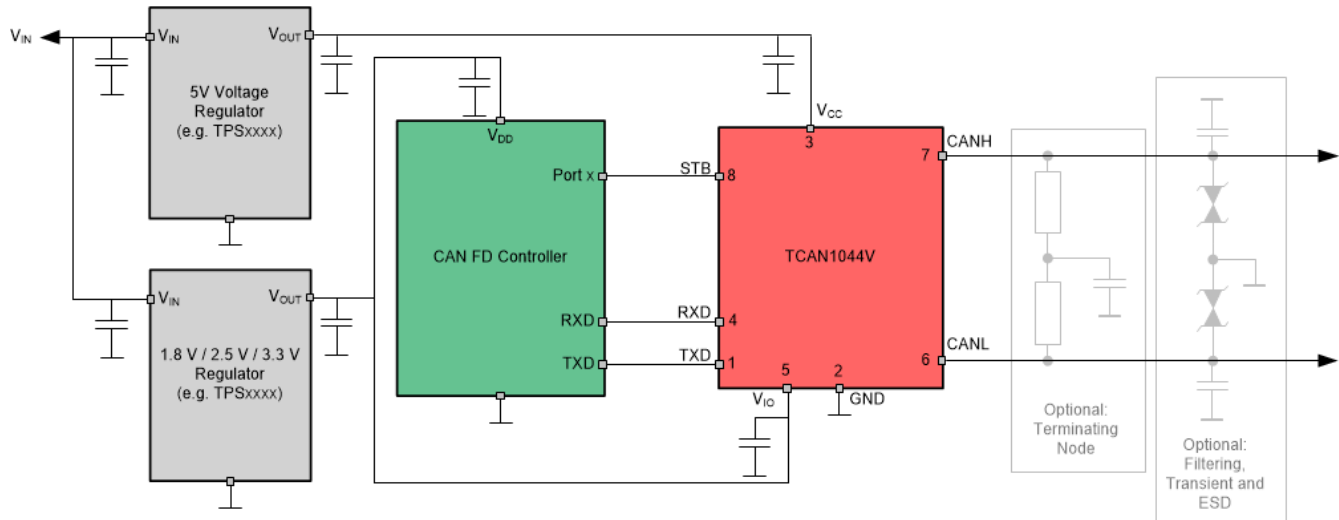


Figure 9-6. Typical Transceiver Application Using 1.8V, 2.5V, 3.3V IO Connections

9.4 Power Supply Recommendations

The TCAN1044-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TCAN1044V-Q1 implements an IO level shifting supply input, V_{IO} , designed for a range between 1.8V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, should be placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

9.5 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

9.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

注

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See [セクション 9.2.1.1](#), [セクション](#)

8.3.4, and 式 2 for information on termination concepts and power ratings needed for the termination resistor(s).

- To limit current, digital lines series resistors can be used. Examples are R2, R3 and R4.
- Pin 1 is shown for the TXD input of the device with R1 as an optional pull-up resistor. If an open drain host controller is used, making sure the bit timing into the device is met is mandatory.
- Pin 8 is shown with R4 assuming the mode pin STB, is used. If the device is used in normal mode only, R4 is not needed and the pads of C4 could be used for the pull down resistor R5 to GND.

9.5.2 Layout Example

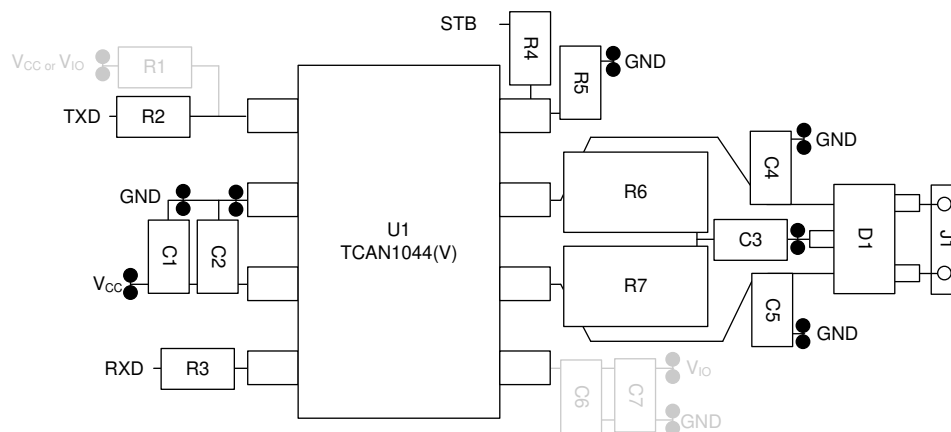


図 9-7. Layout Example

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2024) to Revision D (March 2025)	Page
・ 「概要」の第 2 段落に新しいテキストを追加.....	1
・ Added the <i>Device Comparison</i> table.....	3

Changes from Revision B (October 2021) to Revision C (October 2024)	Page
・ 「特長」「SOIC パッケージで供給...」を変更.....	1
・ データシートのタイトルとヘッダー情報から部品番号 TCAN1044V-Q1 を削除。.....	1
・ 「製品情報」表を「パッケージ情報」表に変更.....	1

Changes from Revision A (December 2019) to Revision B (October 2021)	Page
・ 「特長」に「機能安全対応」を追加.....	1
・ 「概略回路図」を変更.....	1
・ Changed  9-2	26

Changes from Revision * (August 2019) to Revision A (December 2019)	Page
• データシートの最初の公開リリース.....	1
• Added SAE j2962-2 ESD.....	5
• Changed footnote to Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011).....	5

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1044DRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044
TCAN1044DRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044
TCAN1044DRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044
TCAN1044DRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044
TCAN1044VDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26SF
TCAN1044VDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26SF
TCAN1044VDRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044V
TCAN1044VDRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044V
TCAN1044VDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044V
TCAN1044VDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044V

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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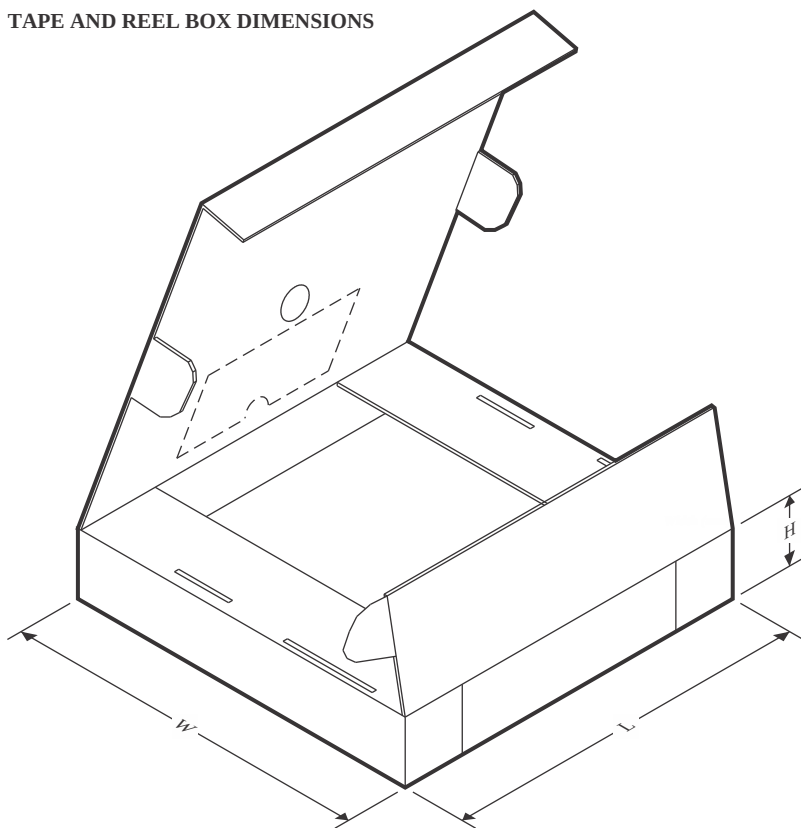
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1044DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1044DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1044VDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1044VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1044VDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1044DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1044DRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1044VDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1044VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1044VDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

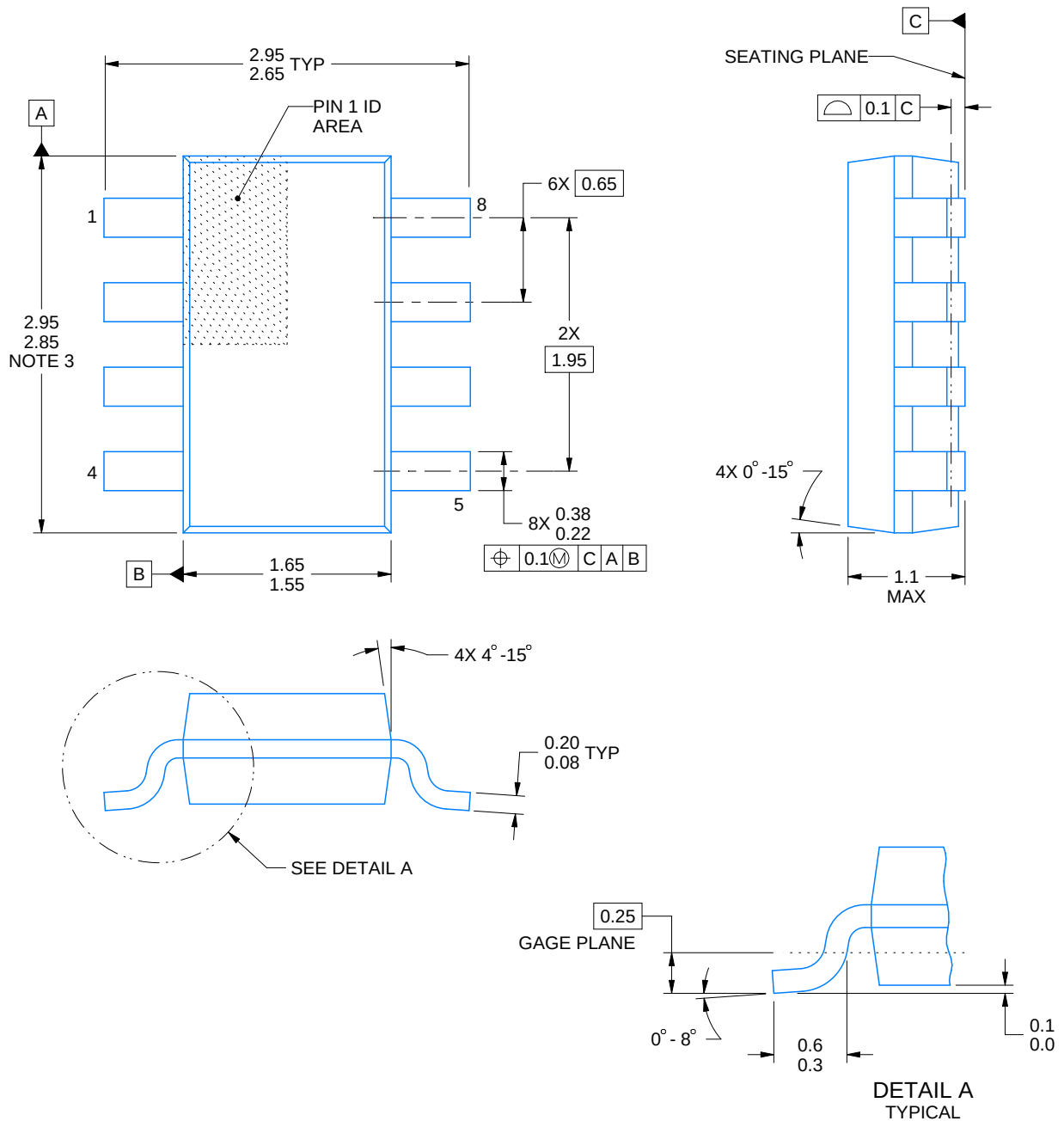
DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

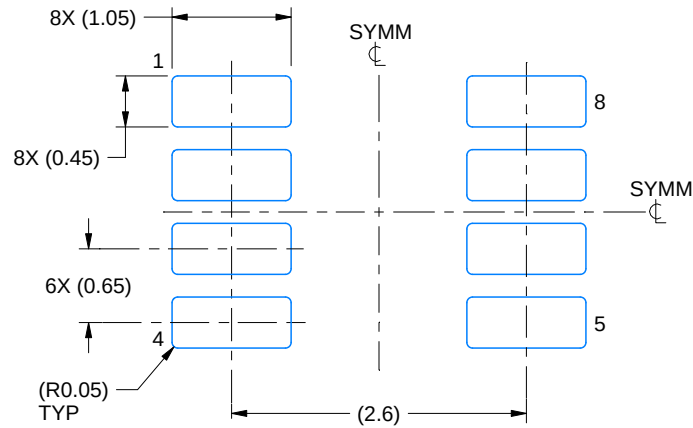
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

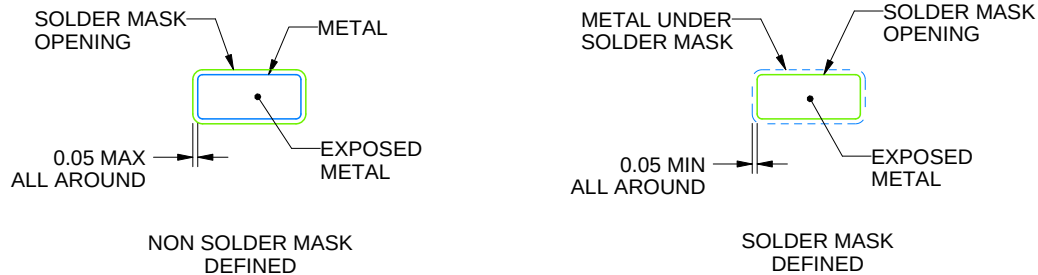
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

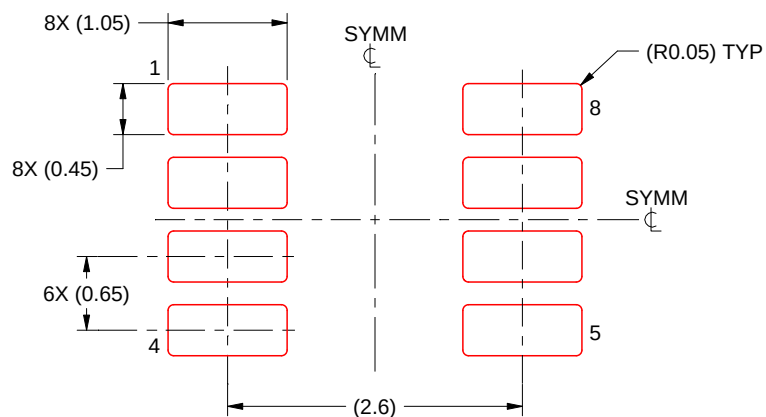
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

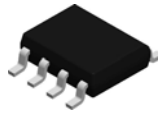


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

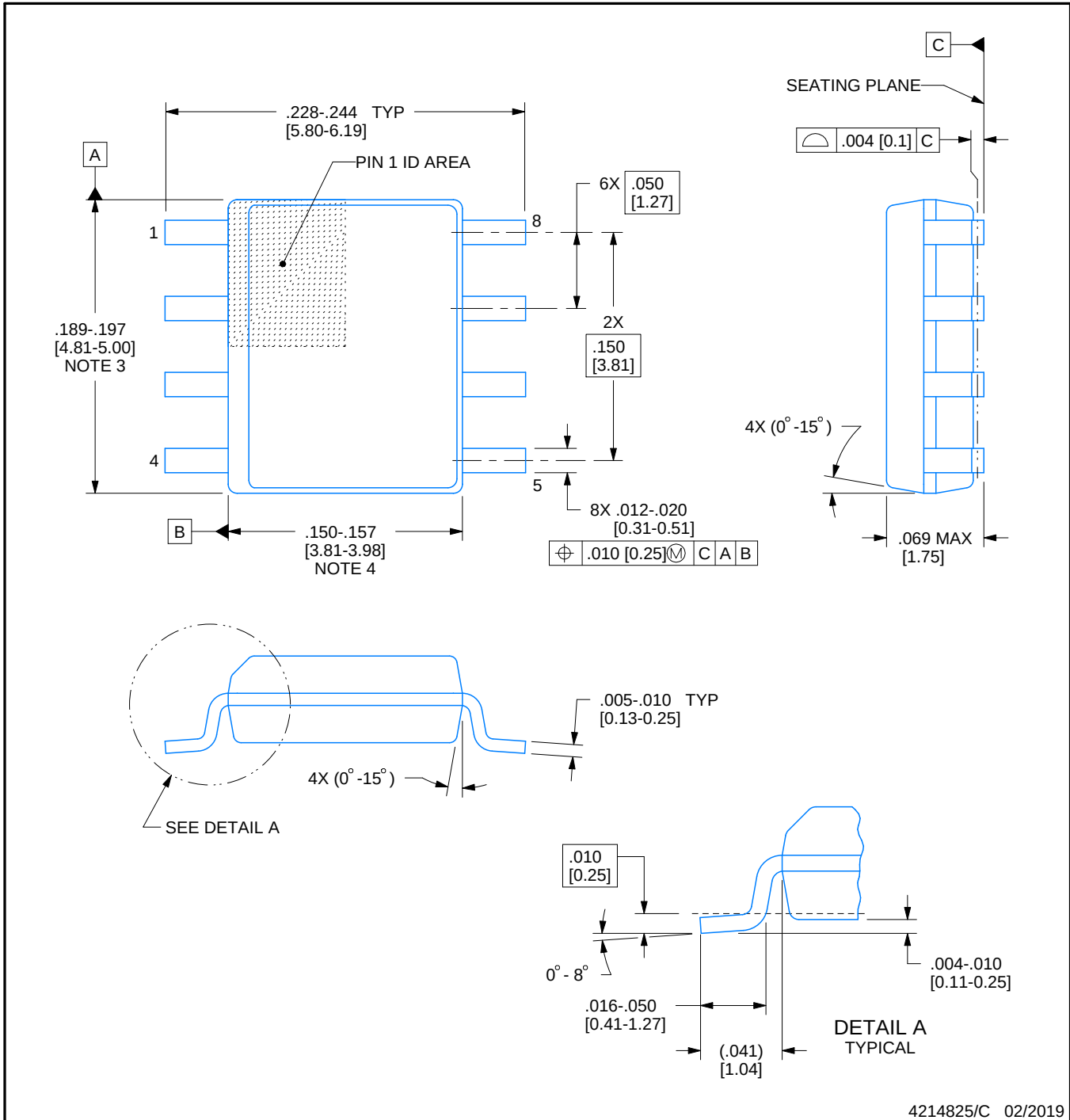


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

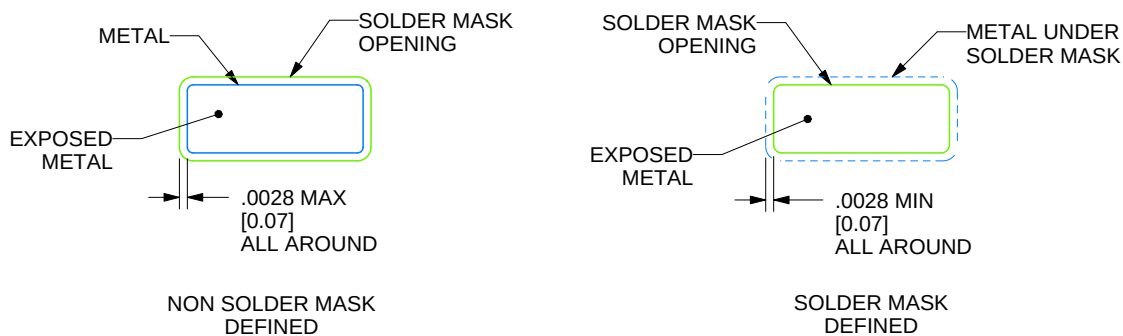
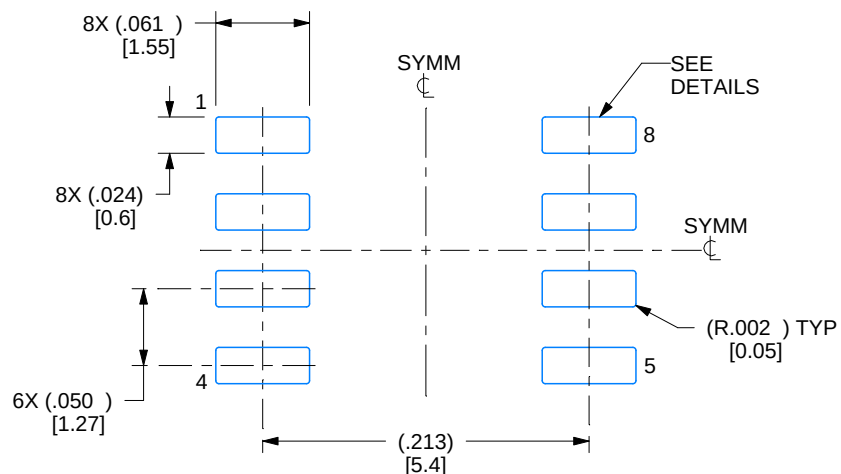
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

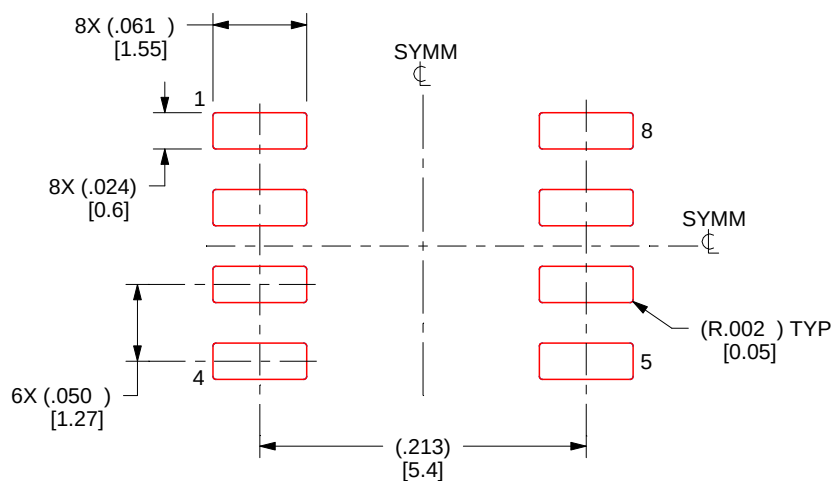
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

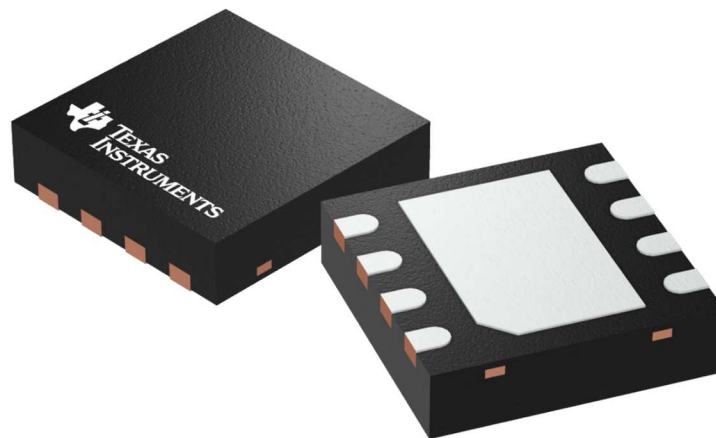
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRB 8

GENERIC PACKAGE VIEW

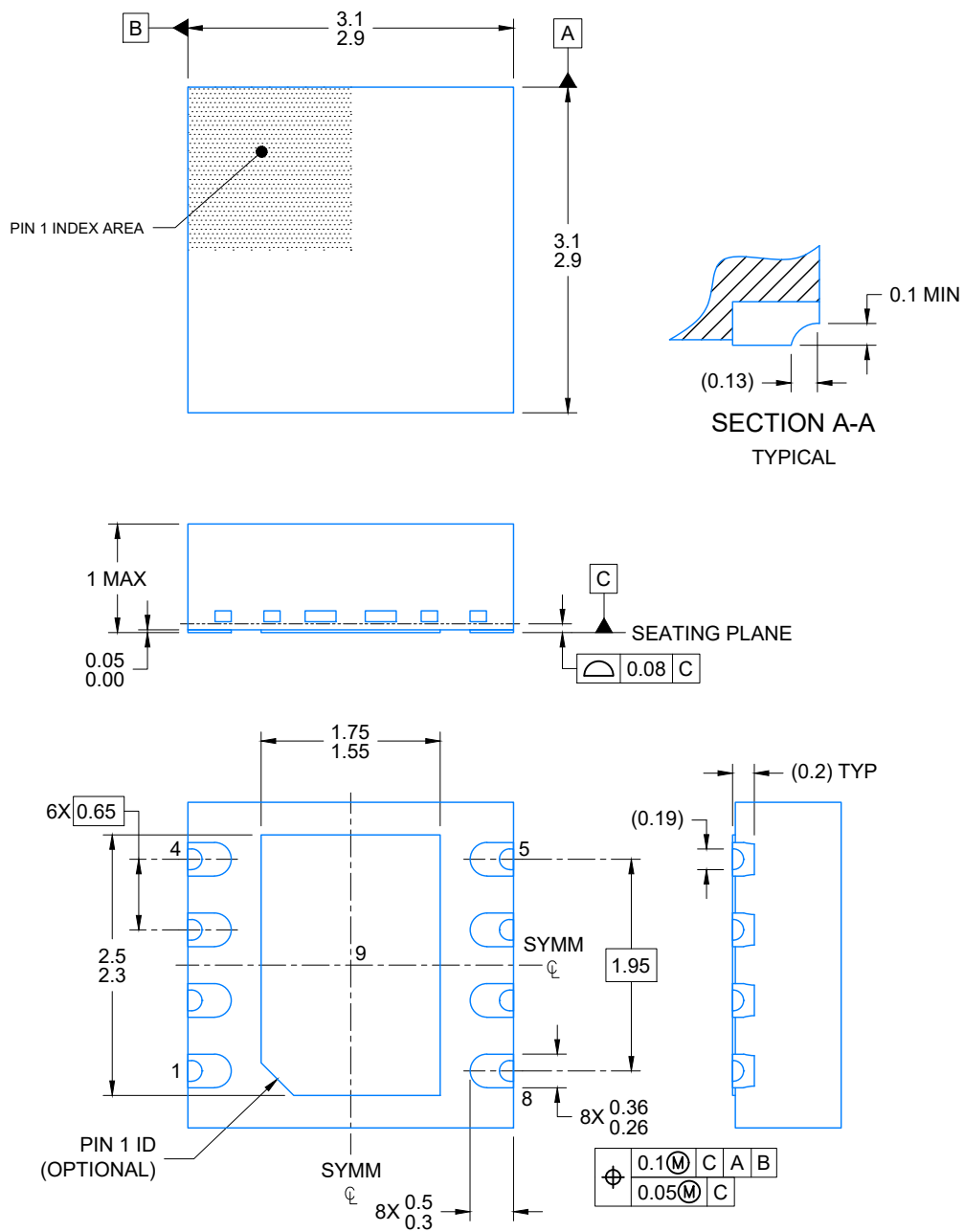
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

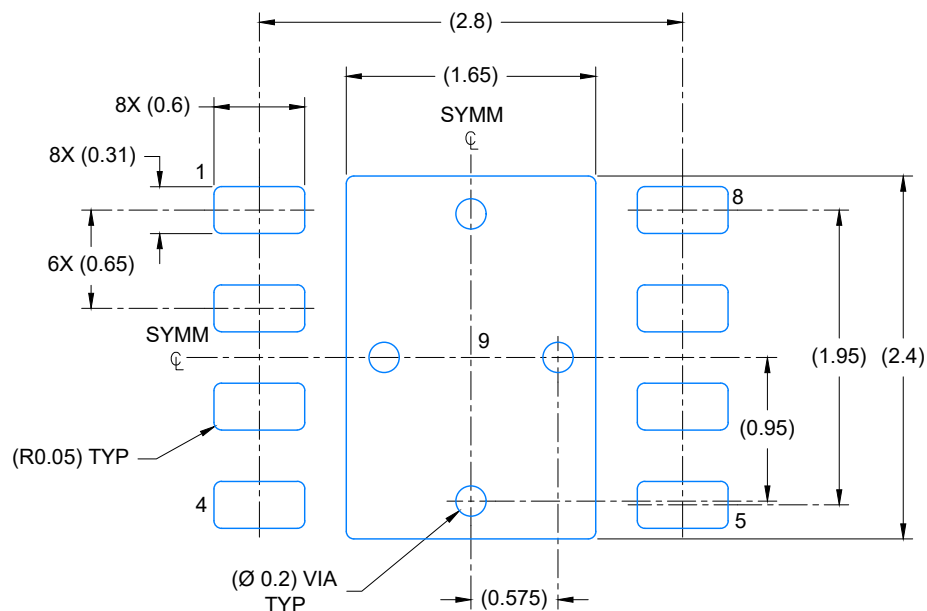
4203482/L



4225036/A 06/2019

NOTES:

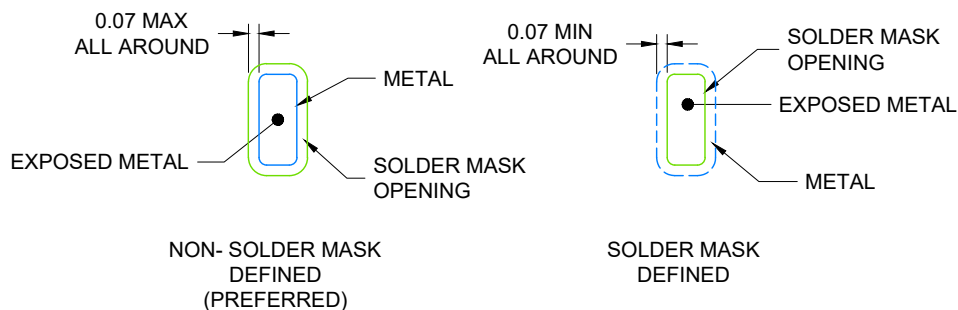
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X

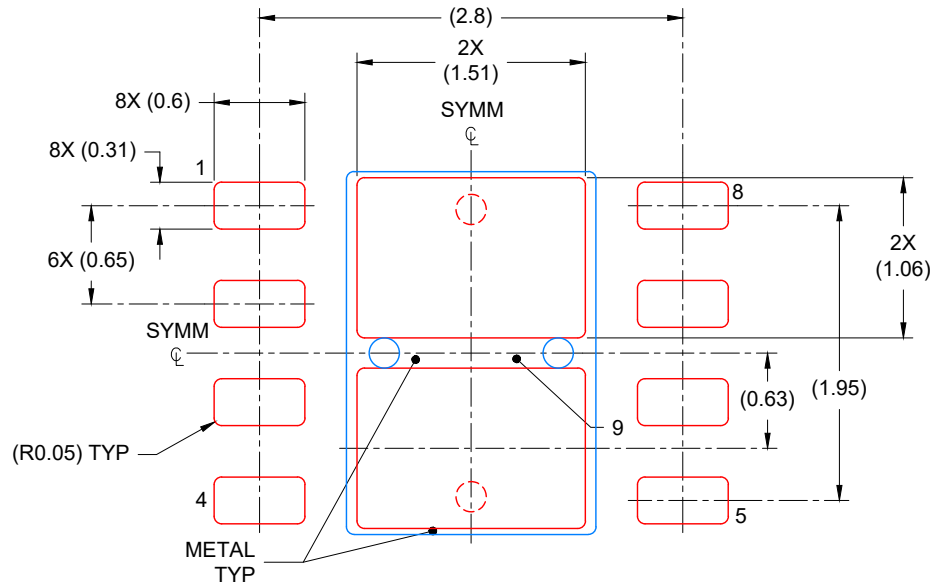


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 81% PRINTED COVERAGE BY AREA
 SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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