TCA9538 Low Voltage 8-Bit I²C and SMBus Low-Power I/O Expander with Interrupt Output, Reset, and Configuration Registers

1 Features

- Low Standby Current Consumption
- I²C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Active-Low Reset Input
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I²C Bus
- Two Hardware Address Pins Allow up to Four Devices on the I²C/SMBus
- Input and Output Configuration Register
- Polarity Inversion Register
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (example: Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

3 Description

The TCA9538 is a 16-pin device that provides 8 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V. The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA9538 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, etc.

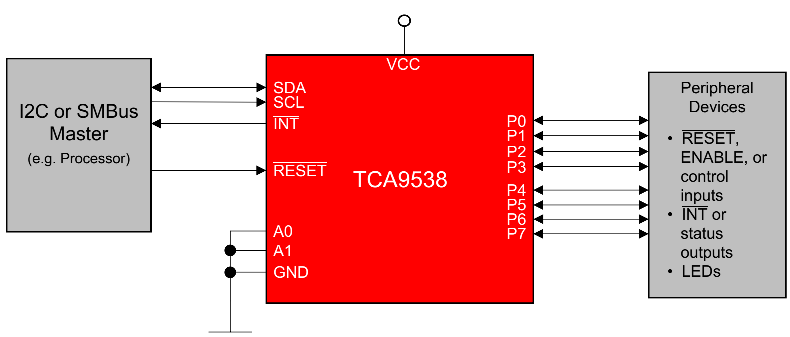
The features of the TCA9538 include an interrupt that is generated on the INT pin whenever an input port changes state. The A0 and A1 hardware selectable address pins allow up to four TCA9538 devices on the same I²C bus. The device can also be reset to its default sate by using the RESET feature or by cycling the power supply and causing a power-on reset.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9538	TSSOP (16)	5.00 mm × 4.40 mm
	SSOP (16)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D	Page
• Updated Figure 18	19

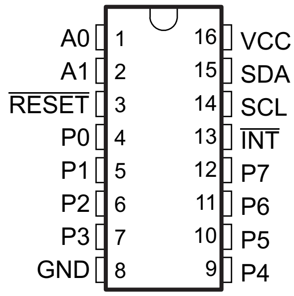
Changes from Revision B (September 2015) to Revision C	Page
• Added "Time to reset; V_{CC} = 1.65 V-2.3 V" parameter to $\overline{\text{RESET}}$ Timing Requirements table.	7
• Added "Output data valid; V_{CC} = 1.65 V-2.3 V" to Switching Characteristics table.	7
• Updated V_{CC_GW} parameter.	26

Changes from Revision A (September 2014) to Revision B	Page
• Added DB package to datasheet.	1

Changes from Original (August 2014) to Revision A	Page
• Updated document to full version.	1

5 Pin Configuration and Functions

PW, DB Package
16-Pin TSSOP, SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	1	I	Address input. Connect directly to V_{CC} or ground
A1	2	I	Address input. Connect directly to V_{CC} or ground
GND	8	—	Ground
$\overline{\text{INT}}$	13	O	Interrupt output. Connect to V_{CC} through a pull-up resistor
P0	4	I/O	P-port input-output. Push-pull design structure. At power on, P0 is configured as an input
P1	5	I/O	P-port input-output. Push-pull design structure. At power on, P1 is configured as an input
P2	6	I/O	P-port input-output. Push-pull design structure. At power on, P2 is configured as an input
P3	7	I/O	P-port input-output. Push-pull design structure. At power on, P3 is configured as an input
P4	9	I/O	P-port input-output. Push-pull design structure. At power on, P4 is configured as an input
P5	10	I/O	P-port input-output. Push-pull design structure. At power on, P5 is configured as an input
P6	11	I/O	P-port input-output. Push-pull design structure. At power on, P6 is configured as an input
P7	12	I/O	P-port input-output. Push-pull design structure. At power on, P7 is configured as an input
$\overline{\text{RESET}}$	3	I	Active-low reset input. Connect to V_{CC} through a pull-up resistor if no active connection is used
SCL	14	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	15	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
VCC	16	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage [2]		–0.5	6	V
V_O	Output voltage[2]		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current through a single P-port	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current through a single P-port	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND by all P-ports, $\overline{\text{INT}}$, and SDA			250	mA
	Continuous current through V_{CC} by all P-ports			–160	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	0.7 × V_{CC}	V_{CC}[1]	V
		A0, A1, $\overline{\text{RESET}}$, P7–P0	V_{CC} = 1.65 V to 2.7 V	0.7 × V_{CC}	5.5	
			V_{CC} = 3 V to 5.5 V	0.8 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	–0.5	0.3 × V_{CC}	V
		A0, A1, $\overline{\text{RESET}}$, P7–P0	V_{CC} = 1.65 V to 2.7 V	–0.5	0.3 × V_{CC}	
			V_{CC} = 3 V to 5.5 V	–0.5	0.2 × V_{CC}	
I_{OL}	Low-level output current	Any P-port, P7–P0			25	mA
I_{OH}	High-level output current	Any P-port, P7–P0			–10	mA
I_{CC}	Continuous current through GND	All P-ports P7-P0, $\overline{\text{INT}}$, and SDA			200	mA
	Continuous current through V_{CC}	All P-ports P7-P0			–80	
T_A	Operating free-air temperature			–40	85	°C

(1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V_{CC} in the application, or an increase in supply current, I_{CC}, will result.

6.4 Thermal Information

THERMAL METRIC(1)		TCA9538 PW (TSSOP) 16 PINS	TCA9538 DB (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	113.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	63.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	64	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.5	63.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		I_{OH} = –10 mA	1.65 V	1.1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
I_{OL}	SDA (3)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	11		mA
	P port(4)	V_{OL} = 0.5 V	1.65 V	8	10		
			2.3 V	8	13		
			3 V	8	15		
			4.5 V	8	17		
		V_{OL} = 0.7 V	1.65 V	10	14		
			2.3 V	10	17		
			3 V	10	20		
			4.5 V	10	24		
	$\overline{INT}$ (5)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	7		
I_I	SCL, SDA	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	µA
	A0, A1, $\overline{RESET}$					±1	
I_{IH}	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	1.65 V to 5.5 V			–1	µA

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V_{CC} must be limited to a maximum current of 80 mA.
(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(5) The $\overline{INT}$ pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{scl} = 400 kHz, No load t_r = 3 ns	5.5 V		18	30	μA
		$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{scl} = 400 kHz, No load $t_{r,max}$ = 300 ns	5.5 V		34		
			3.6 V		15		
			2.7 V		9		
			1.65 V		5		
		$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{scl} = 100 kHz, No load $t_{r,max}$ = 1 µs	5.5 V		20		
			3.6 V		8		
			2.7 V		5		
			1.65 V		3		
	Standby mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		1.9	3.5	μA
			3.6 V		1.1	1.8	
			2.7 V		1	1.6	
			1.65 V		0.4	1	
ΔI_{CC}	Additional current in standby mode	One P-port input at V_{CC} – 0.6 V, Other P-port inputs at V_{CC} or GND	1.65 V to 5.5 V			70	μA
C_i	SCL	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

6.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 9)

			MIN	MAX	UNIT
STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		µs
t_{sth}	I²C Start or repeated Start condition hold		4		µs
t_{sps}	I²C Stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	ns
FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns

I²C Interface Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted) (see Figure 9)

			MIN	MAX	UNIT
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{DD} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{DD} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	ns

6.7 $\overline{\text{RESET}}$ Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
STANDARD and FAST MODE				
t_w	Reset pulse duration	4		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset; V_{CC} = 2.3 V-5.5 V	400		ns
	Time to reset; V_{CC} = 1.65 V-2.3 V	550		

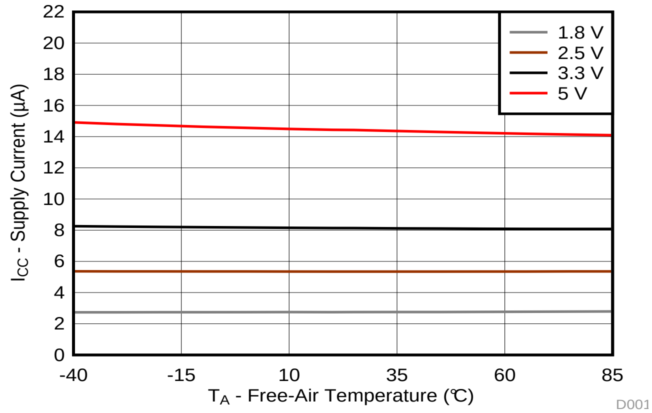
6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 10 and Figure 11)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
STANDARD and FAST MODE						
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid; V_{CC} = 2.3 V-5.5 V	SCL	P7–P0		200	ns
	Output data valid; V_{CC} = 1.65 V-2.3 V				300	
t_{ps}	Input data setup time	P port	SCL	100		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

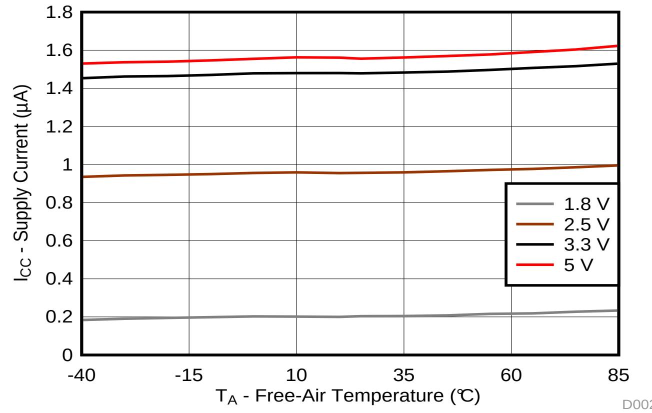
6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)



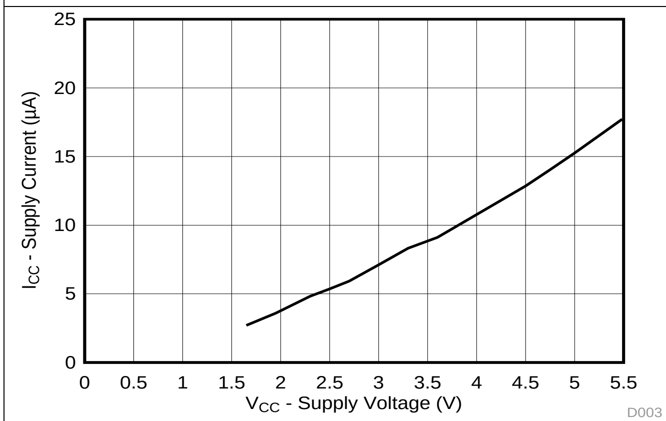
f_{SCL} = 400 kHz I/Os = High or Low Inputs

Figure 1. Supply Current (I_{CC}, Operating Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 0 kHz I/Os = High or Low Inputs

Figure 2. Supply Current (ICC, Standby Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 400 kHz I/Os = High or Low Inputs T_A = 25°C

Figure 3. Supply Current (I_{CC}, Operating Mode) vs Supply Voltage (V_{CC})

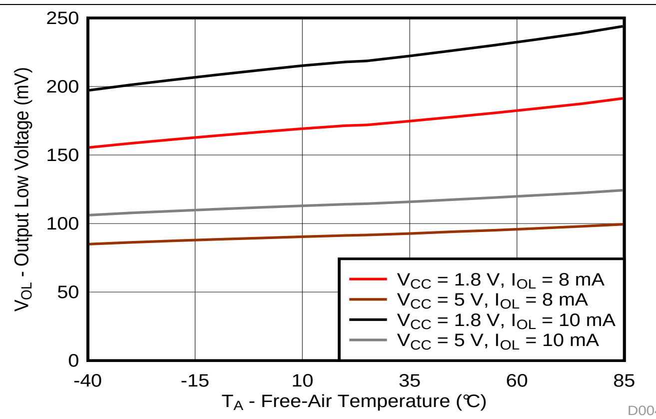
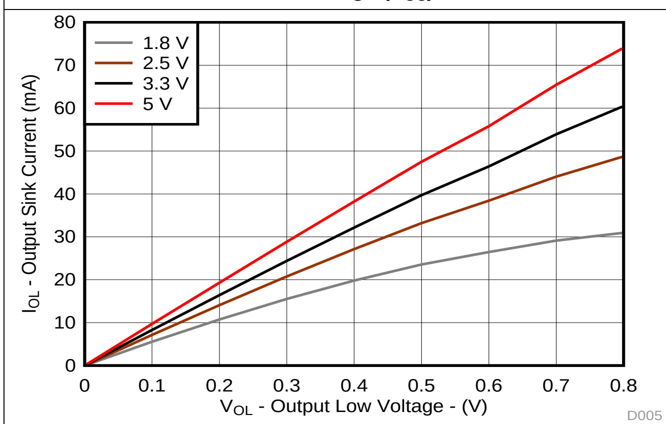


Figure 4. Output Low Voltage (V_{OL}) vs Temperature (T_A) for P-Port I/Os



T_A = 25°C

Figure 5. Sink Current (I_{OL}) vs Output Low Voltage (V_{OL}) for P-Ports at Four Supply Voltages

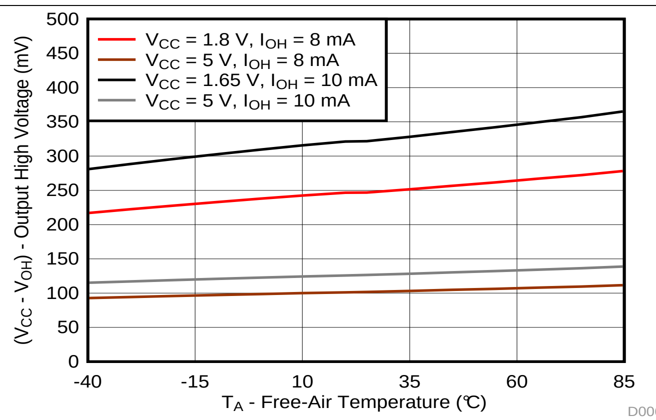
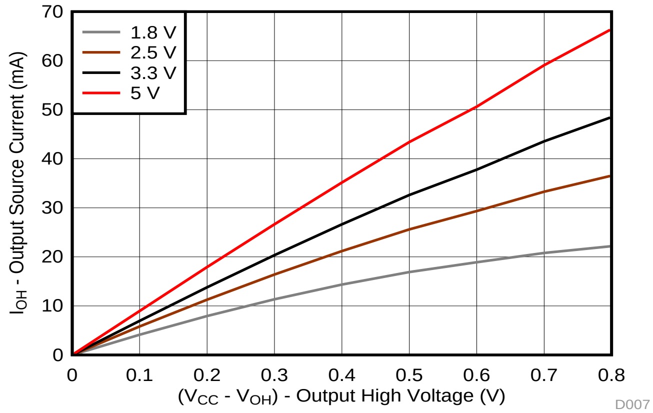


Figure 6. Output High Voltage (V_{CC} – V_{OH}) vs Temperature (T_A) for P-Ports

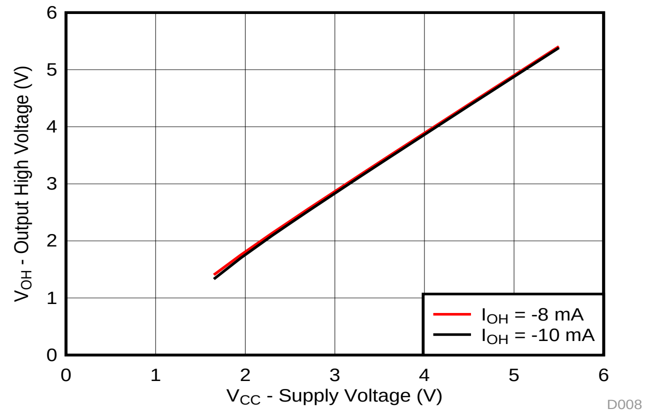
Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



T_A = 25°C

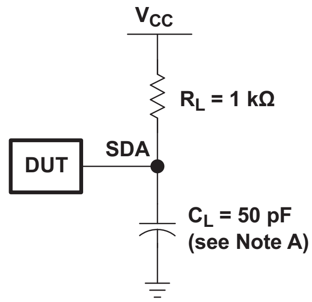
Figure 7. Source Current (I_{OH}) vs Output High Voltage (V_{OH}) for P-Ports at Four Supply Voltages



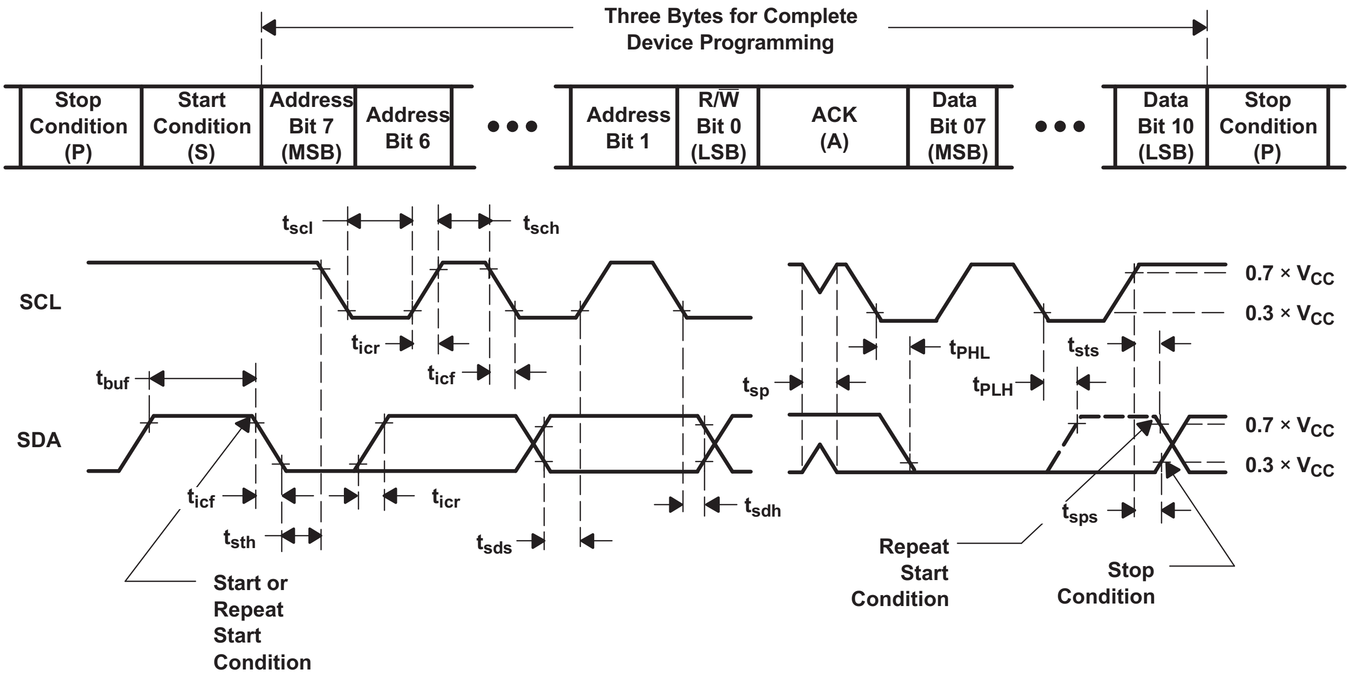
T_A = 25°C

Figure 8. Output High Voltage (V_{OH}) vs Supply Voltage (V_{CC}) for P-Ports

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

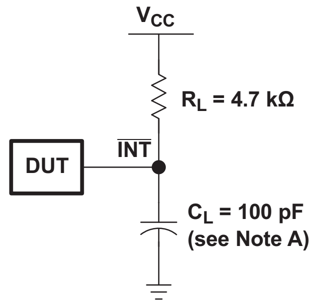
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

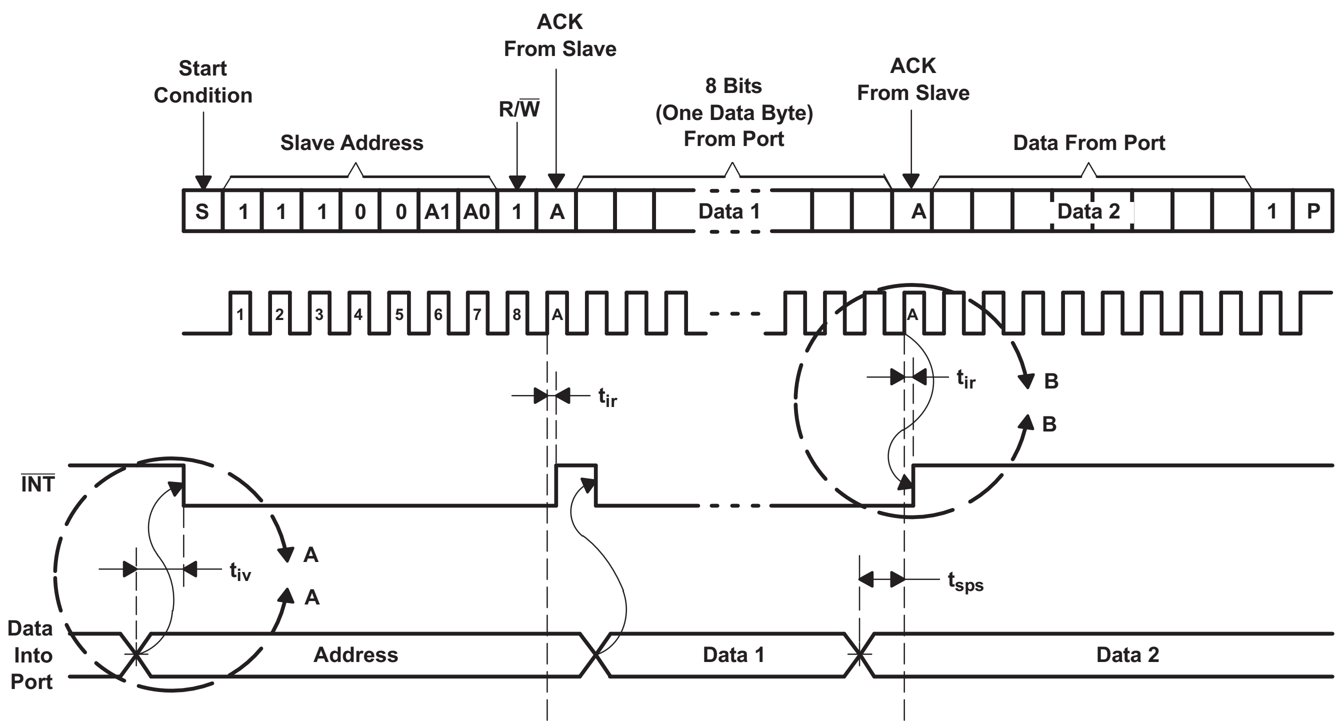
C. All parameters and waveforms are not applicable to all devices.

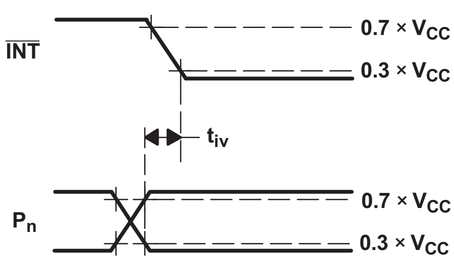
Figure 9. I²C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

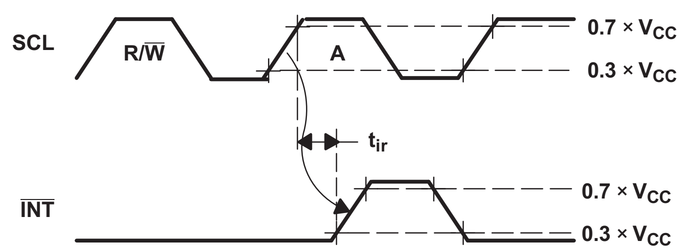


INTERRUPT LOAD CONFIGURATION





View A−A



View B−B

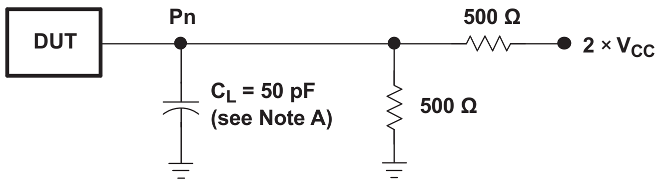
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

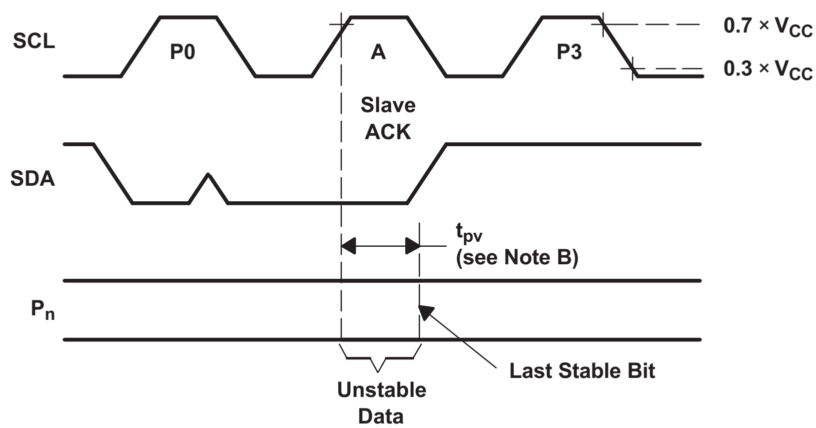
C. All parameters and waveforms are not applicable to all devices.

Figure 10. Interrupt Load Circuit and Voltage Waveforms

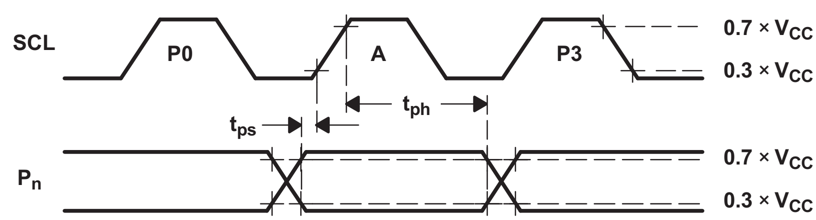
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)

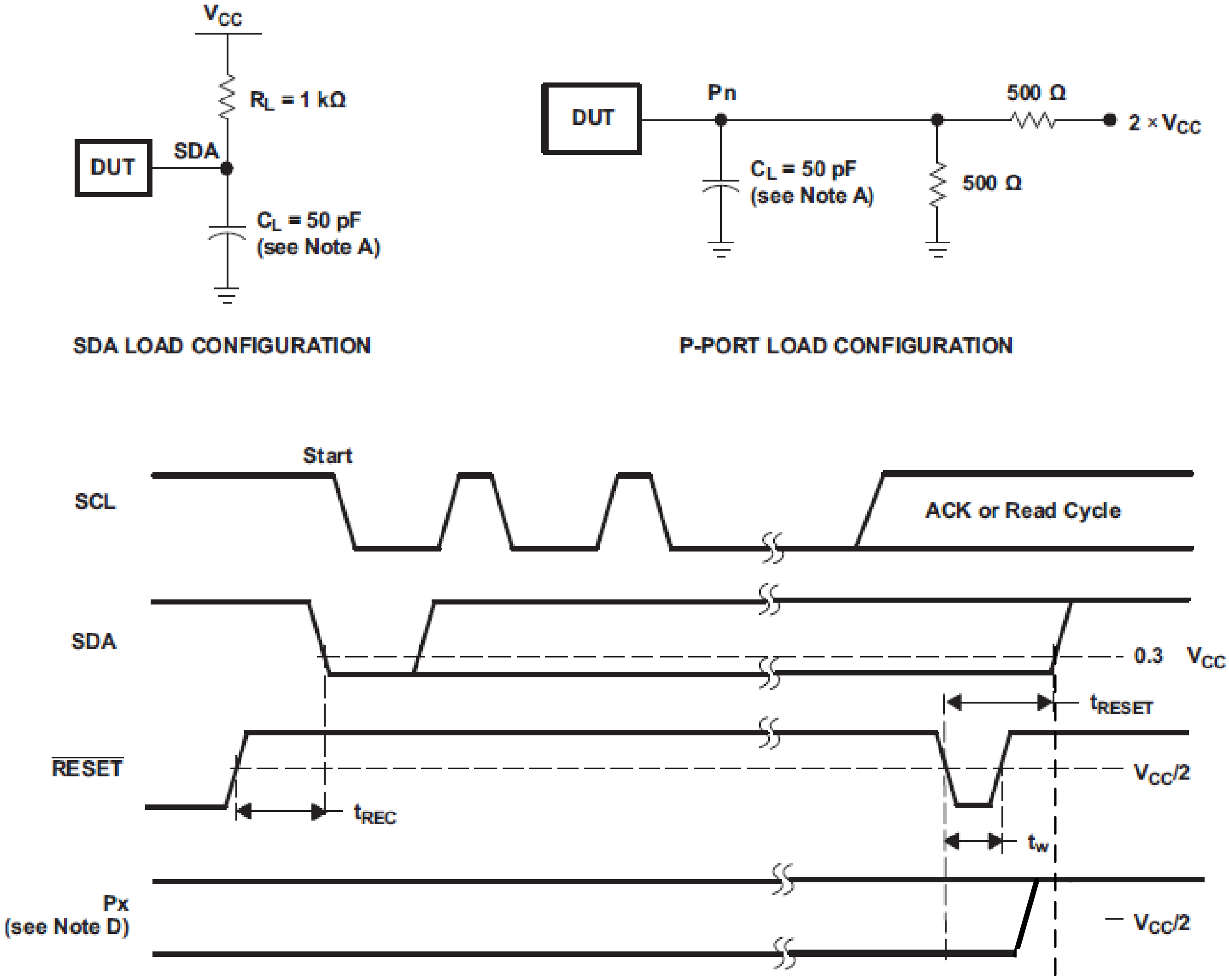


READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. All parameters and waveforms are not applicable to all devices.

Figure 11. P-Port Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 12. Reset Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9538 is an 8-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I^2C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9538 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I2C bus. Thus, the TCA9538 can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

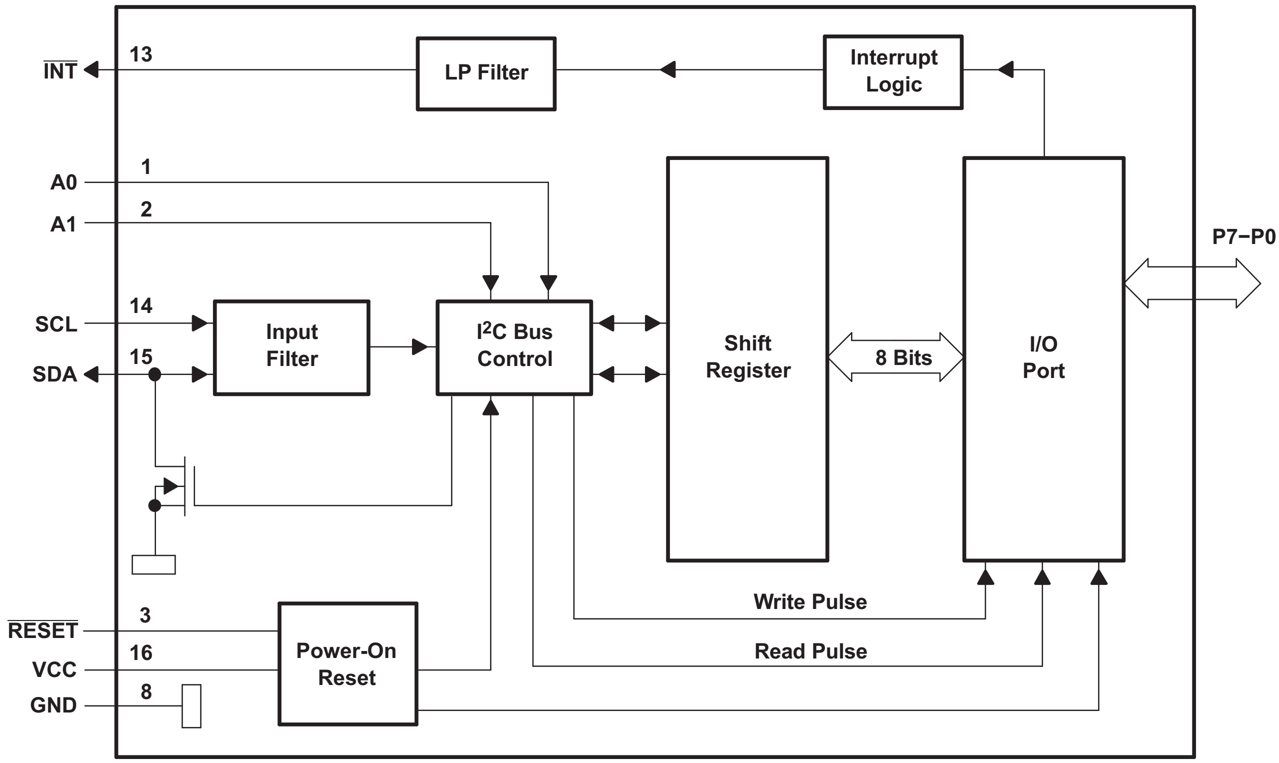
Two hardware pins (A0 and A1) are used to program and vary the fixed I^2C slave address and allow up to four devices to share the same I^2C bus or SMBus.

The system master can reset the TCA9538 in the event of a timeout or other improper operation by asserting a low on the $\overline{RESET}$ input pin or by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I^2C /SMBus state machine. The $\overline{RESET}$ feature and a POR cause the same reset/initialization to occur, but the $\overline{RESET}$ feature does so without powering down the part.

The TCA9538 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9538 is identical to the TCA9554 except for the removal of the internal I/O pull-up resistors, which greatly reduces power consumption when the I/Os are held LOW, the replacement of A2 with $\overline{RESET}$, and different slave address range.

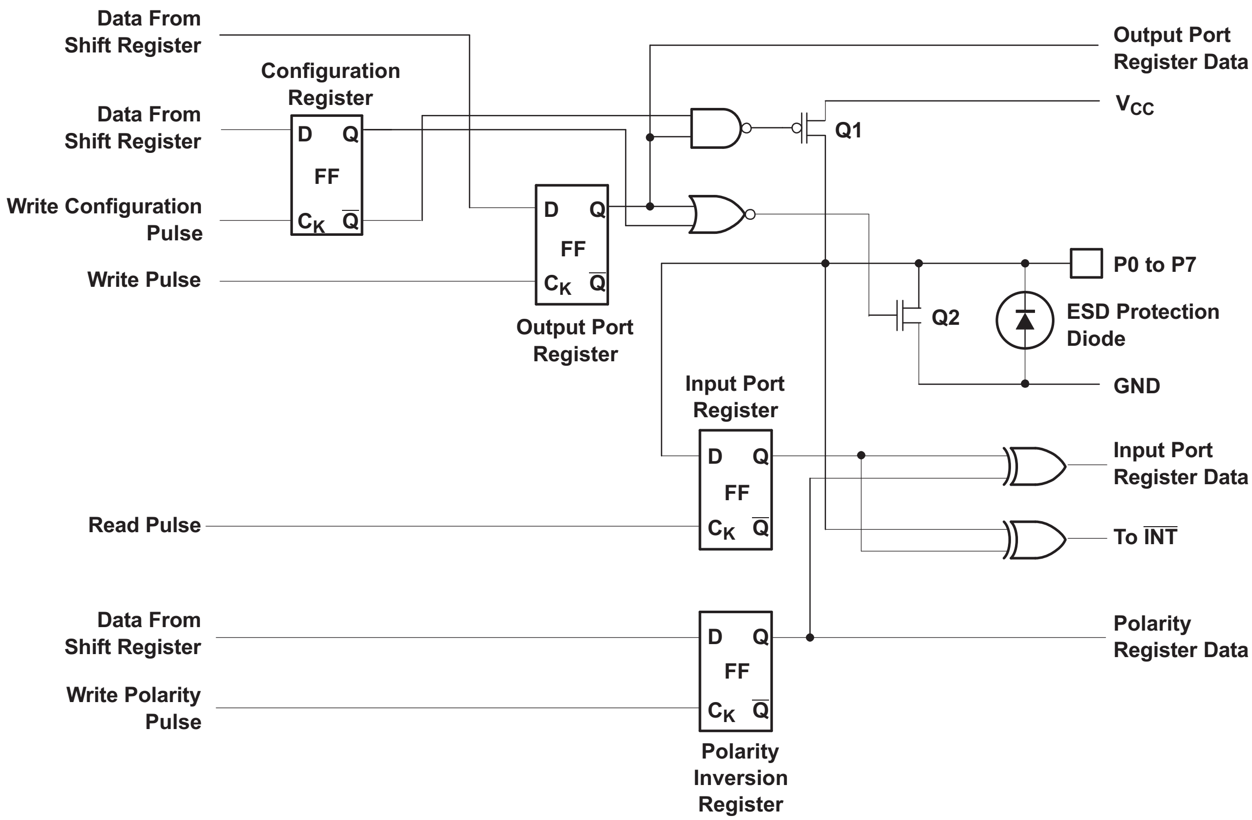
8.2 Functional Block Diagram



Pin numbers shown are for the PW package.

Figure 13. Functional Block Diagram

Functional Block Diagram (continued)



At power-on reset, all registers return to default values.

Figure 14. Simplified Schematic of P0 to P7

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

8.3.2 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of any P-port I/O configured as an input. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the ports is changed back to the original state or when data is read from the Input Port register. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as an interrupt on the $\overline{INT}$ pin.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

Feature Description (continued)

8.3.3 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be asserted to reset the system while keeping the V_{CC} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA9538 registers and I²C/SMBus state machine are changed to their default states once $\overline{\text{RESET}}$ is low (0). Once $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to V_{CC} if no active connection is used.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to VCC, an internal power-on reset holds the TCA9538 in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9538 registers and SMBus/I²C state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and then back up to the operating voltage for a power-on reset cycle.

8.5 Programming

8.5.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 15). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{\text{W}}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A1) of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 16).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 15).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 17). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

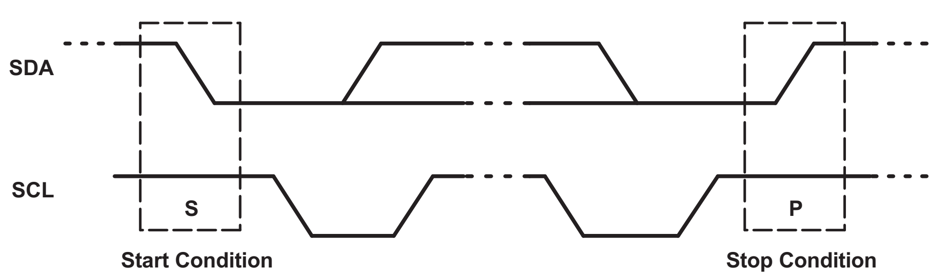


Figure 15. Definition of Start and Stop Conditions

Programming (continued)

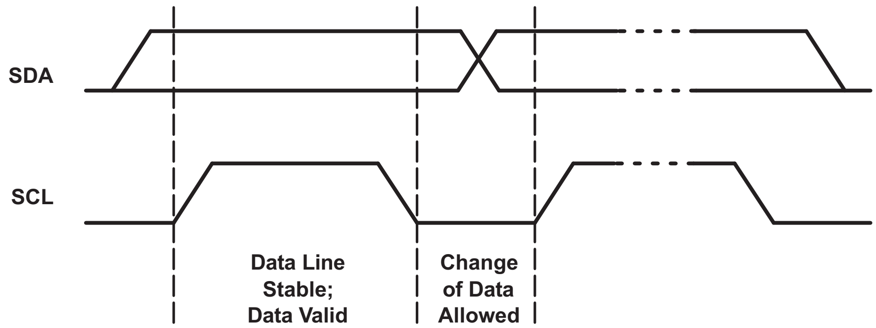


Figure 16. Bit Transfer

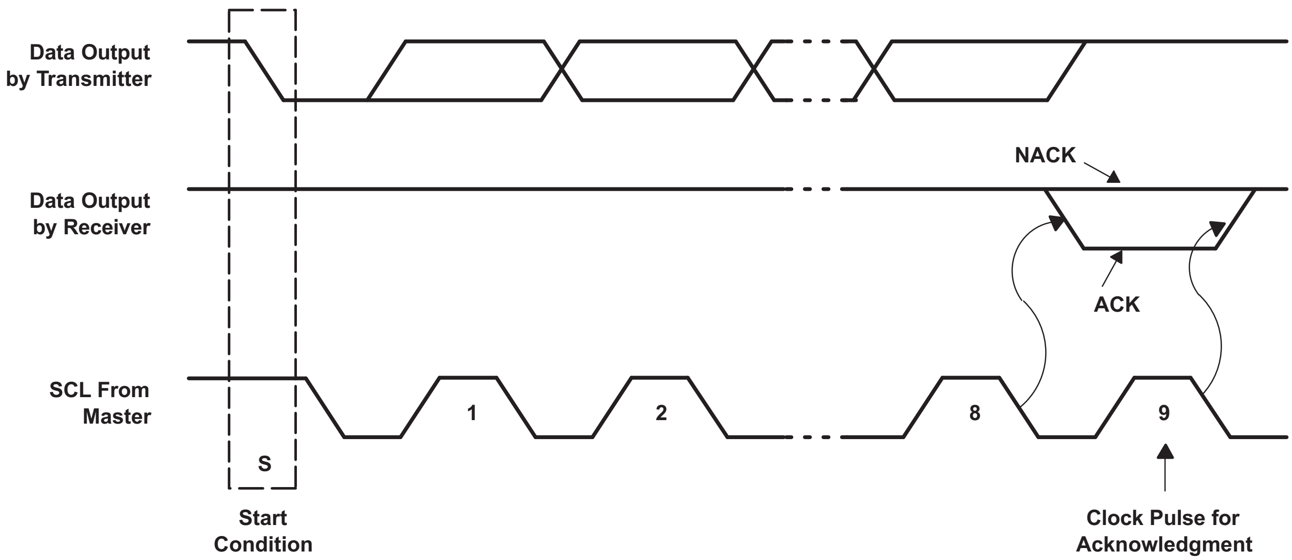


Figure 17. Acknowledgment on I²C Bus

Table 1 shows the TCA9538 interface definition.

Table 1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	H	H	H	L	L	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.6 Register Map

8.6.1 Device Address

Figure 18 shows the address byte of the TCA9538.

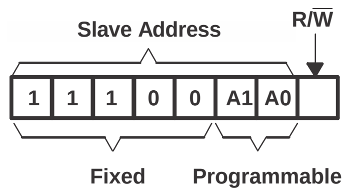


Figure 18. TCA9538 Address

Table 2 shows the Address Reference of the TCA9538.

Table 2. Address Reference Table

INPUTS		I^2C BUS SLAVE ADDRESS
A1	A0	
L	L	112 (decimal), 70 (hexadecimal)
L	H	113 (decimal), 71 (hexadecimal)
H	L	114 (decimal), 72 (hexadecimal)
H	H	115 (decimal), 73 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9538 (see Figure 19). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	B2	B1	B0

Figure 19. Control Register Bits

Table 3 shows the TCA9538 Command byte.

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next. See Table 4.

Table 4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See Table 5.

Table 5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See Table 6.

Table 6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See Table 7.

Table 7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9538 through write and read commands.

8.6.3.1.1 Writes

Data is transmitted to the TCA9538 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 20 and Figure 21). There is no limitation on the number of data bytes sent in one write transmission.

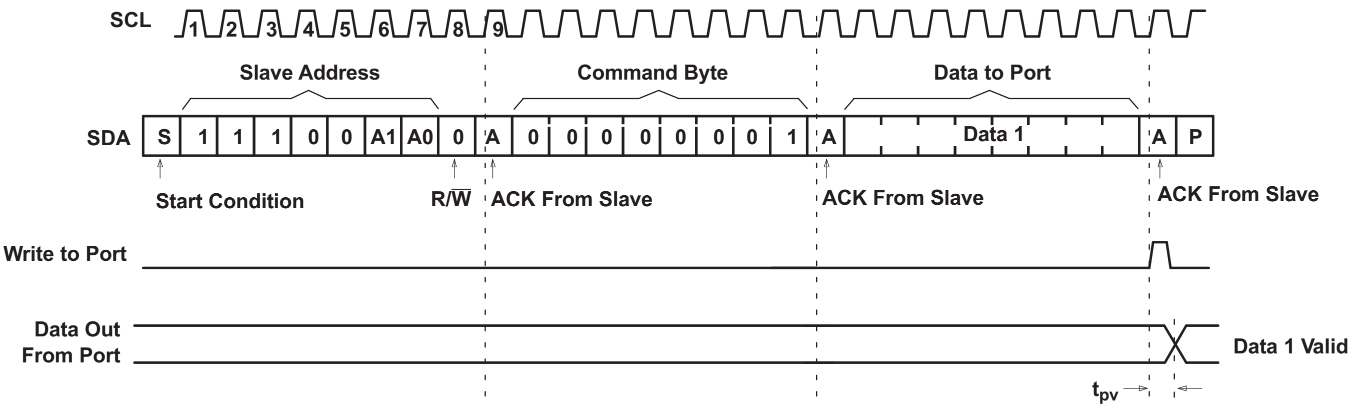


Figure 20. Write to Output Port Register

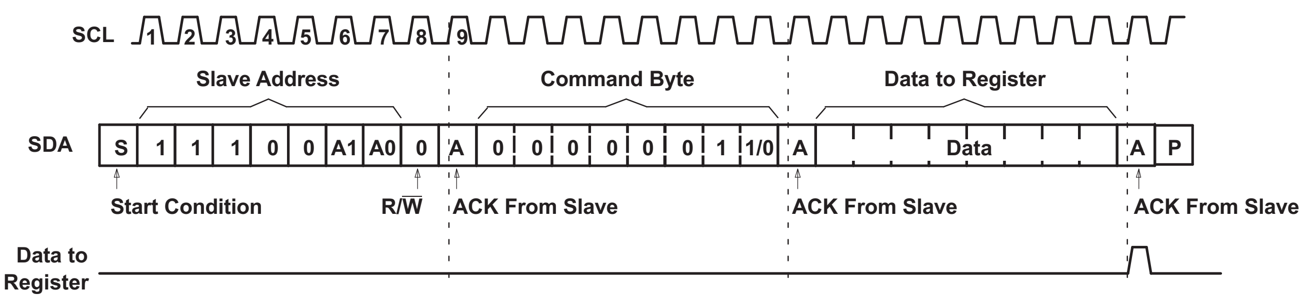


Figure 21. Write to Configuration or Polarity Inversion Registers

8.6.3.1.2 Reads

The bus master first must send the TCA9538 address with the LSB set to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9538 (see Figure 22 and Figure 23). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

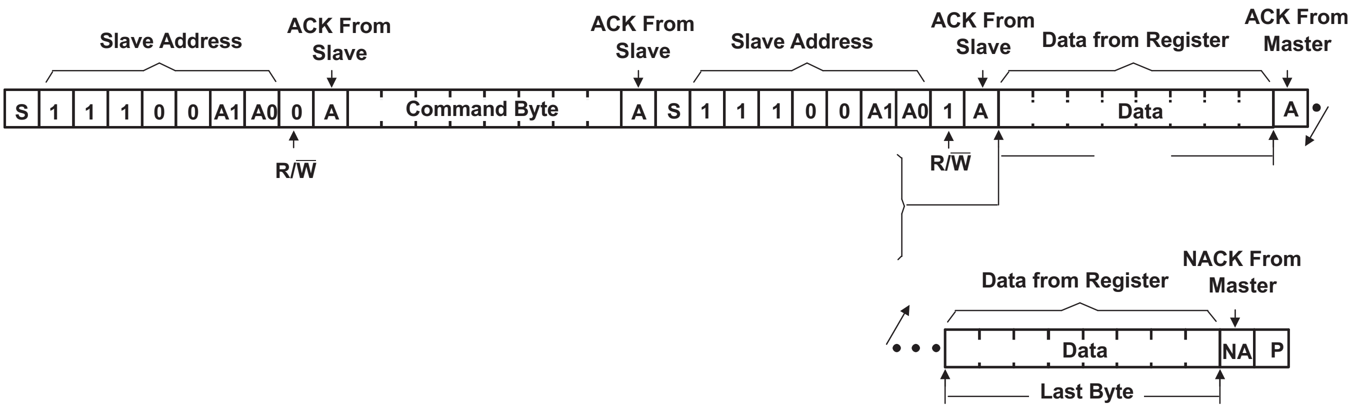
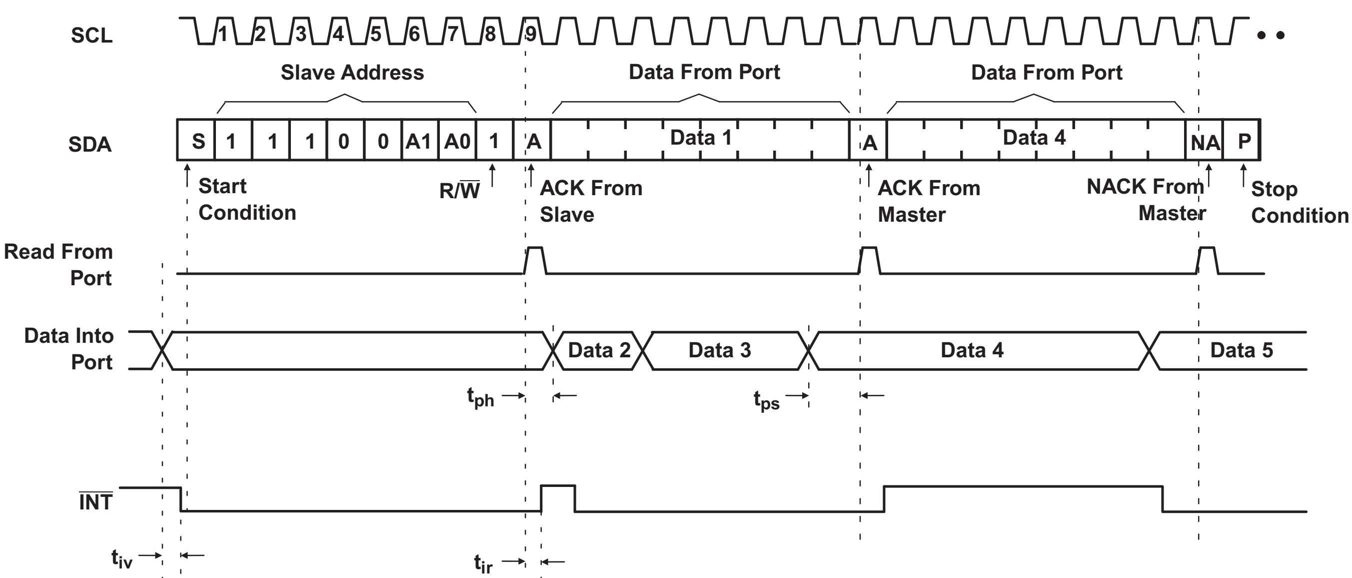


Figure 22. Read From Register



A. This figure assumes the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See Figure 22 for these details.

Figure 23. Read From Input Port Register

9 Application and Implementation

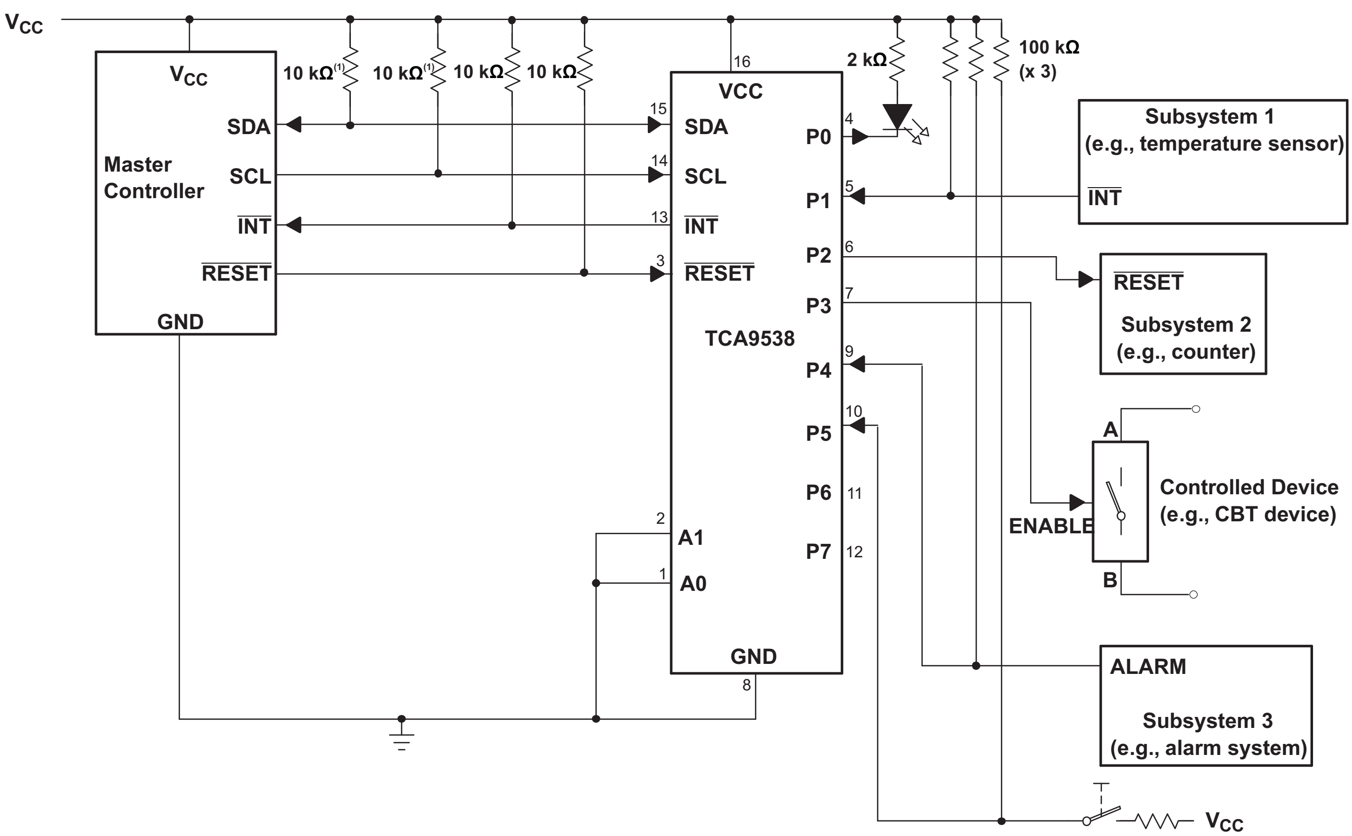
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 24 shows an application in which the TCA9538 can be used.

9.2 Typical Application



(1) The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, increases as a result.

A. Device address is configured as 1110000 for this example.

B. P0, P2, and P3 are configured as outputs.

C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and must be configured as outputs.

Figure 24. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 24. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED is off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 25 shows a high-value resistor in parallel with the LED. Figure 26 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

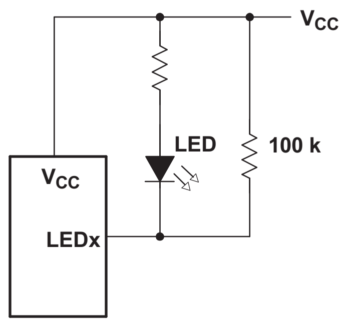


Figure 25. High-Value Resistor in Parallel with LED

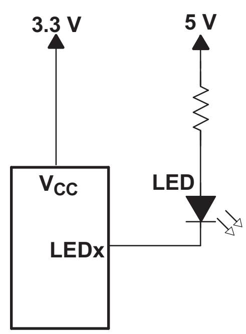


Figure 26. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 1:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{1}$$

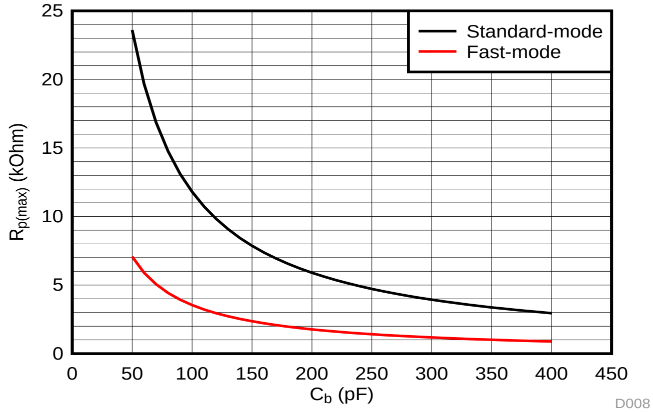
The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9538, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

Typical Application (continued)

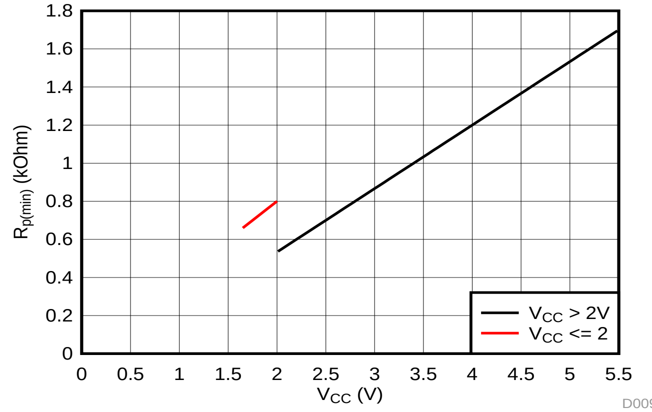
9.2.3 Application Curves



Standard-mode
(f_{SCL} = 100 kHz, t_r = 1 µs)

Fast-mode
(f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 27. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



$V_{OL} = 0.2*V_{CC}$, I_{OL} = 2 mA
when $V_{CC} \leq 2$ V

V_{OL} = 0.4 V, I_{OL} = 3 mA
when V_{CC} > 2 V

Figure 28. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the TCA9538 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and Figure 29.

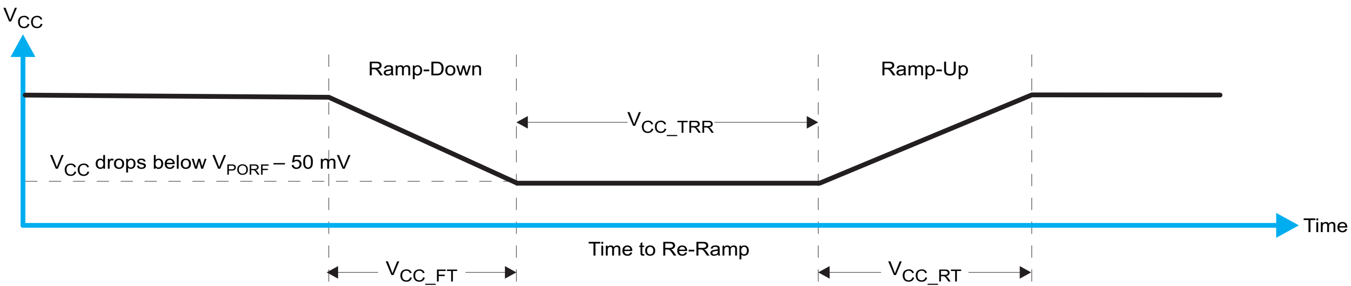


Figure 29. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 8 specifies the performance of the power-on reset feature for the TCA9538 for both types of power-on reset.

Table 8. Recommended Supply Sequencing And Ramp Rates[(1)]

PARAMETER			MIN	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 29	1		ms
V_{CC_RT}	Rise rate	See Figure 29	0.1		ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 29	2		µs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs	See Figure 30		1.2	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when $V_{CC\_GH} = 0.5 \times V_{CC}$ (For VCC > 3 V)	See Figure 30		10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 30 and Table 8 provide more information on how to measure these specifications.

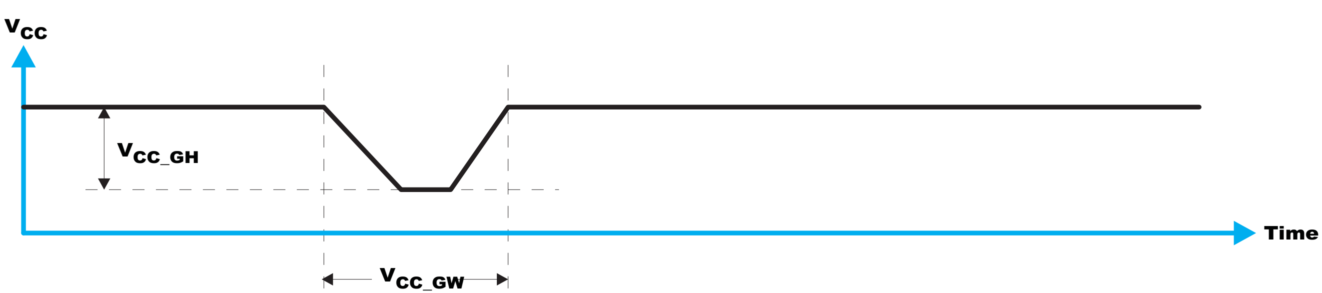


Figure 30. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 31 and Table 8 provide more details on this specification.

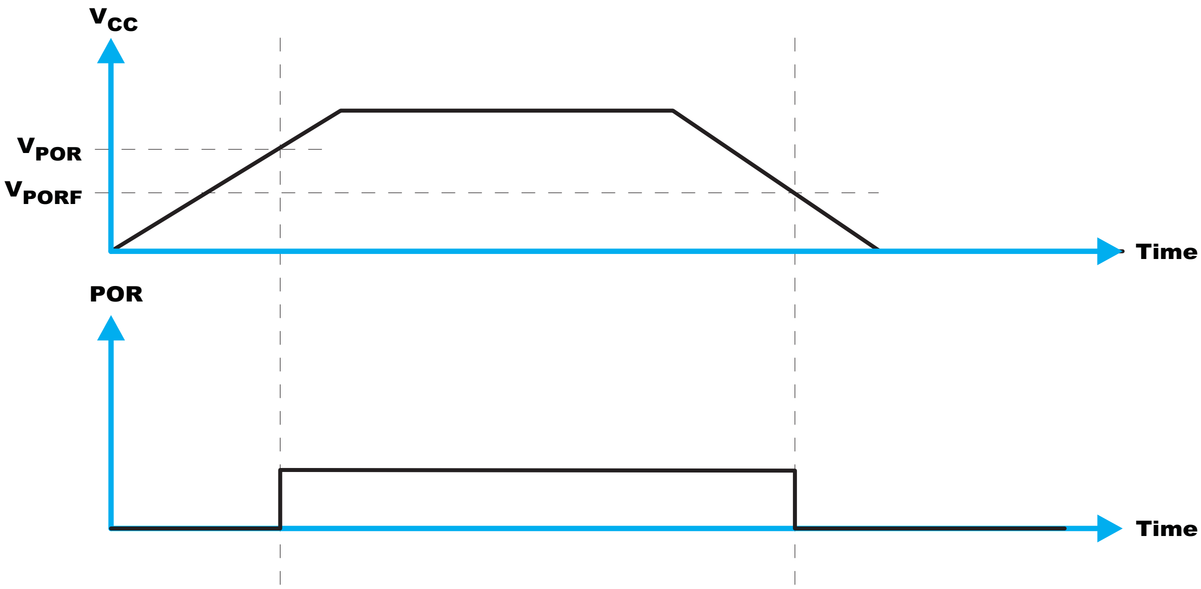


Figure 31. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9538, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9538 as possible. These best practices are shown in Figure 32.

For the layout example provided in Figure 32, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 32.

11.2 Layout Example

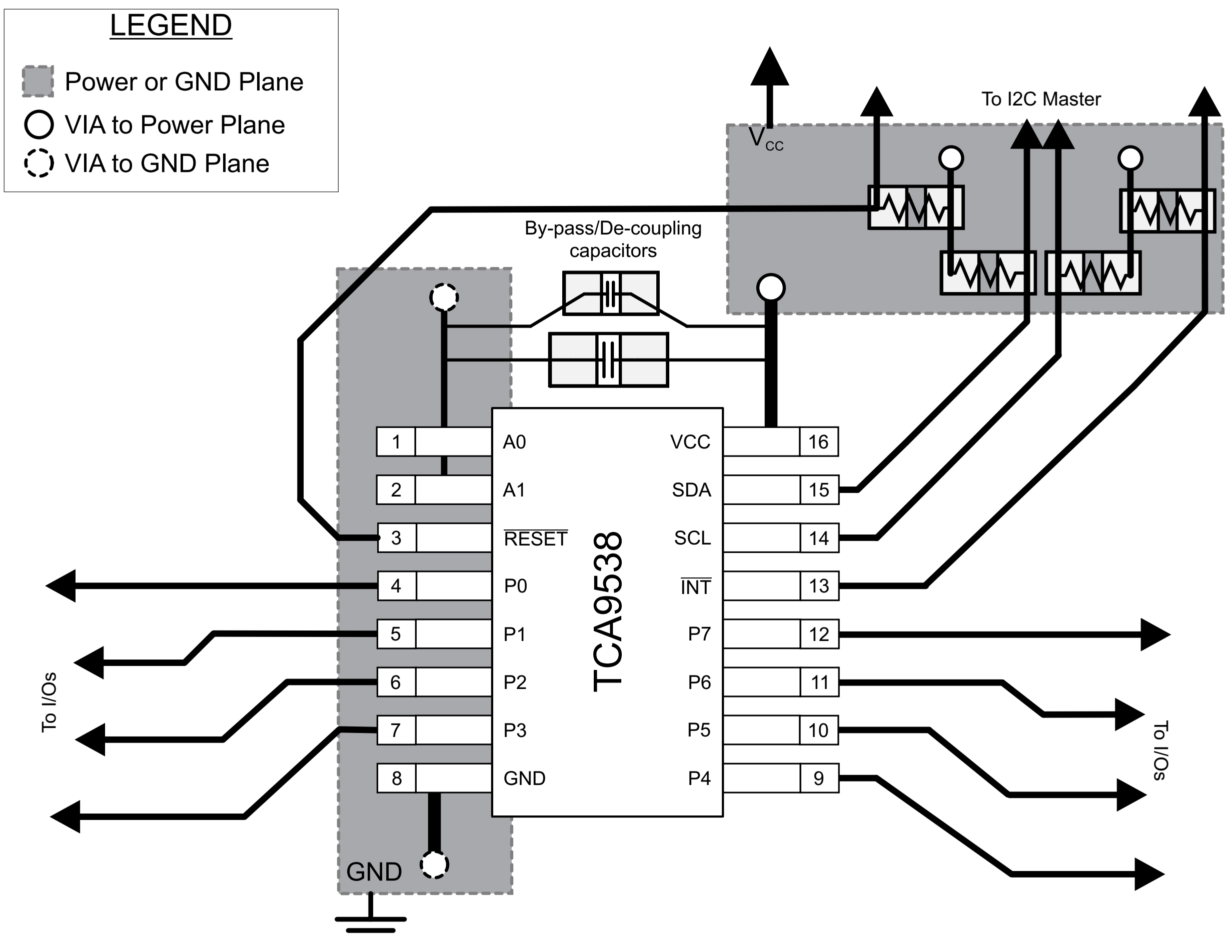


Figure 32. TCA9538 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *I2C Bus Pull-Up Resistor Calculation*
- *Maximum Clock Frequency of I2C Bus Using Repeaters*
- *Introduction to Logic*
- *Understanding the I2C Bus*
- *Choosing the Correct I2C Device for New Designs*
- *I/O Expander EVM User's Guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9538DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538DBR.B	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538DBRG4	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538DBRG4.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538DBRG4.B	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD538
TCA9538PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538
TCA9538PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538
TCA9538PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538
TCA9538PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538
TCA9538PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538
TCA9538PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW538

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

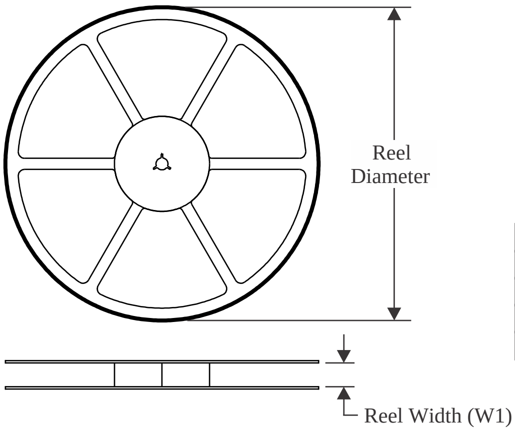
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

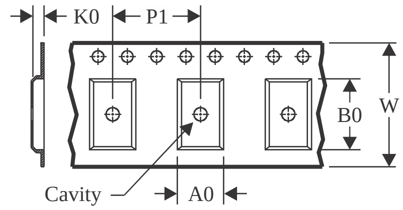
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

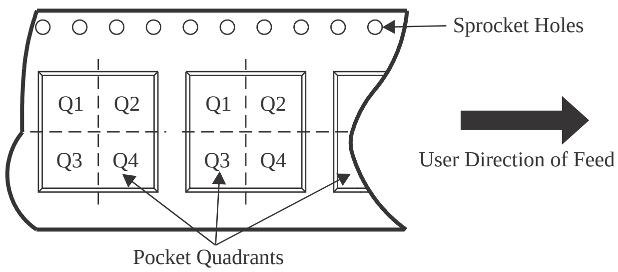


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

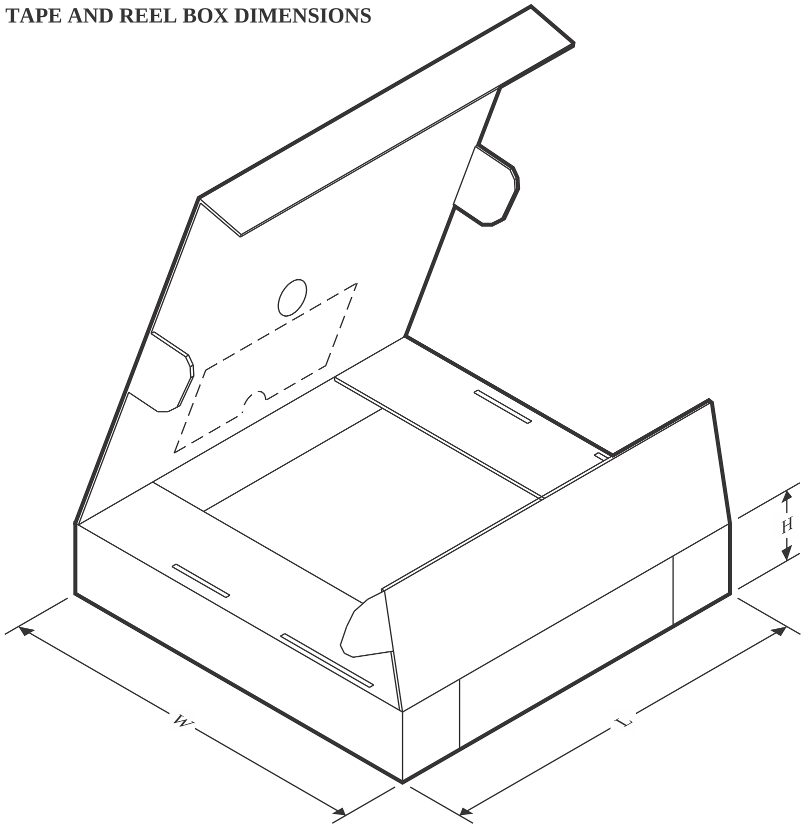
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

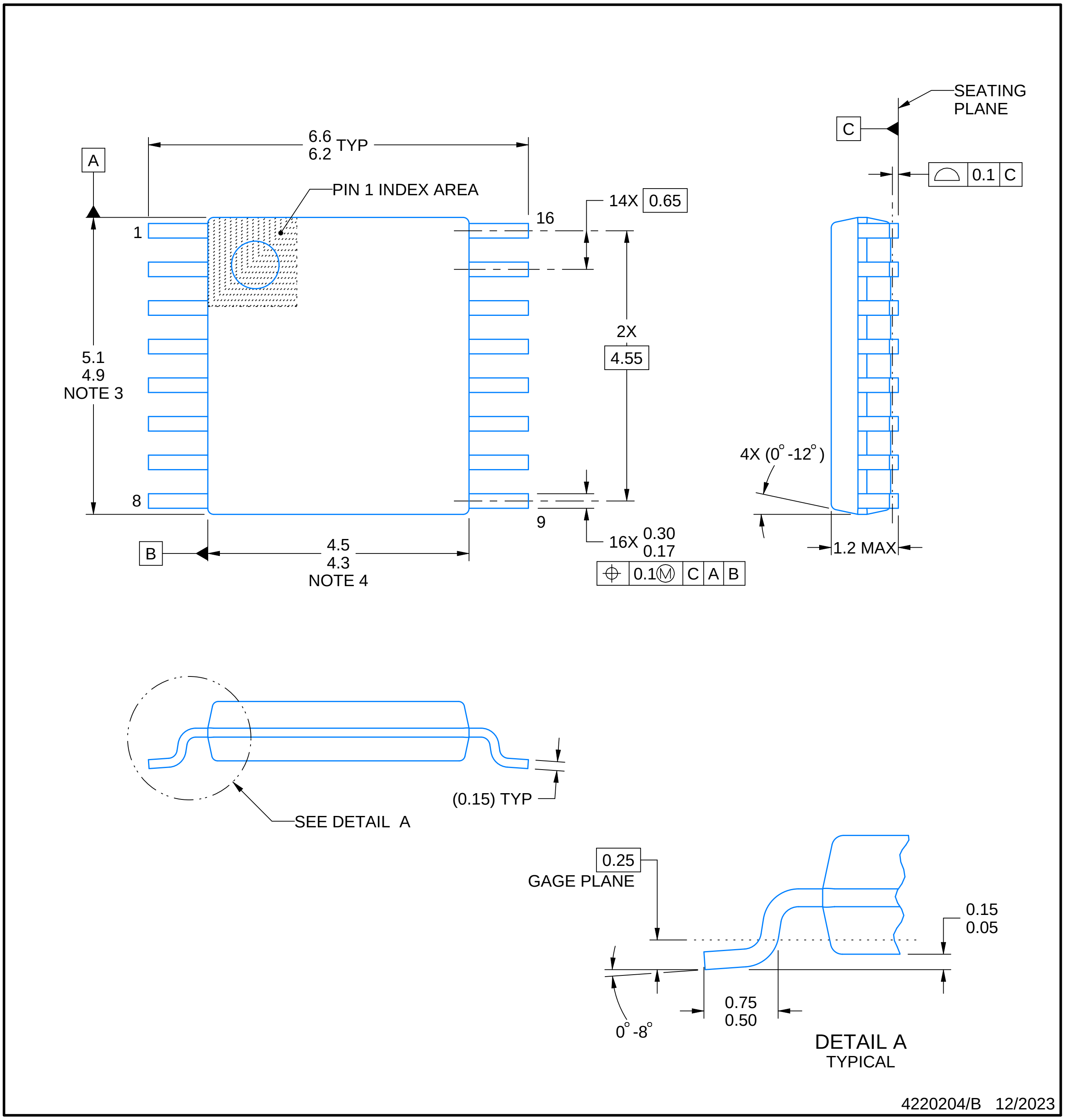
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9538DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TCA9538DBRG4	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TCA9538PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TCA9538PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

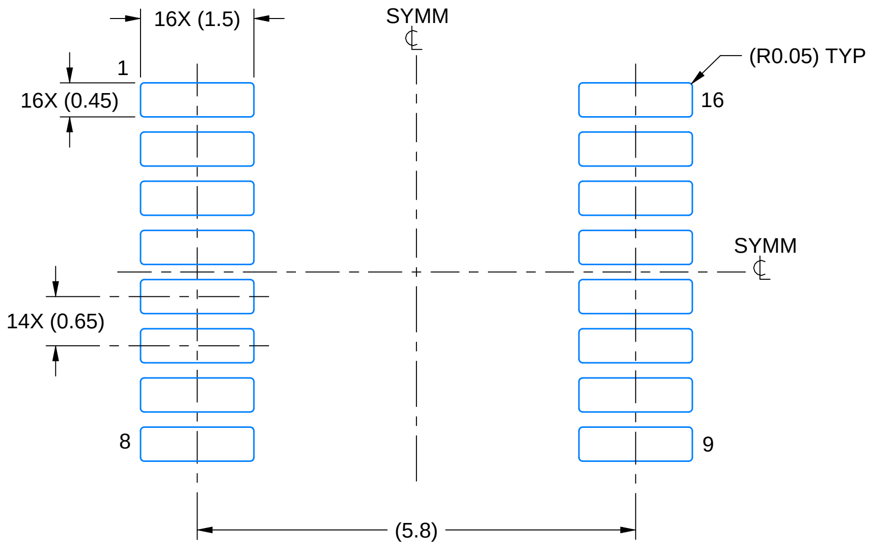
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9538DBR	SSOP	DB	16	2000	353.0	353.0	32.0
TCA9538DBRG4	SSOP	DB	16	2000	353.0	353.0	32.0
TCA9538PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TCA9538PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0



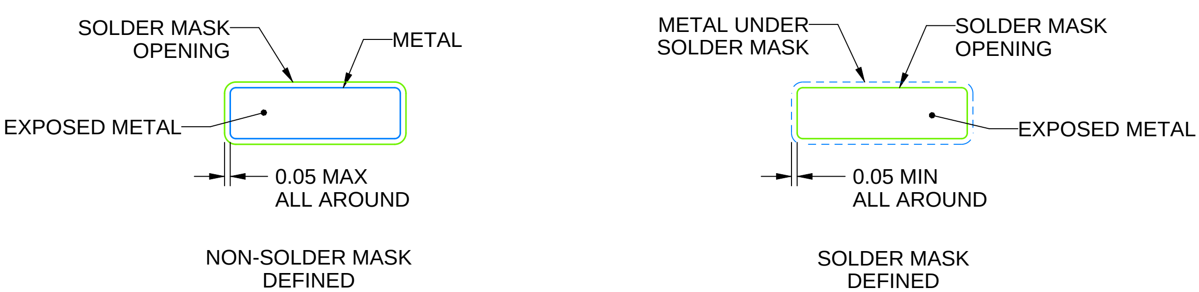
4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

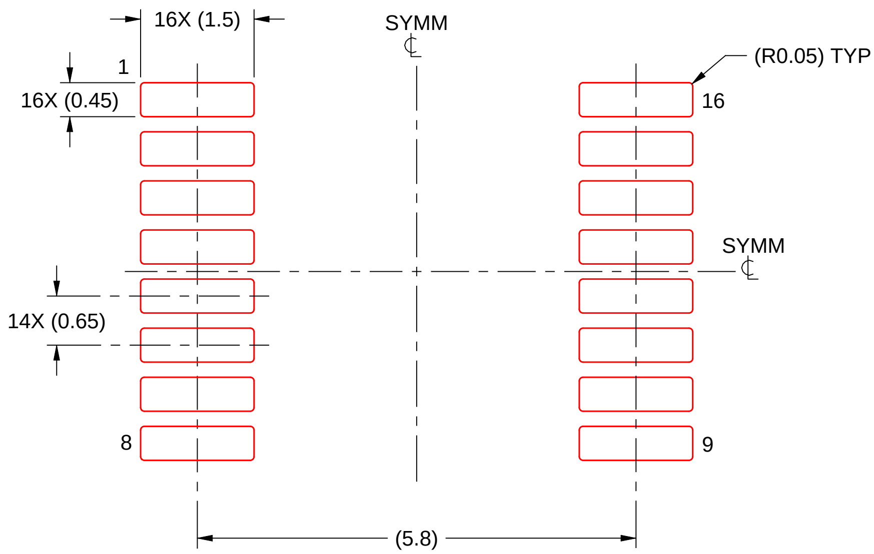


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

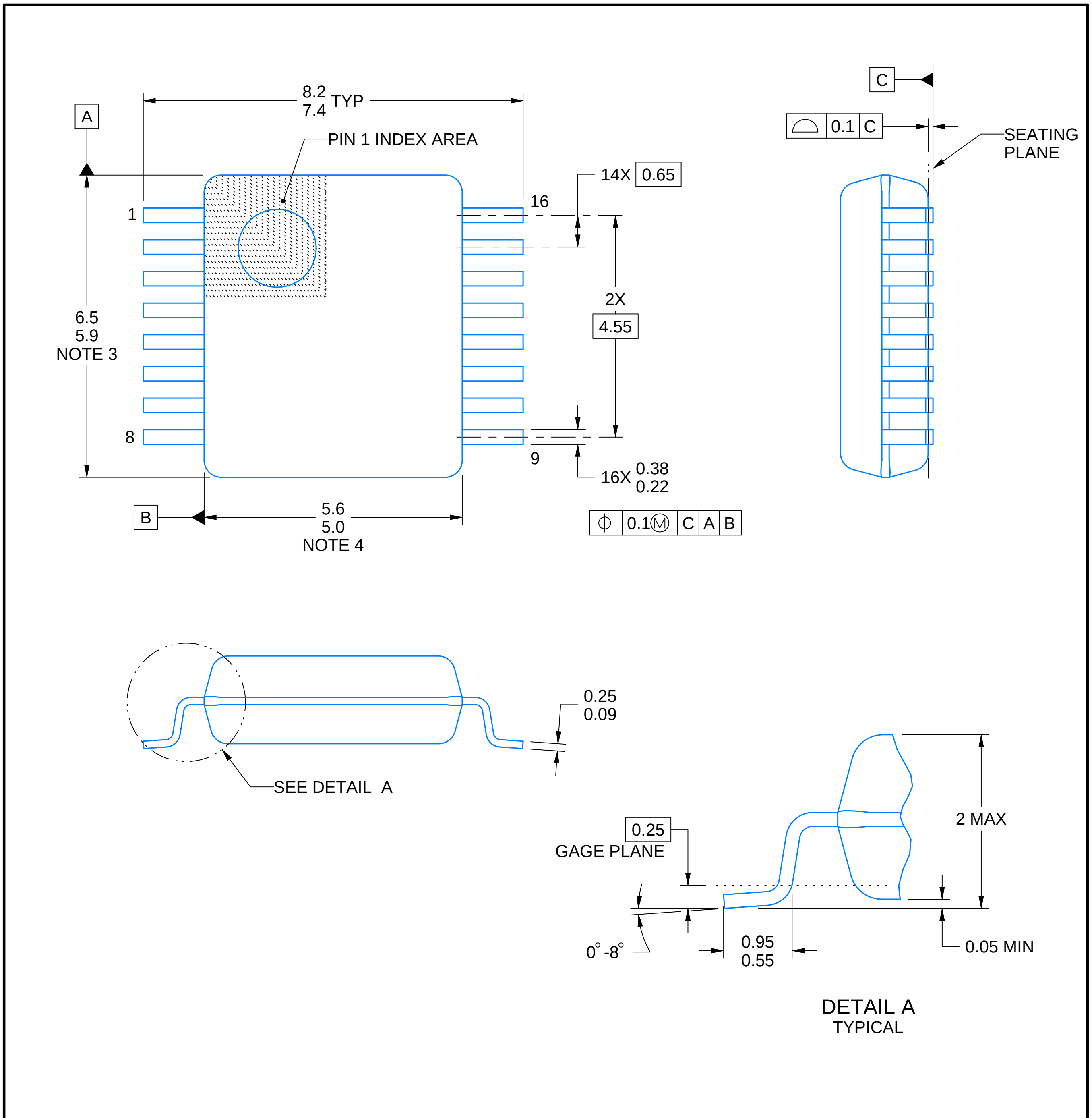


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

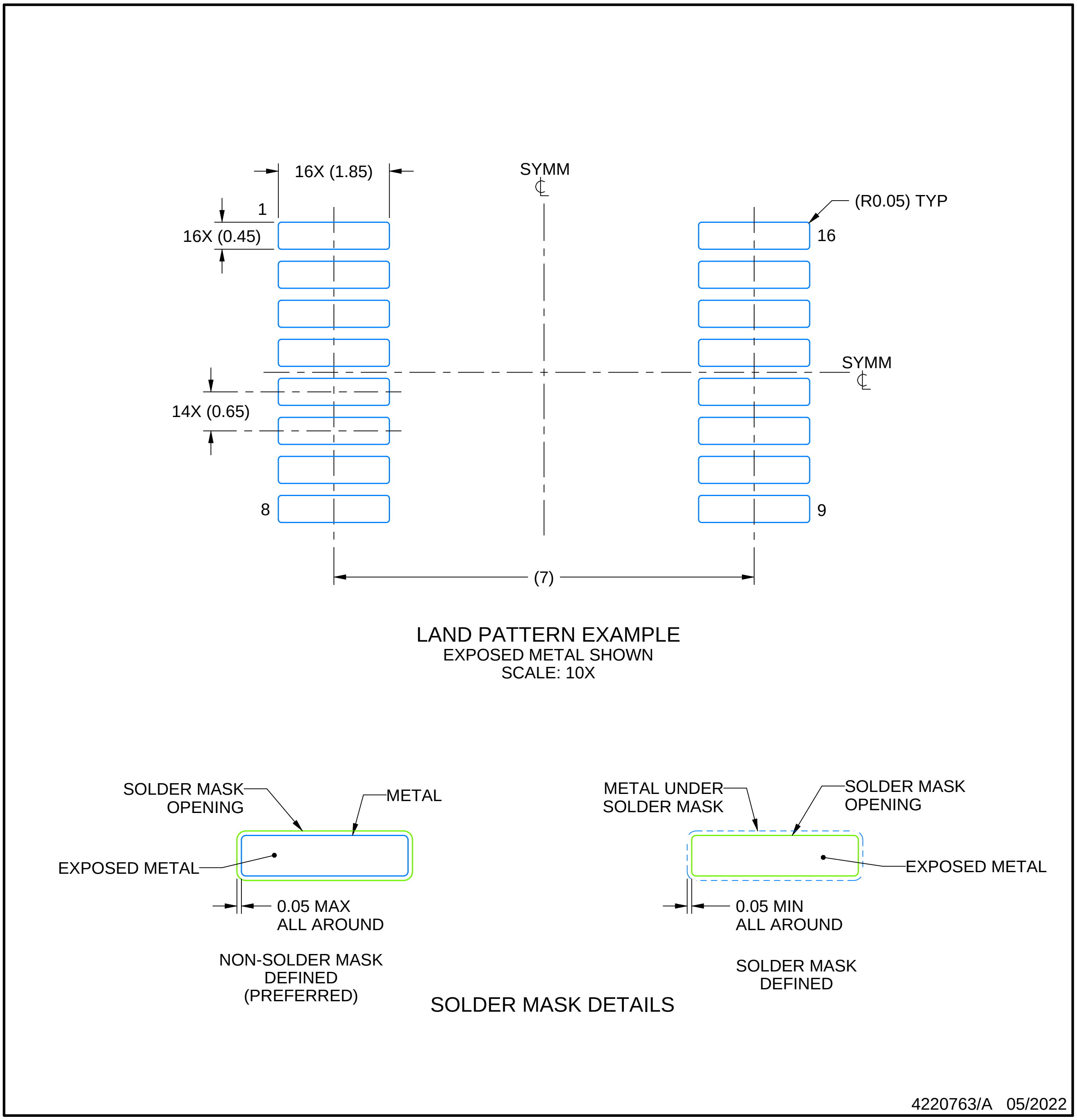
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

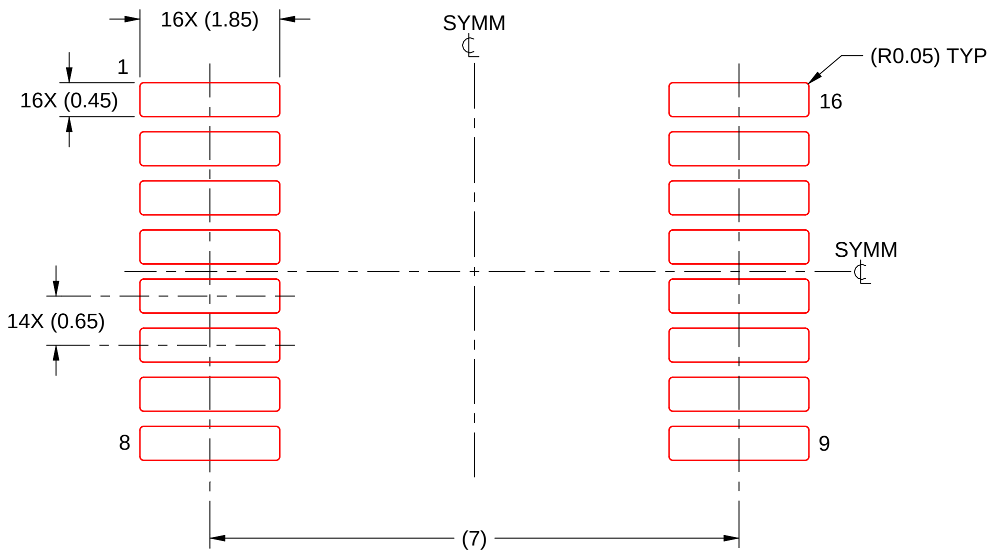
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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