

# TCA9534A Low Voltage 8-Bit I<sup>2</sup>C and SMBUS Low-Power I/O Expander With Interrupt Output and Configuration Registers

## 1 Features

- Low Standby Current Consumption
- I<sup>2</sup>C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I<sup>2</sup>C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I<sup>2</sup>C/SMBus
- Input and Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (for example: Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

## 3 Description

The TCA9534A is a 16-pin device that provides 8 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I<sup>2</sup>C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V, which allows for use with a wide range of devices. The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA9534A provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

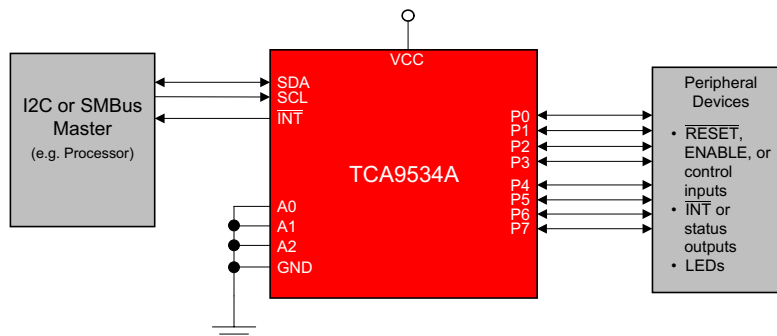
The features of the TCA9534A include an interrupt that is generated on the INT pin. This allows the master to know when an input port changes state. The A0, A1, and A2 hardware selectable address pins allow up to eight TCA9534A devices on the same I<sup>2</sup>C bus. The device can also be reset to its default state by cycling the power supply and causing a power-on reset.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| TCA9534A    | TSSOP (16) | 5.00 mm × 4.40 mm  |
|             | SOIC (16)  | 10.30 mm × 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (December 2016) to Revision C | Page |
|-------------------------------------------------------|------|
| • Updated <a href="#">Figure 20</a> .....             | 13   |
| • Updated address in <a href="#">Table 1</a> .....    | 18   |

| Changes from Revision A (September 2014) to Revision B                                                       | Page |
|--------------------------------------------------------------------------------------------------------------|------|
| • Updated the <a href="#">Description</a> section .....                                                      | 1    |
| • Added DW package.....                                                                                      | 1    |
| • Corrected ESD ratings to reflect $\pm$ ratings .....                                                       | 5    |
| • VIH values, improved performance .....                                                                     | 5    |
| • Made changes to I <sub>OL</sub> in the <a href="#">Recommended Operating Conditions</a> table.....         | 5    |
| • Changed V <sub>PORR</sub> limits.....                                                                      | 6    |
| • Changed V <sub>OH</sub> at V <sub>CC</sub> = 1.65 V .....                                                  | 6    |
| • Updated I <sub>OL</sub> in the <a href="#">Electrical Characteristics</a> table.....                       | 6    |
| • Changed I <sub>CC</sub> in the <a href="#">Electrical Characteristics</a> table .....                      | 7    |
| • Deleted $\Delta$ I <sub>CC</sub> parameter from the <a href="#">Electrical Characteristics</a> table ..... | 7    |
| • Increased the pin capacitance maximum, decreased typical .....                                             | 7    |
| • Updated graphs in <a href="#">Typical Characteristics</a> section .....                                    | 9    |
| • Updated <a href="#">Interrupt Output (INT)</a> section .....                                               | 17   |
| • Added the <a href="#">Calculating Junction Temperature and Power Dissipation</a> section.....              | 25   |
| • Updated parameter values in <a href="#">Table 8</a> .....                                                  | 27   |
| • Added V <sub>CC_MV</sub> to <a href="#">Table 8</a> .....                                                  | 27   |
| • Updated <a href="#">Figure 39</a> .....                                                                    | 27   |

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**Changes from Original (August 2014) to Revision A**

**Page**

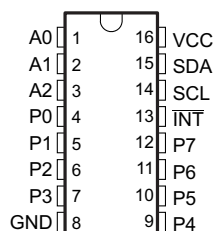
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|                                         |                   |
|-----------------------------------------|-------------------|
| • Initial release of full version ..... | <a href="#">1</a> |
|-----------------------------------------|-------------------|

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## 5 Pin Configuration and Functions

**PW and DW Package  
16-Pin TSSOP and SOIC  
Top View**



**Pin Functions**

| PIN |                         | I/O | DESCRIPTION                                                                                |
|-----|-------------------------|-----|--------------------------------------------------------------------------------------------|
| NO. | NAME                    |     |                                                                                            |
| 1   | A0                      | I   | Address input. Connect directly to V <sub>CC</sub> or ground                               |
| 2   | A1                      | I   | Address input. Connect directly to V <sub>CC</sub> or ground                               |
| 3   | A2                      | I   | Address input. Connect directly to V <sub>CC</sub> or ground                               |
| 4   | P0                      | I/O | P-port input-output. Push-pull design structure. At power on, P0 is configured as an input |
| 5   | P1                      | I/O | P-port input-output. Push-pull design structure. At power on, P1 is configured as an input |
| 6   | P2                      | I/O | P-port input-output. Push-pull design structure. At power on, P2 is configured as an input |
| 7   | P3                      | I/O | P-port input-output. Push-pull design structure. At power on, P3 is configured as an input |
| 8   | GND                     | —   | Ground                                                                                     |
| 9   | P4                      | I/O | P-port input-output. Push-pull design structure. At power on, P4 is configured as an input |
| 10  | P5                      | I/O | P-port input-output. Push-pull design structure. At power on, P5 is configured as an input |
| 11  | P6                      | I/O | P-port input-output. Push-pull design structure. At power on, P6 is configured as an input |
| 12  | P7                      | I/O | P-port input-output. Push-pull design structure. At power on, P7 is configured as an input |
| 13  | $\overline{\text{INT}}$ | O   | Interrupt output. Connect to V <sub>CC</sub> through a pull-up resistor                    |
| 14  | SCL                     | I   | Serial clock bus. Connect to V <sub>CC</sub> through a pull-up resistor                    |
| 15  | SDA                     | I/O | Serial data bus. Connect to V <sub>CC</sub> through a pull-up resistor                     |
| 16  | VCC                     | —   | Supply voltage                                                                             |

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                     |                                                                                  |                                                        | MIN  | MAX  | UNIT |
|---------------------|----------------------------------------------------------------------------------|--------------------------------------------------------|------|------|------|
| V <sub>CC</sub>     | Supply voltage                                                                   |                                                        | −0.5 | 6    | V    |
| V <sub>I</sub>      | Input voltage <sup>(2)</sup>                                                     |                                                        | −0.5 | 6    | V    |
| V <sub>O</sub>      | Output voltage <sup>(2)</sup>                                                    |                                                        | −0.5 | 6    | V    |
| I <sub>IK</sub>     | Input clamp current                                                              | V <sub>I</sub> < 0                                     |      | −20  | mA   |
| I <sub>OK</sub>     | Output clamp current                                                             | V <sub>O</sub> < 0                                     |      | −20  | mA   |
| I <sub>IOK</sub>    | Input-output clamp current                                                       | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |      | ±20  | mA   |
| I <sub>OL</sub>     | Continuous output low current through a single P-port                            | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | 50   | mA   |
| I <sub>OH</sub>     | Continuous output high current through a single P-port                           | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | −50  | mA   |
| I <sub>CC</sub>     | Continuous current through GND by all P-ports, $\overline{\text{INT}}$ , and SDA |                                                        |      | 250  | mA   |
|                     | Continuous current through V <sub>CC</sub> by all P-ports                        |                                                        |      | −160 |      |
| T <sub>J(MAX)</sub> | Maximum junction temperature                                                     |                                                        |      | 100  | °C   |
| T <sub>stg</sub>    | Storage temperature                                                              |                                                        | −65  | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 Handling Ratings

|                    |                         |                                                                                          | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                 |                                            |                                                      |                                   | MIN                   | MAX                            | UNIT |
|-----------------|--------------------------------------------|------------------------------------------------------|-----------------------------------|-----------------------|--------------------------------|------|
| V <sub>CC</sub> | Supply voltage                             |                                                      |                                   | 1.65                  | 5.5                            | V    |
| V <sub>IH</sub> | High-level input voltage                   | SCL, SDA                                             | V <sub>CC</sub> = 1.65 V to 5.5 V | 0.7 × V <sub>CC</sub> | V <sub>CC</sub> <sup>(1)</sup> | V    |
|                 |                                            | A0, A1, A2, P7–P0                                    | V <sub>CC</sub> = 1.65 V to 2.7 V | 0.7 × V <sub>CC</sub> | 5.5                            |      |
| V <sub>IL</sub> | Low-level input voltage                    | SCL, SDA                                             | V <sub>CC</sub> = 1.65 V to 5.5 V | −0.5                  | 0.3 × V <sub>CC</sub>          | V    |
|                 |                                            | A0, A1, A2, P7–P0                                    | V <sub>CC</sub> = 1.65 V to 2.7 V | −0.5                  | 0.3 × V <sub>CC</sub>          |      |
|                 |                                            |                                                      | V <sub>CC</sub> = 3 V to 5.5 V    | −0.5                  | 0.2 × V <sub>CC</sub>          |      |
| I <sub>OH</sub> | High-level output current                  | Any P-port, P7–P0                                    |                                   |                       | −10                            | mA   |
| I <sub>OL</sub> | Low-level output current <sup>(2)</sup>    | P00-P07, P10-P17                                     | T <sub>J</sub> ≤ 65°C             |                       | 25                             | mA   |
|                 |                                            |                                                      | T <sub>J</sub> ≤ 85°C             |                       | 18                             |      |
|                 |                                            |                                                      | T <sub>J</sub> ≤ 100°C            |                       | 9                              |      |
|                 |                                            | $\overline{\text{INT}}$ , SDA                        | T <sub>J</sub> ≤ 85°C             |                       | 6                              |      |
|                 |                                            |                                                      | T <sub>J</sub> ≤ 100°C            |                       | 3                              |      |
| I <sub>CC</sub> | Continuous current through GND             | All P-ports P7-P0, $\overline{\text{INT}}$ , and SDA |                                   |                       | 200                            | mA   |
|                 | Continuous current through V <sub>CC</sub> | All P-ports P7-P0                                    |                                   |                       | −80                            |      |
| T <sub>A</sub>  | Operating free-air temperature             |                                                      |                                   | −40                   | 85                             | °C   |

- (1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V<sub>CC</sub> in the application, or an increase in leakage current, I<sub>I</sub>, will result.
- (2) The values shown apply to specific junction temperatures. See the [Calculating Junction Temperature and Power Dissipation](#) section on how to calculate the junction temperature.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TCA9534A   |           | UNIT |
|-------------------------------|----------------------------------------------|------------|-----------|------|
|                               |                                              | PW (TSSOP) | DW (SOIC) |      |
|                               |                                              | 16 PINS    | 16 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 122        | 92.2      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 56.4       | 53.8      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 67.1       | 56.9      | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 10.8       | 26.4      | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 66.5       | 56.4      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER          |                                                 | TEST CONDITIONS                                             | V <sub>CC</sub> | MIN  | TYP <sup>(1)</sup> | MAX | UNIT |
|--------------------|-------------------------------------------------|-------------------------------------------------------------|-----------------|------|--------------------|-----|------|
| V <sub>IK</sub>    | Input diode clamp voltage                       | I <sub>I</sub> = –18 mA                                     | 1.65 V to 5.5 V | –1.2 |                    |     | V    |
| V <sub>POR R</sub> | Power-on reset voltage, V <sub>CC</sub> rising  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 |                 |      | 1.2                | 1.5 | V    |
| V <sub>POR F</sub> | Power-on reset voltage, V <sub>CC</sub> falling | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 |                 | 0.75 | 1                  |     | V    |
| V <sub>OH</sub>    | P-port high-level output voltage <sup>(2)</sup> | I <sub>OH</sub> = –8 mA                                     | 1.65 V          | 1.2  |                    |     | V    |
|                    |                                                 |                                                             | 2.3 V           | 1.8  |                    |     |      |
|                    |                                                 |                                                             | 3 V             | 2.6  |                    |     |      |
|                    |                                                 |                                                             | 4.5 V           | 4.1  |                    |     |      |
|                    |                                                 | I <sub>OH</sub> = –10 mA                                    | 1.65 V          | 1    |                    |     |      |
|                    |                                                 |                                                             | 2.3 V           | 1.7  |                    |     |      |
|                    |                                                 |                                                             | 3 V             | 2.5  |                    |     |      |
|                    |                                                 |                                                             | 4.5 V           | 4    |                    |     |      |
| I <sub>OL</sub>    | SDA <sup>(3)</sup>                              | V <sub>OL</sub> = 0.4 V                                     | 1.65 V to 5.5 V | 3    |                    |     | mA   |
|                    | P port <sup>(4)</sup>                           | V <sub>OL</sub> = 0.5 V                                     | 1.65 V to 5.5 V | 8    |                    |     |      |
|                    |                                                 | V <sub>OL</sub> = 0.7 V                                     | 1.65 V to 5.5 V | 10   |                    |     |      |
|                    | INT <sup>(5)</sup>                              | V <sub>OL</sub> = 0.4 V                                     | 1.65 V to 5.5 V | 3    |                    |     |      |
| I <sub>I</sub>     | SCL, SDA                                        | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 1.65 V to 5.5 V |      |                    | ±1  | μA   |
|                    | A2–A0                                           |                                                             |                 |      |                    | ±1  |      |
| I <sub>IH</sub>    | P port                                          | V <sub>I</sub> = V <sub>CC</sub>                            | 1.65 V to 5.5 V |      |                    | 1   | μA   |
| I <sub>IL</sub>    | P port                                          | V <sub>I</sub> = GND                                        | 1.65 V to 5.5 V |      |                    | –1  | μA   |

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V<sub>CC</sub> must be limited to a maximum current of 80 mA.

(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0, INT, and SDA) through GND must be limited to a maximum current of 200 mA.

(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0, INT, and SDA) through GND must be limited to a maximum current of 200 mA.

(5) The INT pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0, INT, and SDA) through GND must be limited to a maximum current of 200 mA.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                | TEST CONDITIONS                                                                                                   |        | V <sub>CC</sub> | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|-----------------|----------------|-------------------------------------------------------------------------------------------------------------------|--------|-----------------|-----|--------------------|-----|------|
| I <sub>CC</sub> | Operating mode | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,<br>I/O = inputs, f <sub>scl</sub> = 400 kHz, no load |        | 5.5 V           |     | 22                 | 40  | μA   |
|                 |                |                                                                                                                   |        | 3.6 V           |     | 11                 | 30  |      |
|                 |                |                                                                                                                   |        | 2.7 V           |     | 8                  | 19  |      |
|                 |                |                                                                                                                   |        | 1.65            |     | 5                  | 11  |      |
|                 | Standby mode   | V <sub>I</sub> = V <sub>CC</sub>                                                                                  | 5.5 V  |                 | 1.5 | 3.9                |     |      |
|                 |                |                                                                                                                   | 3.6 V  |                 | 0.9 | 2.2                |     |      |
|                 |                |                                                                                                                   | 2.7 V  |                 | 0.6 | 1.8                |     |      |
|                 |                |                                                                                                                   | 1.95 V |                 | 0.4 | 1.5                |     |      |
|                 |                | V <sub>I</sub> = GND                                                                                              | 5.5 V  |                 | 1.5 | 8.7                |     |      |
|                 |                |                                                                                                                   | 3.6 V  |                 | 0.9 | 4                  |     |      |
|                 |                |                                                                                                                   | 2.7 V  |                 | 0.6 | 3                  |     |      |
|                 |                |                                                                                                                   | 1.95 V |                 | 0.4 | 2.2                |     |      |
| C <sub>i</sub>  | SCL            | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                           |        | 1.65 V to 5.5 V |     | 3                  | 8   | pF   |
| C <sub>io</sub> | SDA            | V <sub>IO</sub> = V <sub>CC</sub> or GND                                                                          |        | 1.65 V to 5.5 V |     | 3                  | 9.5 | pF   |
|                 | P port         |                                                                                                                   |        |                 |     | 3.7                | 9.5 |      |

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see [Figure 19](#))

|                       |                                                          |                                          | MIN | MAX  | UNIT |
|-----------------------|----------------------------------------------------------|------------------------------------------|-----|------|------|
| STANDARD MODE         |                                                          |                                          |     |      |      |
| f <sub>scl</sub>      | I <sup>2</sup> C clock frequency                         |                                          | 0   | 100  | kHz  |
| t <sub>sch</sub>      | I <sup>2</sup> C clock high time                         |                                          | 4   |      | μs   |
| t <sub>scl</sub>      | I <sup>2</sup> C clock low time                          |                                          | 4.7 |      | μs   |
| t <sub>sp</sub>       | I <sup>2</sup> C spike time                              |                                          |     | 50   | ns   |
| t <sub>sds</sub>      | I <sup>2</sup> C serial-data setup time                  |                                          | 250 |      | ns   |
| t <sub>sdh</sub>      | I <sup>2</sup> C serial-data hold time                   |                                          | 0   |      | ns   |
| t <sub>icr</sub>      | I <sup>2</sup> C input rise time                         |                                          |     | 1000 | ns   |
| t <sub>icf</sub>      | I <sup>2</sup> C input fall time                         |                                          |     | 300  | ns   |
| t <sub>ocf</sub>      | I <sup>2</sup> C output fall time                        | 10-pF to 400-pF bus                      |     | 300  | ns   |
| t <sub>buf</sub>      | I <sup>2</sup> C bus free time between stop and start    |                                          | 4.7 |      | μs   |
| t <sub>sts</sub>      | I <sup>2</sup> C start or repeated start condition setup |                                          | 4.7 |      | μs   |
| t <sub>sth</sub>      | I <sup>2</sup> C start or repeated start condition hold  |                                          | 4   |      | μs   |
| t <sub>sps</sub>      | I <sup>2</sup> C stop condition setup                    |                                          | 4   |      | μs   |
| t <sub>vd(data)</sub> | Valid data time                                          | SCL low to SDA output valid              |     | 3.45 | ns   |
| t <sub>vd(ack)</sub>  | Valid data time of ACK condition                         | ACK signal from SCL low to SDA (out) low |     | 3.45 | μs   |
| C <sub>b</sub>        | I <sup>2</sup> C bus capacitive load                     |                                          |     | 400  | pF   |
| FAST MODE             |                                                          |                                          |     |      |      |
| f <sub>scl</sub>      | I <sup>2</sup> C clock frequency                         |                                          | 0   | 400  | kHz  |
| t <sub>sch</sub>      | I <sup>2</sup> C clock high time                         |                                          | 0.6 |      | μs   |
| t <sub>scl</sub>      | I <sup>2</sup> C clock low time                          |                                          | 1.3 |      | μs   |
| t <sub>sp</sub>       | I <sup>2</sup> C spike time                              |                                          |     | 50   | ns   |
| t <sub>sds</sub>      | I <sup>2</sup> C serial-data setup time                  |                                          | 100 |      | ns   |
| t <sub>sdh</sub>      | I <sup>2</sup> C serial-data hold time                   |                                          | 0   |      | ns   |
| t <sub>icr</sub>      | I <sup>2</sup> C input rise time                         |                                          | 20  | 300  | ns   |

## I<sup>2</sup>C Interface Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted) (see [Figure 19](#))

|                       |                                                          |                                          | MIN                            | MAX | UNIT |
|-----------------------|----------------------------------------------------------|------------------------------------------|--------------------------------|-----|------|
| t <sub>icf</sub>      | I <sup>2</sup> C input fall time                         |                                          | 20 × (V <sub>DD</sub> / 5.5 V) | 300 | ns   |
| t <sub>ocf</sub>      | I <sup>2</sup> C output fall time                        | 10-pF to 400-pF bus                      | 20 × (V <sub>DD</sub> / 5.5 V) | 300 | ns   |
| t <sub>buf</sub>      | I <sup>2</sup> C bus free time between stop and start    |                                          | 1.3                            |     | μs   |
| t <sub>sts</sub>      | I <sup>2</sup> C start or repeated start condition setup |                                          | 0.6                            |     | μs   |
| t <sub>sth</sub>      | I <sup>2</sup> C start or repeated start condition hold  |                                          | 0.6                            |     | μs   |
| t <sub>sps</sub>      | I <sup>2</sup> C stop condition setup                    |                                          | 0.6                            |     | μs   |
| t <sub>vd(data)</sub> | Valid data time                                          | SCL low to SDA output valid              |                                | 0.9 | ns   |
| t <sub>vd(ack)</sub>  | Valid data time of ACK condition                         | ACK signal from SCL low to SDA (out) low |                                | 0.9 | μs   |
| C <sub>b</sub>        | I <sup>2</sup> C bus capacitive load                     |                                          |                                | 400 | pF   |

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 20](#) and [Figure 21](#))

| PARAMETER                     |                            | FROM<br>(INPUT) | TO<br>(OUTPUT)          | MIN | MAX | UNIT |
|-------------------------------|----------------------------|-----------------|-------------------------|-----|-----|------|
| <b>STANDARD and FAST MODE</b> |                            |                 |                         |     |     |      |
| t <sub>iv</sub>               | Interrupt valid time       | P port          | $\overline{\text{INT}}$ |     | 4   | μs   |
| t <sub>ir</sub>               | Interrupt reset delay time | SCL             | $\overline{\text{INT}}$ |     | 4   | μs   |
| t <sub>pv</sub>               | Output data valid          | SCL             | P7–P0                   |     | 350 | ns   |
| t <sub>ps</sub>               | Input data setup time      | P port          | SCL                     | 100 |     | ns   |
| t <sub>ph</sub>               | Input data hold time       | P port          | SCL                     | 1   |     | μs   |

## 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

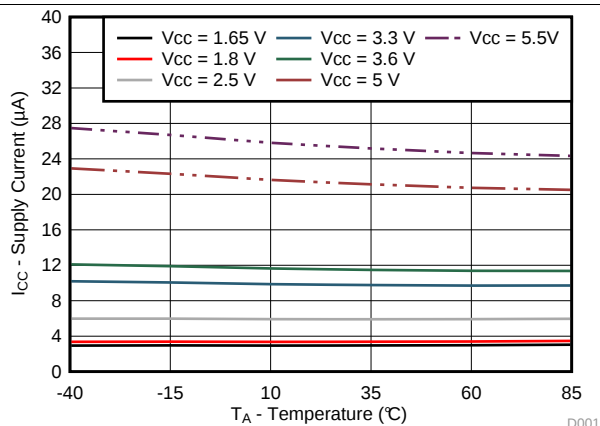


Figure 1. Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

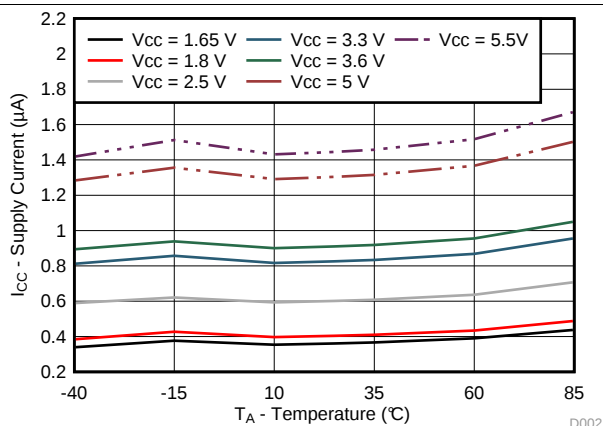


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

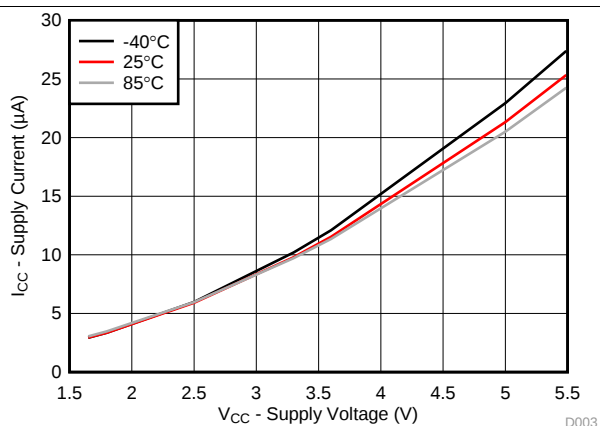


Figure 3. Supply Current vs Supply Voltage for Different Temperature ( $T_A$ )

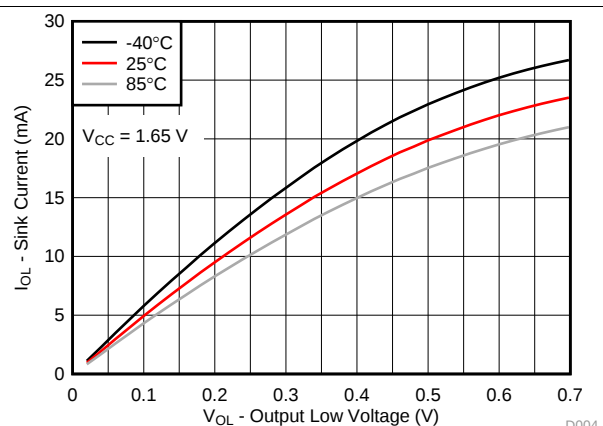


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

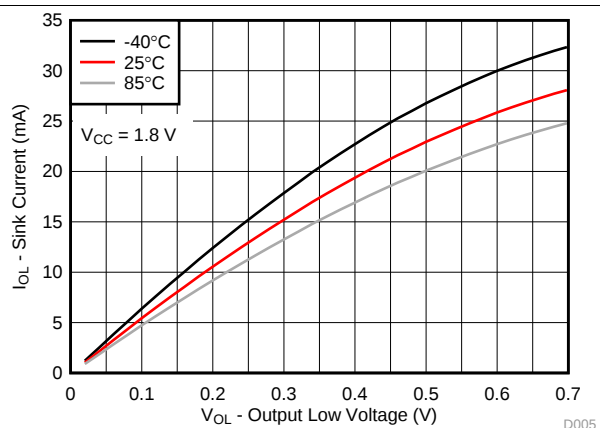


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

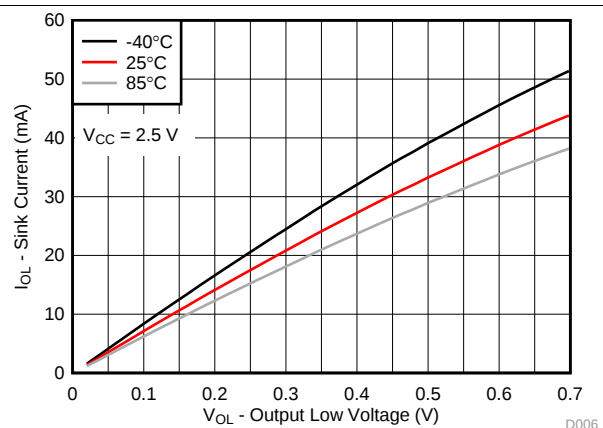


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

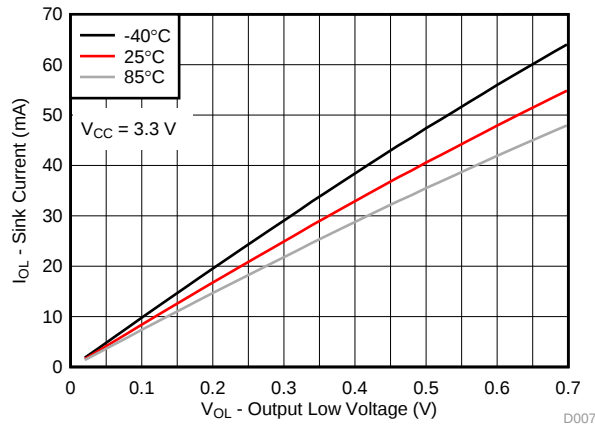


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$

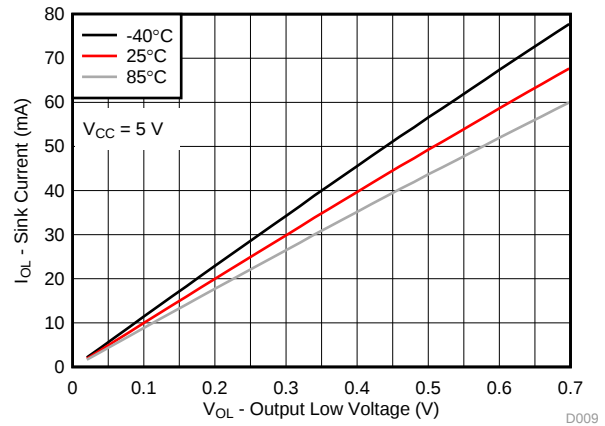


Figure 8. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$

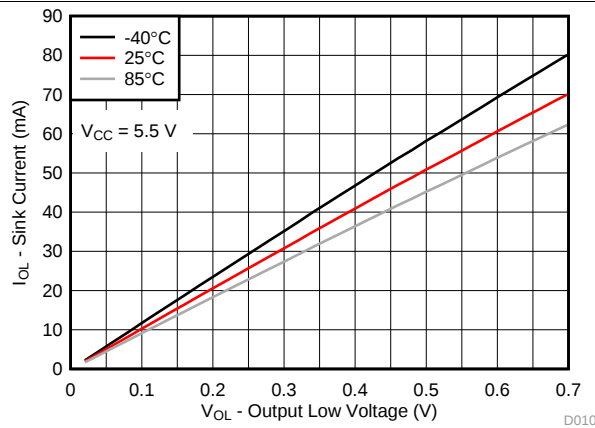


Figure 9. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$

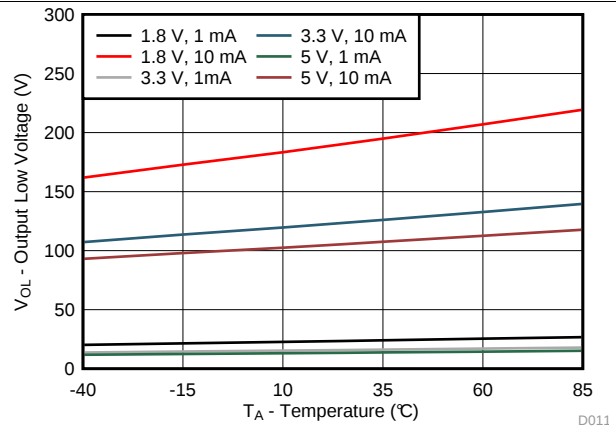


Figure 10. I/O Low Voltage vs Temperature for Different  $V_{CC}$  and  $I_{OL}$

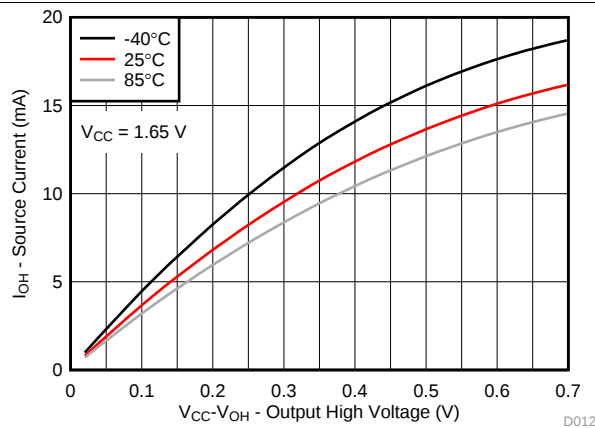


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

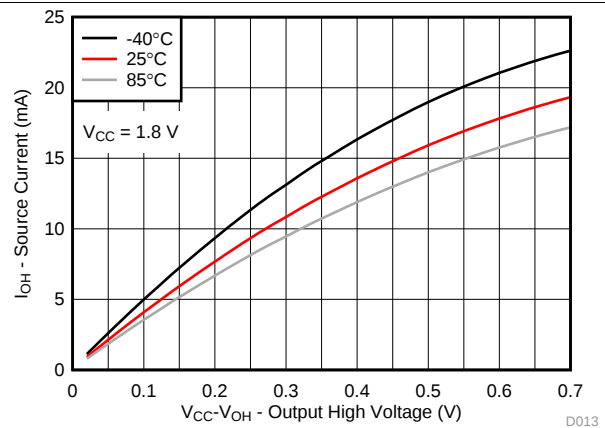
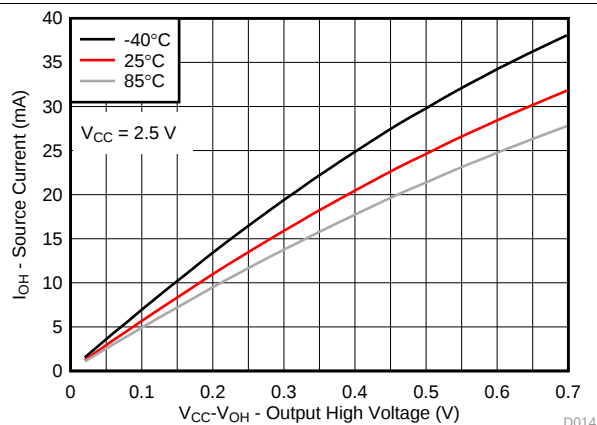


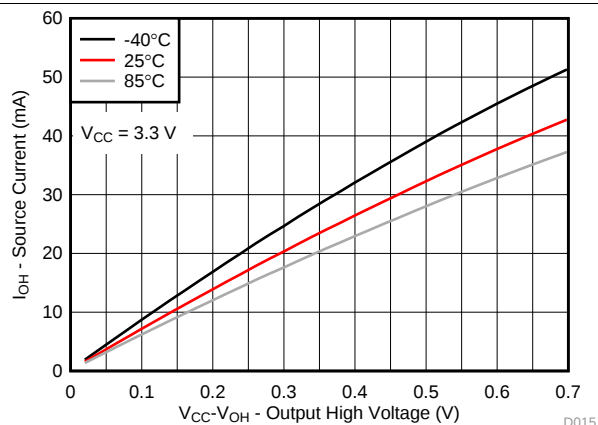
Figure 12. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

## Typical Characteristics (continued)

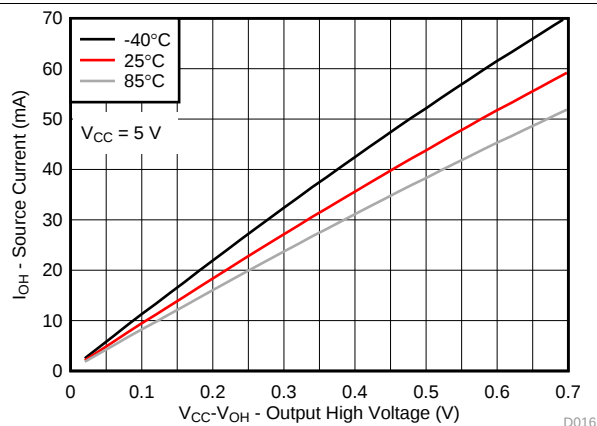
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



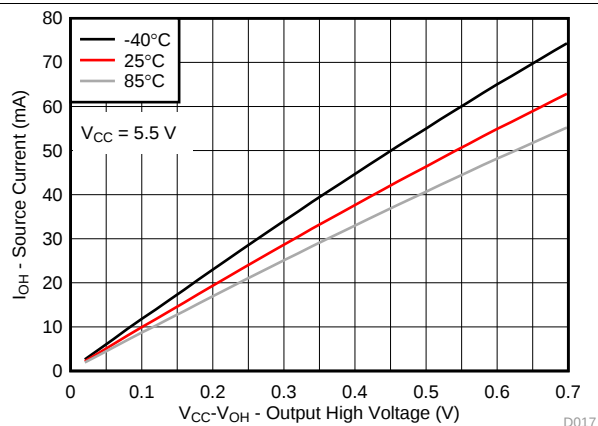
**Figure 13. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$**



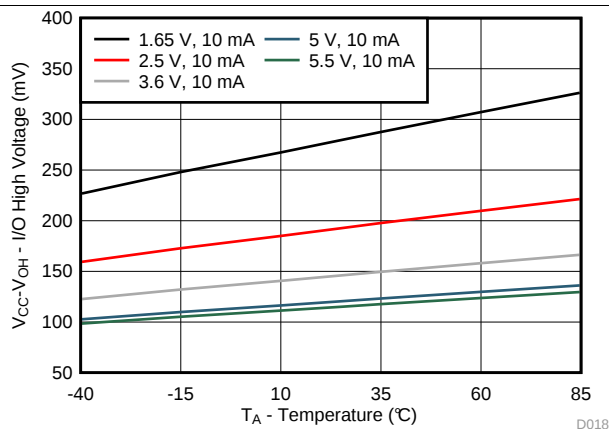
**Figure 14. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$**



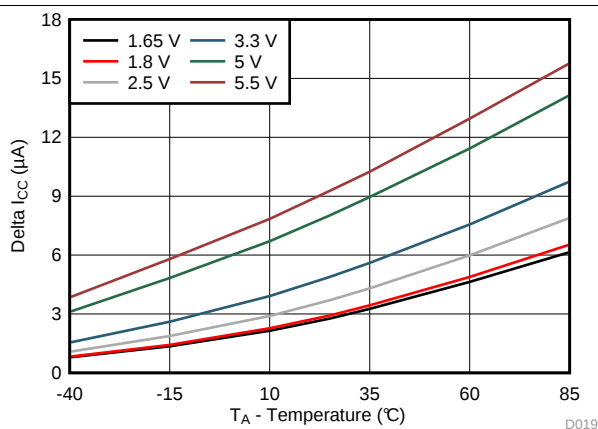
**Figure 15. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$**



**Figure 16. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$**

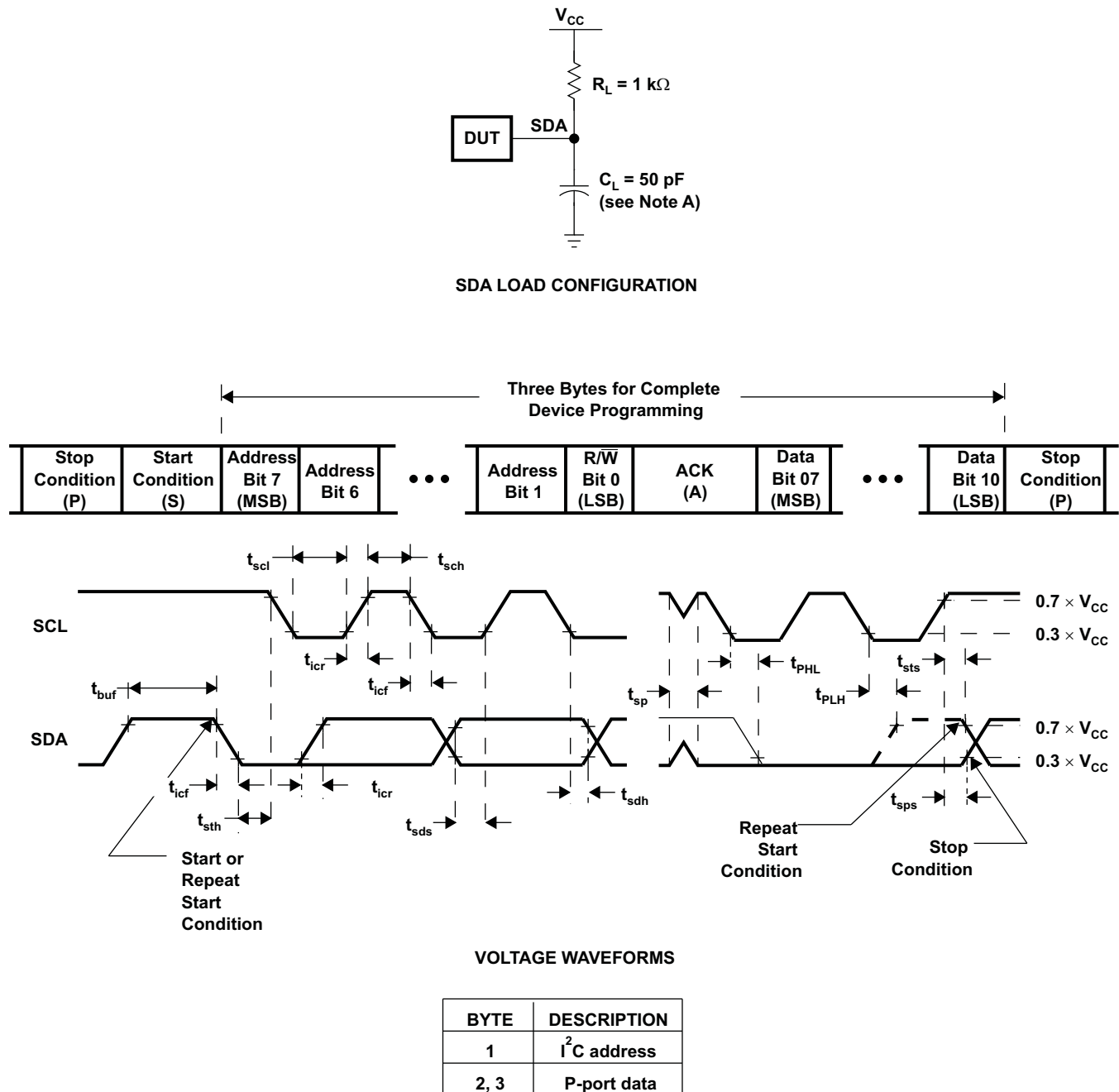


**Figure 17.  $V_{CC} - V_{OH}$  Voltage vs Temperature for Different  $V_{CC}$**



**Figure 18.  $\Delta I_{CC}$  vs Temperature for Different  $V_{CC}$  ( $V_I = V_{CC} - 0.6\text{ V}$ )**

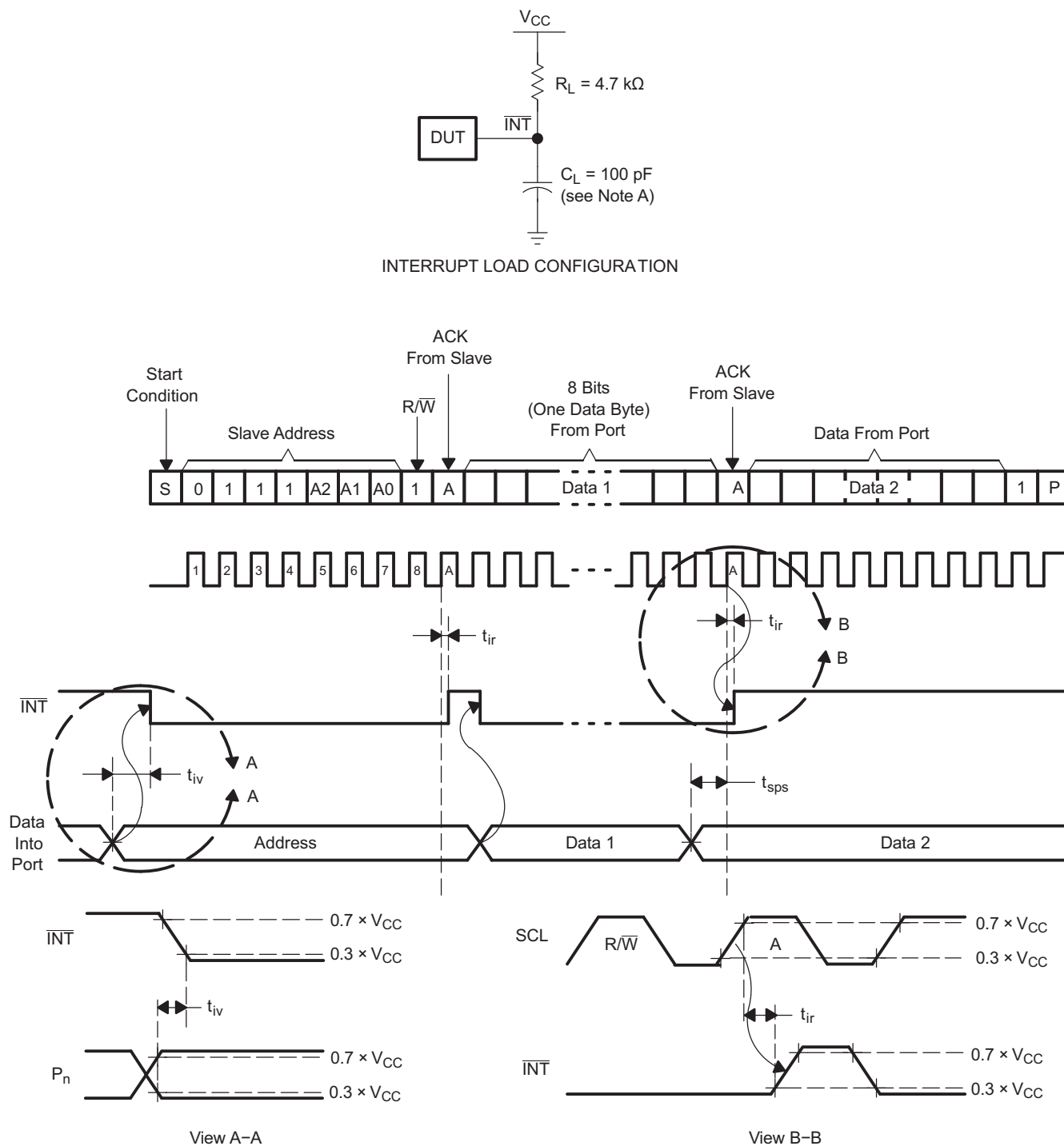
## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

**Figure 19. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**

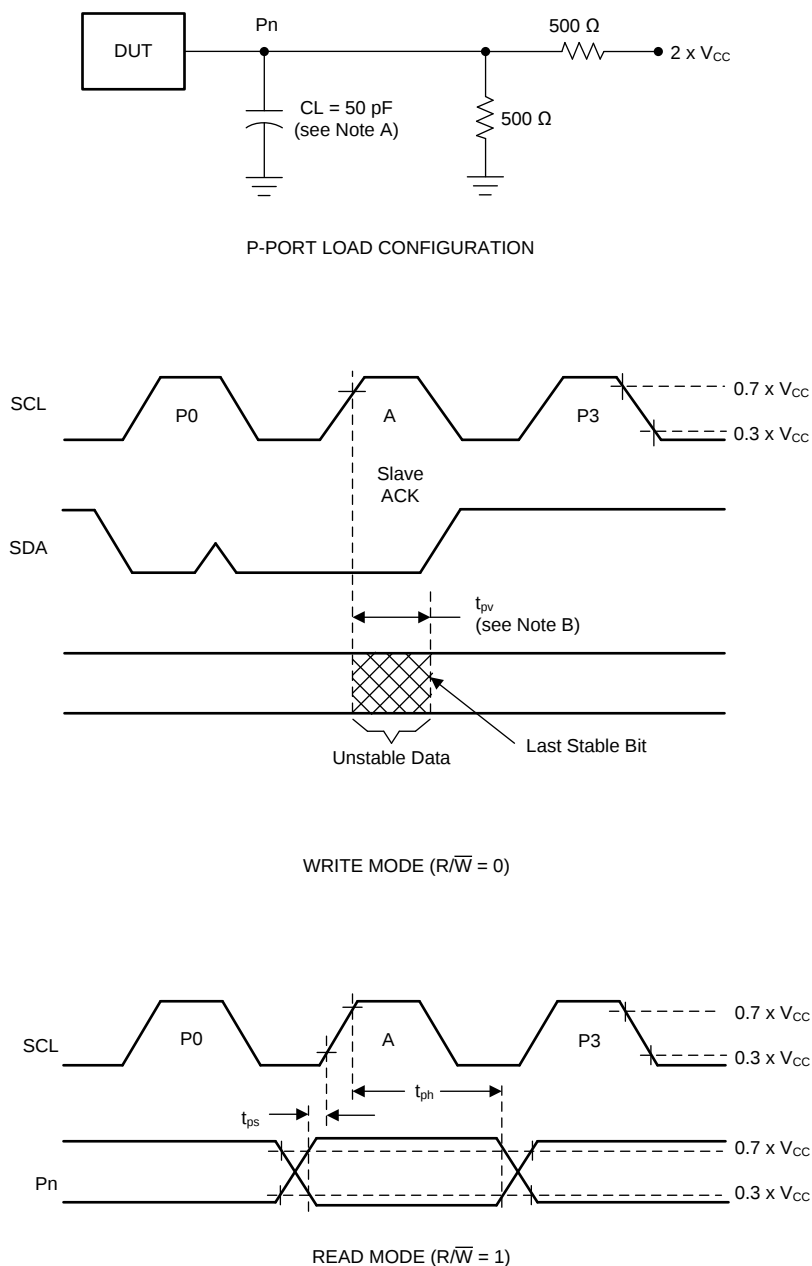
## Parameter Measurement Information (continued)



- $C_L$  includes probe and jig capacitance.
- All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- All parameters and waveforms are not applicable to all devices.

**Figure 20. Interrupt Load Circuit and Voltage Waveforms**

## Parameter Measurement Information (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 21. P-Port Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TCA9534A is an 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 1.65-V to 5.5-V  $V_{CC}$  operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I<sup>2</sup>C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9534A open-drain interrupt ( $\overline{INT}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The INT pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA9534A can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C slave address and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

The system master can reset the TCA9534A in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I<sup>2</sup>C /SMBus state machine.

The TCA9534A consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9534A is identical to the TCA9554 except for the removal of the internal I/O pull-up resistors, which greatly reduces power consumption when the I/Os are held LOW.



## 8.3 Feature Description

### 8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

### 8.3.2 Interrupt Output ( $\overline{INT}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time,  $t_{iv}$ , the signal  $\overline{INT}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the  $\overline{INT}$  is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The  $\overline{INT}$  output has an open-drain structure and requires pull-up resistor to  $V_{CC}$ .

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the TCA9534A in a reset condition until  $V_{CC}$  has reached  $V_{PORR}$ . At that point, the reset condition is released and the TCA9534A registers and SMBus/I<sup>2</sup>C state machine initialize to their default states. After that,  $V_{CC}$  must be lowered to below  $V_{PORF}$  and then back up to the operating voltage for a power-on reset cycle.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The TCA9534A has a standard bidirectional I<sup>2</sup>C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I<sup>2</sup>C bus has a specific device address to differentiate between other slave devices that are on the same I<sup>2</sup>C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see the [Understanding the I<sup>2</sup>C Bus](#) application report.

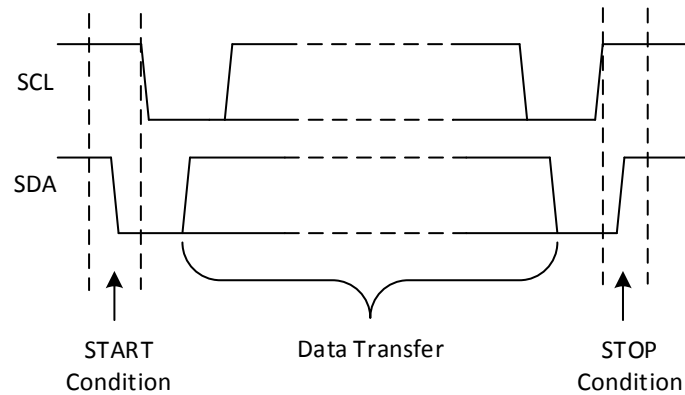
The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to  $V_{CC}$  through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. For further details, see the [I<sup>2</sup>C Pull-up Resistor Calculation](#) application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

[Figure 24](#) and [Figure 25](#) show the general procedure for a master to access a slave device:

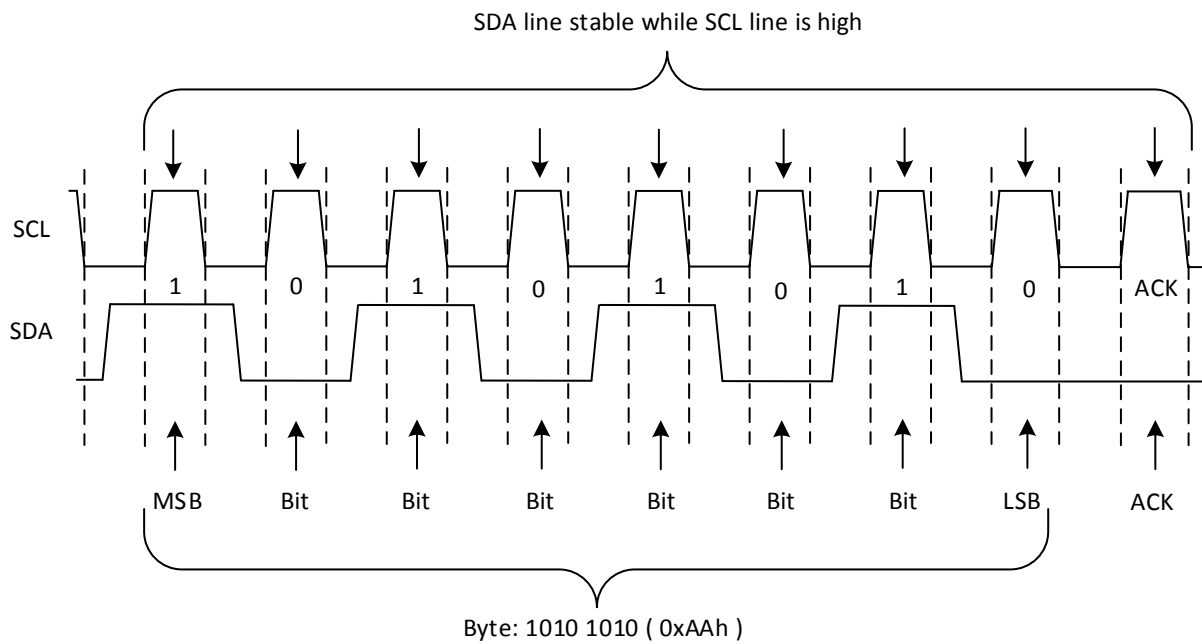
1. If a master wants to send data to a slave:
  - Master-transmitter sends a START condition and addresses the slave-receiver.
  - Master-transmitter sends data to slave-receiver.
  - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
  - Master-receiver sends a START condition and addresses the slave-transmitter.
  - Master-receiver sends the requested register to read to slave-transmitter.
  - Master-receiver receives data from the slave-transmitter.

## Programming (continued)

- Master-receiver terminates the transfer with a STOP condition.



**Figure 24. Definition of Start and Stop Conditions**



**Figure 25. Bit Transfer**

Table 1 shows the TCA9534A interface definition.

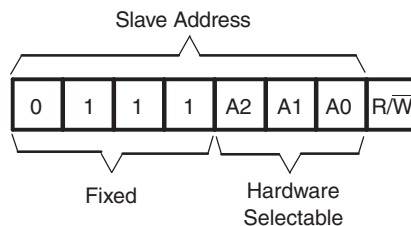
**Table 1. Interface Definition Table**

| BYTE                           | BIT     |    |    |    |    |    |    |                  |
|--------------------------------|---------|----|----|----|----|----|----|------------------|
|                                | 7 (MSB) | 6  | 5  | 4  | 3  | 2  | 1  | 0 (LSB)          |
| I <sup>2</sup> C slave address | L       | H  | H  | H  | A2 | A1 | A0 | R $\overline{W}$ |
| Px I/O data bus                | P7      | P6 | P5 | P4 | P3 | P2 | P1 | P0               |

## 8.6 Register Maps

### 8.6.1 Device Address

Figure 26 shows the address byte of the TCA9534A.



**Figure 26. TCA9534A Address**

Table 2 shows the TCA9534A address reference.

**Table 2. Address Reference**

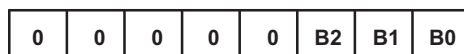
| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2     | A1 | A0 |                                    |
| L      | L  | L  | 56 (decimal), 38 (hexadecimal)     |
| L      | L  | H  | 57 (decimal), 39 (hexadecimal)     |
| L      | H  | L  | 58 (decimal), 3A (hexadecimal)     |
| L      | H  | H  | 59 (decimal), 3B (hexadecimal)     |
| H      | L  | L  | 60 (decimal), 3C (hexadecimal)     |
| H      | L  | H  | 61 (decimal), 3D (hexadecimal)     |
| H      | H  | L  | 62 (decimal), 3E (hexadecimal)     |
| H      | H  | H  | 63 (decimal), 3F (hexadecimal)     |

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9534A (see Figure 27). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that is affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.



**Figure 27. Control Register Bits**

Table 3 shows the TCA9534A command byte.

**Table 3. Command Byte Table**

| CONTROL REGISTER BITS |    | COMMAND BYTE (HEX) | REGISTER           | PROTOCOL        | POWER-UP DEFAULT |
|-----------------------|----|--------------------|--------------------|-----------------|------------------|
| B1                    | B0 |                    |                    |                 |                  |
| 0                     | 0  | 0x00               | Input Port         | Read byte       | XXXX XXXX        |
| 0                     | 1  | 0x01               | Output Port        | Read/write byte | 1111 1111        |
| 1                     | 0  | 0x02               | Polarity Inversion | Read/write byte | 0000 0000        |
| 1                     | 1  | 0x03               | Configuration      | Read/write byte | 1111 1111        |

### 8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See [Table 4](#).

Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port register is accessed next.

**Table 4. Register 0 (Input Port Register) Table**

| BIT     | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | X  | X  | X  | X  | X  | X  | X  | X  |

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See [Table 5](#).

**Table 5. Register 1 (Output Port Register) Table**

| BIT     | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See [Table 6](#).

**Table 6. Register 2 (Polarity Inversion Register) Table**

| BIT     | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See [Table 7](#).

**Table 7. Register 3 (Configuration Register) Table**

| BIT     | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

### 8.6.3.1 Bus Transactions

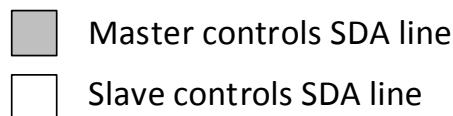
Data is exchanged between the master and the TCA9534A through write and read commands.

#### 8.6.3.1.1 Writes

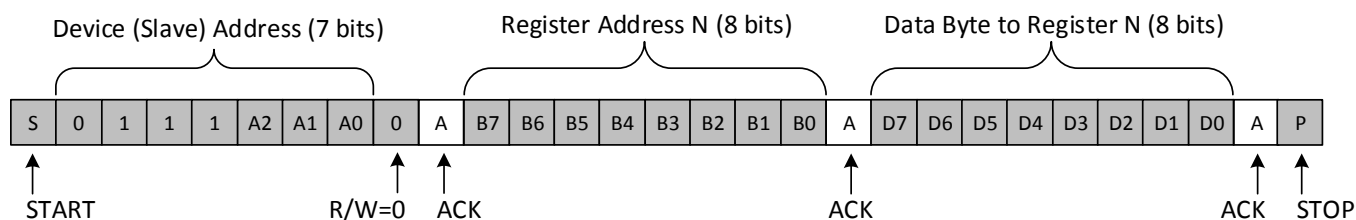
To write on the I<sup>2</sup>C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See [Table 3](#) to see list of the internal registers and a description of each one.

[Figure 28](#) shows an example of writing a single byte to a slave register.

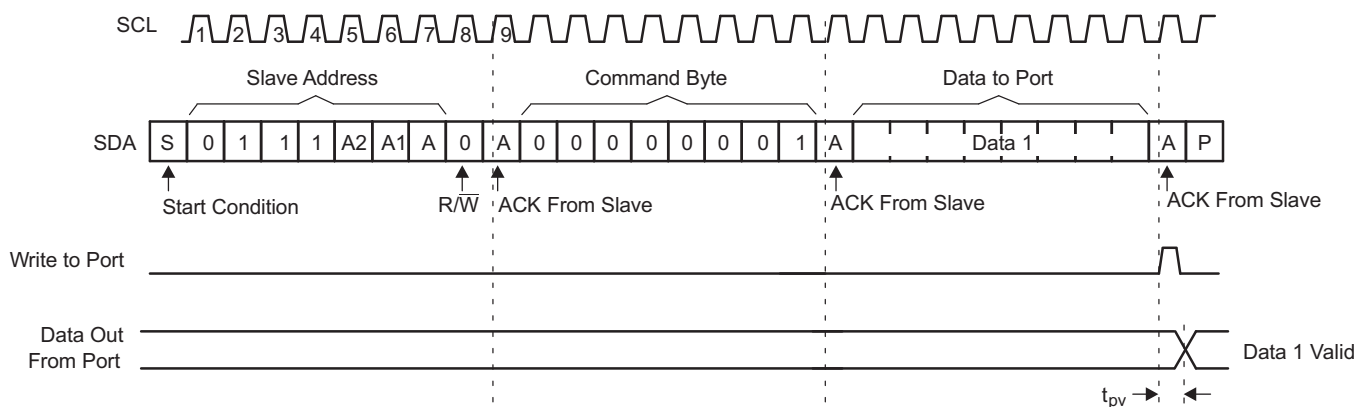


#### Write to one register in a device



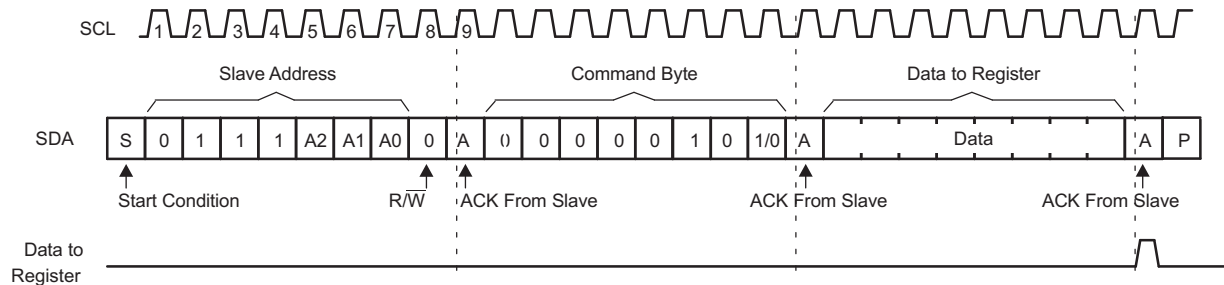
**Figure 28. Write to Register**

[Figure 29](#) shows an example of writing to the output port register.



**Figure 29. Write to Output Port Register**

[Figure 30](#) shows an example of writing to the configuration or polarity inversion registers.



**Figure 30. Write to Configuration or Polarity Inversion Registers**

#### 8.6.3.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

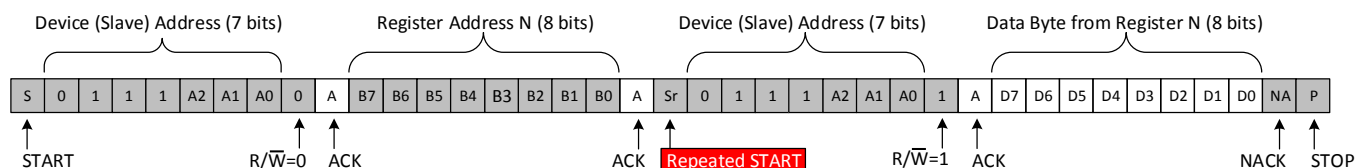
See [Table 3](#) for the list of the internal registers and a description of each one.

If a read is requested by the master after a POR without first setting the command byte via a write, the device will NACK until a command byte-register address is set as described above.

[Figure 31](#) shows an example of reading a single byte from a slave register.

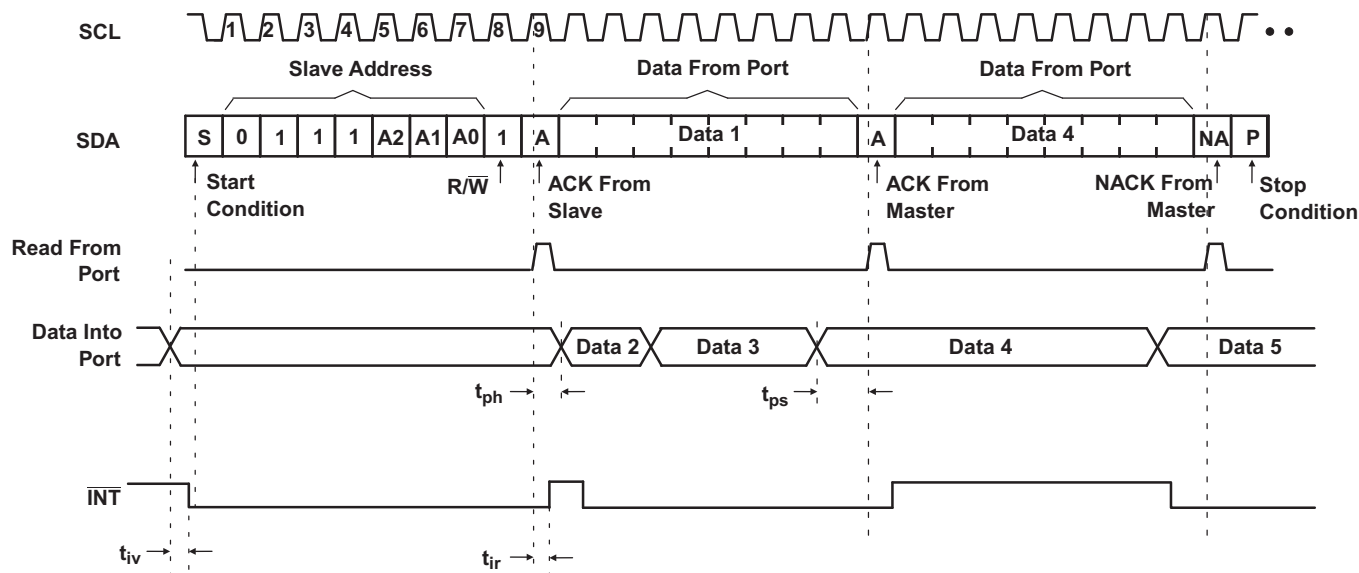
- ☒ Master controls SDA line
- ☐ Slave controls SDA line

#### Read from one register in a device



**Figure 31. Read From Register**

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. See [Figure 32](#).



- A. This figure assumes the command byte has previously been programmed with 00h.
- B. Transfer of data can be stopped at any moment by a Stop condition.
- C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See the [Reads](#) section for these details.

**Figure 32. Read From Input Port Register**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

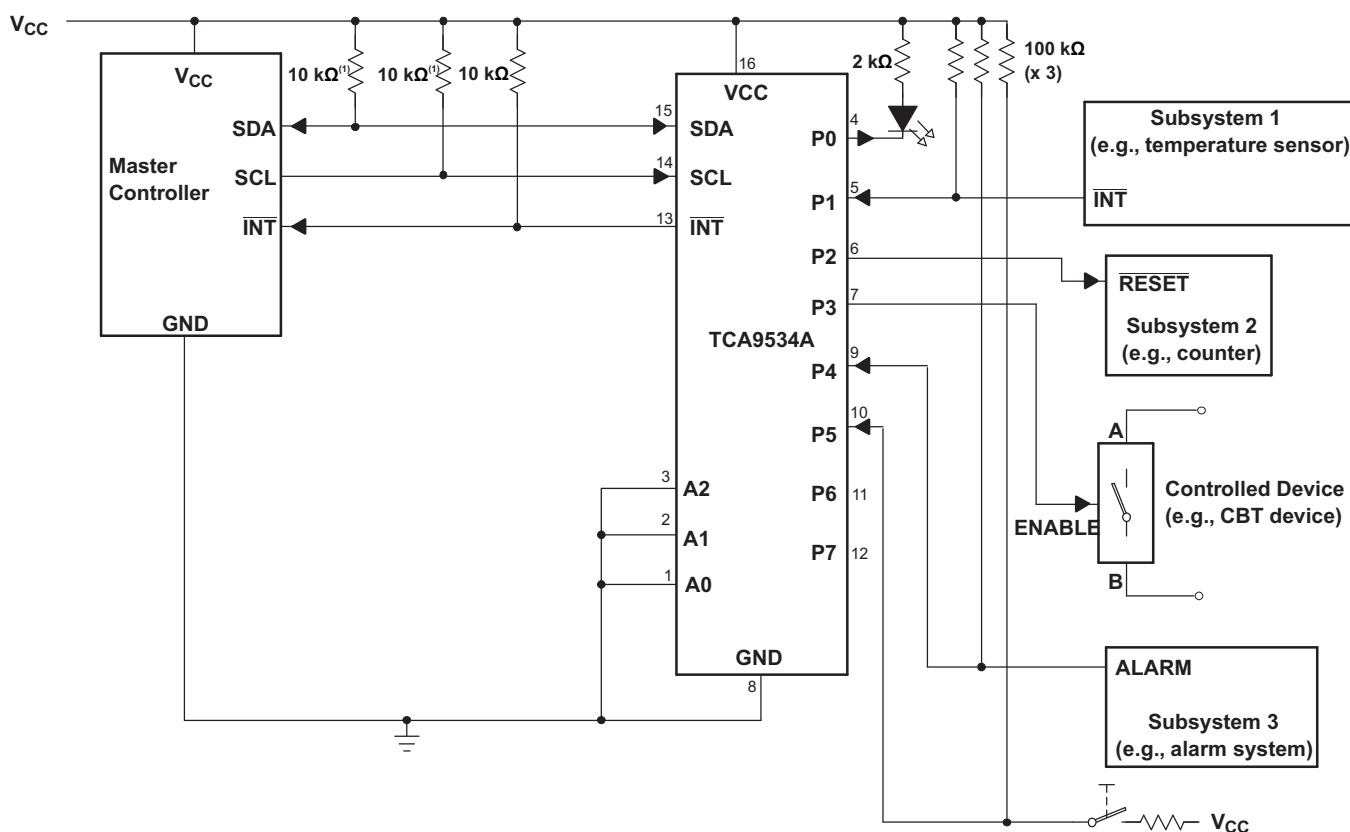
### 9.1 Application Information

Figure 33 shows an application in which the TCA9534A can be used.

IO Expanders such as the TCA9534A are commonly used to obtain more general purpose I/Os. There are many common uses for these additional I/Os:

- Inputs from other ICs, such as interrupt signals from sensors
- Inputs from physical buttons (for detecting button presses)
- Outputs to control RESET or ENABLE signals on other ICs
- Outputs for controlling LEDs for visual feedback to a user

### 9.2 Typical Application



The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that can be powered on while VCC is powered off, then the supply current, ICC, increases as a result.

Device address is configured as 0111000 for this example.

P0, P2, and P3 are configured as outputs.

P1, P4, and P5 are configured as inputs.

P6 and P7 are not used and must be configured as outputs.

**Figure 33. Application Schematic**

## Typical Application (continued)

### 9.2.1 Design Requirements

#### 9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA9534A, it is important that the [Recommended Operating Conditions](#) not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in [Equation 1](#).

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

$\theta_{JA}$  is the standard junction to ambient thermal resistance measurement of the package, as seen in [Thermal Information](#) table.  $P_d$  is the total power dissipation of the device, and the approximation is shown in [Equation 2](#).

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

[Equation 2](#) is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the INT and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using [Equation 3](#) to calculate the power dissipation in INT or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

[Equation 3](#) shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the  $V_{OL}$  of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

[Equation 4](#) shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between  $V_{CC}$  and the output voltage).

#### 9.2.1.2 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in [Figure 33](#). For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED is off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. [Figure 34](#) shows a high-value resistor in parallel with the LED. [Figure 35](#) shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

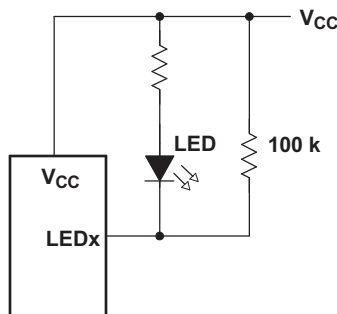
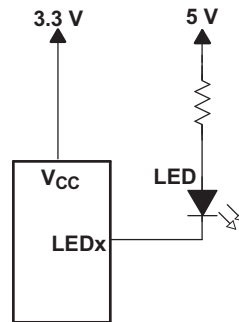


Figure 34. High-Value Resistor in Parallel With LED

## Typical Application (continued)



**Figure 35. Device Supplied by a Lower Voltage**

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_P$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in Equation 5.

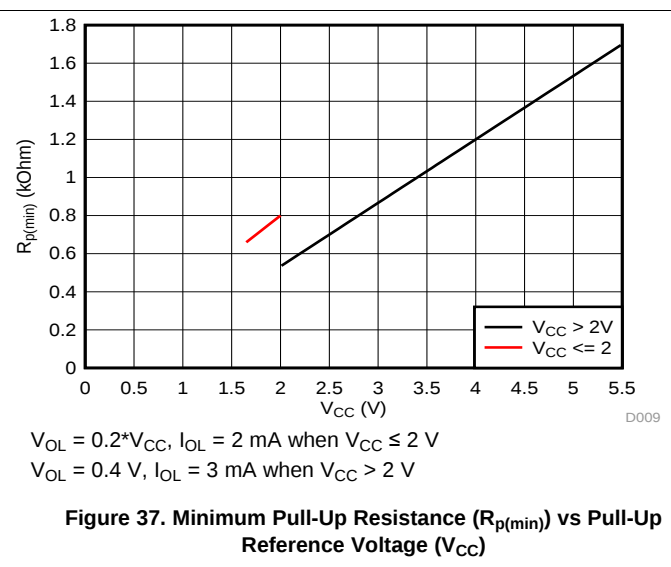
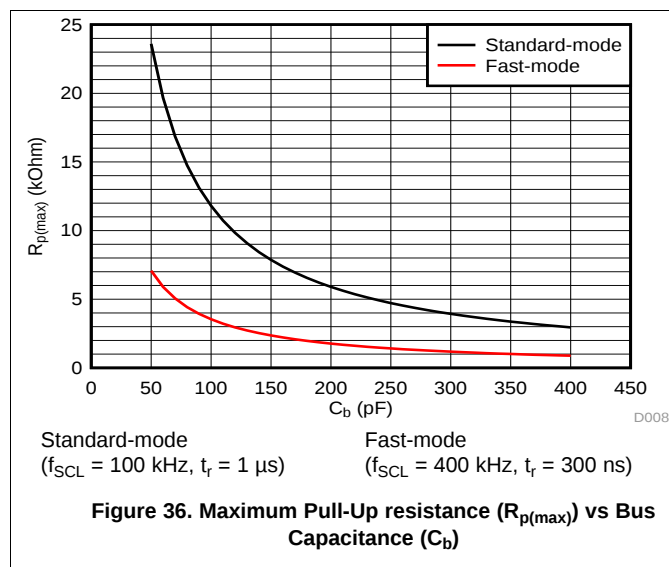
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9534A,  $C_i$  for SCL or  $C_{i0}$  for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

### 9.2.3 Application Curves

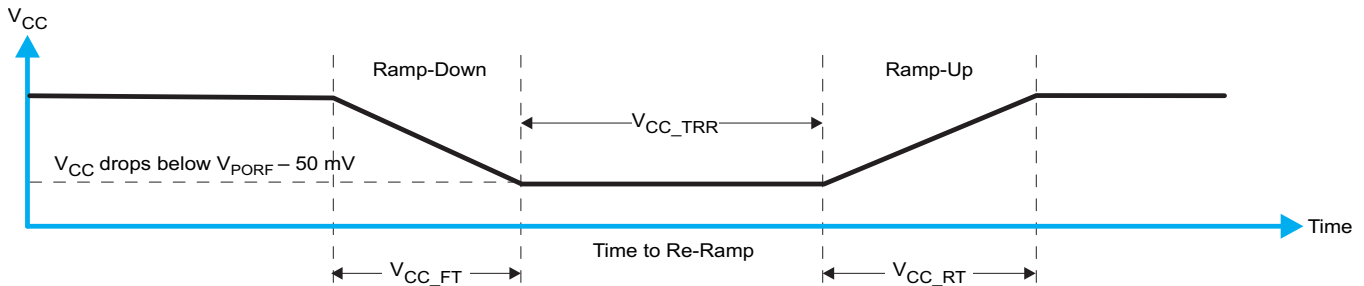


## 10 Power Supply Recommendations

### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the TCA9534A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and [Figure 38](#).



**Figure 38.  $V_{CC}$  is Lowered Below the POR Threshold, then Ramped Back Up to  $V_{CC}$**

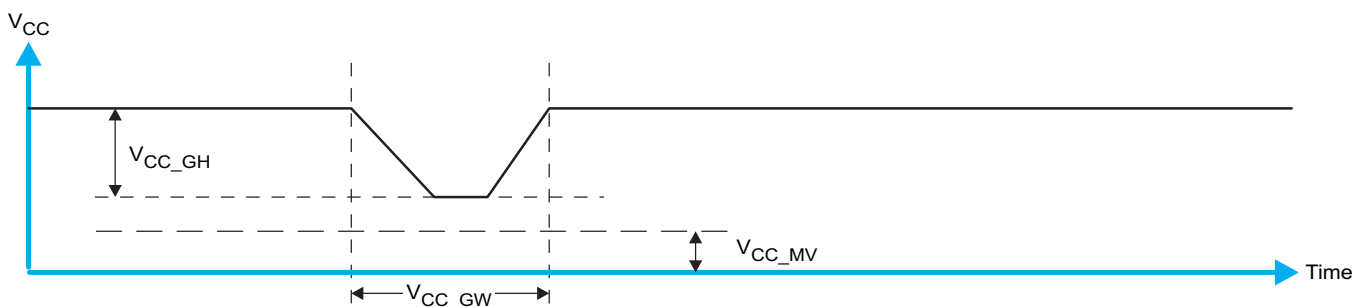
[Table 8](#) specifies the performance of the power-on reset feature for the TCA9534A for both types of power-on reset.

**Table 8. Recommended Supply Sequencing and Ramp Rates<sup>(1)</sup>**

| PARAMETER     |                                                                                                                   |                               | MIN | MAX  | UNIT    |
|---------------|-------------------------------------------------------------------------------------------------------------------|-------------------------------|-----|------|---------|
| $V_{CC\_FT}$  | Fall rate                                                                                                         | See <a href="#">Figure 38</a> | 1   | 2000 | ms      |
| $V_{CC\_RT}$  | Rise rate                                                                                                         | See <a href="#">Figure 38</a> | 0.1 | 2000 | ms      |
| $V_{CC\_TRR}$ | Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV or when $V_{CC}$ drops to GND)                     | See <a href="#">Figure 38</a> | 1   |      | $\mu$ s |
| $V_{CC\_GH}$  | Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s     | See <a href="#">Figure 39</a> |     | 1.2  | V       |
| $V_{CC\_MV}$  | The minimum voltage that $V_{CC}$ can glitch down to without causing a reset ( $V_{CC\_GH}$ must not be violated) | See <a href="#">Figure 39</a> | 1.5 |      | V       |
| $V_{CC\_GW}$  | Glitch width that does not cause a functional disruption when $V_{CC\_GH} = 0.5 \times V_{CCX}$                   | See <a href="#">Figure 39</a> |     | 10   | $\mu$ s |

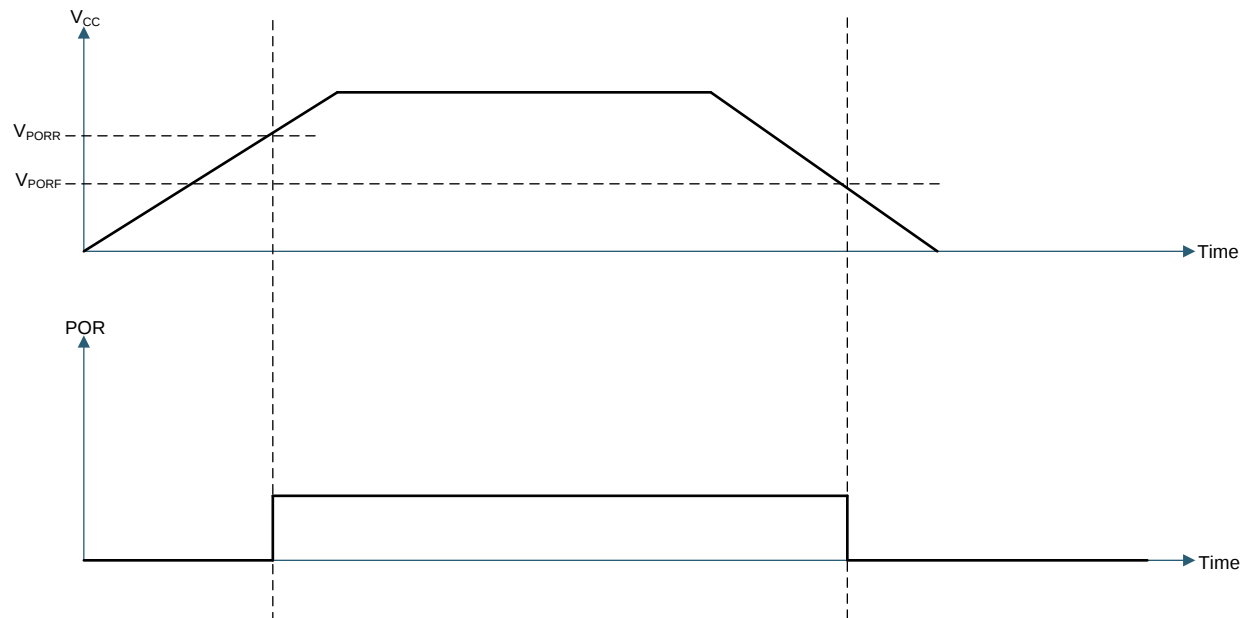
(1) All supply sequencing and ramp rate values are measured at  $T_A = 25^\circ\text{C}$

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 39](#) and [Table 8](#) provide more information on how to measure these specifications.



**Figure 39. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. [Figure 40](#) and [Table 8](#) provide more details on this specification.



**Figure 40.  $V_{POR}$**

## 11 Layout

### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9534A, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9534A as possible. These best practices are shown in Figure 41.

For the layout example provided in Figure 41, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub> or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 41.

### 11.2 Layout Example

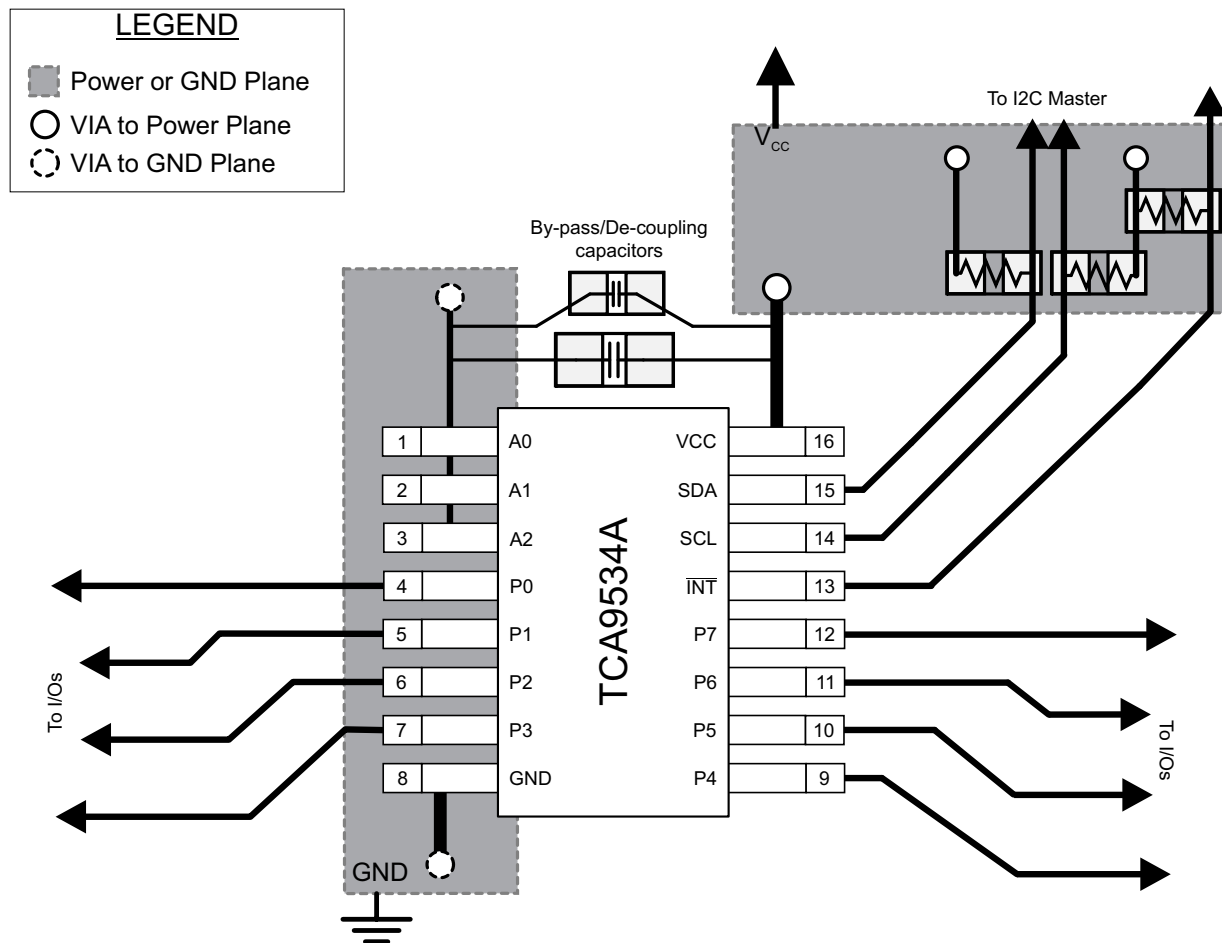


Figure 41. TCA9534A Layout

## 12 Device and Documentation Support

### 12.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [IO Expander EVM User's Guide](#)
- [Choosing the Correct I2C Device for New Designs](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TCA9534ADWR</a> | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| TCA9534ADWR.A               | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| TCA9534ADWR.B               | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| <a href="#">TCA9534ADWT</a> | Active        | Production           | SOIC (DW)   16  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| TCA9534ADWT.A               | Active        | Production           | SOIC (DW)   16  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| TCA9534ADWT.B               | Active        | Production           | SOIC (DW)   16  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TCA9534A            |
| <a href="#">TCA9534APWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |
| TCA9534APWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |
| TCA9534APWR.B               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |
| TCA9534APWRG4               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |
| TCA9534APWRG4.A             | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |
| TCA9534APWRG4.B             | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PW534A              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TCA9534ADWR   | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| TCA9534APWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TCA9534APWRG4 | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TCA9534ADWR   | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| TCA9534APWR   | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| TCA9534APWRG4 | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## GENERIC PACKAGE VIEW

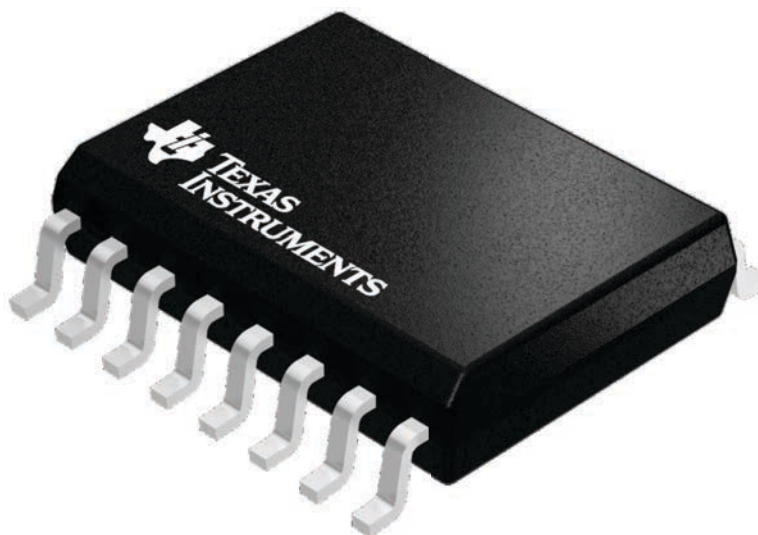
**DW 16**

**SOIC - 2.65 mm max height**

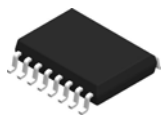
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

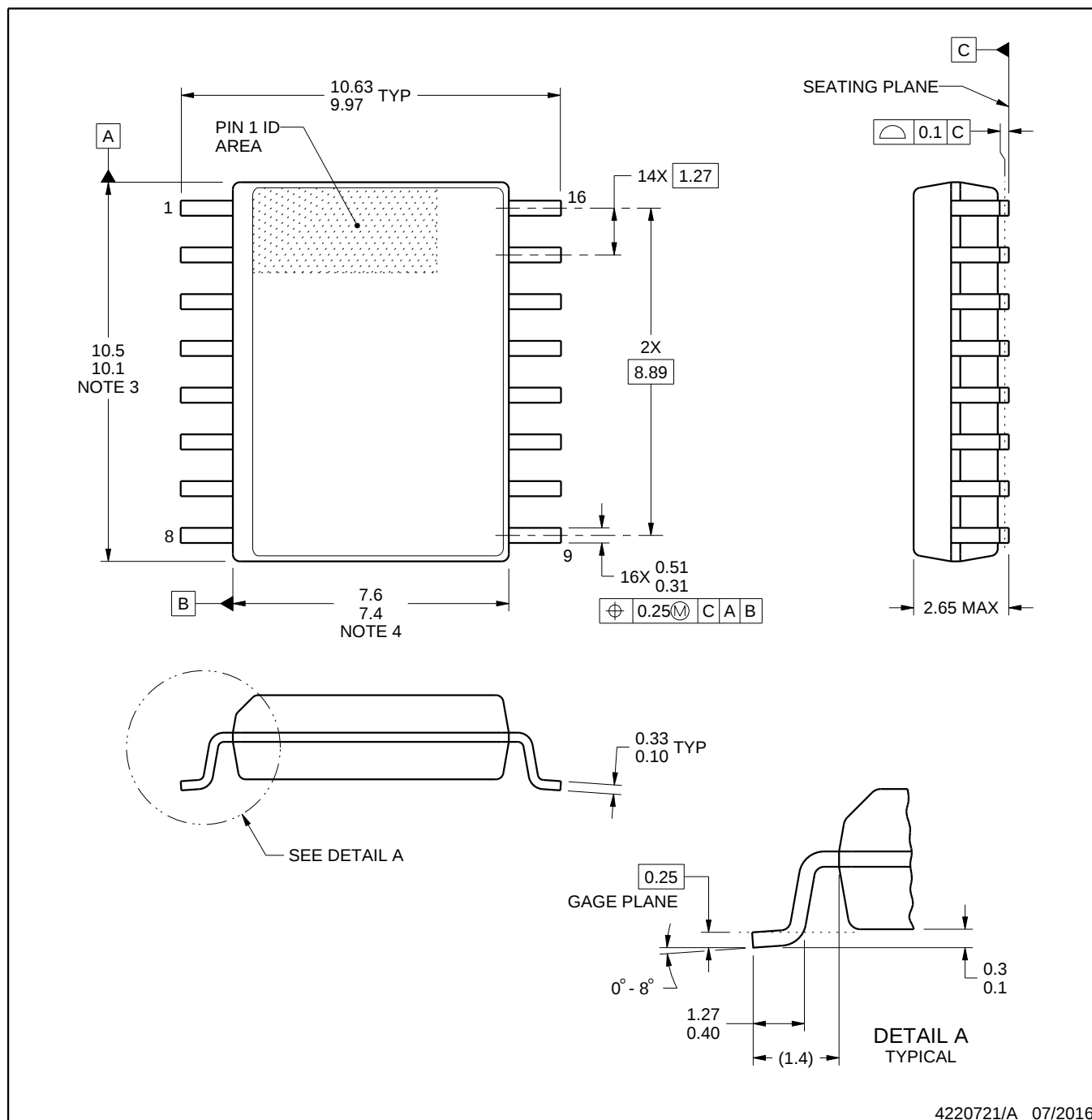


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

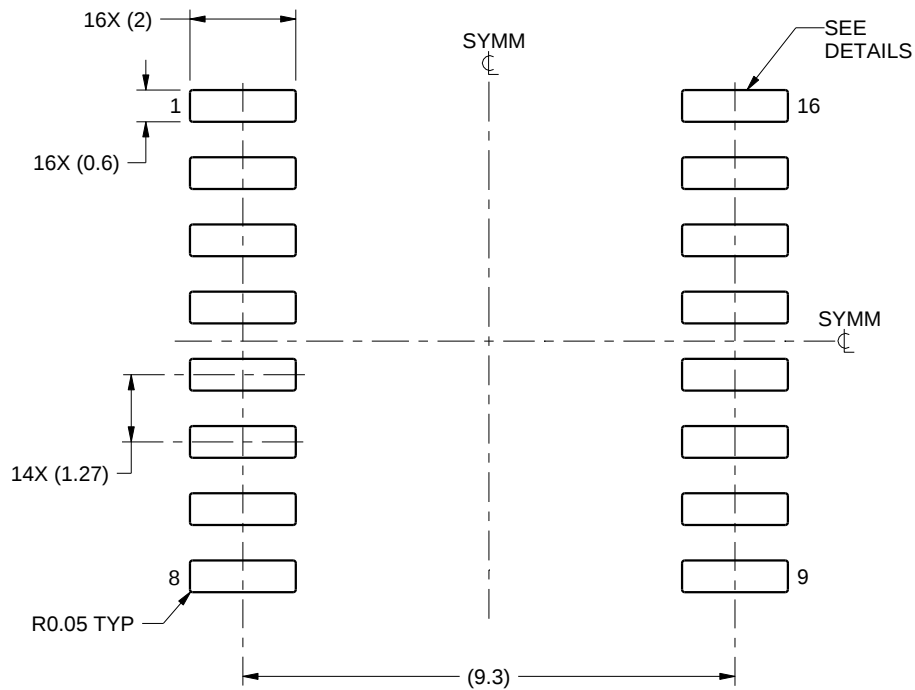
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

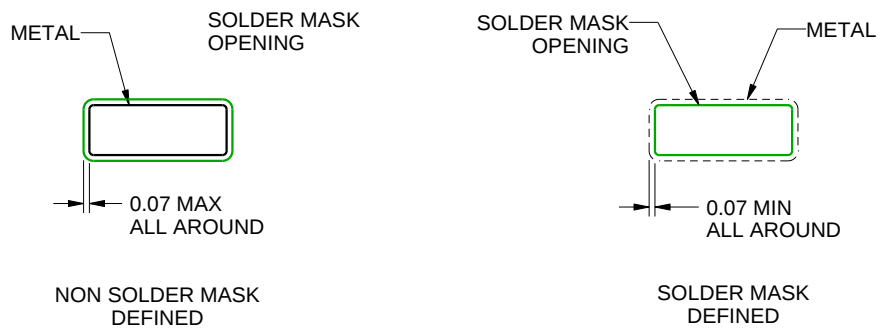
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

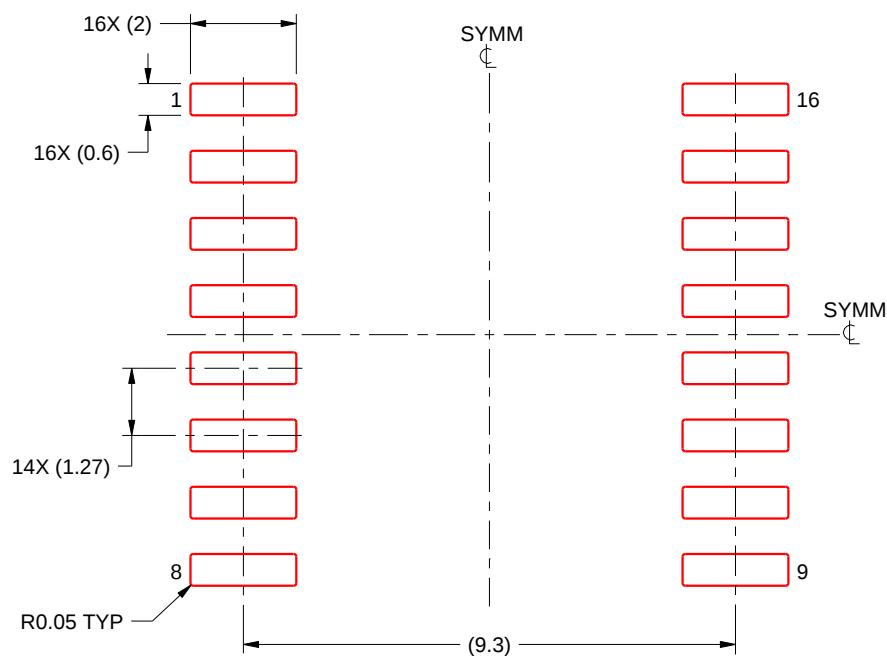
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



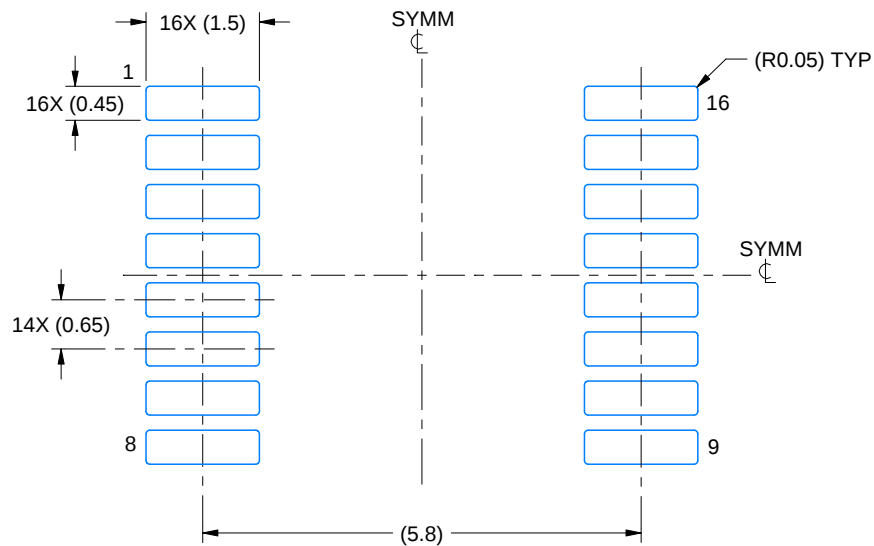
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

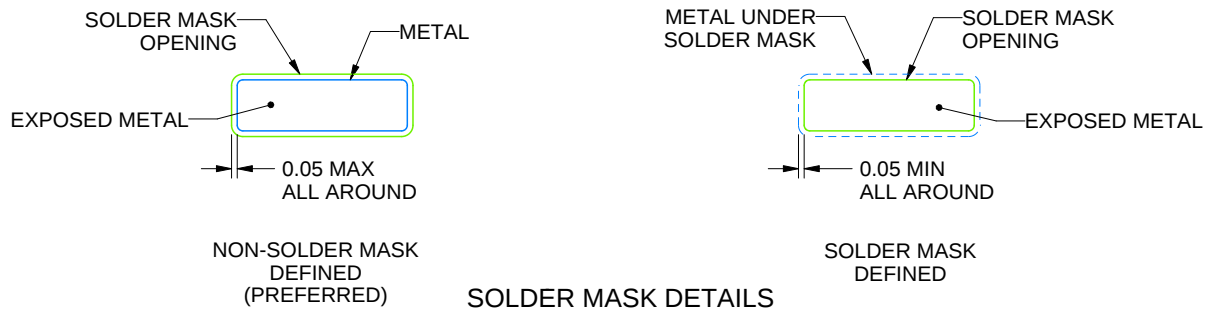
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

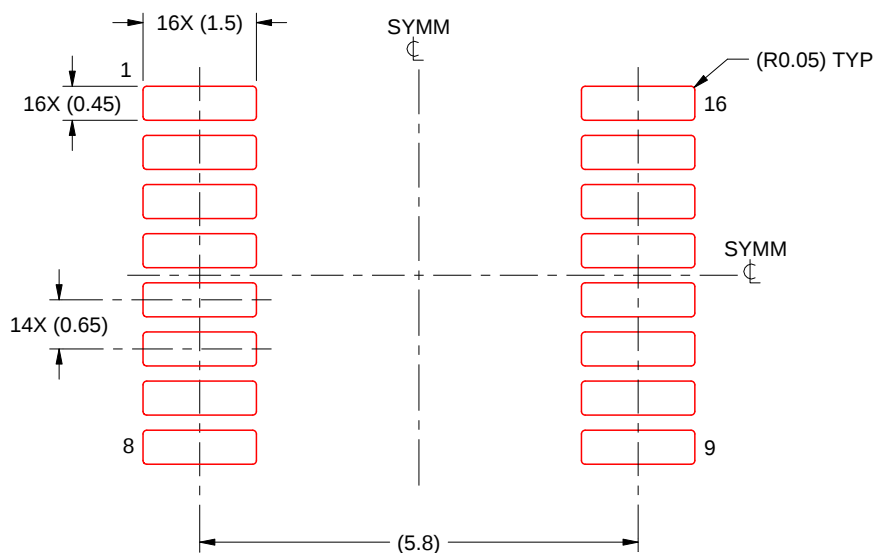
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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