TCA9517-Q1 レベル変換 I2C バス・リピータ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度:–40℃～125℃、T_A
  - デバイス HBM 分類レベル:±5500V
  - デバイス CDM 分類レベル:±1000V
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 2 チャネルの双方向バッファ
- I^2C バスおよび SMBus 互換
- A 側の動作電源電圧範囲:0.9V～5.25V
- B 側の動作電源電圧範囲:2.7V～5.25V
- 0.9V から 5.25V へと、2.7V から 5.25V への電圧レベル変換
- アクティブ HIGH のリピータ・イネーブル入力
- オープン・ドレインの I^2C I/O
- 5.25V 許容の I^2C およびイネーブル入力で、混在モードの信号動作に対応
- 標準モードおよびファースト・モード I^2C デバイスおよび複数のコントローラに対応
- 電源オフ時に I^2C ピンが高インピーダンス
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- サーバー
- ルーター (テレコム・スイッチング機器)
- 産業用機器
- 多くの I^2C ターゲットや長い PCB 配線を持つ製品

3 概要

TCA9517-Q1 は、I^2C および SMBus システム用の、レベル・シフト機能付き双方向バッファです。混在モード・アプリケーションで、低電圧 (最低 0.9V) と、より高い電圧 (2.7V～5.25V) との間の双方向電圧レベル変換 (昇圧変換 / 降圧変換) を行います。このデバイスにより、I^2C および SMBus システムを拡張でき、レベル・シフト時にも性能損失を防ぐことができます。

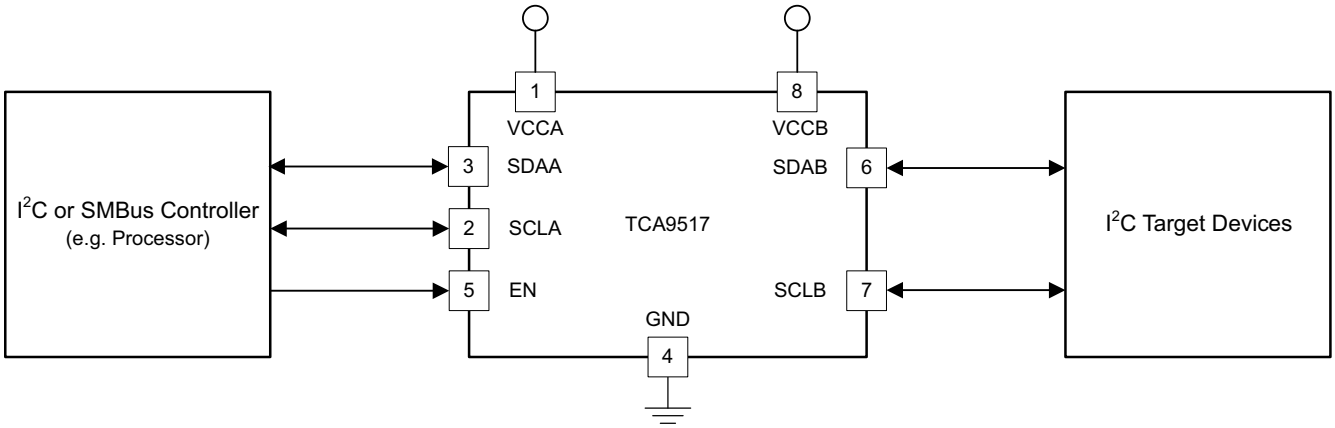
TCA9517-Q1 は、I^2C バス上でシリアル・データ (SDA) とシリアル・クロック (SCL) 信号の両方をバッファするため、最大 400pF のバス容量を持つ 2 つのバスを I^2C アプリケーション内で接続できます。

TCA9517-Q1 は、2 種類のドライバ (A 側ドライバと B 側ドライバ) を備えています。すべての入力と I/O は、デバイスの電源がオフのとき (V_{CCB}、V_{CCA} = 0V) も含めて、5.25V までの過電圧を許容します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCA9517-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 概要 (続き) ... 3
6 Pin Configuration and Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 6
7.5 Electrical Characteristics ... 7
7.6 Timing Requirements ... 7
7.7 I^2C Interface Switching Characteristics ... 8
7.8 Typical Characteristics ... 9
8 Parameter Measurement Information ... 10
9 Detailed Description ... 11
9.1 Overview ... 11
9.2 Functional Block Diagram ... 11
9.3 Feature Description ... 12
9.4 Device Functional Modes ... 12
10 Application and Implementation ... 13
10.1 Application Information ... 13
10.2 Typical Application ... 13
11 Power Supply Recommendations ... 16
12 Layout ... 17
12.1 Layout Guidelines ... 17
12.2 Layout Example ... 17
13 Device and Documentation Support ... 18
13.1 Device Support ... 18
13.2 Receiving Notification of Documentation Updates ... 18
13.3 サポート・リソース ... 18
13.4 Trademarks ... 18
13.5 Electrostatic Discharge Caution ... 18
13.6 Glossary ... 18

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2018) to Revision A (February 2022)	Page
• すべての古い用語をコントローラおよびターゲットに変更	1
• 「*特長*」に「機能安全対応」を追加	1

5 概要 (続き)

B 側のバッファ設計により、静的電圧オフセットを使用するデバイスと直列に使用することが防止されます。このデバイスはバッファされた LOW 信号を有効な LOW とは認識せず、バッファされた LOW として再度伝搬することはありません。

B 側のドライバは、2.7V～5.25V で動作します。この内部バッファの出力 LOW レベルは約 0.5V です。出力が内部で LOW に駆動されるとき、入力電圧は出力 LOW レベルよりも 70mV 以上低い必要があります。より電圧の高い LOW 信号は、バッファされた LOW と呼ばれます。B 側の I/O が内部で LOW に駆動されるとき、この LOW は入力によって LOW と認識されません。この機能により、入力 LOW 条件が解除されたとき、ロックアップ状況が発生することが防止されます。

A 側のドライバは 0.9V～5.25V で動作し、より多くの電流を駆動します。これらのドライバには、バッファされた LOW の機能 (または、静的なオフセット電圧) が必要ありません。B 側の LOW 信号は、A 側ではほぼ 0V の LOW に変換されます。これによって、低電圧のロジックの小さな電圧スイングに対応できます。A 側の出力プルダウンは、ハード LOW を駆動します。この入力レベルは、低電圧側の電源電圧が最低 0.9V のシステムにおいて、低い LOW レベルの要求に対応できるよう、0.3 × V_{CCA} に設定されます。

2 つ以上の TCA9517-Q1 デバイスの A 側を互いに接続可能です。これは、A 側を共通バスとした多くの回路形式 (図 8、図 9 を参照) を可能にします。A 側は、静的または動的オフセット電圧を持つその他のすべてのバッファに直接接続できます。複数の TCA9517-Q1 デバイスを A 側から B 側へ直列に接続でき、この場合にオフセット電圧の蓄積はなく、タイム・オブ・フライト遅延のみを考慮すれば十分です。B 側からのバッファされた LOW 電圧の関係で、TCA9517-Q1 を B 側から B 側に接続することはできません。B 側は、立ち上がり時間アクセラレータを持つデバイスには接続できません。

VCCA は、A 側の入力コンパレータに 0.3 × V_{CCA} の基準電圧を供給するためと、パワー・グッド検出回路にのみ使用されます。TCA9517-Q1 のロジックおよびすべての I/O は、VCCB ピンから電力を供給されます。

標準の I^2C システムと同様に、バッファされたバスにロジック HIGH レベルを与えるにはプルアップ抵抗が必要です。TCA9517-Q1 は、I^2C バスの標準的なオープン・ドレイン構成を持っています。これらのプルアップ抵抗のサイズはシステムに依存しますが、リピータの各側にプルアップ抵抗が必要です。このデバイスは、SMBus デバイスに加えて、標準モードおよびファースト・モードの I^2C デバイスとともに動作するよう設計されています。標準モードの I^2C デバイスは、一般的な I^2C システムで 3mA のみが規定されており、標準モード・デバイスと複数のマスタを使用可能です。場合によっては、より大きな終端電流を使用できます。

6 Pin Configuration and Functions

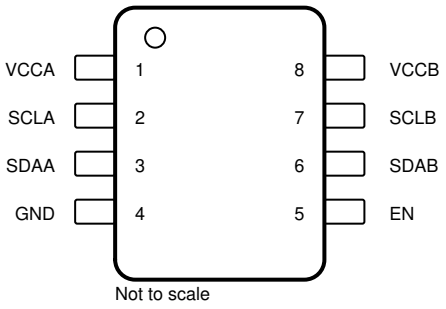


図 6-1. DGK (VSSOP) Package, 8-Pin, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9 V to 5.25 V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7 V to 5.25 V)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9(2)	5.25	V
V_{CCB}	Supply voltage, B-side bus	$V_{CCA} \le V_{CCB}$	2.7	5.25	V
		$V_{CCA} > V_{CCB}$	2.9	5.25	
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	5.25	V
		SDAB, SCLB	0.7 × V_{CCB}	5.25	
		EN	0.7 × V_{CCB}	5.25	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB(1)		0.3 × V_{CCB}	
		EN		0.3 × V_{CCB}	
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature		–40	125	°C

(1) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See *セクション 10.2.2.2* for V_{ILC} application information
(2) Low-level supply voltage

7.4 Thermal Information

THERMAL METRIC(1)		TCA9517-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.25 V, GND = 0 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.7 V to 5.25 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100 µA or 6 mA, V_{ILA} = V_{ILB} = 0 V	2.7 V to 5.25 V	0.45	0.52	0.6	V
		SDAA, SCLA	I_{OL} = 6 mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB	ensured by design	2.7 V to 5.25 V		70		mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7 V to 5.25 V		0.4		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.25 V		1.5	5	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			3	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7 V to 5.25 V			±1	µA
			V_I = 0.2 V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2 V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2 V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V	2.7 V to 5.25 V			10	µA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V		6	10	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V		8	13	
				0 V		7	11	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V		8	13	pF
				0 V		7	11	

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

7.7 I²C Interface Switching Characteristics

V_{CCB} = 2.7 V to 5.25 V, GND = 0 V, T_A = –40°C to 125°C (unless otherwise noted)(1) (4)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(5)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(3) (see 図 8-4)	SDAA, SCLA(3) (see 図 8-4)			141	250	ns
			SDAA, SCLA(2) (see 図 8-3)	SDAB, SCLB(2) (see 図 8-3)			74	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	V_{CCA} ≤ 2.7 V (see 図 8-2)		76(6)	110	ns
					V_{CCA} ≥ 3 V (see 図 8-2)		95	290	
			SDAA, SCLA(2) (see 図 8-3)	SDAB, SCLB(2) (see 図 8-3)			107	230	
t_{TLH}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see 図 8-3)		12		ns
					V_{CCA} ≥ 3 V (see 図 8-3)		42		
		A side to B-side (see 図 8-2)					125		
t_{THL}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see 図 8-3)		67(6)	200	ns
					V_{CCA} ≥ 3 V (see 図 8-3)		86	240	
		A side to B-side (see 図 8-2)					48	120	

(1) Times are specified with loads of 1.35-kΩ pull-up resistance and 50-pF load capacitance on the B-side. On the A side, for 0.9-V ≤ V_{CCA} ≤ 2.7-V, a 167-Ω pull-up and 57-pF load capacitance. For V_{CCA} ≥ 3.0-V, a 450-Ω pull-up and 57-pF load capacitance. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) The proportional delay data from A to B-side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B-side.
(3) The t_{PLH} delay data from B to A side is measured at 0.4 V on the B-side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(4) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
(5) Typical values were measured with V_{CCA} = V_{CCB} = 3.3 V at T_A = 25°C, unless otherwise noted.
(6) Typical value measured with V_{CCA} = 2.7 V at T_A = 25°C

7.8 Typical Characteristics

V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

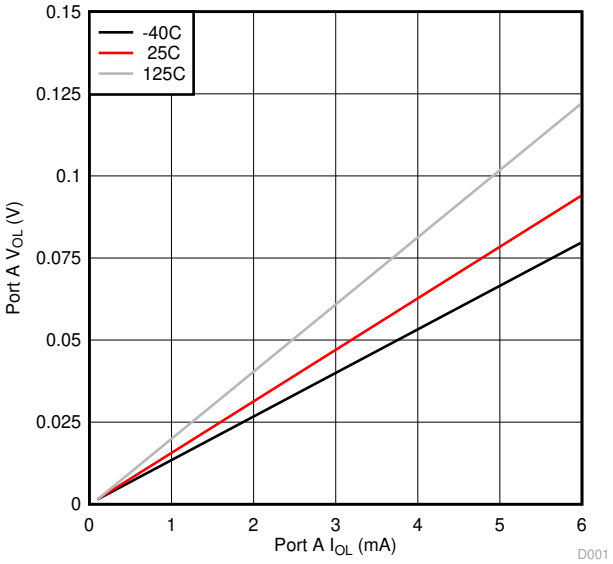


図 7-1. Port A V_{OL} vs I_{OL}

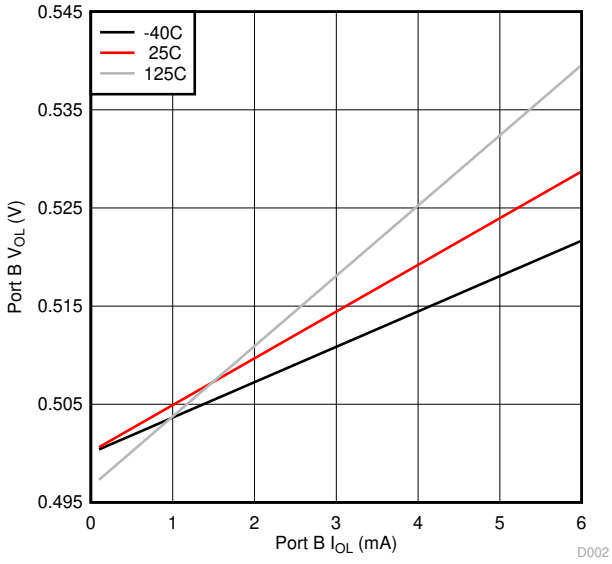
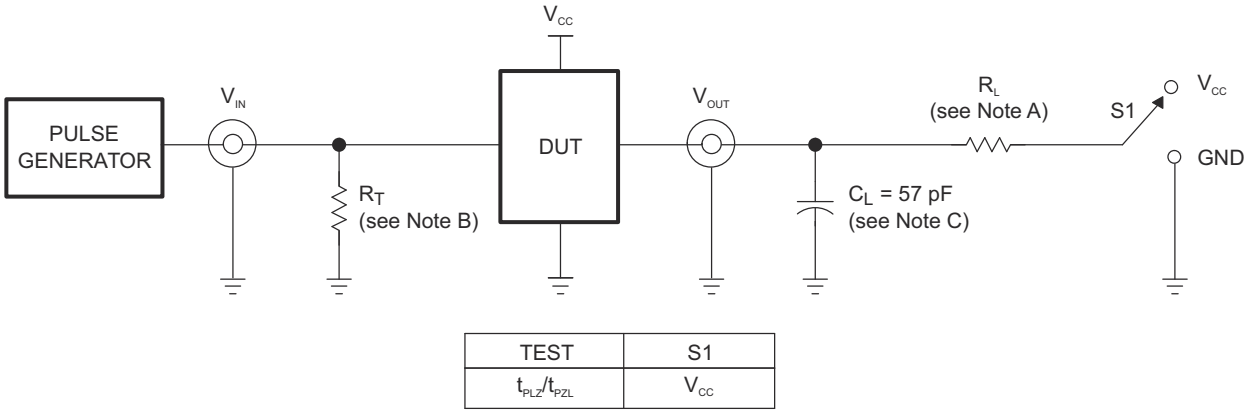


図 7-2. Port B V_{OL} vs I_{OL}

8 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

A. R_L = 167 Ω (0.9 V to 2.7 V) and R_L = 450 Ω (3.0 V to 5.25 V) on the A side and 1.35 kΩ on the B-side
B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
C. C_L includes probe and jig capacitance. C_L = 50 pF when on the B-side.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
H. t_{PZL} and t_{PZH} are the same as t_{en}.

図 8-1. Test Circuit

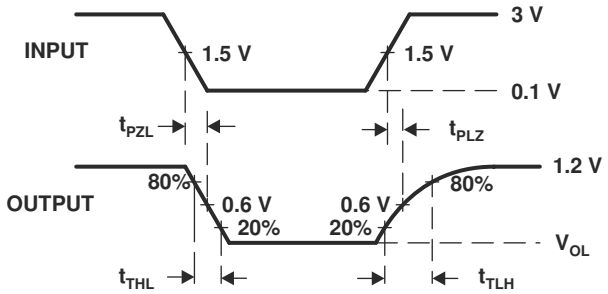


図 8-2. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

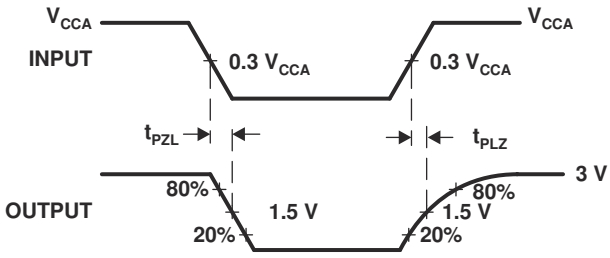


図 8-3. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

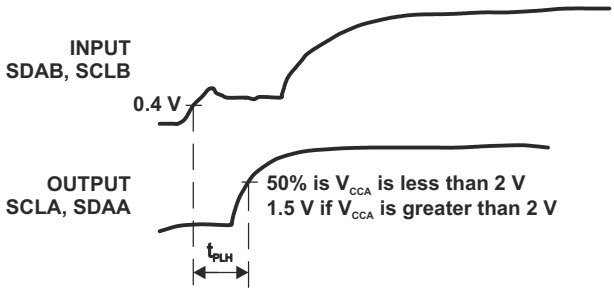


図 8-4. Waveform 3 – Propagation Delay for B-side to A-side

9 Detailed Description

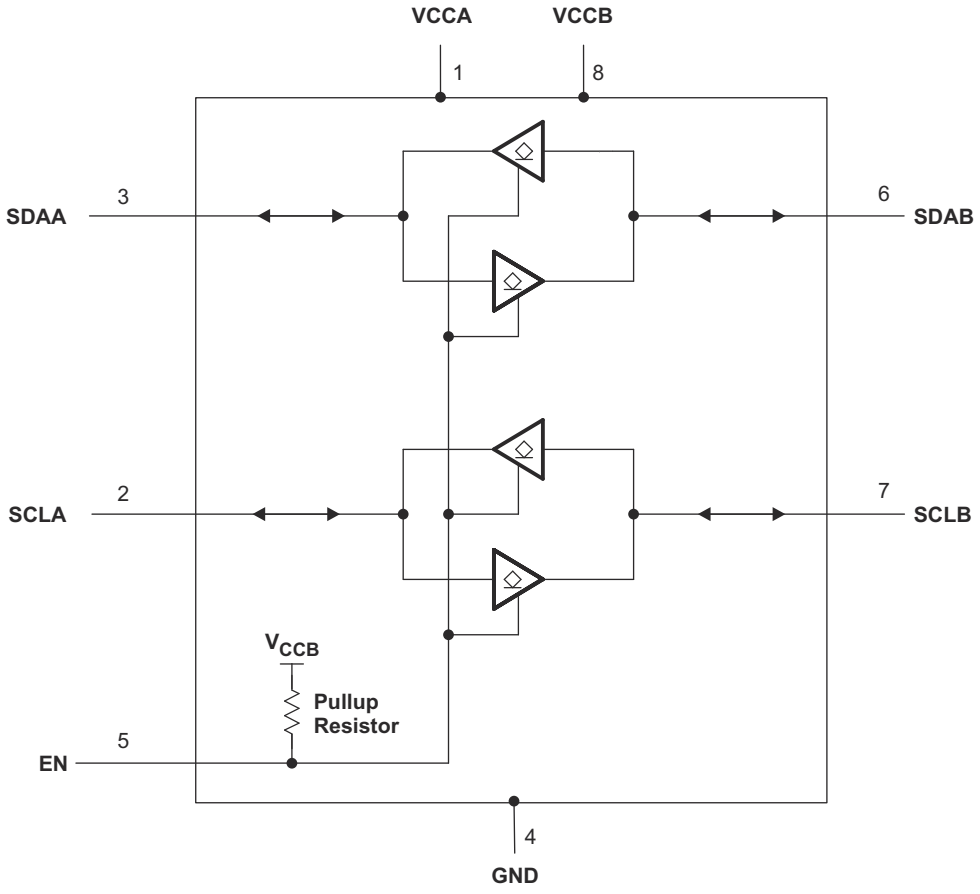
9.1 Overview

The TCA9517-Q1 is a bidirectional buffer with level shifting capabilities for I^2C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.25 V) in mixed-mode applications. This device enables I^2C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517-Q1 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I^2C application.

The TCA9517-Q1 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.25 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517-Q1 is a two-channel bidirectional buffer with level-shifting capabilities

9.3.2 Active-High Repeater-Enable Input

The TCA9517-Q1 has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved target on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.25 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517-Q1 supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

表 9-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

10 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

A typical application is shown in 図 10-1. In this example, the system controller is running on a 3.3 V I^2C bus, and the target is connected to a 1.2 V I^2C bus. Both buses run at 400 kHz. Controller devices can be placed on either bus.

The TCA9517-Q1 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.25 V bus voltages and 2.7 V to 5.25 V bus voltages.

When the A side of the TCA9517-Q1 is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517-Q1 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to 図 10-3 and 図 10-4. If the bus controller in 図 10-1 were to write to the target through the TCA9517-Q1, waveforms shown in 図 10-3 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517-Q1, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517-Q1. After the eighth clock pulse, the data line is pulled to the V_{OL} of the target device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517-Q1 for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

10.2 Typical Application

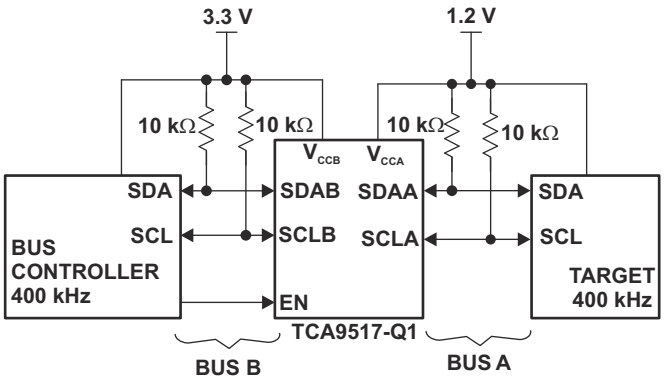


図 10-1. Typical Application Schematic

10.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9 V to 5.25 V
- V_{CCB} = 2.7 to 5.25 V
- B-side ports must not be connected together

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9517-Q1 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

10.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517-Q1 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.4 V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

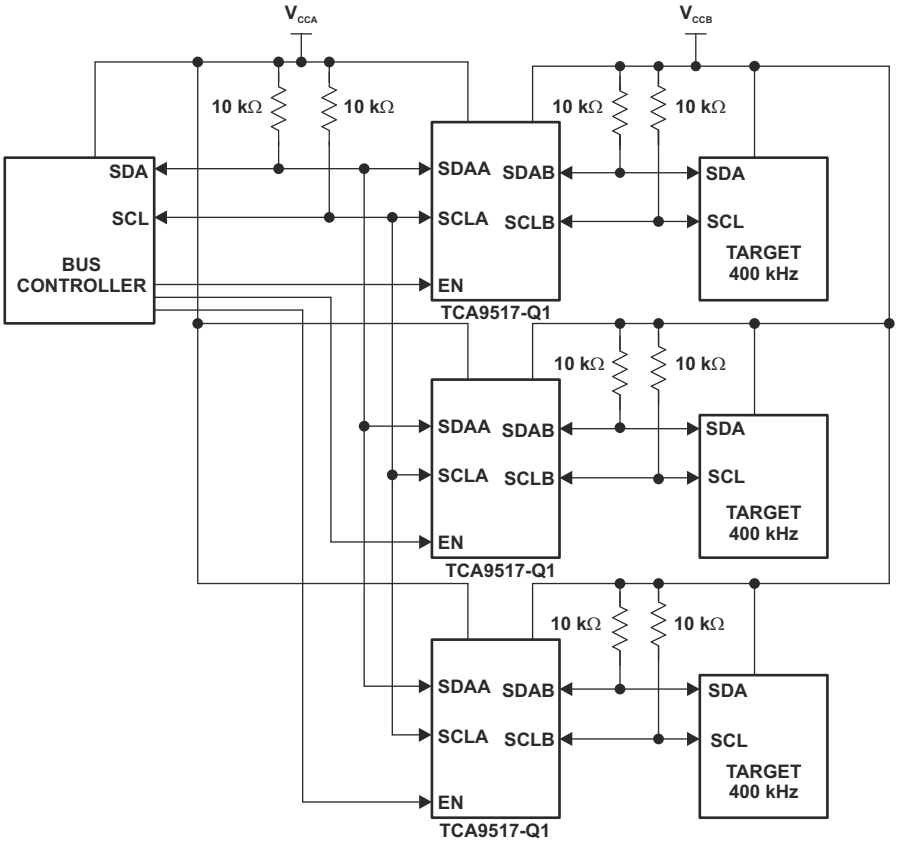


図 10-2. Typical Star Application

Multiple A sides of TCA9517-Q1s can be connected in a star configuration, allowing all nodes to communicate with each other.

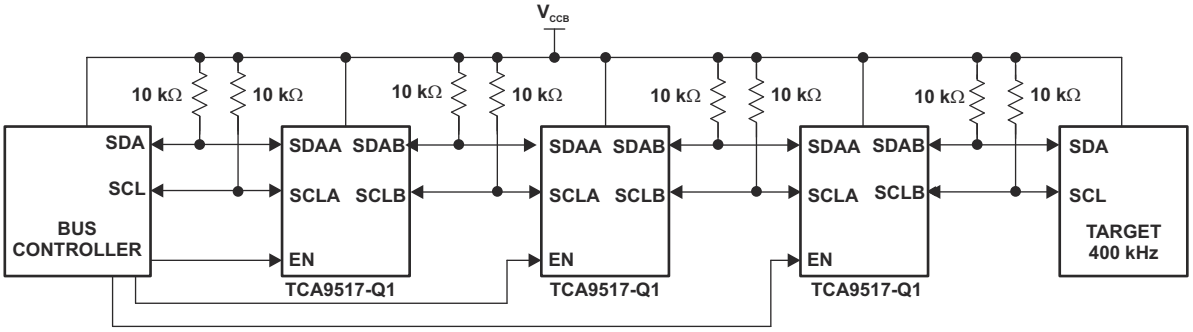


図 10-3. Typical Series Application

To further extend the I^2C bus for long traces/cables, multiple TCA9517-Q1s can be connected in series as long as the A-side is connected to the B-side. I^2C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

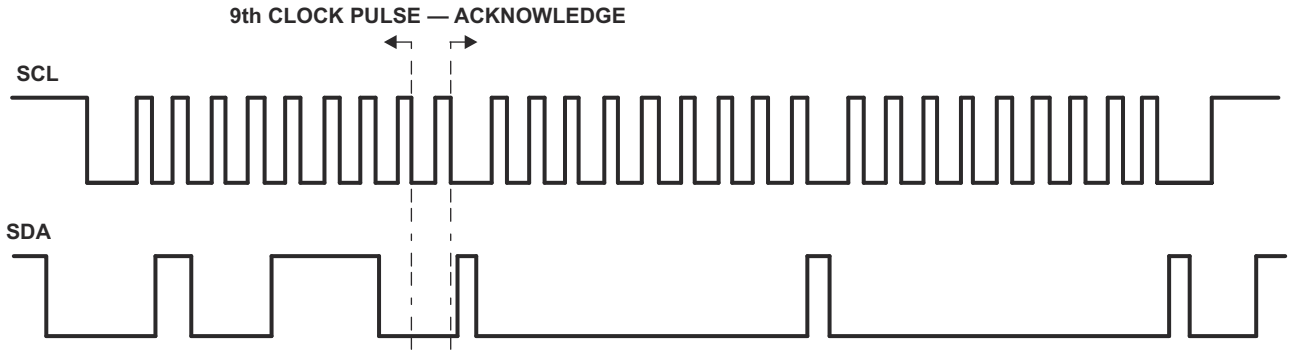


図 10-4. Bus A (0.9 V to 5.25 V Bus) Waveform

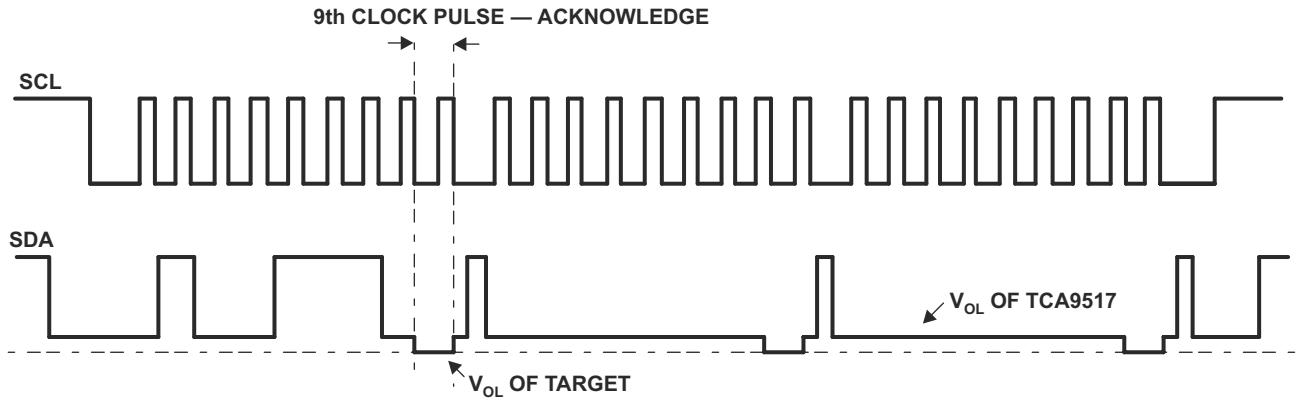


図 10-5. Bus B (2.7 V to 5.25 V Bus) Waveform

10.2.3 Application Curve

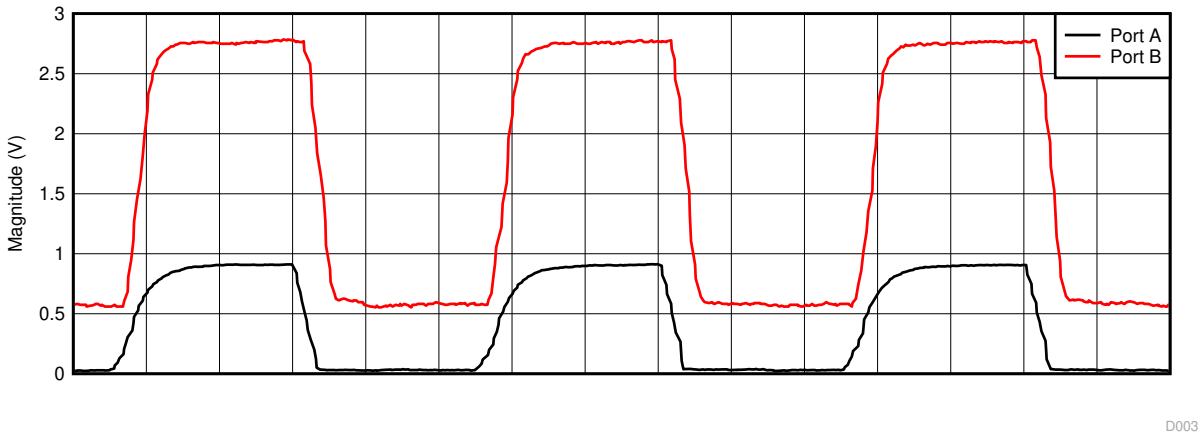


図 10-6. Voltage Translation at 400 kHz, V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517-Q1 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the A-side (below 0.3 × V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above 0.3 × V_{CCA}, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below 0.3 × V_{CCB}, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above 0.7 × V_{CCB}. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above 0.3 × V_{CCA}.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.

12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517-Q1.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

図 12-1 shows an example layout of the DGK package.

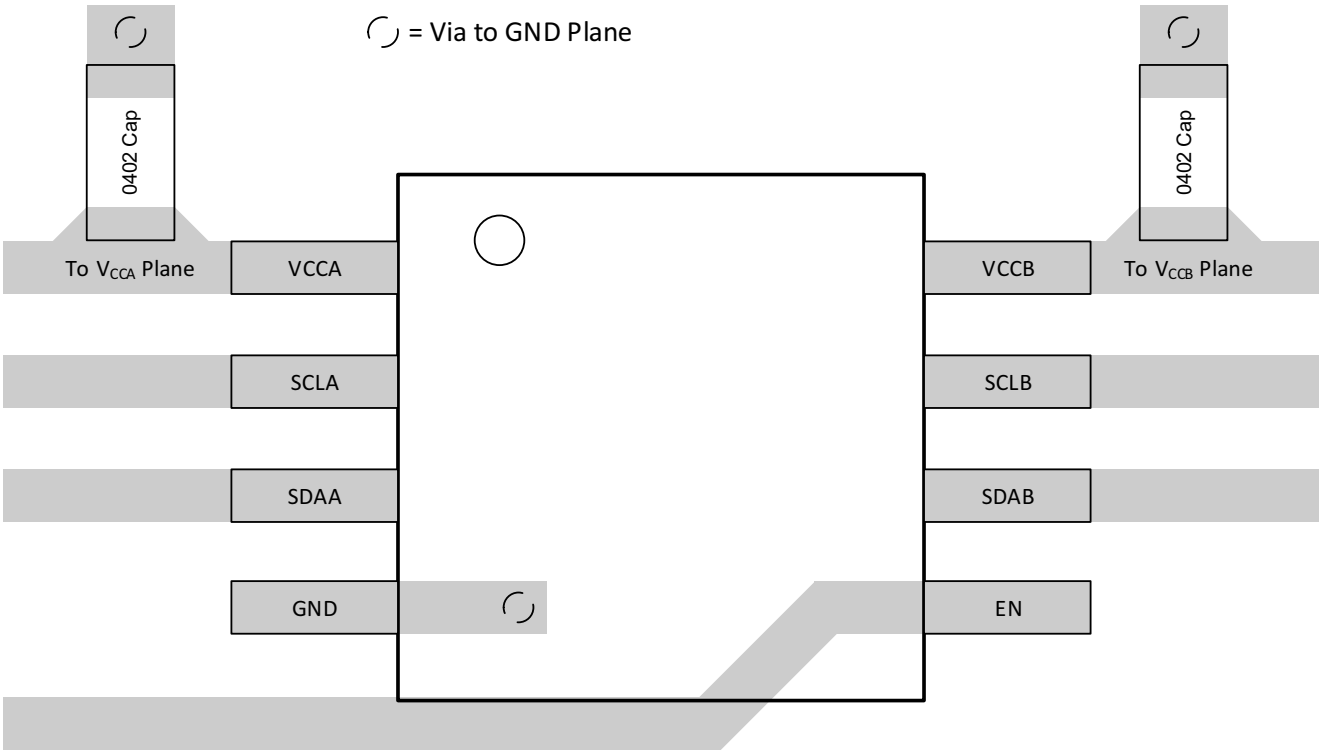


図 12-1. TCA9517-Q1A Layout Example

13 Device and Documentation Support

13.1 Device Support

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9517DGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1N2
TCA9517DGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TCA9517-Q1 :

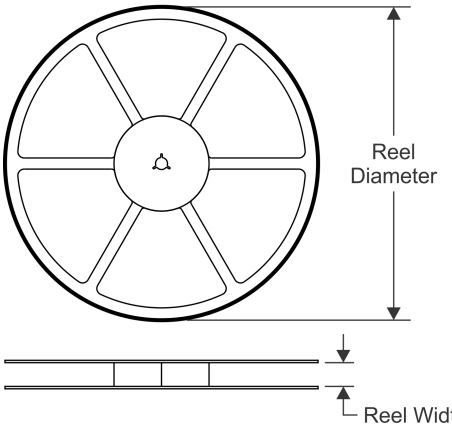
- Catalog : TCA9517

NOTE: Qualified Version Definitions:

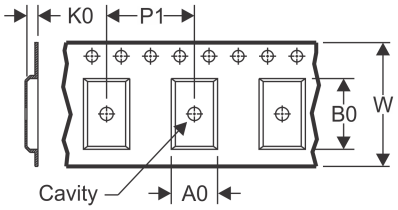
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

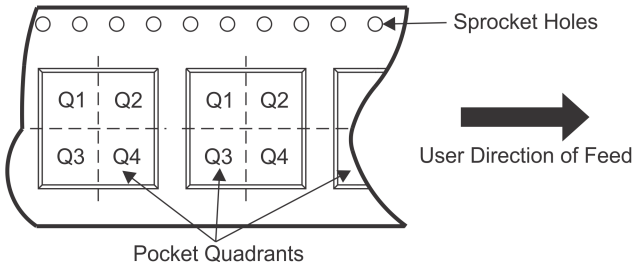


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

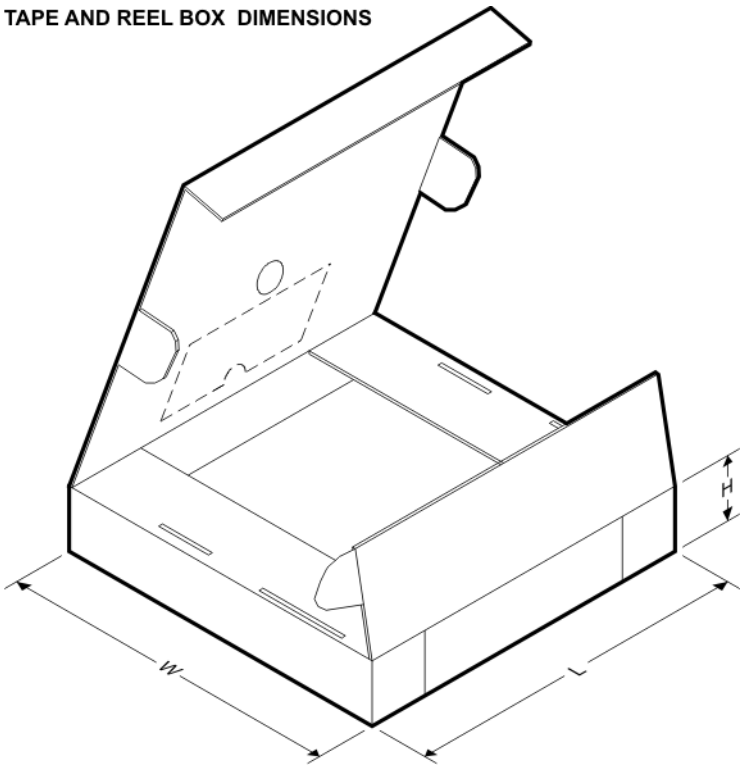
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9517DGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

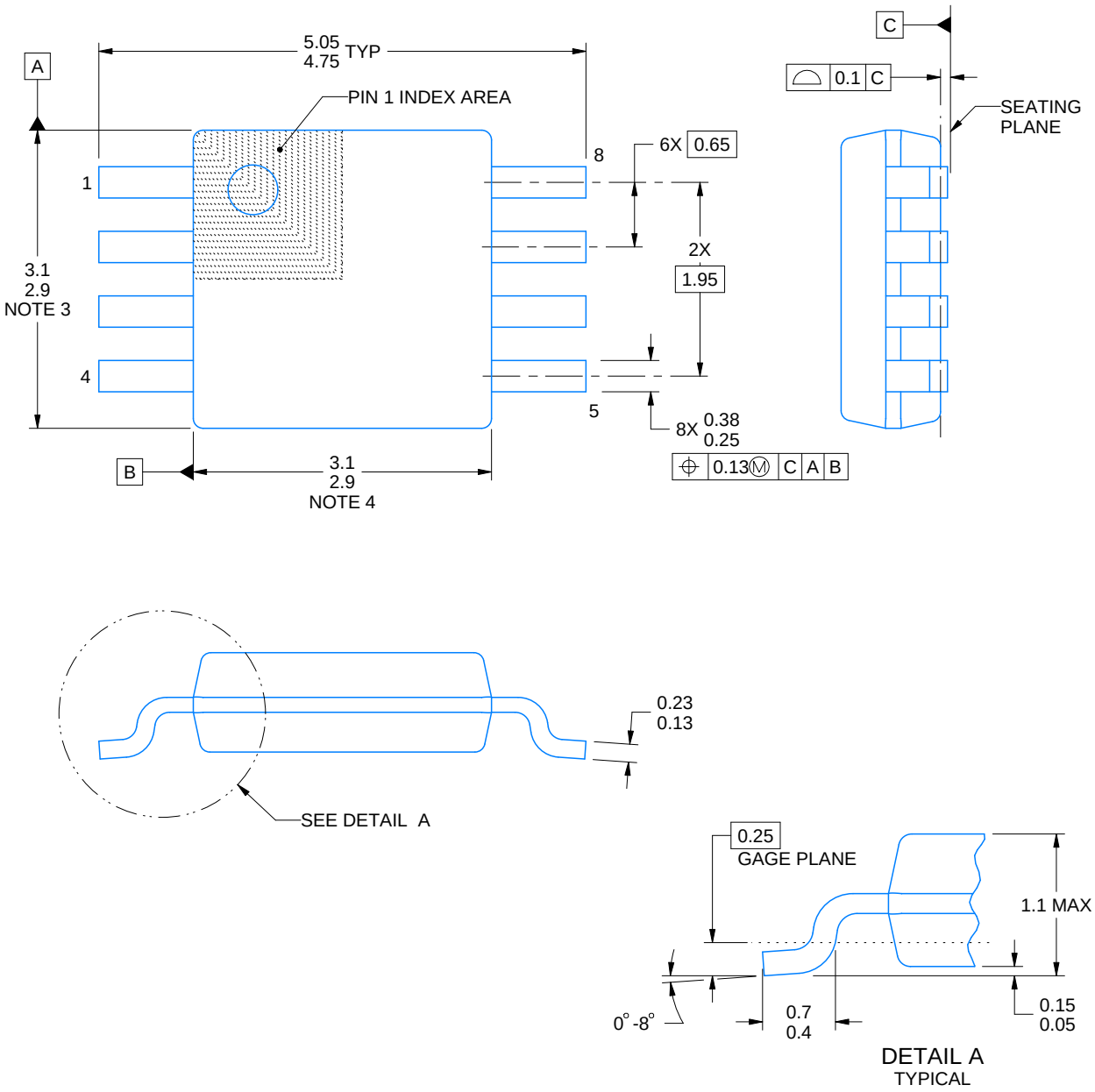
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9517DGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

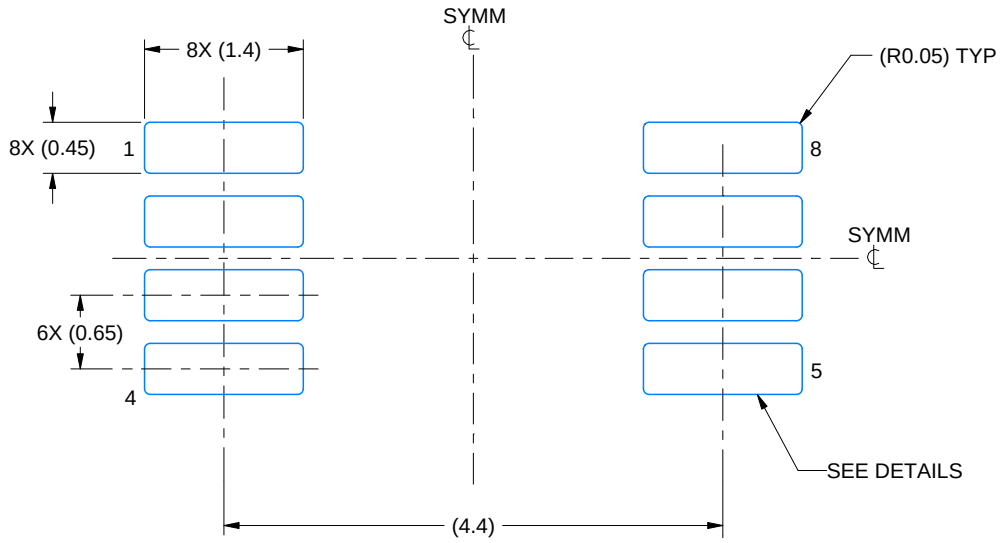
SMALL OUTLINE PACKAGE



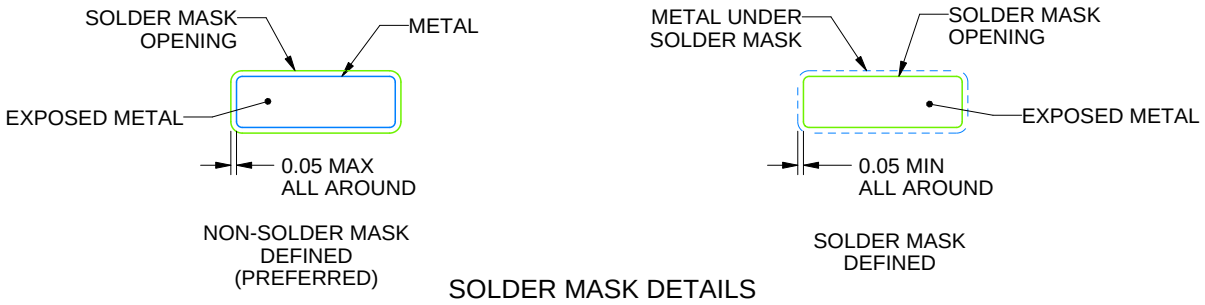
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

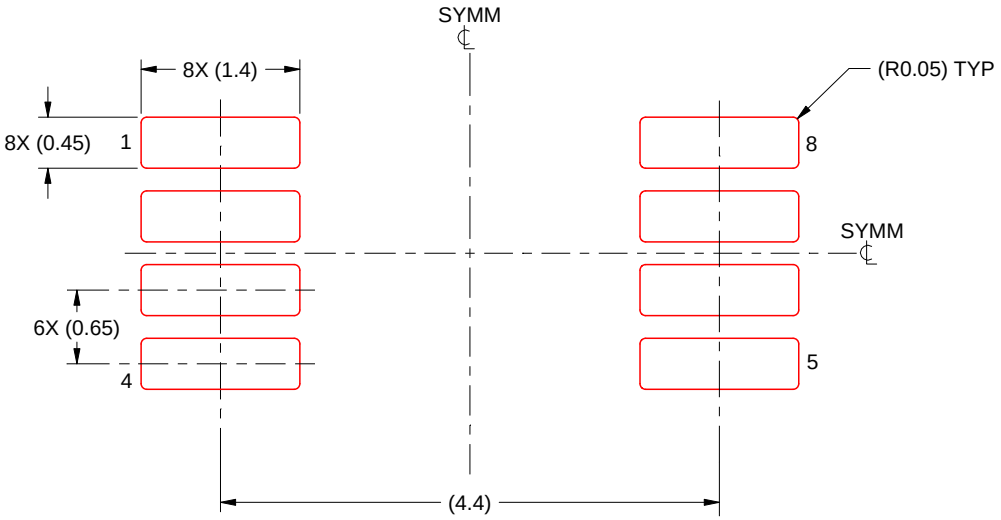


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月