



Now



Support & 20 Community



TAS5782M

JAJSDH3A – MARCH 2016 – REVISED JULY 2017

TAS5782M 96kHzプロセッシングの30WステレオClass-Dアンフ

1 特長

Texas

柔軟なオーディオI/O構成

INSTRUMENTS

- I²S、TDM、LJ、RJデジタル入力をサポート
- サンプル・レートのサポート
- BDアンプ変調
- 3線式のデジタル・オーディオ・インターフェイスを サポート(MCLK不要)
- 高性能のクローズド・ループ・アーキテクチャ $(PVDD = 12V, R_{SPK} = 8\Omega, SPK_GAIN = 20dB)$
 - クローズド・ループによりコンポーネント数の削減と 小さなソリューション・サイズを実現
 - アイドル・チャネル・ノイズ = 62µVrms (A-Wtd)
 - THD+N = 0.2% (1W、1kHzのとき)
 - SNR = 103dB A-Wtd (THD+N = 1%を基準)
- 柔軟な処理機能
 - 15 BiQuads/SmartEQ
 - X-Over/EQ用の2x5 BiQuads
 - 3バンドの高度なDRC + AGL
 - 動的EQおよびSmartBass
 - SFS (Sound Field Spatializer)
 - 96kHzのプロセッサ・サンプリング
- 通信機能

ΔĀ

- I²Cポートによるソフトウェア・モード制御
- 2つのアドレス選択ピン 最大4デバイス
- 堅牢性および信頼性の特長
 - クロック誤差、DC、および短絡保護
 - 過熱および過電流からの保護機能



2 アプリケーション

- LCD、LED TV、多用途モニタ
- サウンド・バー、ドッキング・ステーション、PC オーディオ
- ワイヤレス・サブウーファー、Bluetoothスピー カ、アクティブ・スピーカ

3 概要

TAS5782Mデバイスは高性能のステレオ、クローズド・ ループ、Class-Dアンプで、最高96kHzアーキテクチャの オーディオ・プロセッサが内蔵されています。デジタルから アナログへの変換を行うため、デバイスは高性能のDACと Burr Brown™オーディオ・テクノロジを使用します。必要 な電源は、低電圧回路用のDVDD 1つと、高電圧回路用 のPVDD 1つだけです。このデバイスは、標準のI²C通信 を使用して、ソフトウェア制御ポートにより制御されます。

r_{DS(on)}が90mΩの出力MOSFETにより、熱性能とデバイス のコストについて最良のバランスが達成されます。さらに、 熱的に強化された48ピンTSSOPは、今日のコンシューマ 向け電子機器にみられる高い周辺温度において、非常に 優れた動作を実現します。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TAS5782M	TSSOP (48)	12.50mm×6.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末 尾にある注文情報を参照してください。



10% THD+Nでの電力とPVDDとの関係⁽¹⁾

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内 容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。 English Data Sheet: SLASEG8

目次

1	特長1	
2	アプリケーション1	
3	概要1	
4	改訂履歴	2
5	Device Comparison Table 3	5
6	Pin Configuration and Functions 4	ŀ
	6.1 Internal Pin Configurations	5
7	Specifications)
	7.1 Absolute Maximum Ratings 9)
	7.2 ESD Ratings 9)
	7.3 Recommended Operating Conditions 10)
	7.4 Thermal Information 10)
	7.5 Electrical Characteristics 11	
	7.6 Power Dissipation Characteristics 15	,
	7.7 MCLK Timing 20)
	7.8 Serial Audio Port Timing - Slave Mode 20)
	7.9 Serial Audio Port Timing – Master Mode 21	
	7.10 I ² C Bus Timing – Standard 21	
	7.11 I ² C Bus Timing – Fast 21	
	7.12 SPK_MUTE Timing 22)
	7.13 Typical Characteristics 24	ł
8	Parametric Measurement Information	5
9	Detailed Description 34	ł

	9.1	Overview	34
	9.2	Functional Block Diagram	34
	9.3	Feature Description	35
	9.4	Device Functional Modes	56
10	Арр	lication and Implementation	<mark>5</mark> 9
	10.1	Application Information	<mark>59</mark>
	10.2	Typical Applications	61
11	Pow	ver Supply Recommendations	70
	11.1	Power Supplies	70
12	Lay	out	72
	12.1	Layout Guidelines	72
	12.2	Layout Example	74
13	Reg	ister Maps	80
	13.1	Registers - Page 0	80
	13.2	Registers - Page 1	116
14	デバ	イスおよびドキュメントのサポート	120
	14.1	デバイス・サポート	120
	14.2	ドキュメントの更新通知を受け取る方法	120
	14.3	コミュニティ・リソース	121
	14.4	商標	121
	14.5	静電気放電に関する注意事項	121
	14.6	Glossary	121
15	メカニ	ニカル、パッケージ、および注文情報	121

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年3月発行のものから更新

•	Added missing cross references to the Quick Reference Table	. 24
•	Changed Changed the Volume Ramp Up/Down Step default value to 11	. 50
•	Changed 5th bit of the PC Slave Address table	. 54
•	Added DSP Book, Page, and Register Update section	. 56
•	Deleted Page 0 Registers 0x0A, 0x50, 0x51, 0x52, and 0x54	. 80
•	Changed the PLLE bit type of Register 4 from R to R/W	. 81
•	Changed Bit configuration of Register 0x14	. 88
•	Changed PJDV bit in Register 21 from 5-4 to 5-0	. 89
•	Changed Reset value of Register 0x3D to '00110000'	. 98
•	Changed Bit configuration of Register 0x5D	112
•	Deleted Page 1 Registers 0x05 and 0x08	116

INSTRUMENTS

Texas

www.ti.com

Page

5 Device Comparison Table

DEVICE NAME	MODULATION STYLE	PROCESSING TYPE
TAS5782MDCA	BD Modulation	100 MIPs, Flexible Process flow (Uses mixture of RAM and ROM components to create several process flows)
TAS5754MDCA	1SPW (Ternary)	50 MIPs, HybridFlow (Uses mixture of RAM and ROM components to create several process flows)
TAS5756MDCA	BD Modulation	50 MIPs, HybridFlow (Uses mixture of RAM and ROM components to create several process flows)
TAS5766MDCA	BD Modulation	50 MIPs, Fixed-Function (Uses single ROM image of process flow)

TAS5782M JAJSDH3A – MARCH 2016–REVISED JULY 2017



www.ti.com

6 Pin Configuration and Functions





Pin Functions

PIN			INTERNAL	DESCRIPTION				
NAME	NO.	ITPE"	TERMINATION	DESCRIPTION				
ADR0	26	DI		Sets the LSB of the I ² C address to 0 if pulled to GND, to 1 if pulled to DVDD				
ADR1	20	DI		Sets the second LSB of the I ² C address to 0 if pulled to GND, to 1 if pulled to DVDD				
AGND	10 15	G	_	Ground reference for analog circuitry ⁽²⁾				
AVDD	14	Р	Figure 2	Power supply for internal analog circuitry				
BSTRPA-	1	Р		Connection point for the SPK_OUTA- bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTA-				
BSTRPA+	5	Р	Figure 2	Connection point for the SPK_OUTA+ bootstrap capacitor which is used to create a power supply for he high-side gate drive for SPK_OUTA+ Connection point for the SPK_OUTB– bootstrap capacitor which is used to create a power supply for				
BSTRPB-	48	Р	Figure 5	Connection point for the SPK_OUTB– bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB–				
BSTRPB+	44	Р		Connection point for the SPK_OUTB+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB+				
CN	34	Р	Figure 14	Negative pin for capacitor connection used in the line-driver charge pump				
CP	32	Р	Figure 13	Positive pin for capacitor connection used in the line-driver charge pump				
CPVDD	31	Р	Figure 2	Power supply for charge pump circuitry				
CPVSS	35	Р	Figure 14	-3.3-V supply generated by charge pump for the DAC				
DAC_OUTA	13	AO	Figure 9	Single-ended output for Channel A of the DAC				
DAC_OUTB	36	AO	Figure o	Single-ended output for Channel B of the DAC				
DGND	29	G	_	Ground reference for digital circuitry. Connect this pin to the system ground.				
DVDD	30	Р	Figure 2	Power supply for the internal digital circuitry				
DVDD_REG	28	Р	Figure 15	Voltage regulator derived from DVDD supply for use for internal digital circuitry. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.				
GND	33	G	_	Ground pin for device. This pin should be connected to the system ground.				
GPIO0	18	51/2						
GPIO2	21	DI/O		General purpose input/output pins (GPIOx). Refer to GPIO registers for configuration.				
GVDD_REG	8	Р	Figure 5	Voltage regulator derived from PVDD supply to generate the voltage required for the gate drive of output MOSFETs. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.				
LRCK/FS	25	DI/O	Figure 11	Word select clock for the digital signal that is active on the serial port's input data line. In I ² S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.				
MCLK	22	DI		Master clock used for internal clock tree and sub-circuit and state machine clocking				
	3							
PGND	39	G	_	Ground reference for power device circuitry. Connect this pin to the system ground.				
	46							
	6							
	7							
PVDD	41	Р	Figure 1	Power supply for internal power circuitry				
	42							
	43							
RESET	19	DI	Figure 17	Device reset input. Pull down to reset, pull up to activate device.				
SCL	17	DI	Figure 10	I ² C serial control port clock				
SCLK	23	DI/O	Figure 11	Bit clock for the digital signal that is active on the input data line of the serial data port				
SDA	16	DI/O	Figure 9	I ² C serial control port data				
SDIN	24	D1	Figure 11	Data line to the serial data port				
SPK INA-	11	AI		Negative pin for differential speaker amplifier input A				
SPK INA+	12	AI	1	Positive pin for differential speaker amplifier input A				
SPK INB-	38	AI	Figure 7	Negative pin for differential speaker amplifier input B				
SPK INB+	37	AI	1	Positive pin for differential speaker amplifier input B				
			1					

AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)
 This pin should be connected to the system ground.

TAS5782M JAJSDH3A – MARCH 2016–REVISED JULY 2017

www.ti.com

NSTRUMENTS

ÈXAS

Pin Functions (continued)

PIN			INTERNAL	DESCRIPTION
NAME	NO.	TTPE	TERMINATION	DESCRIPTION
SPK_FAULT	40	DO	Figure 16	Fault pin which is pulled low when an overcurrent, overtemperature, or DC detect fault occurs
SPK_GAIN/F REQ	9	AI	Figure 6	Sets the gain and switching frequency of the speaker amplifier, latched in upon start-up of the device.
SPK_OUTA-	2	AO		Negative pin for differential speaker amplifier output A
SPK_OUTA+	4	AO	Figure 4	Positive pin for differential speaker amplifier output A
SPK_OUTB-	B– 47 AO Figure 4		Figure 4	Negative pin for differential speaker amplifier output B
SPK_OUTB+	45	AO		Positive pin for differential speaker amplifier output B
SPK_MUTE	27	I	Figure 12	Speaker amplifier mute which must be pulled low (connected to DGND) to mute the device and pulled high (connected to DVDD) to unmute the device.
PowerPAD —		G	_	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it through solder. For proper electrical operation, this ground pad must be connected to the system ground.

6.1 Internal Pin Configurations





Figure 3. BSTRPxx Pins



Figure 2. AVDD, DVDD and CPVDD Pins







Internal Pin Configurations (continued)



Figure 5. GVDD_REG Pin



Figure 7. SPK_INxx Pins





Figure 6. SPK_GAIN/FREQ Pin



Figure 8. DAC_OUTx Pins



Figure 10. SCL Pin

FEXAS NSTRUMENTS

www.ti.com

Internal Pin Configurations (continued)











Figure 12. SPK_MUTE Pin







Figure 16. SPK_FAULT Pin



Internal Pin Configurations (continued)



7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
DVDD, AVDD, CPVDD	Low-voltage digital, analog, charge pump supply	-0.3	3.9	V
PVDD	PVDD supply	-0.3	30	V
V _{I(AmpCtrl)}	Input voltage for SPK_GAIN/FREQ and SPK_FAULT pins	-0.3	V_{GVDD} + 0.3	V
V _{I(DigIn)}	DVDD referenced digital inputs ⁽²⁾	-0.5	$V_{DVDD} + 0.5$	V
V _{I(SPK_INxx)}	Analog input into speaker amplifier	-0.3	6.3	V
V _{I(SPK_OUTxx)}	Voltage at speaker output pins	-0.3	32	V
	Ambient operating temperature, T _A	-25	85	°C
TJ	Operating junction temperature, digital die	-40	125	°C
	Operating junction temperature, power die	-40	165	°C
T _{stg}	Storage temperature	-40	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) <u>DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK, RESET, SCL, SCLK, SDA, SDIN, and SPK_MUTE.</u>

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	N/
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	V

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Free-air room temperature 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _(POWER)	Dowor oupply inputo	DVDD, AVDD, CPVDD	2.9		3.63	V
	Power supply inputs	PVDD	4.5		26.4	
P		BTL Mode	3			Ω
R _{SPK}	Minimum speaker load	PBTL Mode	2			Ω
V _{IH(DigIn)}	Input logic high for DVDD	referenced digital inputs ⁽¹⁾⁽²⁾	$0.9 \times V_{DVDD}$		V _{DVDD}	V
V _{IL(DigIn)}	Input logic low for DVDD	referenced digital inputs ⁽¹⁾⁽³⁾	V _{DVDD}	0	$0.1 \times V_{DVDD}$	V
L _{OUT}	Minimum inductor value i condition	n LC filter under short-circuit	1	4.7		μH

(1) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK, RESET, SCL, SCLK, SDA, SDIN, and SPK_MUTE.

(2) The best practice for driving the input pins of the TAS5782M device is to power the drive circuit or pullup resistor from the same supply which provides the DVDD power supply.

(3) The best practice for driving the input pins of the TAS5782M device low is to pull them down, either actively or through pulldown resistors to the system ground.

7.4 Thermal Information

		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5782MEVM 4-LAYER PCB	Ciari	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	27.6	19.4	°C/W	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.4	14.4	14.4	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	9.4	9.4	°C/W	
ΨJT	Junction-to-top characterization parameter	0.6	0.6	2	°C/W	
Ψјв	Junction-to-board characterization parameter	8.1	9.3	4.8	°C/W	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



7.5 Electrical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
DIGITAL I/O					
IIH 1	Input logic high current level for DVDD referenced digital input pins ⁽¹⁾	$V_{IN(DigIn)} = V_{DVDD}$		10	μA
IIL 1	Input logic low current level for DVDD referenced digital input pins ⁽¹⁾	V _{IN(DigIn)} = 0 V		-10	μA
V _{IH1}	Input logic high threshold for DVDD referenced digital inputs ⁽¹⁾		70%		V _{DVDD}
V _{IL1}	Input logic low threshold for DVDD referenced digital inputs ⁽¹⁾			30%	V _{DVDD}
V _{OH(DigOut)}	Output logic high voltage level ⁽¹⁾	I _{OH} = 4 mA	80%		V _{DVDD}
V _{OL(DigOut)}	Output logic low voltage level ⁽¹⁾	I _{OH} = -4 mA		22%	V _{DVDD}
VOL(SPK_FAULT)	Out <u>put logic low</u> voltage level for SPK_FAULT	With 100-k Ω pullup resistor		0.8	V
GVDD_REG	GVDD regulator voltage			7	V
I ² C CONTROL PO	ORT				
C _{L(I2C)}	Allowable load capacitance for each I ² C Line			400	pF
f _{SCL(fast)}	Support SCL frequency	No wait states, fast mode		400	kHz
f _{SCL(slow)}	Support SCL frequency	No wait states, slow mode		100	kHz
V _{NH}	Noise margin at High level for each connected device (including hysteresis)		$0.2 \times V_{DD}$		V
MCLK AND PLL	SPECIFICATIONS				
D _{MCLK}	Allowable MCLK duty cycle		40%	60%	
f _{MCLK}	Supported MCLK frequencies	Up to 50 MHz	128	512	f _S ⁽²⁾
f		Clock divider uses fractional divide $D > 0, P = 1$	6.7	20	
PLL	PLL input frequency	Clock divider uses integer divide $D = 0, P = 1$	1	20	
SERIAL AUDIO F	PORT				
t _{DLY}	Required LRCK/FS to SCLK rising edge delay		5		ns
D _{SCLK}	Allowable SCLK duty cycle		40%	60%	
f _S	Supported input sample rates		8	96	kHz
f _{SCLK}	Supported SCLK frequencies		32	64	f _S ⁽²⁾
f _{SCLK}	SCLK frequency	Either master mode or slave mode		24.576	MHz
SPEAKER AMPL	IFIER (ALL OUTPUT CONFIGUE	RATIONS)			
A	Speaker amplifier gain	SPK_GAIN/FREQ voltage < 3 V, see Adjustable Amplifier Gain and Switching Frequency Selection		20	dBV
Y V(SPK_AMP)	Speaker amplifier gain	SPK_GAIN/FREQ voltage > 3.3 V, see Adjustable Amplifier Gain and Switching Frequency Selection		26	άDν
$\Delta A_{V(SPK_AMP)}$	Typical variation of speaker amplifier gain			±1	dBV

⁽¹⁾ DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO2, LRCK/FS, MCLK, RESET, SCL, SCLK, SDA, SDIN, and SPK_MUTE.

⁽²⁾ A unit of f_S indicates that the specification is the value listed in the table multiplied by the sample rate of the audio used in the TAS5782M device.



Electrical Characteristics (continued)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{spk_amp}	Switching frequency of the speaker amplifier	Switching frequency depends on voltage presented at SPK_GAIN/FREQ pin and the clocking arrangement, including the incoming sample rate, see <i>Adjustable Amplifier Gain and</i> <i>Switching Frequency Selection</i>	176.4		768	kHz
K _{SVR}	Power supply rejection ratio	Injected Noise = 50 Hz to 60 Hz, 200 mV _{P-P} , Gain = 26 dB, input audio signal = digital zero		60		dB
r _{DS(on)}	Drain-to-source on resistance of the individual output MOSEETs	$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 24 \mbox{ V}, I_{(SPK_OUT)} = 500 \mbox{ mA}, \mbox{ T}_J = 25^{\circ}C, \\ includes \mbox{ PVDD/PGND pins, leadframe, bondwires} \\ and \mbox{ metallization layers.} \end{array}$		120		mΩ
		$V_{PVDD} = 24 \text{ V}, \text{ I}_{(SPK_OUT)} = 500 \text{ mA}, \text{ T}_J = 25^{\circ}\text{C}$		90		
OCE _{THRES}	SPK_OUTxx overcurrent error threshold			7.5		А
OTE _{THRES}	Overtemperature error threshold			165		°C
OCE _{CLRTIME}	Time required to clear overcurrent error after error condition is removed.			1.3		S
OTE _{CLRTIME}	Time required to clear overtemperature error after error condition is removed.			1.3		S
OVE _{THRES(PVDD)}	PVDD overvoltage error threshold			27		V
UVE _{THRES(PVDD)}	PVDD undervoltage error threshold			4.3		V
SPEAKER AMPL	IFIER (STEREO BTL)					
V _{OS}	Amplifier offset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20 dB gain, V_{PVDD} = 12 V		2		
		Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 26 dB gain, V_{PVDD} = 24 V		5	15	mv
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 $\Omega,$ A-Weighted		49		
		V_{PVDD} = 15 V, SPK_GAIN = 20 dB, R_{SPK} = 8 $\Omega,$ A-Weighted		59		
I _{CN(SPK)}	Idle channel noise	V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted		81		μν _{RMS}
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted		82		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{\text{SPK}} = 4 $\Omega,$ THD+N = 0.1%		14		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{\text{SPK}} = 8 $\Omega,$ THD+N = 0.1%		8		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{\text{SPK}} = 4 $\Omega,$ THD+N = 0.1%		23		
5		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R_{\text{SPK}} = 8 $\Omega,$ THD+N = 0.1%		13		10/
PO(SPK)	Output Power (Per Channel)	$\rm V_{PVDD}$ = 19 V, SPK_GAIN = 26 dB, $\rm R_{SPK}$ = 4 $\Omega,$ THD+N = 0.1%		34		W
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 19 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 8 \; \Omega, \\ THD \texttt{+N} = 0.1\% \end{array}$		20		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 24 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 4 \; \Omega, \\ THD \texttt{+N} = 0.1\% \end{array}$		40		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , THD+N = 0.1%		33		



Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{\text{SPK}} = 8 $\Omega,$ A-Weighted, –120 dBFS Input	103		
SND	Signal-to-noise ratio	V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	102		dP
SINK	signal)	V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	103		uВ
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	105		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 12 \ V, \ SPK_GAIN = 20 \ dB, \ R_{SPK} = 4 \ \Omega, \\ P_{O} = 1 \ W, \ f = 1 kHz \end{array}$	0.021%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R_{SPK} = 8 $\Omega,$ P_{O} = 1 W, f = 1kHz	0.022%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 15 \ V, \ SPK_GAIN = 26 \ dB, \ R_{SPK} = 4 \ \Omega, \\ P_{O} = 1 \ W, \ f = 1kHz \end{array}$	0.02%		
	Total harmonic distortion and	$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 15 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 8 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0.037%		
I HD+N _{SPK}	noise	$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 19 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 4 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0021%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 19 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 8 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0.028%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 24 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 4 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0.027%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , P _O = 1 W, f = 1kHz	0.038%		
		$V_{PVDD} = 12 V$, SPK_GAIN = 20 dB, R _{SPK} = 8 Ω , Input Signal 250 mVrms, 1-kHz Sine, across f(S)	-90		
X tolk	Cross-talk (worst case	$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 15 \ V, \ SPK_GAIN = 26 \ dBV, \ R_{SPK} = 8 \ \Omega, \\ Input \ Signal \ 250 \ mVrms, \\ 1\text{-kHz} \ Sine, \ across \ f(S) \end{array}$	-102		dP
A-Idik _{SPK}	right-to-left coupling)	$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 19 \; V, \; SPK_GAIN = 26 \; dBV, \; R_{SPK} = 8 \; \Omega, \\ Input \; Signal \; 250 \; mVrms, \\ 1\text{-kHz} \; Sine, \; across \; f(S) \end{array}$	-93		uв
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 24 \; V, \; SPK_GAIN = 26 \; dBV, \; R_{SPK} = 8 \; \Omega, \\ Input \; Signal \; 250 \; mVrms, \\ 1\text{-kHz} \; Sine, \; across \; f(S) \end{array}$	-93		
SPEAKER AMP	LIFIER (MONO PBTL)				
	Amplifier offect veltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20 dB gain, V_{PVDD} = 12 V	0.7		m\(
IVOSI	Ampliner onset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 26 dB gain, V_{PVDD} = 24 V	4		ΠV
		$V_{PVDD} =$ 12 V, SPK_GAIN = 20 dB, R _{SPK} = 8 Ω , A-Weighted	48		
	Idle channel reise	$V_{PVDD} = 15 \text{ V}, \text{SPK}_G\text{AIN} = 20 \text{ dB}, \text{RSPK} = 8 \Omega, \text{A-Weighted}$	49		
'CN	Idle channel noise	$V_{PVDD} =$ 19 V, SPK_GAIN = 26 dB, RSPK = 8 Ω , A-Weighted	83		µ v _{RMS}
		$$V_{\text{PVDD}}$$ = 24 V, SPK_GAIN = 26 dB, $\text{R}_{\text{SPK}}$$ = 8 $\Omega,$ A-Weighted	82		

Electrical Characteristics (continued)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R _{SPK} = 2 Ω , THD+N = 0.1%, Unless otherwise noted	30		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R _{SPK} = 4 Ω , THD+N = 0.1%, Unless otherwise noted	16		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R _{SPK} = 8 Ω , THD+N = 0.1%	9		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 2 Ω , THD+N = 0.1%, Unless otherwise noted	44		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 4 Ω , THD+N = 0.1%, Unless otherwise noted	22		
_		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , THD+N = 0.1%	13		
Po	Output power (per channel)	V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 2 Ω , THD+N = 0.1%, Unless otherwise noted	50		W
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 4 Ω , THD+N = 0.1%, Unless otherwise noted	36		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , THD+N = 0.1%	20		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 2 Ω , THD+N = 0.1%, Unless otherwise noted	40		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R _{SPK} = 4 Ω , THD+N = 0.1%, Unless otherwise noted	61		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{\text{SPK}} = 8 $\Omega,$ THD+N = 0.1%	34		
	Signal-to-noise ratio (referenced to 0 dBFS input signal)	V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	105		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	104		10
SNR		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , A-Weighted, -120 dBFS Input	105		dB
		V_{PVDD} = 24 V, SPK_GAIN = 26 dB, R_{SPK} = 8 $\Omega,$ A-Weighted, –120 dBFS Input	107		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 12 \; V, \; SPK_GAIN = 20 \; dB, \; R_{SPK} = 2 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1 \; kHz \end{array}$	0.014%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dB, R _{SPK} = 4 Ω , P _O = 1 W, f = 1kHz	0.011%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 12 \; V, \; SPK_GAIN = 20 \; dB, \; R_{SPK} = 8 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0.014%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 15 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 2 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1kHz \end{array}$	0.015%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 15 \; V, \; SPK_GAIN = 26 \; dB, \; R_{SPK} = 4 \; \Omega, \\ P_{O} = 1 \; W, \; f = 1 \; kHz \end{array}$	0.013%		
THD+N	Total harmonic distortion and	V_{PVDD} = 15 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , P _O = 1 W, f = 1kHz	0.015%		
	noise	V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 2 Ω , P _O = 1 W, f = 1kHz	0.018%		
		V, $R_{SPK} = 4 \Omega$, $P_O = 1 W$, $f = 1 kHz$	0.012%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dB, R _{SPK} = 8 Ω , P _O = 1 W, f = 1kHz	0.020%		
		$\label{eq:VPVDD} \begin{array}{l} V_{PVDD} = 24 \ V, \ SPK_GAIN = 26 \ dB, \ R_{SPK} = 2 \ \Omega, \\ P_{O} = 1 \ W, \ f = 1 kHz \end{array}$	0.028%		
			0.02%		
			0.027%		



7.6 Power Dissipation Characteristics

Free-air room temperature 25°C (unless otherwise noted)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	l _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	21.30	59.70	0.355
			Idle	6	21.33	59.68	0.355
				8	21.30	59.70	0.355
				4	21.33	58.82	0.352
			Mute	6	21.34	58.81	0.352
		384		8	21.36	58.81	0.352
		304		4	2.08	12.41	0.056
			Standby	6	2.11	12.41	0.057
	20			8	2.17	12.41	0.057
				4	2.03	0.730	0.017
			Powerdown	6	2.04	0.740	0.018
7 /				8	2.06	0.740	0.018
7.4			Idle	4	27.48	59.7	0.400
				6	27.49	59.73	0.401
				8	24.46	59.72	0.378
				4	27.50	58.8	0.398
			Mute	6	27.51	58.8	0.398
		769		8	27.52	58.81	0.398
		700		4	2.04	12.41	0.056
			Standby	6	2.08	12.41	0.056
				8	2.11	12.41	0.057
				4	2.06	0.73	0.018
			Powerdown	6	2.07	0.74	0.018
				8	2.08	0.74	0.018

(1) Mute: B0-P0-R3-D0,D4 = 1

- (2) Standby: B0-P0-R2-D4 = 1
 (3) Power down: B0-P0-R2-D0 = 1
- I_{PVDD} refers to all current that flows through the PVDD supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed. (4)
- I_{DVDD} refers to all current that flows through the DVDD (3.3-V) supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed. (5)

Power Dissipation Characteristics (continued)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	I _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	24.33	59.74	0.467
			Idle	6	24.32	59.74	0.467
				8	24.36	59.70	0.467
				4	24.36	58.81	0.464
			Mute	6	24.32	58.82	0.464
		204		8	24.37	58.84	0.465
	20	384	Standby	4	3.58	12.40	0.081
				6	3.57	12.41	0.081
				8	3.58	12.42	0.081
				4	3.52	0.74	0.042
			Powerdown	6	3.52	0.74	0.042
11 1				8	3.54	0.74	0.042
11.1			Idle	4	30.70	59.70	0.538
				6	30.65	59.72	0.537
				8	30.67	59.71	0.537
				4	3.072	58.80	0.528
			Mute	6	30.69	58.81	0.535
		769		8	30.69	58.81	0.535
		700		4	3.54	12.40	0.080
			Standby	6	3.54	12.41	0.080
				8	3.58	12.42	0.081
		Powerd		4	3.53	0.74	0.042
			Powerdown	6	3.53	0.74	0.042
				8	3.55	0.74	0.042



Power Dissipation Characteristics (continued)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	l _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	25.07	59.72	0.498
			Idle	6	25.08	59.73	0.498
				8	25.10	59.71	0.498
				4	25.12	58.84	0.496
			Mute	6	25.08	58.82	0.495
		294		8	25.11	58.82	0.495
		304	Standby	4	3.92	12.40	0.088
				6	3.93	12.41	0.088
				8	3.94	12.41	0.088
				4	3.87	0.75	0.049
	20		Powerdown	6	3.85	0.74	0.049
12				8	3.87	0.75	0.049
12				4	31.31	59.72	0.573
			Idle	6	31.29	59.71	0.573
				8	31.31	59.74	0.573
				4	31.31	58.80	0.570
			Mute	6	31.33	58.81	0.570
		768		8	31.32	58.81	0.570
		700		4	3.88	12.40	0.087
			Standby	6	3.90	12.41	0.088
				8	3.91	12.41	0.088
				4	3.89	0.75	0.049
			Powerdown	6	3.91	0.74	0.049
				8	3.88	0.75	0.049

Power Dissipation Characteristics (continued)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	l _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	27.94	59.73	0.616
			Idle	6	27.91	59.75	0.616
				8	27.75	59.69	0.613
				4	27.98	58.84	0.614
			Mute	6	27.94	58.87	0.613
		204		8	27.88	58.85	0.612
	26	384		4	5.09	12.41	0.117
			Standby	6	5.12	12.41	0.118
				8	5.19	12.41	0.119
				4	5.02	0.74	0.078
			Powerdown	6	5.06	0.74	0.078
15				8	5.14	0.74	0.080
15			Idle	4	33.05	59.7	0.693
				6	33.03	59.72	0.693
				8	33.08	59.68	0.693
				4	33.03	58.81	0.690
			Mute	6	33.04	58.81	0.690
		769		8	33.05	58.80	0.690
		700		4	5.07	12.41	0.117
			Standby	6	5.09	12.41	0.117
				8	5.14	12.41	0.118
				4	5.02	0.74	0.078
			Powerdown	6	5.04	0.74	0.078
				8	5.09	0.74	0.079



Power Dissipation Characteristics (continued)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	l _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	32.27	59.77	0.830
			Idle	6	32.19	59.76	0.828
				8	32.08	59.75	0.826
				4	32.27	58.85	0.827
			Mute	6	32.24	58.87	0.826
		204		8	32.22	58.86	0.826
		304		4	6.95	12.40	0.177
	26		Standby	6	6.93	12.42	0.177
				8	7.00	12.41	0.178
				4	6.89	0.74	0.137
			Powerdown	6	6.90	0.74	0.138
10.6				8	6.96	0.73	0.139
19.0			Idle	4	34.99	59.74	0.883
				6	34.95	59.74	0.882
				8	34.97	59.71	0.882
				4	34.96	58.85	0.879
			Mute	6	34.98	58.83	0.880
		769		8	34.96	58.81	0.879
		700		4	6.93	12.40	0.177
			Standby	6	6.93	12.42	0.177
				8	6.98	12.41	0.178
				4	6.84	0.74	0.137
			Powerdown	6	6.89	0.74	0.137
				8	6.90	0.73	0.138



Power Dissipation Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

V _{PVDD} (V)	SPK_GAIN ⁽¹⁾⁽²⁾⁽³⁾ (dBV)	f _{SPK_AMP} (kHz)	STATE OF OPERATION	R _{SPK} (Ω)	l _{PVDD} ⁽⁴⁾ (mA)	I _{DVDD} ⁽⁵⁾ (mA)	P _{DISS} (W)
				4	36.93	59.80	1.084
			Idle	6	36.87	59.81	1.082
				8	36.77	59.76	1.080
				4	36.94	58.91	1.081
			Mute	6	36.89	58.89	1.080
		204		8	36.85	58.90	1.079
		304	Standby	4	8.73	12.40	0.250
				6	8.72	12.40	0.250
				8	8.71	12.40	0.250
				4	8.64	0.74	0.210
			Powerdown	6	8.66	0.74	0.210
24	26			8	8.69	0.73	0.211
24			ldle	4	36.84	59.73	1.081
				6	36.86	59.76	1.082
				8	36.83	59.78	1.081
				4	36.85	58.85	1.079
			Mute	6	36.84	58.84	1.078
		769		8	36.82	58.83	1.078
		700		4	8.66	12.40	0.249
			Standby	6	8.68	12.40	0.249
				8	8.71	12.40	0.250
				4	8.63	0.74	0.210
			Powerdown	6	8.64	0.74	0.210
				8	8.65	0.73	0.210

7.7 MCLK Timing

See Figure 18.

		MIN	NOM	MAX	UNIT
t _{MCLK}	MCLK period	20		1000	ns
t _{MCLKH}	MCLK pulse width, high	9			ns
t _{MCLKL}	MCLK pulse width, low	9			ns

7.8 Serial Audio Port Timing – Slave Mode

See Figure 19.

		MIN	NOM	MAX	UNIT
f _{SCLK}	SCLK frequency	1.024			MHz
t _{SCLK}	SCLK period	40			ns
t _{SCLKL}	SCLK pulse width, low	16			ns
t _{SCLKH}	SCLK pulse width, high	16			ns
t _{SL}	SCLK rising to LRCK/FS edge	8			ns
t _{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t _{SU}	Data setup time, before SCLK rising edge	8			ns
t _{DH}	Data hold time, after SCLK rising edge	8			ns
t _{DFS}	Data delay time from SCLK falling edge			15	ns

7.9 Serial Audio Port Timing – Master Mode

See Figure 20.

		MIN	NOM	MAX	UNIT
t _{SCLK}	SCLK period	40			ns
t _{SCLKL}	SCLK pulse width, low	16			ns
t _{SCLKH}	SCLK pulse width, high	16			ns
t _{LRD}	LRCK/FS delay time from to SCLK falling edge	-10		20	ns
t _{SU}	Data setup time, before SCLK rising edge	8			ns
t _{DH}	Data hold time, after SCLK rising edge	8			ns
t _{DFS}	Data delay time from SCLK falling edge			15	ns

7.10 I²C Bus Timing – Standard

		MIN	MAX	UNIT
f _{SCL}	SCL clock frequency		100	kHz
t _{BUF}	Bus free time between a STOP and START condition	4.7		μs
t _{LOW}	Low period of the SCL clock	4.7		μs
t _{HI}	High period of the SCL clock	4		μs
t _{RS-SU}	Setup time for (repeated) START condition	4.7		μs
t _{S-HD}	Hold time for (repeated) START condition	4		μs
t _{D-SU}	Data setup time	250		ns
t _{D-HD}	Data hold time	0	900	ns
t _{SCL-R}	Rise time of SCL signal	$20 + 0.1C_{B}$	1000	ns
t _{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	20 + 0.1C _B	1000	ns
t _{SCL-F}	Fall time of SCL signal	20 + 0.1C _B	1000	ns
t _{SDA-R}	Rise time of SDA signal	20 + 0.1C _B	1000	ns
t _{SDA-F}	Fall time of SDA signal	20 + 0.1C _B	1000	ns
t _{P-SU}	Setup time for STOP condition	4		μs

7.11 I²C Bus Timing – Fast

See Figure 21.

		MIN	MAX	UNIT
f _{SCL}	SCL clock frequency		400	kHz
t _{BUF}	Bus free time between a STOP and START condition	1.3		μs
t _{LOW}	Low period of the SCL clock	1.3		μs
t _{HI}	High period of the SCL clock	600		ns
t _{RS-SU}	Setup time for (repeated)START condition	600		ns
t _{RS-HD}	Hold time for (repeated)START condition	600		ns
t _{D-SU}	Data setup time	100		ns
t _{D-HD}	Data hold time	0	900	ns
t _{SCL-R}	Rise time of SCL signal	20 + 0.1C _B	300	ns
t _{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	20 + 0.1C _B	300	ns
t _{SCL-F}	Fall time of SCL signal	20 + 0.1C _B	300	ns
t _{SDA-R}	Rise time of SDA signal	20 + 0.1C _B	300	ns
t _{SDA-F}	Fall time of SDA signal	20 + 0.1C _B	300	ns
t _{P-SU}	Setup time for STOP condition	600		ns
t _{SP}	Pulse width of spike suppressed		50	ns

JAJSDH3A-MARCH 2016-REVISED JULY 2017

ISTRUMENTS

EXAS

7.12 SPK_MUTE Timing







Figure 19. Serial Audio Port Timing in Slave Mode







Figure 20. Serial Audio Port Timing in Master Mode











7.13 Typical Characteristics

All performance plots were taken using the TAS5782MEVM Board at room temperature, unless otherwise noted. The term "traditional LC filter" refers to the output filter that is present by default on the TAS5782MEVM Board.

OUTPUT CONFIGURATIONS	PLOT TITLE	FIGURE NUMBER
	Frequency Response	Figure 42
	Output Power vs PVDD	Figure 23
	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 24
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 25
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 26
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 27
	THD+N vs Power, V _{PVDD} = 12 V	Figure 28
	THD+N vs Power, V _{PVDD} = 15 V	Figure 29
	THD+N vs Power, V _{PVDD} = 18 V	Figure 30
	THD+N vs Power, V _{PVDD} = 24 V	Figure 31
	Idle Channel Noise vs PVDD	Figure 32
Bridge Tied Load (BTL)	Efficiency vs Output Power	Figure 33
Configuration Curves	Efficiency vs Output Power	Figure 34
	Efficiency vs Output Power	Figure 35
	Idle Current Draw (Filterless) vs PVDD	Figure 36
	Crosstalk vs. Frequency	Figure 37
	PVDD PSRR vs Frequency	Figure 38
	DVDD PSRR vs Frequency	Figure 39
	AVDD PSRR vs Frequency	Figure 40
	CPVDD PSRR vs Frequency	Figure 41
	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 43
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 44
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 45
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 46
	Output Power vs PVDD	Figure 47
	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 48
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 49
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 50
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 51
	THD+N vs Power, V _{PVDD} = 12 V	Figure 52
	THD+N vs Power, V _{PVDD} = 15 V	Figure 53
Parallel Bridge Tied Load	THD+N vs Power, V _{PVDD} = 18 V	Figure 54
(I DTL) Configuration	THD+N vs Power, V _{PVDD} = 24 V	Figure 55
	Idle Channel Noise vs PVDD	Figure 56
	Efficiency vs Output Power	Figure 57
	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 60
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 61
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 62
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 63

Table 1. Quick Reference Table



7.13.1 Bridge Tied Load (BTL) Configuration Curves

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5782MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 40-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, unless otherwise noted. For both the BTL plots and the PBTL plots, the LC filter used was 4.7 μ H / 0.68 μ F. Return to *Quick Reference Table*.



TEXAS INSTRUMENTS

www.ti.com

TAS5782M

JAJSDH3A - MARCH 2016 - REVISED JULY 2017





JAJSDH3A - MARCH 2016 - REVISED JULY 2017



TEXAS INSTRUMENTS

www.ti.com

TAS5782M







TAS5782M





7.13.2 Parallel Bridge Tied Load (PBTL) Configuration

Return to Quick Reference Table.





TAS5782M





Texas INSTRUMENTS

TAS5782M

JAJSDH3A - MARCH 2016 - REVISED JULY 2017





8 Parametric Measurement Information

PARAMETER	FIGURE
Stereo BTL	図 80
Mono PBTL	図 81

TEXAS INSTRUMENTS

www.ti.com

9 Detailed Description

9.1 Overview

The TAS5782M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed below:

- A stereo audio DAC, boasting a strong Burr-Brown heritage with a highly flexible serial audio port.
- A µCDSP audio processing core, with different RAM and ROM options.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I²C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low-voltage digital and analog circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. The operating range for these supplies is shown in the *Recommended Operating Conditions* table.

Communication with the device is accomplished through the I²C control port. A speaker amplifier fault line is also provided to notify a system controller of the occurrence of an overtemperature , overcurrent, or DC error in the speaker amplifier. Two digital GPIO pins are available for use. In the selectable process flows of the TAS5782M, the GPIO2 pin is used as an SDOUT terminal. The other GPIO is unused.

The μ CDSP audio processing core is pre-programmed with a configurable DSP program. The PPC3 provides a means by which to manipulate the controls associated with that Process Flow.

9.2 Functional Block Diagram





9.3 Feature Description

9.3.1 Power-on-Reset (POR) Function

The TAS5782M device has a power-on reset function. The power-on reset feature resets all of the registers to their default configuration as the device is powering up. When the low-voltage power supply used to power DVDD, AVDD, and CPVDD exceeds the POR threshold, the device sets all of the internal registers to their default values and holds them there until the device receives valid MCLK, SCLK, and LRCK/FS toggling for a period of approximately 4 ms. After the toggling period has passed, the internal reset of the registers is removed and the registers can be programmed via the I²C Control Port.

9.3.2 Device Clocking

The TAS5782M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another.



Figure 64. Audio Flow with Respective Clocks

Figure 64 shows the basic data flow at basic sample rate (f_s). When the data is brought into the serial audio interface, the data is processed, interpolated and modulated to 128 × f_s before arriving at the current segments for the final digital to analog conversion.

Figure 65 shows the clock tree.



Feature Description (continued)



Figure 65. TAS5782M Clock Distribution Tree

The Serial Audio Interface typically has 4 connection pins which are listed as follows:

- MCLK (System Master Clock)
- SCLK (Bit Clock)
- LRCK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)
- The output data, SDOUT, is presented on one of the GPIO pins.
- See the GPIO Port and Hardware Control Pins section)

The device has an internal PLL that is used to take either MCLK or SCLK and create the higher rate clocks required by the DSP and the DAC clock.

In situations where the highest audio performance is required, bringing MCLK to the device along with SCLK and LRCK/FS is recommended. The device should be configured so that the PLL is only providing a clock source to the DSP. All other clocks are then a division of the incoming MCLK. To enable the MCLK as the main source clock, with all others being created as divisions of the incoming MCLK, set the DAC CLK source Mux (SDAC in Figure 65) to use MCLK as a source, rather than the output of the MCLK/PLL Mux.

9.3.3 Serial Audio Port

9.3.3.1 Clock Master Mode from Audio Rate Master Clock

In Master Mode, the device generates bit clock and left-right and frame sync clock and outputs them on the appropriate pins. To configure the device in master mode, first put the device into reset, then use registers SCLKO and LRKO (P0-R9). Then reset the LRCK/FS and SCLK divider counters using bits RSCLK and RLRK (P0-R12). Finally, exit reset.

Figure 66 shows a simplified serial port clock tree for the device in master mode.


Feature Description (continued)



Figure 66. Simplified Clock Tree for MCLK Sourced Master Mode

In master mode, MCLK is an input and SCLK and LRCK/FS are outputs. SCLK and LRCK/FS are integer divisions of MCLK. Master mode with a non-audio rate master clock source requires external GPIO's to use the PLL in standalone mode. The PLL should be configured to ensure that the on-chip processor can be driven at the maximum clock rate. The master mode of operation is described in the *Clock Master from a Non-Audio Rate Master Clock* section.

When used with audio rate master clocks, the register changes that should be done include switching the device into master mode, and setting the divider ratio. An example of the master mode of operations is using 24.576 MHz MCLK as a master clock source and driving the SCLK and LRCK/FS with integer dividers to create 48 kHz sample rate clock output. In master mode, the DAC section of the device is also running from the PLL output. The TAS5782M device is able to meet the specified audio performance while using the internal PLL. However, using the MCLK CMOS oscillator source will have less jitter than the PLL.

To switch the DAC clocks (SDAC in the Figure 65) the following registers should be modified

- DAC and OSR Source Clock Register (P0-R14). Set to 0x30 (MCLK input, and OSR is set to whatever the DAC source is)
- The DAC clock divider should be 16 f_S.
 - 16 × 48 kHz = 768 kHz
 - 24.576 MHz (MCLK in) / 768 kHz = 32
 - Therefore, the divide ratio for register DDAC (P0-R28) should be set to 32. The register mapping gives 0x00 = 1, therefore 32 must be converter to 0x1F (31dec).

9.3.3.2 Clock Master from a Non-Audio Rate Master Clock

The classic example here is running a 96-kHz sampling system. Given the clock tree for the device (shown in Figure 65), a non-audio clock rate cannot be brought into the MCLK to the PLL in master mode. Therefore, the PLL source must be configured to be a GPIO pin, and the output brought back into another GPIO pin.

TEXAS INSTRUMENTS

www.ti.com

Feature Description (continued)



Figure 67. Generating Audio Clocks Using Non-Audio Clock Sources

The clock flow through the system is shown in Figure 67. The newly generated MCLK must be brought out of the device on a GPIO pin, then brought into the MCLK pin for integer division to create SCLK and LRCK/FS outputs.

NOTE

Pull-up resistors should be used on SCLK and LRCK/FS in master mode to ensure the device remains out of sleep mode.

9.3.3.3 Clock Slave Mode with 4-Wire Operation (SCLK, MCLK, LRCK/FS, SDIN)

The TAS5782M device requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the MCLK input and supports up to 50 MHz. The TAS5782M device system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 32 kHz, (44.1 – 48 kHz), (88.2 – 96 kHz) are supported.

NOTE

Values in the parentheses are grouped when detected, for example, 88.2 kHz and 96 kHz are detected as *double rate*, 32 kHz, 44.1 kHz and 48 kHz are detected as *single rate* and so on.

Also note, there is one process flow which has only a (1/2)X SRC.

In the presence of a valid bit MCLK, SCLK and LRCK/FS, the device automatically configures the clock tree and PLL to drive the μ CDSP as required.

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 2 shows examples of system clock frequencies for common audio sampling rates.

Feature Description (continued)

MCLK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are supported by configuring various PLL and clock-divider registers directly. In slave mode, auto clock mode should be disabled using P0-R37. Additionally, the user can be required to ignore clock error detection if external clocks are not available for some time during configuration or if the clocks presented on the pins of the device are invalid. The extended programmability allows the device to operate in an advanced mode in which the device becomes a clock master and drive the host serial port with LRCK/FS and SCLK, from a non-audio related clock (for example, using a setting of 12 MHz to generate 44.1 kHz [LRCK/FS] and 2.8224 MHz [SCLK]).

Table 2 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise. For MCLK timing requirements, refer to the *Serial Audio Port Timing – Master Mode* section.

SAMPLING		SYSTEM CLOCK FREQUENCY (f _{MCLK}) (MHz)													
FREQUENCY	64 f _S	128 f _S	192 f _S	256 f _S	384 f _S	512 f _S									
8 kHz		1.024 ⁽²⁾	1.536 ⁽²⁾	2.048	3.072	4.096									
16 kHz		2.048 ⁽²⁾	3.072 ⁽²⁾	4.096	6.144	8.192									
32 kHz		4.096 ⁽²⁾	6.144 ⁽²⁾	8.192	12.288	16.384									
44.1 kHz	See ⁽¹⁾	5.6488 ⁽²⁾	8.4672 ⁽²⁾	11.2896	16.9344	22.5792									
48 kHz		6.144 ⁽²⁾	9.216 ⁽²⁾	12.288	18.432	24.576									
88.2 kHz		11.2896 ⁽²⁾	16.9344	22.5792	33.8688	45.1584									
96 kHz	-	12.288 ⁽²⁾	18.432	24.576	36.864	49.152									

|--|

(1) This system clock rate is not supported for the given sampling frequency.

(2) This system clock rate is supported by PLL mode.

9.3.3.4 Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)

9.3.3.4.1 Clock Generation using the PLL

The TAS5782M device supports a wide range of options to generate the required clocks as shown in Figure 65.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming SCLK or MCLK, a GPIO can also be used.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on P0-R13, D[6:4]. The TAS5782M device provides several programmable clock dividers to achieve a variety of sampling rates. See Figure 65.

If PLL functionality is not required, set the PLLEN value on P0-R4, D[0] to 0. In this situation, an external master clock is required.

	CLOCK MULTIPLEXER													
REGISTER	FUNCTION	BITS												
SREF	PLL Reference	B0-P0-R13-D[6:4]												
DDSP	Clock divider	B0-P0-R27-D[6:0]												
DSCLK	External SCLK Div	B0-P0-R32-D[6:0]												
DLRK	External LRCK/FS Div	B0-P0-R33-D[7:0]												

Table 3.	PLL	Configuration	Registers
----------	-----	---------------	-----------

TAS5782M JAJSDH3A – MARCH 2016– REVISED JULY 2017



9.3.3.4.2 PLL Calculation

The TAS5782M device has an on-chip PLL with fractional multiplication to generate the clock frequency required by the Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 1 MHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be enabled by writing to P0-R4, D[0]. When the PLL is enabled, the PLL output clock PLLCK is given by Equation 1:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \text{ or } PLLCK = \frac{PLLCKIN \times R \times K}{P}$$

where

• R = 1, 2, 3,4, ... , 15, 16

- $J = 4,5,6, \ldots$ 63, and $D = 0000, 0001, 0002, \ldots$ 9999
- K = [J value].[D value]
- P = 1, 2, 3, ... 15

(1)

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

9.3.3.4.2.1 Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied:

- 1 MHz \leq (PLLCKIN / P) \leq 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 1 ≤ J ≤ 63

When the PLL is enabled and $D \neq 0000$, the following conditions must be satisfied:

- 6.667 MHz \leq PLLCLKIN / P \leq 20 MHz
- 64 MHz \leq (PLLCKIN x K x R / P) \leq 100 MHz
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled,

• $f_S = (PLLCLKIN \times K \times R) / (2048 \times P)$

• The value of N is selected so that f_S × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12 MHz and $f_S = 44.1$ kHz, (N=2048)

Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12 MHz and f_s = 48.0 kHz, (N=2048)

Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 4.

		- J
DIVIDER	FUNCTION	BITS
PLLE	PLL enable	P0-R4, D[0]
PPDV	PLL P	P0-R20, D[3:0]
PJDV	PLL J	P0-R21, D[5:0]
		P0-R22, D[5:0]
PDDV	PLL D	P0-R23, D[7:0]
PRDV	PLL R	P0-R24, D[3:0]

Table 4. PLL Registers



Table 5. FLL Configuration Recommendations
--

EQUATIONS	DESCRIPTION
f _S (kHz)	Sampling frequency
R _{MCLK}	Ratio between sampling frequency and MCLK frequency (MCLK frequency = RMCLK x sampling frequency)
MCLK (MHz)	System master clock frequency at MCLK input (pin 20)
PLL VCO (MHz)	PLL VCO frequency as PLLCK in Figure 65
Р	One of the PLL coefficients in Equation 1
PLL REF (MHz)	Internal reference clock frequency which is produced by MCLK / P
$M = K \times R$	The final PLL multiplication factor computed from K and R as described in Equation 1
K = J.D	One of the PLL coefficients in Equation 1
R	One of the PLL coefficients in Equation 1
PLL f _S	Ratio between f_S and PLL VCO frequency (PLL VCO / f_S)
DSP f _S	Ratio between operating clock rate and f_S (PLL f_S / NMAC)
NMAC	The clock divider value in Table 3
DSP CLK (MHz)	The operating frequency as DSPCK in Figure 65
MOD f _S	Ratio between DAC operating clock frequency and f_S (PLL f_S / NDAC)
MOD f (kHz)	DAC operating frequency as DACCK in
NDAC	DAC clock divider value in Table 3
DOSR	OSR clock divider value in Table 3 for generating OSRCK in Figure 65. DOSR must be chosen so that MOD f_S / DOSR = 16 for correct operation.
NCP	NCP (negative charge pump) clock divider value in Table 3
CP f	Negative charge pump clock frequency ($f_S \times MOD f_S / NCP$)
% Error	 Percentage of error between PLL VCO / PLL f_S and f_S (mismatch error). This value is typically zero but can be non-zero especially when K is not an integer (D is not zero).
	This value can be non-zero only when the TAS5782M device acts as a master.

The previous equations explain how to calculate all necessary coefficients and controls to configure the PLL. Table 6 provides for easy reference to the recommended clock divider settings for the PLL as a Master Clock.

TAS5782M JAJSDH3A – MARCH 2016–REVISED JULY 2017

Ų	Texas Instruments
---	----------------------

www.ti.com

Table 6. Recommended	Clock Divider	Settings fo	or PLL as	Master	Clock
		••••••••••••••••••••••••••••••••••••••		maoto	0.00.

f _s (kHz)	R _{MCLK}	MCLK (MHz)	PLL VCO (MHz)	Р	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f _s	DSP f _s	NMAC	DSP CLK (MHz)	MOD f _s	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
	128	1.024	98.304	1	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	192	1.536	98.304	1	1.536	64	32	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	256	2.048	98.304	1	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	384	3.072	98.304	3	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	512	4.096	98.304	3	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	768	6.144	98.304	3	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1024	8.192	98.304	3	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1152	9.216	98.304	9	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1536	12.288	98.304	9	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	2048	16.384	98.304	9	1.82	54	54	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	3072	24.576	98.304	9	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	128	1.4112	90.3168	1	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	192	2.1168	90.3168	3	0.706	128	32	4	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	256	2.8224	90.3168	1	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	384	4.2336	90.3168	3	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	512	5.6448	90.3168	3	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	768	8.4672	90.3168	3	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1024	11.2896	90.3168	3	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1152	12.7008	90.3168	9	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1536	16.9344	90.3168	9	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	2048	22.5792	90.3168	9	2.509	36	36	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	3072	33.8688	90.3168	9	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	64	1.024	98.304	1	1.024	96	48	2	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	128	2.048	98.304	1	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	192	3.072	98.304	1	3.072	32	32	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	256	4.096	98.304	1	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	384	6.144	98.304	3	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	512	8.192	98.304	3	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
10	768	12.288	98.304	3	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1024	16.384	98.304	3	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1152	18.432	98.304	3	6.144	16	16	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1536	24.576	98.304	9	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	2048	32.768	98.304	9	3.641	27	27	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	3072	49.152	98.304	9	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536

														•	,				
f _s (kHz)	R _{MCLK}	MCLK (MHz)	PLL VCO (MHz)	Р	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f _s	DSP f _s	NMAC	DSP CLK (MHz)	MOD f _s	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
	64	1.4112	90.3168	1	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	128	2.8224	90.3168	1	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	192	4.2336	90.3168	3	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	256	5.6448	90.3168	1	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	384	8.4672	90.3168	3	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	512	11.2896	90.3168	3	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	768	16.9344	90.3168	3	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1024	22.5792	90.3168	3	7.526	12	12	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1152	25.4016	90.3168	9	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1536	33.8688	90.3168	9	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	2048	45.1584	90.3168	9	5.018	18	18	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	32	1.024	98.304	1	1.024	96	48	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	48	1.536	98.304	1	1.536	64	16	4	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	64	2.048	98.304	1	2.048	48	24	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	128	4.096	98.304	1	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	192	6.144	98.304	3	2.048	48	48	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	256	8.192	98.304	2	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	384	12.288	98.304	3	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	512	16.384	98.304	3	5.461	18	18	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	768	24.576	98.304	3	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1024	32.768	98.304	3	10.923	9	9	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1152	36.864	98.304	9	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1536	49.152	98.304	6	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	32	1.4112	90.3168	1	1.411	64	32	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	64	2.8224	90.3168	1	2.822	32	16	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	128	5.6448	90.3168	1	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	192	8.4672	90.3168	3	2.822	32	32	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	256	11.2896	90.3168	2	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	384	16.9344	90.3168	3	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	512	22.5792	90.3168	3	7.526	12	12	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	768	33.8688	90.3168	3	11.29	8	8	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	1024	45.1584	90.3168	3	15.053	6	6	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)

JAJSDH3A - MARCH 2016 - REVISED JULY 2017

f _s (kHz)	R _{MCLK}	MCLK (MHz)	PLL VCO (MHz)	Р	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f _S	DSP f _s	NMAC	DSP CLK (MHz)	MOD f _s	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
	32	1.536	98.304	1	1.536	64	32	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	64	3.072	98.304	1	3.072	32	16	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	128	6.144	98.304	1	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	192	9.216	98.304	3	3.072	32	32	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	256	12.288	98.304	2	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
-	384	18.432	98.304	3	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	512	24.576	98.304	3	8.192	12	12	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	768	36.864	98.304	3	12.288	8	8	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	1024	49.152	98.304	3	16.384	6	6	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	32	3.072	98.304	1	3.072	32	16	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	48	4.608	98.304	3	1.536	64	32	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	64	6.144	98.304	1	6.144	16	8	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
00	128	12.288	98.304	2	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
90	192	18.432	98.304	3	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	256	24.576	98.304	4	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	384	36.864	98.304	6	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	512	49.152	98.304	8	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)



9.3.3.5 Serial Audio Port – Data Formats and Bit Depths

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS (pin 25), SCLK (pin 23), and SDIN (pin 24). SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5782M device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

FORMAT	DATA BITS	MAXIMUM LRCK/FS FREQUENCY (kHz) MCLK RATE (f _S)		SCLK RATE (f _S)
I ² S/LJ/RJ	32, 24, 20, 16	Up to 96	128 to 3072 (≤ 50 MHz)	64, 48, 32
TDM	22 24 20 46	Up to 48	128 to 3072	125, 256
I DIVI	32, 24, 20, 16	96	128 to 512	125, 256

Table 7. TAS5782M Audio Data Formats, Bit Depths and Clock Rates

The TAS5782M device requires the synchronization of LRCK/FS and system clock, but does not require a specific phase relation between LRCK/FS and system clock.

If the relationship between LRCK/FS and system clock changes more than ±5 MCLK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK/FS and system clock is completed.

If the relationship between LRCK/FS and SCLK are invalid more than 4 LRCK/FS periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK/FS and SCLK is completed.

9.3.3.5.1 Data Formats and Master/Slave Modes of Operation

The TAS5782M device supports industry-standard audio data formats, including standard I²S and left-justified. Data formats are selected via Register (P0-R40). All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. The data formats are detailed in Figure 68 through Figure 73.

The TAS5782M device also supports right-justified, and TDM data. I²S, LJ, RJ, and TDM are selected using Register (P0-R40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I²S and 24 bit word length. The I²S slave timing is shown in Figure 20.

shows a detailed timing diagram for the serial audio interface.

In addition to acting as a I²S slave, the TAS5782M device can act as an I²S master, by generating SCLK and LRCK/FS as outputs from the MCLK input. Table 8 lists the registers used to place the device into Master or Slave mode. Please refer to the *Serial Audio Port Timing – Master Mode* section for serial audio Interface timing requirements in Master Mode. For Slave Mode timing, please refer to the *Serial Audio Port Timing – Slave Mode* section.

Table 8.	I ² S Master	Mode	Registers
----------	-------------------------	------	-----------

REGISTER	FUNCTION
P0-R9-B0, B4, and B5	I ² S Master mode select
P0-R32-D[6:0]	SCLK divider and LDCK/ES divider
P0-R33-D[7:0]	SCLK divider and LRCK/FS divider



I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 69. I²S Audio Data Format

www.ti.com





The following data formats are only available in software mode.



In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 71. TDM 1 Audio Data Format

TAS5782M JAJSDH3A - MARCH 2016 - REVISED JULY 2017

www.ti.com

TRUMENTS



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 72. TDM 2 Audio Data Format



In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 73. TDM 3 Audio Data Format



9.3.3.6 Input Signal Sensing (Power-Save Mode)

The TAS5782M device has a zero-detect function. The zero-detect function can be applied to both channels of data as an AND function or an OR function, via controls provided in the control port in P0-R65-D[2:1].Continuous Zero data cycles are counted by LRCK/FS, and the threshold of decision for analog mute can be set by P0-R59, D[6:4] for the data which is clocked in on the left frame of an I²S signal or Slot 1 of a TDM signal and P0-R59, D[2:0] for the data which is clocked in on the right frame of an I²S signal or Slot 2 of a TDM signal as shown in Table 10. Default values are 0 for both channels.

ATMUTECTL	VALUE	FUNCTION
Dit - 0	0	Zero data triggers for the two channels for zero detection are ORed together.
BIL 2	1 (Default)	Zero data triggers for the two channels for zero detection are ANDed together.
Bit : 1	0	Zero detection and analog mute are disabled for the data clocked in on the right frame of an I ² S signal or Slot 2 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
Bit · O	0	Zero detection analog mute are disabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.
Dit : U	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.

Table 9. Zero Detection Mode

Table 10. Zero Data Detection Time

ATMUTETIML OR ATMA	NUMBER OF LRCK/FS CYCLES	TIME at 48 kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
010	10240	213 ms
011	25600	533 ms
100	51200	1.066 secs
1 0 1	102400	2.133 secs
110	256000	5.333 secs
111	512000	10.66 secs

9.3.4 Enable Device

To play audio after the device is powered up or reset the device must be enabled by writing book 0x00, page 0x00, register 0x02 to 0x00.

9.3.4.1 Example

The following is a sample script for enabling the device:

#Enable DUT w 90 00 00 #Go to page 0 w 90 7f 00 #Go to book 0 w 90 02 00 #Enable device

9.3.5 Volume Control

For more information regarding the TAS5782 flexible processing system, see the TAS5782M Process Flows

9.3.5.1 DAC Digital Gain Control

Ramp-up frequency and ramp-down frequency can be controlled by P0-R63, D[7:6] and D[3:2] as shown in Table 11. Also ramp-up step and ramp-down step can be controlled by P0-R63, D[5:4] and D[1:0] as shown in Table 12.

				-	
RAMP UP SPEED	EVERY N f _S	COMMENTS	RAMP DOWN FREQUENCY	EVERY N f _S	COMMENTS
00	1	Default	00	1	Default
01	2		01	2	
10	4		10	4	
11	Direct change		11	Direct change	

Table 11. Ramp Up or Down Frequency

Table 12. Ramp Up or Down Step

RAMP UP STEP	STEP dB	COMMENTS	RAMP DOWN STEP	STEP dB	COMMENTS
00	4.0		00	-4.0	
01	2.0		01	-2.0	
10	1.0		10	-1.0	
11	0.5	Default	11	-0.5	Default

9.3.5.1.1 Emergency Volume Ramp Down

Emergency ramp down of the volume is provided for situations such as I^2S clock error and power supply failure. Ramp-down speed is controlled by P0-R64-D[7:6]. Ramp-down step can be controlled by P0-R64-D[5:4]. Default is ramp-down by every f_S cycle with –4dB step.

9.3.6 Adjustable Amplifier Gain and Switching Frequency Selection

The voltage divider between the GVDD_REG pin and the SPK_GAIN/FREQ pin is used to set the gain and switching frequency of the amplifier. Upon start-up of the device, the voltage presented on the SPK_GAIN/FREQ pin is digitized and then decoded into a 3-bit word which is interpreted inside the TAS5782M device to correspond to a given gain and switching frequency. In order to change the SPK_GAIN or switching frequency of the amplifier, the PVDD must be cycled off and on while the new voltage level is present on the SPK_GAIN/FREQ pin.

Because the amplifier adds gain to both the signal and the noise present in the audio signal, the lowest gain setting that can meet voltage-limited output power targets should be used. Using the lowest gain setting ensures that the power target can be reached while minimizing the idle channel noise of the system. The switching frequency selection affects three important operating characteristics of the device. The three affected characteristics are the power dissipation in the device, the power dissipation in the inductor, and the target output filter for the application.

Higher switching frequencies typically result in slightly higher power dissipation in the TAS5782M device and lower dissipation in the inductor in the system, due to decreased ripple current through the inductor and increased charging and discharging current in device and parasitic capacitances. Switching at the higher of the available switching frequencies will result in lower overall dissipation in the system and lower operating temperature of the inductors. However, the thermally limited power output of the device can be decreased in this situation, because some of the TAS5782M device thermal headroom will be absorbed by the higher switching frequency to reduce the ripple current.

Another advantage of increasing the switching frequency is that the higher frequency carrier signal can be filtered by an L-C filter with a higher corner frequency, leading to physically smaller components. Use the highest switching frequency that continues to meet the thermally limited power targets for the application. If thermal constraints require heat reduction in the TAS5782M device, use a lower switching rate.

The switching frequency of the speaker amplifier is dependent on an internal synchronizing signal, (f_{SYNC}), which is synchronous with the sample rate. The rate of the synchronizing signal is also dependent on the sample rate. Refer to Table 13 below for details regarding how the sample rates correlate to the synchronizing signal.

SAMPLE RATE [kHz]	f _{SYNC} [kHz]
8	
16	
32	06
48	96
96	
192	
11.025	
22.05	88.3
44.1	00.2
88.2	

Table 13. Sample Rates vs Synchronization Signal

Table 14 summarizes the de-code of the voltage presented to the SPK_GAIN/FREQ pin. The voltage presented to the SPK_GAIN/FREQ pin is latched in upon startup of the device. Subsequent changes require power cycling the device. A gain setting of 20 dB is recommended for nominal supply voltages of 13 V and lower, while a gain of 26 dB is recommended for supply voltages up to 26.4 V. Table 14 shows the voltage required at the SPK_GAIN/FREQ pin for various gain and switching scenarios as well some example resistor values for meeting the voltage range requirements.

V _{SPK_GAI}	N/FREQ (V)	RESISTOR EXAMPLES		
MIN	МАХ	R100 (kΩ): RESISTOR TO GROUND R101 (kΩ): RESISTOR TO GVDD_REG	GAIN MODE	AMPLIFIER SWITCHING FREQUENCY MODE
6.61	7	Reserved	Reserved	Reserved
5.44	6.6	R100 = 750 R101 = 150		8 × f _{SYNC}
4.67	5.43	R100 = 390 R101 = 150		6 × f _{SYNC}
3.89	3.89 4.66	R100 = 220 R101 = 150	26 dBV	5 × f _{SYNC}
3.11	3.88	R100 = 150 R101 = 150		4 × f _{SYNC}
2.33	3.1	R100 = 100 R101 = 150		8 × f _{SYNC}
1.56	2.32	R100 = 56 R101 = 150	20 40/	6 × f _{SYNC}
0.78	1.55	R100 = 33 R101 = 150	20 08 0	5 × f _{SYNC}
0	0.77	R100 = 8.2 R101 = 150		4 × f _{SYNC}

Table 14. Amplifier Switching Mode vs. SPK_GAIN/FREQ Voltage

9.3.7 Error Handling and Protection Suite

9.3.7.1 Device Overtemperature Protection

The TAS5782M device continuously monitors die temperature to ensure the temperature does not exceed the OTE_{THRES} level specified in the *Recommended Operating Conditions* table. If an OTE event occurs, the SPK_FAULT line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This is a non-latched error and the device will attempt to self clear after OTE_{CLRTIME} has passed.

TAS5782M JAJSDH3A – MARCH 2016 – REVISED JULY 2017



9.3.7.2 SPK_OUTxx Overcurrent Protection

The TAS5782M device continuously monitors the output current of each amplifier output to ensure the output current does not exceed the OCE_{THRES} level specified in the *Recommended Operating Conditions* table. If an OCE event occurs, the SPK_FAULT line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This is a non-latched error and the device will attempt to self clear after $OCE_{CLRTIME}$ has passed.

9.3.7.3 DC Offset Protection

If the TAS5782M device measures a DC offset in the output voltage, the SPK_FAULT line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This latched error requires the SPK_MUTE line to toggle to reset the error. Alternatively, pulling the MCLK, SCLK, or LRCK low causes a clock error, which also resets the device. Normal operation resumes by re-starting the stopped lock.

9.3.7.4 Internal V_{AVDD} Undervoltage-Error Protection

The TAS5782M device internally monitors the AVDD net to protect against the AVDD supply dropping unexpectedly. To enable this feature, P1-R5-B0 is used.

9.3.7.5 Internal V_{PVDD} Undervoltage-Error Protection

If the voltage presented on the PVDD supply drops below the UVE_{THRES(PVDD)} value listed in the *Recommended Operating Conditions* table, the SPK_OUTxx outputs transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the *Recommended Operating Conditions* table, the device resumes normal operation.

9.3.7.6 Internal V_{PVDD} Overvoltage-Error Protection

If the voltage presented on the PVDD supply exceeds the OVE_{THRES(PVDD)} value listed in the *Recommended Operating Conditions* table, the SPK_OUTxx outputs will transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the *Recommended Operating Conditions* table, the device will resume normal operation.

NOTE

The voltage presented on the PVDD supply only protects up to the level described in the *Recommended Operating Conditions* table for the PVDD voltage. Exceeding the absolute maximum rating may cause damage and possible device failure, because the levels exceed that which can be protected by the OVE protection circuit.

9.3.7.7 External Undervoltage-Error Protection

The SPK_MUTE pin can also be used to monitor a system voltage, such as a LCD TV backlight, a battery pack in portable device, by using a voltage divider created with two resistors (see Figure 74).

- If the SPK_MUTE pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage protection mode, which uses two trigger levels.
- When the SPK_MUTE pin level reaches 2 V, soft mute process begins.
- When the SPK_MUTE pin level reaches 1.2 V, analog output mute engages, regardless of digital audio level, and analog output shutdown begins.

Figure 75 shows a timing diagram for external undervoltage error protection.



NOTE

The SPK_MUTE input pin voltage range is provided in the *Recommended Operating Conditions* table. The ratio of external resistors must produce a voltage within the provided input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the SPK_MUTE pin higher than the level specified in the *Recommended Operating Conditions* table, potentially causing damage to or failure of the device. Therefore, any monitored voltage (including all ripple, power supply variation, resistor divider variation, transient spikes, and others) must be scaled by the resistor divider network to never drive the voltage on the SPK_MUTE pin higher than the maximum level specified in the *Recommended Operating Conditions* table.

When the divider is set correctly, any DC voltage can be monitored. Figure 74 shows a 12-V example of how the SPK_MUTE is used for external undervoltage error protection.



Figure 74. SPK_MUTE Used in External Undervoltage Error Protection





9.3.7.8 Internal Clock Error Notification (CLKE)

When a clock error is detected on the incoming data clock, the TAS5782M device switches to an internal oscillator and continues to the drive the DAC, while attenuating the data from the last known value. Once this process is complete, the DAC outputs will be hard muted to the ground and the class D PWM output will stop switching. The clock error can be monitored at B0-P0-R94 and R95. The clock error status bits are non-latching, except for MCLK halted B0-P0-R95-D[4] and CERF B0-P0-R95-D[0] which are cleared when read.

TAS5782M JAJSDH3A – MARCH 2016 – REVISED JULY 2017

www.ti.com

NSTRUMENTS

FXAS

9.3.8 GPIO Port and Hardware Control Pins



Figure 76. GPIO Port

9.3.9 I²C Communication Port

The TAS5782M device supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. Because the TAS5782M register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes. Changing from book to book is accomplished by first changing to page 0x00 by writing 0x00 to register 0x00 and then writing the book number to register 0x7f of page 0. Changing from page to page is accomplished via register 0x00 on each page. The register value selects the register page, from 0 to 255.

9.3.9.1 Slave Address

Table 15. I²C Slave Address

MSB							LSB
1	0	0	1	0	ADR2	ADR1	R/\overline{W}

The TAS5782M device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 10010 (0x9x). The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four devices can be connected on the same bus at one time, which gives a range of 0x90, 0x92, 0x94 and 0x96, as detailed in Table 16. Each TAS5782M device responds when it receives the slave address.

ADR1	ADR0	I ² C SLAVE ADDRESS [R/W]
0	0	0x90
0	1	0x92
1	0	0x94
1	1	0x96

Table 16. I²C Address Configuration via ADR0 and ADR1 Pins



9.3.9.2 Register Address Auto-Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations. The TAS5782M device supports auto-increment mode automatically. Auto-increment stops at page boundaries.

9.3.9.3 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The TAS5782M device supports only slave receivers and slave transmitters.



Figure 77. Packet Protocol

Table 17.	Write O	peration -	Basic I ² C	Framework
		•		

Transmitter	М	М	М	S	М	S	М	S	S	М
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK	ACK	Sp

Table 18. Read Operation - Basic I²C Framework

Transmitter	М	М	М	S	S	М	S	М	М	М
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK	NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

9.3.9.4 Write Register

A master can write to any TAS5782M device registers using single or multiple accesses. The master sends a TAS5782M device slave address with a write bit, a register address, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 19 shows the write operation.

Table 19. Write Operation

Transmitter	М	М	М	S	I	И	S	М	S	М	S	S	М
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	write data 1	ACK	write data 2	ACK	ACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

9.3.9.5 Read Register

A master can read the TAS5782M device register. The value of the register address is stored in an indirect index register in advance. The master sends a TAS5782M device slave address with a read bit after storing the register address. Then the TAS5782M device transfers the data which the index register points to. When autoincrement is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 20 lists the read operation.

Table 20. Read Operation

								-						
Transmitter	М	М	М	S	М	S	М	М	М	S	S	М	М	М

Table 20. Read Operation (continued)

Data Type St slave addr W ACK inc	reg addr ACK Sr slave addr R	ACK data ACK NACK Sp
-----------------------------------	------------------------------------	----------------------

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

9.3.9.6 DSP Book, Page, and Register Update

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

9.3.9.6.1 Book and Page Change

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

9.3.9.6.2 Swap Flag

The swap flag is used to copy the audio coefficient from the host memory to the DSP memory. The swap flag feature is important to maintain the stability of the BQs. A BQ is a closed-loop system with 5 coefficients. To avoid instability in the BQ in an update transition between two different filters, update all five parameters within one audio sample. The internal swap flag insures all 5 coefficients for each filter are transferred from host memory to DSP memory occurs within an audio sample. The swap flag stays high until the full host buffer is transferred to DSP memory. Updates to the Host buffer should not be made while the swap flag is high.

All writes to book 0x8C from page 0x11 and register 0x58 through page 0x21 and register 0x78 require the swap flag. The swap flag is located in book 0x8C, page 0x23, and register 0x14 and must be set to 0x00 00 00 01 for a swap.

9.3.9.6.3 Example Use

The following is a sample script for configuring a device on I2C slave address 0x90 and using the DSP host memory to change the fine volume to the default value of 0 dB:

w 90 00 00 #Go to page 0 w 90 7f 8c #Change the book to 0x8C w 90 00 1e #Go to page 0x1E w 90 44 00 80 00 00 #Fine volume Left w 90 48 00 80 00 00 #Fine volume Right #Run the swap flag for the DSP to work on the new coefficients w 90 00 00 #Go to page 0 w 90 7f 8c #Change the book to 0x8C w 90 00 23 #Go to page 0x23 w 90 14 00 00 00 01 #Swap flag

9.4 Device Functional Modes

Because the TAS5782M device is a highly configurable device, numerous modes of operation can exist for the device. For the sake of succinct documentation, these modes are divided into two modes:

- Fundamental operating modes
- Secondary usage modes

Fundamental operating modes are the primary modes of operation that affect the major operational characteristics of the device, which are the most basic configurations that are chosen to ensure compatibility with the intended application or the other components that interact with the device in the final system. Some examples of the operating modes are the communication protocol used by the control port, the output configuration of the amplifier, or the Master/Slave clocking configuration.

The fundamental operating modes are described starting in the Serial Audio Port Operating Modes section.



www.ti.com

56



Device Functional Modes (continued)

Secondary usage modes are best described as modes of operation that are used after the fundamental operating modes are chosen to fine tune how the device operates within a given system. These secondary usage modes can include selecting between left justified and right justified Serial Audio Port data formats, or enabling some slight gain/attenuation within the DAC path. Secondary usage modes are accomplished through manipulation of the registers and controls in the I²C control port. Those modes of operation are described in their respective register/bit descriptions and, to avoid redundancy, are not included in this section.

9.4.1 Serial Audio Port Operating Modes

The serial audio port in the TAS5782M device supports industry-standard audio data formats, including I^2S , Time Division Multiplexing (TDM), Left-Justified (LJ), and Right-Justified (RJ) formats. To select the data format that will be used with the device, controls are provided on P0-R40. The timing diagrams for the serial audio port are shown in the *Serial Audio Port Timing – Slave Mode* section, and the data formats are shown in the *Serial Audio Port Timing – Slave Mode* section.

9.4.2 Communication Port Operating Modes

The TAS5782M device is configured via an I^2C communication port. The device does not support a hardware only mode of operation, nor Serial Peripheral Interface (SPI) communication. The I^2C Communication Protocol is detailed in the I^2C Communication Port section. The I^2C timing requirements are described in the I^2C Bus Timing – Standard and I^2C Bus Timing – Fast sections.

9.4.3 Speaker Amplifier Operating Modes

The TAS5782M device can be used in two different amplifier configurations:

- Stereo Mode
- Mono Mode

9.4.3.1 Stereo Mode

The familiar stereo mode of operation uses the TAS5782M device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as SPK_OUTA± and SPK_OUTB±. The routing of the audio data which is presented on the SPK_OUTxx outputs can be changed according to the Audio Process Flow which is used and the configuration of registers P0-R42-D[5:4] and P0-R42-D[1:0]. The familiar stereo mode of operation is shown in .

By default, the TAS5782M device is configured to output the Right frame of a I²S input on the Channel A output and the left frame on the Channel B output.

9.4.3.2 Mono Mode

The mono mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the audio output channel. This is also known as Parallel Bridge Tied Load (PBTL).

On the output side of the TAS5782M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter PBTL. However, the two outputs may be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. This process is called *Post-Filter PBTL*. Both variants of mono operation are shown in Figure 78 and Figure 79.



www.tij.co.jp

Device Functional Modes (continued)



On the input side of the TAS5782M device, the input signal to the mono amplifier can be selected from the any slot in a TDM stream or the left or right frame from an I²S, LJ, or RJ signal. The TAS5782M device can also be configured to amplify some mixture of two signals, as in the case of a subwoofer channel which mixes the left and right channel together and sends the mixture through a low-pass filter to create a mono, low-frequency signal.

The mono mode of operation is shown in the Mono (PBTL) Systems section.

9.4.3.3 Master and Slave Mode Clocking for Digital Serial Audio Port

The digital audio serial port in the TAS5782M device can be configured to receive clocks from another device as a serial audio slave device. The slave mode of operation is described in the *Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)* section. If no system processor is available to provide the audio clocks, the TAS5782M device can be placed into Master Mode. In master mode, the TAS5782M device provides the clocks to the other audio devices in the system. For more details regarding the Master and Slave mode operation within the TAS5782M device, see the *Serial Audio Port Operating Modes* section.



10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5782M device into the larger system.

10.1.1 External Component Selection Criteria

The Supporting Component Requirements table in each application description section lists the details of the supporting required components in each of the System Application Schematics.

Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design, to ease inventory management, and to reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor may be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, several unique resistors that have all the same size and value but different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation can seem excessive, the benefits of having fewer components in the design can far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in it during normal use case.

10.1.2 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list was intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extensions from the TAS5782M device and into to the surrounding copper for increased heat-sinking of the device. While components may be offered in smaller or larger package sizes, it is highly recommended that the package size remain identical to the size used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, which optimizes thermal, electromagnetic, and audio performance of the TAS5782M device in circuit in the final system.

10.1.3 Amplifier Output Filtering

The TAS5782M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the *L*-*C Filter*, due to the presence of an inductive element *L* and a capacitive element *C* to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report *Class-D LC Filter Design* (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.



Application Information (continued)

10.1.4 Programming the TAS5782M

The TAS5782M device includes an I²C compatible control port to configure the internal registers of the TAS5782M device. The control console software provided by TI is required to configure the device. More details regarding programming steps, and a few important notes are available below and also in the design examples that follow.

10.1.4.1 Resetting the TAS5782M Registers and Modules

The TAS5782M device has several methods by which the device can reset the register, interpolation filters, and DAC modules. The registers offer the flexibility to do these in or out of shutdown as well as in or out of standby. However, there can be issues if the reset bits are toggled in certain illegal operation modes.

Any of the following routines can be used with no issue:

- Reset Routine 1
 - Place device in Standby
 - Reset modules
- Reset Routine 2
 - Place device in Standby + Power Down
 - Reset registers
- Reset Routine 3
 - Place device in Power Down
- Reset registers
- Reset Routine 4
 - Place device in Standby
 - Reset registers
- Reset Routine 5
 - Place device in Standby + Power Down
 - Reset modules + Reset registers
- Reset Routine 6
 - Place device in Power Down
 - Reset modules + Reset registers
- Reset Routine 7
 - Place device in Standby
 - Reset modules + Reset registers

Two reset routines are not supported and should be avoided. If used, they can cause the device to become unresponsive. These unsupported routines are shown below.

- Unsupported Reset Routine 1 (do not use)
 - Place device in Standby + Power Down
 - Reset modules
- Unsupported Reset Routine 2 (do not use)
 - Place device in Power Down
 - Reset modules



www.tij.co.jp

10.2 Typical Applications

10.2.1 2.0 (Stereo BTL) System

For the stereo (BTL) PCB layout, see 🛛 85.

A 2.0 system refers to a system in which there are two full range speakers without a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a *stereo pair*, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

図 80 shows the 2.0 (Stereo BTL) system application.



図 80. 2.0 (Stereo BTL) System Application Schematic

10.2.1.1 Design Requirements

- Power supplies:
 - 3.3-V supply
 - 5-V to 24-V supply
- Communication: host processor serving as I²C compliant master
- External memory (such as EEPROM and flash) used for coefficients

The requirements for the supporting components for the TAS5782M device in a Stereo 2.0 (BTL) system is provided in $\frac{1}{5}$ 21.

表 21. Supporting Component Requirements for Stereo 2.0 (BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION			
U100	TAS5782M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier			
R100	See the Adjustable	0402	1%, 0.063 W			
R101	Amplifier Gain and Switching Frequency Selection section	0402	1%, 0.063 W			
L100, L101, L102, L103		See the	Amplifier Output Filtering section			
C100, C121	0.1 µF	0402	Ceramic, 0.1 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}			
C104, C108, C111, C115	0.22 µF	0603	Ceramic, 0.22 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}			
C109, C110, C116, C117	0.68 µF	0805	Ceramic, 0.68 μ F, ±10%, X7R Voltage rating must be > 1.8 × V _{PVDD}			
C103	1 µF	0603 (this body size chosen to aid in trace routing)	Ceramic, 1 μF, ±10%, X7R Voltage rating must be > 16 V			
C105, C118, C119, C120	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R			
C106, C107, C113, C114	2.2 µF	0402	Ceramic, 2.2 μ F, ±10%, X5R At a minimum, voltage rating must be > 10V, however higher voltage caps have been shown to have better stability under DC bias. Refer to the guidance provided in the TAS5782M for suggested values.			
C101, C102, C122, C123	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V _{PVDD}			

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
 - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
 - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is
 necessary, go to the E2E forum to request a layout review.

10.2.1.2.2 Step Two: System Level Tuning

• Use the TAS5782MEVM evaluation module and the PPC3 app to configure the desired device settings.

10.2.1.2.3 Step Three: Software Integration

- Use the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.





www.tij.co.jp

10.2.1.3 Application Curves

表 22 shows the application specific performance plots for Stereo 2.0 (BTL) systems.

PLOT TITLE	FIGURE NUMBER
Output Power vs PVDD	Figure 23
THD+N vs Frequency, V _{PVDD} = 12 V	Figure 24
THD+N vs Frequency, V_{PVDD} = 15 V	Figure 25
THD+N vs Frequency, V _{PVDD} = 18 V	Figure 26
THD+N vs Frequency, V _{PVDD} = 24 V	Figure 27
THD+N vs Power, V_{PVDD} = 12 V	Figure 28
THD+N vs Power, V _{PVDD} = 15 V	Figure 29
THD+N vs Power, V _{PVDD} = 18 V	Figure 30
THD+N vs Power, $V_{PVDD} = 24 V$	Figure 31
Idle Channel Noise vs PVDD	Figure 32
Efficiency vs Output Power	Figure 33
DVDD PSRR vs. Frequency	Figure 39
AVDD PSRR vs. Frequency	Figure 40
C _{PVDD} PSRR vs. Frequency	Figure 41

表 22. Relevant Performance Plots

10.2.2 Mono (PBTL) Systems

For the mono (PBTL) PCB layout, see 🛛 87.

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating the TAS5782M device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter to create a single audio signal which contains the low frequency information of the two channels. Conversely, advanced digital signal processing can create a low-frequency signal for a multichannel system, with audio processing which is specifically targeted on low-frequency effects.

Because low-frequency signals are not perceived as having a direction (at least to the extent of high-frequency signals) it is common to reproduce the low-frequency content of a stereo signal that is sent to two separate channels. This configuration pairs one device in Mono PBTL configuration and another device in Stereo BTL configuration in a single system called a 2.1 system. The Mono PBTL configuration is detailed in the 2.1 (Stereo BTL + External Mono Amplifier) Systems section. shows the Mono (PBTL) system application



www<u>.tij.co.jp</u>



Copyright © 2016, Texas Instruments Incorporated

図 81. Mono (PBTL) System Application Schematic

10.2.2.1 Design Requirements

- Power supplies:
 - 3.3-V supply
 - 5-V to 24-V supply
- Communication: Host processor serving as I²C compliant master
- External memory (EEPROM, flash, and others) used for coefficients.

The requirements for the supporting components for the TAS5782M device in a Mono (PBTL) system is provided in 表 23.

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION		
U200	TAS5782M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with 96kHz processing		
R200	See the Adjustable	0402	1%, 0.063 W		
R201	Amplifier Gain and	0402	1%, 0.063 W		
R202	Selection section	0402	1%, 0.063 W		
L200, L201	See the Amplifier Output Filtering section				
C216, C201	0.1 µF	0402	Ceramic, 0.1 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}		
C208, C209, C214, C215	0.22 μF	0603	Ceramic, 0.22 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}		
C220, C221	0.68 µF	0805	Ceramic, 0.68 μ F, ±10%, X7R Voltage rating must be > 1.8 × V _{PVDD}		

表 23. Supporting Component Requirements for Mono (PBTL) Systems

表 23. Supporting Component Requirements for Mono (PBTL) Systems (continued)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C200	1 µF	0603 (this body size chosen to aid in trace routing)	Ceramic, 1 μF, ±10%, X7R Voltage rating must be > 16 V
C205, C211, C213, C212	1 µF	0402	Ceramic, 1 µF, 6.3 V, ±10%, X5R
C202, C217, C352, C367	1 µF	0805 (this body size chosen to aid in trace routing)	Ceramic, 1 μ F, ±10%, X5R Voltage rating must be > 1.45 × V _{PVDD}
C206, C207	2.2 μF	0402	Ceramic, 2.2 μ F, ±10%, X5R At a minimum, voltage rating must be > 10V, however higher voltage caps have been shown to have better stability under DC bias please follow the guidance provided in the TAS5782M for suggested values.
C203, C218	22 µF	0805	Ceramic, 22 μF, ±20%, X5R Voltage rating must be > 1.45 × V _{PVDD}
C204, C219	390 µF	10 × 10	Aluminum, 390 μ F, ±20%, 0.08- Ω Voltage rating must be > 1.45 × V _{PVDD} Anticipating that this application circuit would be followed for higher power subwoofer applications, these capacitors are added to provide local current sources for low-frequency content. These capacitors can be reduced or even removed based upon final system testing, including critical listening tests when evaluating low-frequency designs.

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Step One: Hardware Integration

- Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
 - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
 - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is
 necessary, go to the E2E forum to request a layout review.

10.2.2.2.2 Step Two: System Level Tuning

• Use the TAS5782MEVM evaluation module and the PPC3 app to configure the desired device settings.

10.2.2.2.3 Step Three: Software Integration

- Use the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

www.tij.co.jp

10.2.2.3 Application Specific Performance Plots for Mono (PBTL) Systems

表 24 shows the application specific performance plots for Mono (PBTL) Systems

表	24.	Relevant	Performance	Plots
---	-----	----------	-------------	-------

PLOT TITLE	FIGURE NUMBER
Output Power vs PVDD	Figure 47
THD+N vs Frequency, V _{PVDD} = 12 V	Figure 48
THD+N vs Frequency, V_{PVDD} = 15 V	Figure 49
THD+N vs Frequency, V_{PVDD} = 18 V	Figure 50
THD+N vs Frequency, V_{PVDD} = 24 V	Figure 51
THD+N vs Power, V_{PVDD} = 12 V	Figure 52
THD+N vs Power, V_{PVDD} = 15 V	Figure 53
THD+N vs Power, V_{PVDD} = 18 V	Figure 54
THD+N vs Power, V_{PVDD} = 24 V	Figure 55
Idle Channel Noise vs PVDD	Figure 56
Efficiency vs Output Power	Figure 57

10.2.3 2.1 (Stereo BTL + External Mono Amplifier) Systems

図 89 shows the PCB Layout for the 2.1 System.

To increase the low-frequency output capabilities of an audio system, a single subwoofer can be added to the system. Because the spatial clues for audio are predominately higher frequency than that reproduced by the subwoofer, often a single subwoofer can be used to reproduce the low frequency content of several other channels in the system. This is frequently referred to as a *dot one* system. A stereo system with a subwoofer is referred to as a 2.1 (two-dot-one), a 3 channel system with subwoofer is referred to as a 3.1 (three-dot-one), a popular surround system with five speakers and one subwoofer is referred to as a 5.1, and so on.

10.2.3.1 Advanced 2.1 System (Two TAS5782M devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5782M devices are used — one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5782M device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which might come from a central systems processor. 🛛 82 shows the 2.1 (Stereo BTL + External Mono Amplifier) system application.



図 82. 2.1 (Stereo BTL + External Mono Amplifier) Application Schematic

10.2.3.2 Design Requirements

• Power supplies:

Texas

www.tij.co.jp

INSTRUMENTS

- 3.3-V supply
- 5-V to 24-V supply
- Communication: Host processor serving as I²C compliant master
- External memory (EEPROM, flash, and others) used for coefficients.

The requirements for the supporting components for the TAS5782M device in a 2.1 (Stereo BTL + External Mono Amplifier) system is provided in $\frac{1}{5}$ 25.

www.tij.co.jp

表 25. Supporting Component Requirements for 2.1 (Stereo BTL + External Mono Amplifier) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION				
U300	TAS5782M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier 96kHz Processing				
R300, R350	See the Adjustable	0402	1%, 0.063 W				
R301, R351	Amplifier Gain and Switching Frequency	0402	1%, 0.063 W				
R352	Selection section	0402	1%, 0.063 W				
L300, L301, L302, L303		See the	Amplifier Output Filtering section				
L350, L351							
C394, C395, C396, C397, C398, C399	0.01 µF	0603	Ceramic, 0.01 µF, 50 V, +/-10%, X7R				
C300, C321, C351, C366	0.1 µF	0402	Ceramic, 0.1 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}				
C304, C308, C311, C315, C358, C359, C364, C365	0.22 µF	0603	Ceramic, 0.22 μF, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}				
C309, C310, C316, C317, C370, C371	0.68 µF	0805	Ceramic, 0.68 μ F, ±10%, X7R Voltage rating must be > 1.8 × V _{PVDD}				
C303, C350, C312, C360	1 µF	0603	Ceramic, 1 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}				
C305, C318, C319, C320, C355, C361, C363, C312, C362	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R				
C352, C367	1 µF	0805	Ceramic, 1 μ F, ±10%, X7R Voltage rating must be > 1.45 × V _{PVDD}				
C306, C307, C313, C314, C356, C357,	2.2 µF	0402	Ceramic, 2.2 μ F, ±10%, X5R Voltage rating must be > 1.45 × V _{PVDD}				
C301, C302, C322, C323, C353, C368	22 µF	0805	Ceramic, 22 μ F, ±20%, X5R Voltage rating must be > 1.45 × V _{PVDD}				
C354, C369	390 µF	10 × 10	Aluminum, 390 $\mu\text{F},$ ±20%, 0.08 Ω Voltage rating must be > 1.45 × V_{PVDD}				



10.2.3.3 Application Specific Performance Plots for 2.1 (Stereo BTL + External Mono Amplifier) Systems

表 26 shows the application specific performance plots for 2.1 (Stereo BTL + External Mono Amplifier) Systems

DEVICE	PLOT TITLE	FIGURE NUMBER
U300	Output Power vs PVDD	Figure 23
	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 24
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 25
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 26
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 27
	THD+N vs Power, V _{PVDD} = 12 V	Figure 28
	THD+N vs Power, V _{PVDD} = 15 V	Figure 29
	THD+N vs Power, V _{PVDD} = 18 V	Figure 30
	THD+N vs Power, V _{PVDD} = 24 V	Figure 31
	Idle Channel Noise vs PVDD	Figure 32
	Efficiency vs Output Power	Figure 33
	PVDD PSRR vs Frequency	Figure 38
	Output Power vs PVDD	Figure 47
U301	THD+N vs Frequency, V _{PVDD} = 12 V	Figure 48
	THD+N vs Frequency, V _{PVDD} = 15 V	Figure 49
	THD+N vs Frequency, V _{PVDD} = 18 V	Figure 50
	THD+N vs Frequency, V _{PVDD} = 24 V	Figure 51
	THD+N vs Power, V _{PVDD} = 12 V	Figure 52
	THD+N vs Power, V _{PVDD} = 15 V	Figure 53
	THD+N vs Power, V _{PVDD} = 18 V	Figure 54
	THD+N vs Power, V _{PVDD} = 24 V	Figure 55
	Idle Channel Noise vs PVDD	Figure 56
	Efficiency vs Output Power	Figure 57
U300 and U301	DVDD PSRR vs. Frequency	Figure 39
	AVDD PSRR vs. Frequency	Figure 40
	C _{PVDD} PSRR vs. Frequency	Figure 41
	Powerdown Current Draw vs. PVDD	Figure 47

表 2	6. R	elevant	Performance	Plots
-----	------	---------	-------------	--------------

11 Power Supply Recommendations

11.1 Power Supplies

The TAS5782M device requires two power supplies for proper operation. A *high-voltage* supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one *low-voltage* power supply which is called DVDD is required to power the various low-power portions of the device. The allowable voltage range for both the PVDD and the DVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required powerup sequence. The power supplies can be powered on in any order. TI recommends waiting 100 ms to 240 ms for the DVDD power supplies to stabilize before starting I²C communication and providing stable I²S clock before enabling the device outputs.



図 83. Power Supply Functional Block Diagram

11.1.1 DVDD Supply

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5782M device includes an integrated lowdropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.





www.tij.co.jp

Power Supplies (continued)

The outputs of the high-performance DACs used in the TAS5782M device are ground centered, requiring both a positive low-voltage supply and a negative low-voltage supply. The positive power supply for the DAC output stage is taken from the AVDD pin, which is connected to the DVDD supply provided by the system. A charge pump is integrated in the TAS5782M device to generate the negative low-voltage supply. The power supply input for the charge pump is the CPVDD pin. The CPVSS pin is provided to allow the connection of a filter capacitor on the negative low-voltage supply. As is the case with the other supplies, the component selection, placement, and routing of the external components for these low voltage supplies are shown in the TAS5782M and should be followed as closely as possible to ensure proper operation of the device.

11.1.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5782MEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5782M deviceApplication and Implementation . Lack of proper decoupling, like that shown in the Application and Implementation , results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD_REG pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.



www.tij.co.jp

12 Layout

12.1 Layout Guidelines

12.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in Layout Example. These examples represent exemplary *baseline* balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Example* section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

12.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, CPVDD, and PVDD. However, the capacitors on the PVDD net for the TAS5782M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5782M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section

12.1.3 Optimizing Thermal Performance

Follow the layout examples shown in the *Layout Example* section of this document to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

12.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5782M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5782M device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5782M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5782M device.


Layout Guidelines (continued)

• Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

12.1.3.2 Stencil Pattern

The recommended drawings for the TAS5782M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperatures or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

12.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a *symbol* or *land pattern*) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5782M device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD of the TAS5782M device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5782M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Layout Example* section, this interface can benefit from improved thermal performance.

注 Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias as as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drull must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Example* section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5782M device to open up the current path to and from the device.

12.1.3.2.1.1 Solder Stencil

During the PCB assembly process, a piece of metal called a *stencil* on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself.

TAS5782M

JAJSDH3A-MARCH 2016-REVISED JULY 2017



www.tij.co.jp

Layout Guidelines (continued)

However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

12.2 Layout Example

12.2.1 2.0 (Stereo BTL) System



図 84. 2.0 (Stereo BTL) 3-D View



Layout Example (continued)



図 85. 2.0 (Stereo BTL) Top Copper View

TAS5782M JAJSDH3A – MARCH 2016 – REVISED JULY 2017



www.tij.co.jp

Layout Example (continued)

12.2.2 Mono (PBTL) System



図 86. Mono (PBTL) 3-D View



Layout Example (continued)



図 87. Mono (PBTL) Top Copper View



Layout Example (continued)

12.2.3 2.1 (Stereo BTL + Mono PBTL) Systems



図 88. 2.1 (Stereo BTL + Mono PBTL) 3-D View



Layout Example (continued)



図 89. 2.1 (Stereo BTL + Mono PBTL) Top Copper View

13 Register Maps

13.1 Registers - Page 0

13.1.1 Register 1 (0x01)

Figure 90. Register 1 (0x01)

7	6	5	4	3	2	1	0
	Reserved		RSTM		Reserved		RSTR
	R/W				R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Register 1 (0x01) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved			Reserved
4	RSTM	R/W	0	Reset Modules – This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode.
				0: Normal
				1: Reset modules
3-1	Reserved			Reserved
0	RSTR	R/W	0	Reset Registers – This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported).
				0: Normal
				1: Reset mode registers

Figure 91. Register 2 (0x02)

7	6	5	4	3	2	1	0
DSPR	Rese	erved	RQST		Reserved		RQPD
R/W	R/W		R/W		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Register 2 (0x02) Field Descriptions

Bit	Field	Туре	Reset	Description
7	DSPR	R/W	1	DSP reset – When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are (ASI,MCLK,PLLCLK) are settled so that DMA channels do not go out of sync.
				0: Normal operation 1: Reset the DSP
6-5	Reserved	R/W		Reserved
4	RQST	R/W	0	Standby Request – When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply.
				0: Normal operation 1: Standby mode
3-1	Reserved	R/W		Reserved
0	RQPD	R/W	0	Powerdown Request – When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode.
				0: Normal operation 1: Powerdown mode



Figure 92. Register 3 (0x03)

7	6	5	4	3	2	1	0
	Reserved		RQML		Reserved		RQMR
RO			R/W		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Register 3 (0x03) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	RO		Reserved
4	RQML	R/W	0	Mute Left Channel – This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise.
				0: Normal volume 1: Mute
3-1	Reserved	R/W		Reserved
0	RQMR	R/W	0	Mute Right Channel – This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise.
				0: Normal volume 1: Mute

Figure 93. Register 4 (0x04)

7	6	5	4	3	2	1	0
	Reserved		PLCK		Reserved		PLLE
	R/W		R		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Register 4 (0x04) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W		Reserved
4	PLCK	R	0	PLL Lock Flag – This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked.
				0: The PLL is locked 1: The PLL is not locked
3-1	Reserved	R/W		Reserved
0	PLLE	R/W	1	PLL Enable – This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the MCLK.
				0: Disable PLL 1: Enable PLL

13.1.2 Register 6 (0x06)

Figure 94. Register 6 (0x06)

7	6	5	4	3	2	1	0
	Rese	erved		DBPG		Reserved	
	R	Ŵ		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit	Field	Туре	Reset	Description
7-4	Reserved		0	Reserved
3	DBPG	R/W	0	Page auto increment disable – Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part.
				0: Enable Page auto increment 1: Disable Page auto increment
2-0	Reserved	R/W	0	Reserved

Table 31. Register 6 (0x06) Field Descriptions

13.1.3 Register 7 (0x07)

Figure 95. Register 7 (0x07)

7	6	5	4	3	2	1	0
	Reserved		DEMP		Reserved		SDSL
	R/W		R/W		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Register 7 (0x07) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	DEMP	R/W	0	De-Emphasis Enable – This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1 kHz sampling rate, but can be changed by reprogramming the appropriate coefficients in RAM.
				0: De-emphasis filter is disabled 1: De-emphasis filter is enabled
3-1	Received	P/M	0	Reserved
5-1	Reserved	1.7.4.4	0	Neselveu
0	SDSL	R/W	1	SDOUT Select – This bit selects what is being output as SDOUT via GPIO pins.
				0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

13.1.4 Register 8 (0x08)

Figure 96. Register 8 (0x08)

7	6	5	4	3	2	1	0
Reserv	ved	G2OE	MUTEOE	G0OE		Reserved	
R/W	1	R/W	R/W	R/W		R/W	

Table 33. Register 8 (0x08) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W		Reserved
5	G2OE	R/W	0	GPIO2 Output Enable – This bit sets the direction of the GPIO2 pin 0: GPIO2 is input 1: GPIO2 is output
4	MUTEOE	R/W	0	MUTE Control Enable – This bit sets an enable of MUTE control from PCM to TPA 0: MUTE control disable 1: MUTE control enable



Bit	Field	Туре	Reset	Description
3	GOOE	R/W	0	 GPIO0 Output Enable – This bit sets the direction of the GPIO0 pin 0: GPIO0 is input 1: GPIO0 is output
2-0	Reserved	R/W	0	Reserved

Table 33. Register 8 (0x08) Field Descriptions (continued)

13.1.5 Register 9 (0x09)

Figure 97. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved		SCLKP	SCLKO		Reserved		LRCLKFSO
R/V	V	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 9 (0x09) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved			Reserved
5	SCLKP	R/W	0	SCLK Polarity – This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the SCLK. Normally they are assumed to be aligned to the falling edge of the SCLK. 0: Normal SCLK mode 1: Inverted SCLK mode
4	SCLKO	R/W	0	SCLK Output Enable – This bit sets the SCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R32 to program the division factor of the MCLK to yield the desired SCLK rate (normally 64 FS) 0: SCLK is input (I2S slave mode) 1: SCLK is output (I2S master mode)
3-1	Reserved			Reserved
0	LRKO	R/W	0	LRCLK Output Enable – This bit sets the LRCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R33 to program the division factor of the SCLK to yield 1 FS for LRCLK. 0: LRCLK is input (I2S slave mode) 1: LRCLK is output (I2S master mode)

13.1.6 Register 12 (0x0C)

Figure 98. Register 12 (0x0C)

7	6	5	4	3	2	1	0
	Reserved						
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35	. Register	12	(0x0C)	Field	Descriptions
----------	------------	----	--------	-------	--------------

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W		Reserved
1	RSCLK	R/W	0	Master Mode SCLK Divider Reset – This bit, when set to 0, will reset the MCLK divider to generate SCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.
				0: Master mode SCLK clock divider is reset 1: Master mode SCLK clock divider is functional

STRUMENTS

EXAS

Table 35. Register 12 (0x0C) Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	RLRK	R/W	1	Master Mode LRCLK Divider Reset – This bit, when set to 0, will reset the SCLK divider to generate LRCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.
				0: Master mode LRCLK clock divider is reset 1: Master mode LRCLK clock divider is functional

13.1.7 Register 13 (0x0D)

Figure 99. Register 13 (0x0D)

7	6	5	4	3	2	1	0
	Reserved		SREF	Reserved		SDSP	
	R/W		R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Register 13 (0x0D) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W		Reserved
4	SREF	R/W	0	DSP clock source – This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode.
				0: The PLL reference clock is MCLK
				1: The PLL reference clock is SCLK
				010: The PLL reference clock is oscillator clock
				011: The PLL reference clock is GPIO (selected using P0-R18)
				Others: Reserved (PLL reference is muted)
3	Reserved	R/W		Reserved
2-0	SDSP	R/W	0	DAC clock source – These bits select the source clock for DSP clock divider.
				000: Master clock (PLL/MCLK and OSC auto-select)
				001: PLL clock
				010: OSC clock
				011: MCLK clock
				100: SCLK clock
				101: GPIO (selected using P0-R16)
				Others: Reserved (muted)



13.1.8 Register 14 (0x0E)

Figure 100. Register 14 (0x0E)

7	6	5	4	3	2	1	0
Reserved		SDAC		Reserved		SOSR	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Register 14 (0x0E) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	SDAC	R/W	0	DAC clock source – These bits select the source clock for DAC clock divider. 000: Master clock (PLL/MCLK and OSC auto-select) 001: PLL clock 010: OSC clock 011: MCLK clock 100: SCLK clock 101: GPIO (selected using P0-R16) Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	SOSR	R/W	0	OSR clock source – These bits select the source clock for OSR clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

13.1.9 Register 15 (0x0F)

Figure 101. Register 15 (0x0F)

7	6	5	4	3	2	1	0
		Reserved			SNCP		
		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Register 15 (0x0F) Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	SNCP	R/W	0	NCP clock source – These bits select the source clock for CP clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

13.1.10 Register 16 (0x10)

Figure 102. Register 16 (0x10)

7	6	5	4	3	2	1	0
Reserved		GDSP		Reserved		GDAC	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Register 16 (0x10) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GDSP	R/W	0	GPIO Source for uCDSP clk – These bits select the GPIO pins as clock input source when GPIO is selected as DSP clock divider source.
				000: N/A 001: N/A 010: N/A 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GDAC	R/W	0	GPIO Source for DAC clk – These bits select the GPIO pins as clock input source when GPIO is selected as DAC clock divider source. 000: N/A 001: N/A 010: N/A 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)

13.1.11 Register 17 (0x11)

Figure 103. Register 17 (0x11)

7	6	5	4	3	2	1	0
Reserved		GNCP		Reserved		GOSR	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Register 17 (0x11) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GNCP	R/W	0	GPIO Source for NCP clk – These bits select the GPIO pins as clock input source when GPIO is selected as CP clock divider source
				000: N/A
				001: N/A 010: Reserved
				011: GPI00
				100: N/A
				101: GPIO2 Others: Beserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GOSR	R/W	0	GPIO Source for OSR clk – These bits select the GPIO pins as clock input source when GPIO is selected as OSR clock divider source.
				000: N/A
				001: N/A
				010: Reserved
				011: GPIO0
				100: N/A
				Others: Reserved (muted)

13.1.12 Register 18 (0x12)

Figure 104. Register 18 (0x12)

7	6	5	4	3	2	1	0
		Reserved		GREF			
		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit	Field	Туре	Reset	Description
7-3	Reserved	R/W	0	Reserved
2-0	GREF	R/W	0	GPIO Source for PLL reference clk – These bits select the GPIO pins as clock input source when GPIO is selected as the PLL reference clock source.
				000: N/A 001: N/A 010: Reserved 011: GPIO0 100: N/A 101: GPIO2 Others: Reserved (muted)

13.1.13 Register 20 (0x14)

TAS5782M JAJSDH3A – MARCH 2016 – REVISED JULY 2017 TEXAS INSTRUMENTS

www.ti.com

Figure 105. Register 20 (0x14)

7	6	5	4	3	2	1	0	
	Rese	erved		PPDV				
	R	/W			R/	W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Register 20 (0x14) Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W	0	Reserved
3-0	PPDV	R/W	0	PLL P – These bits set the PLL divider P factor. These bits are ignored in clock auto set mode. 0000: P=1 0001: P=2 1110: P=15 1111: Prohibited (do not set this value)



13.1.14 Register 21 (0x15)

Figure 106. Register 21 (0x15)

7	6	5	4	3	2	1	0
Rese	erved			PJ	DV		
R/	W			R/	W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. Register 21 (0x15) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved		0	Reserved
5-0	PJDV	R/W	001000	PLL J – These bits set the J part of the overall PLL multiplication factor J.D * R.
				These bits are ignored in clock auto set mode.
				000000: Prohibited (do not set this value)
				000001: J=1
				000010: J=2
				111111: J=63

13.1.15 Register 22 (0x16)

Figure 107. Register 22 (0x16)

7	6	5	4	3	2	1	0
Rese	erved			PD	DV		
R/	W			R	/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. Register 22 (0x16) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W		Reserved
5-0	PDDV	R/W	0	PLL D (MSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.
				0 (in decimal): D=0000 1 (in decimal): D=0001 9999 (in decimal): D=9999 Others: Prohibited (do not set)

13.1.16 Register 23 (0x17)

Figure 108. Register 23 (0x17)

7	6	5	4	3	2	1	0	
PDDV								
			R	////				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. Register 23 (0x17) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	PDDV	R/W	0	PLL D (LSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.
				0 (in decimal): D=0000 1 (in decimal): D=0001
				 9999 (in decimal): D=9999 Others: Prohibited (do not set)

13.1.17 Register 24 (0x18)

Figure 109. Register 24 (0x18)

7	6	5	4	3	2	1	0
	Rese	rved			PR	DV	
	R/\	N			R/	W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. Register 24 (0x18) Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W		Reserved
3-0	PRDV	R/W	0	PLL R – These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0000: R=1 0001: R=2 1111: P=16

13.1.18 Register 27 (0x1B)

Figure 110. Register 27 (0x1B)

7	6	5	4	3	2	1	0
Reserved				DDSP			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. Register 27	(0x1B) Field Descriptions
-----------------------	---------------------------

Bit	Field	Туре	Reset	Description
7	Reserved	R/W		Reserved
6-0	DDSP	R/W	0	DSP Clock Divider – These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 1111111: Divide by 128



13.1.19 Register 28 (0x1C)

Figure 111. Register 28 (0x1C)

7	6	5	4	3	2	1	0
Reserved				DDAC			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. Register 28 (0x1C) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved			Reserved
6-4	DDAC	R/W	0	DAC Clock Divider - These bits set the source clock divider value for the DAC clock.
3-0		R/W	1	These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 1111111: Divide by 128

13.1.20 Register 29 (0x1D)

Figure 112. Register 29 (0x1D)

7	6	5	4	3	2	1	0
Reserved				DNCP			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. Register 29 (0x1D) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved			Reserved
6-2	DNCP	R/W	0	NCP Clock Divider - These bits set the source clock divider value for the CP clock.
1-0		R/W	1	These bits are ignored in clock auto set mode.
_				0000000: Divide by 1
				0000001: Divide by 2
				1111111: Divide by 128

13.1.21 Register 30 (0x1E)

Figure 113. Register 30 (0x1E)

7	6	5	4	3	2	1	0
Reserved				DOSR			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

\mathbf{c}

Bit	Field	Туре	Reset	Description
7	Reserved			Reserved
6-4	DOSR	R/W	0	OSR Clock Divider - These bits set the source clock divider value for the OSR clock.
3-0	-	R/W	1	These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 1111111: Divide by 128

13.1.22 Register 32 (0x20)

Figure 114. Register 32 (0x20)

7	6	5	4	3	2	1	0
Reserved				DSCLK			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. Register 32 (0x20) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W		Reserved
6-0	DSCLK	R/W	0	Master Mode SCLK Divider – These bits set the MCLK divider value to generate I2S master SCLK clock.
				0000000: Divide by 1 0000001: Divide by 2
				 1111111: Divide by 128

13.1.23 Register 33 (0x21)

Figure 115. Register 33 (0x21)

7	6	5	4	3	2	1	0
			DL	RK			
			R/	W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. Register 33 (0x21) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DLRK	R/W	0	Master Mode LRCLK Divider – These bits set the I2S master SCLK clock divider value to generate I2S master LRCLK clock 00000000: Divide by 1 00000001: Divide by 2 11111111: Divide by 256



13.1.24 Register 34 (0x22)

Figure 116. Register 34 (0x22)

7	6	5	4	3	2	1 0	
Reserved			I16E	Reserved	FSSP	FSSI	5
R/W			R/W	R/W	R/W	R/W	1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. Register 34 (0x22) Field Descriptions

Bit	Field	Туре	Reset	Description			
7-5	Reserved	R/W		Reserved			
4	116E	R/W	0	16x Interpolation – This bit enables or disables the 16x interpolation mode			
				0: 8x interpolation			
				1: 16x interpolation			
3	Reserved	R/W		Reserved			
2	FSSP	R/W	1	FS Speed Mode – These bits select the FS operation mode, which must be set			
1-0		R/W 0		according to the current audio sampling rate. These bits are ignored in clock auto s mode.			
				000: Reserved			
				001: Reserved			
				010: Reserved			
				011: 48 kHz			
				100: 88.2-96 kHz			
				101: Reserved			
				110: Reserved			
				111: 32kHz			

13.1.25 Register 37 (0x25)

Figure 117. Register 37 (0x25)

7	6	5	4	3	2	1	0
Reserved	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. Register 37 (0x25) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W		Reserved
6	IDFS	R/W	0	Ignore FS Detection – This bit controls whether to ignore the FS detection. When ignored, FS error will not cause a clock error.
				0: Regard FS detection 1: Ignore FS detection
5	IDBK	R/W	0	Ignore SCLK Detection – This bit controls whether to ignore the SCLK detection against LRCLK. The SCLK must be stable between 32 FS and 256 FS inclusive or an error will be reported. When ignored, a SCLK error will not cause a clock error.
				0: Regard SCLK detection 1: Ignore SCLK detection
4	IDSK	R/W	0	Ignore MCLK Detection – This bit controls whether to ignore the MCLK detection against LRCLK. Only some certain MCLK ratios within some error margin are allowed. When ignored, an MCLK error will not cause a clock error.
				0: Regard MCLK detection 1: Ignore MCLK detection
3	IDCH	R/W	0	Ignore Clock Halt Detection – This bit controls whether to ignore the MCLK halt (static or frequency is lower than acceptable) detection. When ignored an MCLK halt will not cause a clock error.
				0: Regard MCLK halt detection 1: Ignore MCLK halt detection
2	IDCM	R/W	0	Ignore LRCLK/SCLK Missing Detection – This bit controls whether to ignore the LRCLK/SCLK missing detection. The LRCLK/SCLK need to be in low state (not only static) to be deemed missing. When ignored an LRCLK/SCLK missing will not cause the DAC go into powerdown mode.
				0: Regard LRCLK/SCLK missing detection 1: Ignore LRCLK/SCLK missing detection
1	DCAS	R/W	0	Disable Clock Divider Autoset – This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually.
				Additionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually.
				0: Enable clock auto set 1: Disable clock auto set
0	IPLK	R/W	0	Ignore PLL Lock Detection – This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at P0-R4, bit 4 is always correct regardless of this bit.
				0: PLL unlocks raise clock error 1: PLL unlocks are ignored



13.1.26 Register 40 (0x28)

Figure 118. Register 40 (0x28)

7	6	5	4	3	2	1	0	
Rese	rved	AFMT		Reserved		ALEN		
R/	W	R/W		R/	W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. Register 40 (0x28) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	-			
5-4	AFMT	R/W	0	I2S Data Format – These bits control both input and output audio interface formats for DAC operation.
				00: I2S 01: DSD
				10' RT.I
				11: LTJ
3-2	Reserved	R/W		Reserved
1	ALEN	R/W	1	I2S Word Length - These bits control both input and output audio interface sample
0		R/W	0	word lengths for DAC operation.
				00: 16 bits
				01: 20 bits
				10: 24 bits
				11: 32 bits

13.1.27 Register 41 (0x29)

Figure 119. Register 41 (0x29)

7	6	5	4	3	2	1	0
			AC	DFS			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. Register 41 (0x29) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	AOFS	R/W	0	I2S Shift – These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample.
				00000000: offset = 0 SCLK (no offset) 00000001: ofsset = 1 SCLK 00000010: offset = 2 SCLKs
				 11111111: offset = 256 SCLKs

13.1.28 Register 42 (0x2A)

Figure 120. Register 42 (0x2A)

7	6	5	4	3	2	1	0	
Rese	erved	AUPL		Reserved		AUPR		
R/	W	R/W		R/	W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. Register 42 (0x2A) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W		Reserved
5	AUPL	R/W	0	Left DAC Data Path - These bits control the left channel audio data path connection.
4		R/W	1	00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	Reserved	R/W		Reserved
1	AUPR	R/W	0	Right DAC Data Path - These bits control the right channel audio data path
0		R/W	1	connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

13.1.29 Register 43 (0x2B)

Figure 121. Register 43 (0x2B)

7	6	5	4	3	2	1	0
	Reserved				PSEL		
	R/W				R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. Register 43 (0x2B) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W		Reserved
4-1	PSEL	R/W	0	DSP Program Selection – These bits select the DSP program to use for audio
0		R/W	1	processing. 00000: Reserved 00001: Rom Mode 1 00010: Reserved 00011: Reserved



13.1.30 Register 44 (0x2C)

Figure 122. Register 44 (0x2C)

7	6	5	4	3	2	1	0
		Reserved				CMDP	
		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. Register 44 (0x2C) Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	Reserved			Reserved
2-0	CMDP	R/W	0	Clock Missing Detection Period – These bits set how long both SCLK and LRCLK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode.
				000: about 1 second 001: about 2 seconds 010: about 3 seconds 111: about 8 seconds

13.1.31 Register 59 (0x3B)

Figure 123. Register 59 (0x3B)

7	6	5	4	3	2	1	0
Reserved		AMTL		Reserved		AMTR	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. Register 59 (0x3B) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W		Reserved
6-4	AMTL	R/W	0	Auto Mute Time for Left Channel – These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates.
				000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	Reserved	R/W		Reserved
2-0	AMTR	R/W	0	Auto Mute Time for Right Channel – These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms
				010: 106.5 ms
				011: 266.5 ms
				100: 0.535 sec
				101: 1.000 Sec 110: 2.665 sec
				111: 5.33 sec

13.1.32 Register 60 (0x3C)

Figure 124. Register 60 (0x3C)

7	6	5	4	3	2	1	0
		Rese	erved			PC	CTL
		R/	Ŵ			R	/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. Register 60 (0x3C) Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	PCTL	R/W	0	Digital Volume Control – These bits control the behavior of the digital volume.
				00: The volume for Left and right channels are independent 01: Right channel volume follows left channel setting

13.1.33 Register 61 (0x3D)

Figure 125. Register 61 (0x3D)

7	6	5	4	3	2	1	0
			VC	DLL			
			R/	W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. Register 61 (0x3D) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	VOLL	R/W	00110000	Left Digital Volume – These bits control the left channel digital volume. The digital volume is 24 dB to –103 dB in –0.5 dB step.
				00000000: +24.0 dB
				0000001: +23.5 dB
				00101111: +0.5 dB
				00110000: 0.0 dB
				00110001: -0.5 dB
				11111110: –103 dB
				11111111: Mute

13.1.34 Register 62 (0x3E)

Figure 126. Register 62 (0x3E)

7	6	5	4	3	2	1	0
			VC	DLR			
			R/	Ŵ			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset



Bit	Field	Туре	Reset	Description
7-0	VOLR	R/W	0011000 0	Right Digital Volume – These bits control the right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.
				00000000: +24.0 dB
				0000001: +23.5 dB
				00101111: +0.5 dB
				00110000: 0.0 dB
				00110001: -0.5 dB
				11111110: –103 dB
				11111111: Mute

Table 63. Register 62 (0x3E) Field Descriptions

13.1.35 Register 63 (0x3F)

Figure	127.	Register	63	(0x3F)	
. igaio		regiotor	00	(0/0)	

7	6	5	4	3	2	1	0	
VNDF		VNDS		VNUF		VNUS		
R/W		R/W		R/	W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. Register 63 (0x3F) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	VNDF	R/W	00	Digital Volume Normal Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3.
				00: Update every 1 FS period
				01: Update every 2 FS periods
				11: Directly set the volume to zero (Instant mute)
5-4	VNDS	R/W	11	Digital Volume Normal Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down.
				The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3.
				00: Decrement by 4 dB for each update
				01: Decrement by 2 dB for each update
				10: Decrement by 1 dB for each update
3-2	VNUF	R/W	00	Digital Volume Normal Ramp Up Frequency – These bits control the frequency of the digital volume updates when the volume is ramping up.
				The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3.
				00: Update every 1 FS period
				01: Update every 2 FS periods
				10: Update every 4 FS periods
				11: Directly restore the volume (Instant unmute)
1-0	VNUS	R/W	11	Digital Volume Normal Ramp Up Step – These bits control the step of the digital volume updates when the volume is ramping up.
				The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3.
				00: Increment by 4 dB for each update
				01: Increment by 2 dB for each update
				10: Increment by 1 dB for each update
1		1	1	I T. Indienieni by 0.5 up 101 each update

13.1.36 Register 64 (0x40)

Figure 128. Register 64 (0x40)

7	6	5	4	3	2	1	0	
VEDF		VEDS		Reserved				
R	/W	R	/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. Register 64 (0x40) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	VEDF	R/W 0	0	Digital Volume Emergency Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.
				00: Update every 1 FS period01: Update every 2 FS periods10: Update every 4 FS periods11: Directly set the volume to zero (Instant mute)
5-4	VEDS	R/W	1	Digital Volume Emergency Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.
				00: Decrement by 4 dB for each update01: Decrement by 2 dB for each update10: Decrement by 1 dB for each update11: Decrement by 0.5 dB for each update
3-0	Reserved	R/W		Reserved

13.1.37 Register 65 (0x41)

Figure 129. Register 65 (0x41)

7	6	5	4	3	2	1	0
		Reserved			ACTL	AMLE	AMRE
		R/W			R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. Register 65 (0x41) Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	Reserved	R/W		Reserved
2	ACTL	R/W	1	Auto Mute Control**NOBUS** – This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with P0-R59.
				0: Auto mute left channel and right channel independently.
				1: Auto mute left and right channels only when both channels are about to be auto muted.
1	AMLE	R/W	1	Auto Mute Left Channel**NOBUS** – This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the left channel will also never be auto muted.
				0: Disable right channel auto mute
				1: Enable right channel auto mute
0	AMRE	R/W	1	Auto Mute Right Channel**NOBUS** – This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the right channel will also never be auto muted.
				0: Disable left channel auto mute 1: Enable left channel auto mute

13.1.38 Register 67 (0x43)



TAS5782M JAJSDH3A – MARCH 2016 – REVISED JULY 2017

Figure 130. Register 67 (0x43)

7	6	5	4	3	2	1	0
DLI	PA	DR	PA	DLI	PM	DR	RPM
R/	W	R/	W	R/	W	R	/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. Register 67 (0x43) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	DLPA	R/W	0	Left DAC primary AC dither gain – These bits control the AC dither gain for left channel primary DAC modulator.
				00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRPA	R/W	0	Right DAC primary AC dither gain – These bits control the AC dither gain for right channel primary DAC modulator.
				00: AC dither gain = 0.125
				01: AC dither gain = 0.25
3-2	DLPM	R/W	0	Left DAC primary DEM dither gain – These bits control the dither gain for left channel primary Galton DEM.
				00: DEM dither gain = 0.5
				01: DEM dither gain = 1.0
				Others: Reserved (do not set)
1-0	DRPM	R/W	0	Right DAC primary DEM dither gain – These bits control the dither gain for right channel primary Galton DEM.
				00: DEM dither gain = 0.5
				01: DEM dither gain = 1.0
				Others: Reserved (do not set)

13.1.39 Register 68 (0x44)

Figure 131. Register 68 (0x44)

7	6	5	4	3	2	1	0
		Reserved				DLPD	
		R/W				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 68. Register 68 (0x44) Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input.
				0000000000 : No DC dither 0000000001 : 2 ⁻¹¹ × 1/32 FS 0000000010 : 2 ⁻¹⁰ × 1/32 FS

13.1.40 Register 69 (0x45)

Figure 132. Register 69 (0x45)

7	6	5	4	3	2	1	0
			DL	.PD			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset



Bit	Field	Туре	Reset	Description						
7-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input.						
				0000000000 : No DC dither 0000000001 : 2 ⁻¹¹ × 1/32 FS 0000000010 : 2 ⁻¹⁰ × 1/32 FS						

Table 69. Register 69 (0x45) Field Descriptions



13.1.41 Register 70 (0x46)

TAS5782M JAJSDH3A – MARCH 2016– REVISED JULY 2017

Figure 133. Register 70 (0x46)

7	6	5	4	3	2	1	0
			DR	(PD			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. Register 70 (0x46) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input.
				0000000000 : No DC dither 0000000001 : 2 ⁻¹¹ × 1/32 FS 0000000010 : 2 ⁻¹⁰ × 1/32 FS

13.1.42 Register 71 (0x47)

Figure 134. Register 71 (0x47)

7	6	5	4	3	2	1	0
			DF	RPD			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. Register 71 (0x47) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input.
				0000000000 : No DC dither 0000000001 : 2 ⁻¹¹ × 1/32 FS 0000000010 : 2 ⁻¹⁰ × 1/32 FS

13.1.43 Register 72 (0x48)

Figure 135. Register 72 (0x48)

7	6	5	4	3	2	1	0
DL	SA	DR	SA	DLS	SM	RS	SM
R/	W	R/	W	R/	W	R/	W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. Register 72 (0x48) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	DLSA	R/W	01	Left DAC secondary AC dither gain – These bits control the AC dither gain for left channel secondary DAC.
				00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRSA	R/W	01	Right DAC secondary AC dither gain – These bits control the AC dither gain for right channel secondary DAC modulator.
				00: AC dither gain = 0.125
				01: AC dither gain = 0.25
				11: no AC dither
3-2	DLSM	R/W	01	Left DAC secondary DEM dither gain – These bits control the dither gain for left channel secondary Galton DEM.
				00: DEM dither gain = 0.5
				01: DEM dither gain = 1.0
1-0	DRSM	R/W	01	Right DAC secondary DEM dither gain – These bits control the dither gain for right channel secondary Galton DEM.
				00: DEM dither gain = 0.5
				01: DEM dither gain = 1.0
				Others: Reserved (do not set)



13.1.44 Register 73 (0x49)

Figure 136. Register 73 (0x49)

7	6	5	4	3	2	1	0
			DL	SD			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. Register 73 (0x49) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input.
				$\begin{array}{l} 00000000001 : \text{No DC differ} \\ 00000000001 : 2^{-11} \times 1/32 \text{ FS} \\ 00000000010 : 2^{-10} \times 1/32 \text{ FS} \end{array}$

13.1.45 Register 74 (0x4A)

Figure 137. Register 74 (0x4A)

7	6	5	4	3	2	1	0
			DL	.SD			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. Register 74 (0x4A) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : $2^{-11} \times 1/32$ FS
				0000000010 : 2 ⁻¹⁰ × 1/32 FS

13.1.46 Register 75 (0x4B)

Figure 138. Register 75 (0x4B)

7	6	5	4	3	2	1	0
			DR	SD			
			R	ΛN			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. Register 75 (0x4B) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DRSD	R/W	0000000 0	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : $2^{-11} \times 1/32$ FS 00000000010 : $2^{-10} \times 1/32$ FS

13.1.47 Register 76 (0x4C)

Figure 139. Register 76 (0x4C)

7	6	5	4	3	2	1	0				
DRSD											
			R	R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. Register 76 (0x4C) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DRSD	R/W	0000000 0	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : $2^{-11} \times 1/32$ FS 0000000001 : $2^{-10} \times 1/32$ FS



Figure 140. Register 78 (0x4E)

7	6	5	4	3	2	1	0
			OL	OF			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. Register 78 (0x4E) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	OLOF	R/W	0000000 0	Left OFSCAL offset – These bits controls the amount of manual DC offset to be added to the left channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV.
				01111111 : -31.75 mV 01111110 : -31.50 mV
				 00000010 : –0.50 mV
				00000001 : -0.25 mV
				00000000 : 0.0 mV
				11111111 : +0.25 mV
				11111110 : +0.50 mV
				10000000 : +32.0 mV

13.1.49 Register 79 (0x4F)

Figure 141. Register 79 (0x4F)

7	6	5	4	3	2	1	0			
OROF										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. Register 79 (0x4F) Field Descriptions

Bit	Field	Туре	Reset	Description						
7-0	OROF	R/W	0	Right OFSCAL offset – These bits controls the amount of manual DC offset to be added to the right channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV.						
				01111111 : -31.75 mV						
				01111110 : -31.50 mV						
				00000010 : -0.50 mV						
				00000001 : -0.25 mV						
				00000000 : 0.0 mV						
				11111111 : +0.25 mV						
				11111110 : +0.50 mV						
				10000000 : +32.0 mV						

TAS5782M JAJSDH3A – MARCH 2016–REVISED JULY 2017 TEXAS INSTRUMENTS

www.ti.com

13.1.50 Register 83 (0x53)

Figure 142. Register 83 (0x53)

7	6	5	4	3	2	1	0
	Reserved		G0SL				
	R/W				R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. Register 83 (0x53) Register Field Descriptions

Bit	Field	Туре	Reset	Description						
7-5	Reserved	R/W		Reserved						
4-0	G0SL	R/W	0	GPIO0 Output Selection – These bits select the signal to output to GPIO0. To actually output the selected signal, the GPIO0 must be set to output mode at P0-R8.						
				0110: Clock invalid flag (clock error or clock changing or clock missing)						
				U111: Serial audio interface data output (SDOUT)						
				1000: Analog mute flag for left channel (low active)						
				1011: Charge nume clock						
				1100: Reserved						
				1101: Reserved						
				1101: Reserved 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DV						
				1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD ** INTERNAL **						
				1100: Short detection flag for left channel						
				1101: Short detection flag for right channel						
				10000: PLL clock/4						
				10001: Oscillator clock/4						
				10010: Impedance sense flag for left channel						
				10011: Impedance sense flag for right channel						
				10100: Internal UVP flag, becomes low when VDD falls below roughly 2.7V						
				10101: Offset calibration flag, asserted when the system is offset calibrating itself.						
				10110: Clock error flag						
				10111: Clock changing flag						
				11000: Clock missing flag						
				11001: Clock halt detection flag						
				11010: DSP boot done flag						
				11011: Charge pump voltage output valid flag (low active)						
				Others: N/A (zero)						

13.1.51 Register 85 (0x55)

Figure 143. Register 85 (0x55)

7	6	5	4	3	2	1	0
Reserved					G2SL		
R/W					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset


Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4-0	G2SL	R/W	0	GPIO2 Output Selection – These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at P0-R8.
				0000: off (low)
				0001: DSP GPIO2 output
				0010: Register GPIO2 output (P0-R86, bit 5)
				0011: Auto mute flag (asserted when both L and R channels are auto muted)
				0100: Auto mute flag for left channel
				0101: Auto mute flag for right channel 0110: Cleak invelid flag (alack arror or alack changing or alack missing)
				0111: Serial audio interface data output (SDOLIT)
				1000: Apalog mute flag for left channel (low active)
				1001: Analog mute flag for right channel (low active)
				1010: PLL lock flag
				1011: Charge pump clock
				1100: Reserved
				1101: Reserved
				1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD
				1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD ** INTERNAL **
				1100: Short detection flag for left channel
				1101: Short detection flag for right channel
				10000: PLL clock/4 10001: Oscillator clock/4
				10010: Impedance sense flag for left channel
				10011: Impedance sense flag for right channel
				10100: Internal UVP flag, becomes low when VDD fails below roughly 2.7V
				10101. Onset calibration hay, asserted when the system is onset calibrating itself.
				10111: Clock changing flag
				11000: Clock missing flag
				11001: Clock halt detection flag
				11010: DSP boot done flag
				11011: Charge pump voltage output valid flag (low active)
				Others: N/A (zero)

13.1.52 Register 86 (0x56)

Figure 144. Register 86 (0x56)

7	6	5	4	3	2	1	0
R/W		R/W	R/W	R/W	R/W	R/\	N

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. Register 86 (0x56) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GOUT2	R/W	0	GPIO Output Control – This bit controls the GPIO2 output when the selection at P0-R85 is set to 0010 (register output)
				0: Output low 1: Output high
4	MUTE	R/W	0	This bit controls the MUTE output when the selection at P0-R84 is set to 0010 (register output).
				0: Output low 1: Output high
3	GOUT0	R/W	0	This bit controls the GPIO0 output when the selection at P0-R83 is set to 0010 (register output)
				0: Output low 1: Output high
2-0	Reserved	R/W	0	Reserved

13.1.53 Register 87 (0x57)

Figure 145. Register 87 (0x57)

7	6	5	4	3	2	1	0
R/W		R/W	R/W	R/W	R/W	R/	W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. Register 87 (0x57) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GINV2	R/W	0	GPIO Output Inversion – This bit controls the polarity of GPIO2 output. When set to 1, the output will be inverted for any signal being selected.
				0: Non-inverted 1: Inverted
4	MUTE	R/W	0	This bit controls the polarity of MUTE output. When set to 1, the output will be inverted for any signal being selected.
				0: Non-inverted 1: Inverted
3	GINV0	R/W	0	This bit controls the polarity of GPIO0 output. When set to 1, the output will be inverted for any signal being selected.
				0: Non-inverted
				1: Inverted
2-0	Reserved	R/W	0	Reserved

13.1.54 Register 88 (0x58)

Figure 146. Register 88 (0x58)

7	6	5	4	3	2	1	0	
DIEI								
			F	२				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset



Table 83. Register 88 (0x58) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DIEI	RO	0x84	Die ID, Device ID = 0x84

13.1.55 Register 91 (0x5B)

Figure 147. Register 91 (0x5B)

7	6	5	4	3	2	1	0
Reserved		DTFS			DT	SR	
R/W		R			F	र	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. Register 91 (0x5B) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	DTFS	R	0	Detected FS – These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range) 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz
3-0	DTSR	R	0	Detected MCLK Ratio – These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz. 0000: Ratio error (The MCLK ratio is not allowed) 0001: MCLK = 32 FS 0010: MCLK = 48 FS 0010: MCLK = 48 FS 0010: MCLK = 64 FS 0100: MCLK = 128 FS 0101: MCLK = 128 FS 0101: MCLK = 192 FS 0111: MCLK = 256 FS 0111: MCLK = 384 FS 1000: MCLK = 512 FS 1001: MCLK = 768 FS 1001: MCLK = 1024 FS 1011: MCLK = 1152 FS 1101: MCLK = 1536 FS 1101: MCLK = 2048 FS 1101: MCLK = 2048 FS

13.1.56 Register 92 (0x5C)

Figure 148. Register 92 (0x5C)

7	6	5	4	3	2	1	0
Reserved							DTBR
			R/W				R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. Register 92 (0x5C) Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	DTBR	R	0	Detected SCLK Ratio (MSB)

13.1.57 Register 93 (0x5D)

Figure 149. Register 93 (0x5D)

7	6	5	4	3	2	1	0
			DT	ſBR			
			R	/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. Register 93 (0x5D) Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DTBR	R/W		Detected SCLK Ratio (LSB) – These bits indicate the currently detected SCLK ratio, i.e. the number of SCLK clocks in one audio frame. Note that for extreme case of SCLK = 1 FS (which is not usable anyway), the detected ratio will be unreliable



13.1.58 Register 94 (0x5E)

Figure 150. Register 94 (0x5E)

7	6	5	4	3	2	1	0
Reserved	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. Register 94 (0x5E) Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved
6	CDST6	R		Clock Detector Status – This bit indicates whether the MCLK clock is present or not. 0: MCLK is present 1: MCLK is missing (halted)
5	CDST5	R		This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is unlocked
4	CDST4	R		This bit indicates whether the both LRCLK and SCLK are missing (tied low) or not. 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
3	CDST3	R		This bit indicates whether the combination of current sampling rate and MCLK ratio is valid for clock auto set. 0: The combination of FS/MCLK ratio is valid 1: Error (clock auto set is not possible)
2	CDST2	R		This bit indicates whether the MCLK is valid or not. The MCLK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCLK is less than or equal to five SCLKs, this flag will be asserted (MCLK invalid reported). 0: MCLK is valid 1: MCLK is invalid
1	CDST1	R		This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-256FS to be valid. 0: SCLK is valid 1: SCLK is invalid
0	CDSTO	R		This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and P0-R37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore). 0: Sampling rate is valid 1: Sampling rate is invalid

13.1.59 Register 95 (0x5F)

Figure 151. Register 95 (0x5F)

7	6	5	4	3	2	1	0
	Reserved		LTSH	Reserved	CKMF	CSRF	CERF
	R/W		R	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. Register 95 (0x5F) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LTSH	R		Latched Clock Halt – This bit indicates whether MCLK halt has occurred. The bit is cleared when read.
				0: MCLK halt has not occurred 1: MCLK halt has occurred since last read
3	Reserved	R/W	0	Reserved
2	CKMF	R		Clock Missing – This bit indicates whether the LRCLK and SCLK are missing (tied low). 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
1	CSRF	R		Clock Resync Request – This bit indicates whether the clock resynchronization is in progress. 0: Not resynchronizing 1: Clock resynchronization is in progress
0	CERF	R		Clock Error – This bit indicates whether a clock error has occurred. The bit is cleared when read 0: Clock error has not occurred 1: Clock error has occurred



13.1.60 Register 108 (0x6C)

Figure 152. Register 108 (0x6C)

7	6	5	4	3	2	1	0
	Reserved						AMRM
		R	R				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. Register 108 (0x6C) Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	AMLM	R		Left Analog Mute Monitor – This bit is a monitor for left channel analog mute status. 0: Mute 1: Unmute
0	AMRM	R		Right Analog Mute Monitor – This bit is a monitor for right channel analog mute status. 0: Mute 1: Unmute

13.1.61 Register 119 (0x77)

Figure 153. Register 119 (0x77)

7	6	5	4	3	2	1	0
Reserved		GPIN2	MUTE	GPIN0	Reserved	Reserved	Reserved
R/W		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. Register 119 (0x77) Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GPIN2	RO		GPIO Input States – This bit indicates the logic level at GPIO2 pin.
				0: Low 1: High
4	MUTE	RO		This bit indicates the logic level at MUTE pin.
				0: Low 1: High
3	GPIN0	RO		This bit indicates the logic level at GPIO0 pin.
				0: Low 1: High
2		RO		N/A
				0: Low
				1: High
1		RO		N/A
				0: Low
				1: High
0		RO		N/A
				0: Low
				1: High

13.1.62 Register 120 (0x78)

JAJSDH3A-MARCH 2016-REVISED JULY 2017

TAS5782M

www.ti.com

RUMENTS

Figure 154. Register 120 (0x78)

7	6	5	4	3	2	1	0
	Reserved		AMFL		Reserved		AMFR
R/W			R		R/W		R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. Register 120 (0x78) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AMFL	R		Auto Mute Flag for Left Channel – This bit indicates the auto mute status for left channel.
				0: Not auto muted
				1: Auto muted
3-1	Reserved	R/W	0	Reserved
0	AMFR	R		Auto Mute Flag for Right Channel – This bit indicates the auto mute status for right channel.
				0: Not auto muted

13.2 Registers - Page 1

13.2.1 Register 1 (0x01)

Figure 155. Register 1 (0x01)

7	6	5	4	3	2	1	0	
Reserved								
R/W								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. Register 1 (0x01) Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	OSEL	R/W	0	Output Amplitude Type - This bit selects the output amplitude type. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled via P0-R37 and the clock dividers must be set manually. 0: VREF mode (Constant output amplitude against AVDD variation) 1: VCOM mode (Output amplitude is proportional to AVDD variation)

13.2.2 Register 2 (0x02)

Figure 156. Register 2 (0x02)

7	6	5	4	3	2	1	0
	Reserved		LAGN		RAGN		
	R/W				R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. Register 2 (0x02) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LAGN	R/W	0	Analog Gain Control for Left Channel - This bit controls the left channel analog gain. 0: 0 dB 1: -6 dB
3-1	Reserved	R/W	0	Reserved

Table 93. Register 2 (0x02) Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	RAGN	R/W	0	Analog Gain Control for Right Channel - This bit controls the right channel analog gain. 0: 0 dB 1: -6 dB

13.2.3 Register 6 (0x06)

Figure 157. Register 6 (0x06)

7	6	5	4	3	2	1	0	
	Reserved							
			R/W				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. Register 6 (0x06) Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	AMCT	R/W	1	Analog Mute Control -This bit enables or disables analog mute following digital mute. 0: Disabled 1: Enabled

13.2.4 Register 7 (0x07)

Figure 158. Register 7 (0x07)

7	6	5	4	3	3 2		0
	Reserved		AGBL		AGBR		
R/W			R/W		R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. Register 7 (0x07) Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AGBL	R/W	0	Analog +10% Gain for Left Channel - This bit enables or disables amplitude boost mode for left channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude
3-1	Reserved	R/W	0	Reserved
0	AGBR	R/W	0	Analog +10% Gain for Right Channel - This bit enables or disables amplitude boost mode for right channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude



www.tij.co.jp

13.2.5 Register 9 (0x09)

Figure 159. Register 9 (0x09)

7	6	5	4	3	2	1	0	
	Reserved							
		R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Register 9 (0x09) Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	DEME	R/W	0	 VCOM Pin as De-emphasis Control - This bit controls whether to use the DEEMP/VCOM pin as De-emphasis control. 0: Disabled (DEEMP/VCOM is not used to control De-emphasis) 1: Enabled (DEEMP/VCOM is used to control De-emphasis)
0	VCPD	R/W	1	Power down control for VCOM - This bit controls VCOM powerdown switch. 0: VCOM is powered on 1: VCOM is powered down



www.tij.co.jp

14 デバイスおよびドキュメントのサポート

14.1 デバイス・サポート

14.1.1 デバイスの項目表記

Glossaryセクションに記載されている用語集は一般的な用語集で、JEDEC、IPC、IEEE、その他の業界標準に準拠する 広範なTIイニシアチブに従って定義された、一般的に使用される頭字語や用語が含まれます。このセクションに示す用語 集では、この製品およびドキュメント、付属品、またはこの製品とともに使用されるサポート・ツールやソフトウェアに固有の単 語、熟語、頭字語が定義されています。定義や用語に関する追加質問については、「e2eオーディオ・アンプ・フォーラム」 を参照してください。

ブリッジ接続負荷(BTL)は、スピーカの一方の端子を1つのハーフブリッジに、もう一方の端子を別のハーフブリッジに接続 する出力構成です。

DUTは、デバイスと別のデバイスとを区別するため、テスト対象のデバイスを指す言葉です。

クローズド・ループ・アーキテクチャは、アンプが出力端子を監視し、出力信号と入力信号とを比較して、出力の非直線性の 補正を試みるトポロジです。

動的制御は、システムまたはエンドユーザーによって、通常の使用中に変更されるものです。

GPIOは、汎用入力/出力ピンです。さまざまな構成が可能な双方向のデジタル・ピンで、システムによって要求される多くの機能を実行できます。

ホスト・プロセッサ(システム・プロセッサ、スカラ、ホスト、システム・コントローラとも呼ばれます)は、中央のシステム・コント ローラとして機能し、接続されているデバイスへ制御情報を提供し、同時に上流のデバイスからオーディオのソース・データ を収集し、他のデバイスへ配信するデバイスを指します。このデバイスは多くの場合、オーディオ・パス内のオーディオ処理 デバイス(TAS5782Mなど)の制御を構成し、周波数応答、時間調整、ターゲットの音圧レベル、システムの安全動作領域、 ユーザーの好みに基づいて、スピーカのオーディオ出力を最適化します。

HybridFlowは、RAMに組み込まれているコンポーネントと、ROMに組み込まれているコンポーネントを使用して、完全に プログラム可能なデバイスよりも使いやすく、しかも複数のアプリケーションで使用できる柔軟性を維持した、構成可能なデ バイスを作り上げます。

最大連続出力電力とは、アンプが25℃の周囲温度で動作しているとき、シャットダウンすることなしに連続的に供給できる 最大出力電力を意味します。テストは、アンプの温度が熱平衡に達し、それ以上上昇しなくなるまでの時間にわたって行わ れます。

並列ブリッジ接続負荷(PBTL)は、スピーカの一方の端子を並列に配置した2つのハーフブリッジに接続し、もう一方の端子を並列に配置した別のハーフブリッジのペアに接続する出力構成です。

rDS(on)は、アンプの出力ステージに使用されているMOSFETのオン抵抗の測定値です。

静的制御/静的構成は、システムが通常状態で使用されている間は変更されない制御です。

ビアは、PCB上の銅メッキされたスルーホールです。

14.1.2 開発サポート

RDGUIソフトウェアについては、お近くの現地サポート・エンジニアへお問い合わせください。

14.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通 知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の 詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。



www.tij.co.jp

14.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ TIのE2E(Engineer-to-Engineer)コミュニティ。エンジニア間の共同作 業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有 し、アイディアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることが できます。技術サポート用の連絡先情報も参照できます。

14.4 商標

Burr Brown, PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

14.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

14.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TAS5782MDCA	Active	Production	HTSSOP (DCA) 48	40 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5782M
TAS5782MDCA.A	Active	Production	HTSSOP (DCA) 48	40 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5782M
TAS5782MDCA.B	Active	Production	HTSSOP (DCA) 48	40 TUBE	-	Call TI	Call TI	-25 to 85	
TAS5782MDCAR	Active	Production	HTSSOP (DCA) 48	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5782M
TAS5782MDCAR.A	Active	Production	HTSSOP (DCA) 48	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	BURR-BROWN TAS5782M
TAS5782MDCAR.B	Active	Production	HTSSOP (DCA) 48	2000 LARGE T&R	-	Call TI	Call TI	-25 to 85	

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative



PACKAGE OPTION ADDENDUM

18-Jul-2025

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCA 48

12.5 x 6.1, 0.5 mm pitch

GENERIC PACKAGE VIEW

HTSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





DCA (R-PDSO-G48)

PowerPAD[™] PLASTIC SMALL-OUTLINE



- NOTES: Α. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - Β. This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15. C.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com. E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

 - F. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



DCA (R-PDSO-G48)

PowerPAD[™] PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD^{\mathbb{N}} package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.



重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みま す)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある 「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証 も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様 のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様の アプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任 を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツル メンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらの リソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権の ライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、 費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは 一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソ ースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありませ ん。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated