



# TAS2110 6.1-W Digital Input Audio Class-D Amplifier With Integrated 11-V Class-H Boost

## 1 Features

- Key Features
  - 11V multi-level Class-H boost
  - Integrated Look Ahead Algorithm with easy to use GUI
- Output Power (1% THD+N, VBAT=3.6V)
  - 6.1-W into 4  $\Omega$
  - 5-W into 8  $\Omega$
- Power Consumption(8 $\Omega$ , VBAT=4.2V)
  - 83.5% efficiency at 1W
  - <1uA in hardware shutdown mode
- Power Supplies
  - VBAT: 2.7 V to 5.5 V
  - VDD: 1.65 V to 1.95 V
- Protections
  - Battery: Advanced Brown Out
  - Clipping: VBAT Tracking Peak Voltage Limiter
  - Device: Thermal and Over Current Protection
- Interfaces and Control
  - I2S/TDM: 8 Channels of 32 bit each up to 96 KSPS
  - I2C: 4 selectable addresses
  - 7.35 KSPS to 192 KSPS Sample Rates
  - MCLK Free operation

## 2 Applications

- [Smart Speakers with Voice Assistance](#)
- [Bluetooth and Wireless Speakers](#)
- [Smart Home](#)
- [IP Camera](#)

## 3 Description

The TAS2110 is a digital input Class-D audio amplifier with an algorithmically controlled, 11V Class-H boost in a QFN package. The look-ahead algorithms optimize boost voltage levels to match the output of the audio signal. This provides all the power needed for peak output while reducing the average power consumption significantly compared to constant output boosts. The algorithms are configured with PurePath Console GUI.

The Class-D audio amplifier is capable of delivering 6.1 W of peak power into a 4  $\Omega$  load at a battery voltage of 3.6 V. TAS2110 is 83.5% efficient at 1 W and consumes less than 1 uA in hardware shutdown mode.

TAS2110 helps protect against system shutdown with configurable brownout protection and VBAT tracking peak voltage limiter, both of which are configurable.

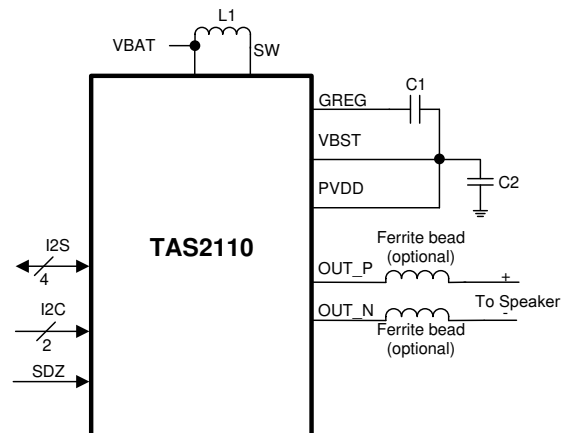
The TAS2110 QFN package is compatible with 2 layer board designs.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|---------|-----------------|
| TAS2110     | QFN     | 4.5 mm x 4 mm   |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



## Table of Contents

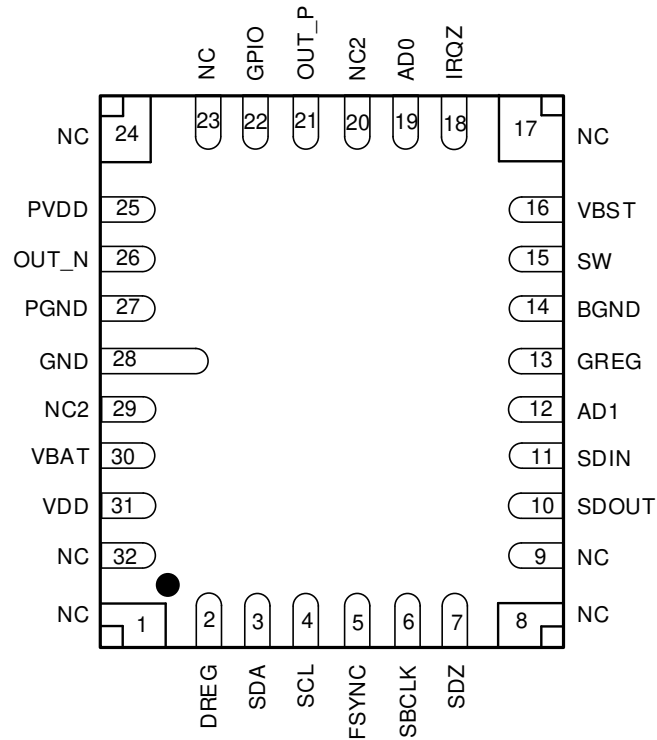
|                                                  |           |                                                                  |           |
|--------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 8.4 Device Functional Modes.....                                 | 26        |
| <b>2 Applications</b> .....                      | <b>1</b>  | 8.5 Register Maps .....                                          | 50        |
| <b>3 Description</b> .....                       | <b>1</b>  | <b>9 Application and Implementation</b> .....                    | <b>89</b> |
| <b>4 Revision History</b> .....                  | <b>2</b>  | 9.1 Application Information.....                                 | 89        |
| <b>5 Pin Configuration and Functions</b> .....   | <b>3</b>  | 9.2 Typical Application .....                                    | 89        |
| <b>6 Specifications</b> .....                    | <b>5</b>  | <b>10 Power Supply Recommendations</b> .....                     | <b>92</b> |
| 6.1 Absolute Maximum Ratings .....               | 5         | 10.1 Power Supplies .....                                        | 92        |
| 6.2 ESD Ratings.....                             | 5         | 10.2 Power Supply Sequencing.....                                | 92        |
| 6.3 Recommended Operating Conditions.....        | 5         | <b>11 Layout</b> .....                                           | <b>93</b> |
| 6.4 Thermal Information .....                    | 5         | 11.1 Layout Guidelines .....                                     | 93        |
| 6.5 Electrical Characteristics.....              | 6         | 11.2 Layout Example .....                                        | 94        |
| 6.6 I <sup>2</sup> C Timing Requirements.....    | 11        | <b>12 Device and Documentation Support</b> .....                 | <b>96</b> |
| 6.7 TDM Port Timing Requirements .....           | 11        | 12.1 Documentation Support .....                                 | 96        |
| 6.8 Typical Characteristics.....                 | 13        | 12.2 Receiving Notification of Documentation Updates             | 96        |
| <b>7 Parameter Measurement Information</b> ..... | <b>18</b> | 12.3 Community Resources.....                                    | 96        |
| <b>8 Detailed Description</b> .....              | <b>19</b> | 12.4 Trademarks .....                                            | 96        |
| 8.1 Overview .....                               | 19        | 12.5 Electrostatic Discharge Caution.....                        | 96        |
| 8.2 Functional Block Diagram .....               | 19        | 12.6 Glossary .....                                              | 96        |
| 8.3 Feature Description.....                     | 19        | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>97</b> |

## 4 Revision History

| DATE          | REVISION | NOTES            |
|---------------|----------|------------------|
| December 2019 | *        | Initial release. |

## 5 Pin Configuration and Functions

**RPP Package  
32-Pin QFN  
Top View**



**Pin Functions**

| PIN   |     | I/O | DESCRIPTION                                                                                                   |
|-------|-----|-----|---------------------------------------------------------------------------------------------------------------|
| NAME  | QFN |     |                                                                                                               |
| AD0   | 19  | I   | I2C address pin LSB.                                                                                          |
| AD1   | 12  | I   | I2C address pin LSB+1.                                                                                        |
| BGND  | 14  | P   | Boost ground. Connect to PCB GND plane.                                                                       |
| DREG  | 2   | P   | Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load.             |
| FSYNC | 5   | IO  | I2S word clock or TDM frame sync.                                                                             |
| GREG  | 13  | P   | High-side gate CP regulator output. Do not connect to external load.                                          |
| GND   | 28  | P   | Digital ground. Connect to PCB GDN plane.                                                                     |
| IRQZ  | 18  | O   | Open drain, active low interrupt pin. Pull up to VDDD with resistor if optional internal pull up is not used. |
| GPIO  | 22  | IO  | General purpose input/output, no connect if not used.                                                         |

**Pin Functions (continued)**

| PIN   |     | I/O | DESCRIPTION                                                                                 |
|-------|-----|-----|---------------------------------------------------------------------------------------------|
| NAME  | QFN |     |                                                                                             |
| NC    | 1   | -   | No Connect. Can float or connect to any support or signal.                                  |
|       | 8   |     |                                                                                             |
|       | 9   |     |                                                                                             |
|       | 17  |     |                                                                                             |
|       | 23  |     |                                                                                             |
|       | 24  |     |                                                                                             |
|       | 32  |     |                                                                                             |
| NC2   | 20  | -   | No Connect. Can float or connect to ground. Do not connect to other signals or supplies.    |
|       | 29  |     |                                                                                             |
| OUT_N | 26  | O   | Class-D negative output for receiver channel.                                               |
| OUT_P | 21  | O   | Class-D positive output for receiver channel.                                               |
| PGND  | 27  | P   | Power stage ground. Connect to PCB GND plane.                                               |
| PVDD  | 25  | P   | Power stage supply.                                                                         |
| SBCLK | 6   | IO  | I2S/TDM serial bit clock.                                                                   |
| SCL   | 4   | I   | I <sup>2</sup> C Clock Pin. Pull up to VDD with a resistor.                                 |
| SDA   | 3   | IO  | I <sup>2</sup> C Data Pin. Pull up to VDD with a resistor.                                  |
| SDIN  | 11  | I   | I2S/TDM serial data input.                                                                  |
| SDOUT | 10  | IO  | I2S/TDM serial data output.                                                                 |
| SDZ   | 7   | I   | Active low hardware shutdown.                                                               |
| SW    | 15  | P   | Boost converter switch input.                                                               |
| VBAT  | 30  | P   | Battery power supply input. Connect to 2.7 V to 5.5 V supply and decouple with a cap.       |
| VBST  | 16  | P   | Boost converter output. Do not connect to external load.                                    |
| VDD   | 31  | P   | Analog, digital, and IO power supply. Connect to 1.8 V supply and decouple to GND with cap. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                                |                                      | MIN      | MAX     | UNIT |
|------------------------------------------------|--------------------------------------|----------|---------|------|
| Analog / IO Supply Voltage                     | VDD                                  | −0.3     | 2       | V    |
| Battery Supply Voltage                         | VBAT                                 | −0.3     | 6       | V    |
| Boost Pin                                      | VBST <sup>(2)(3)</sup>               | −0.3     | 18.5    | V    |
| Power Supply Voltage                           | PVDD <sup>(2)(3)</sup>               | −0.3     | 18.5    | V    |
| Switching Pin                                  | SW                                   | −0.7     | 16      | V    |
| High Side Regulator Pin                        | GREG                                 | PVDD−0.3 | PVDD+6  | V    |
| Digital Regular Pin                            | DREG                                 | −0.3     | 1.65    | V    |
| Input voltage <sup>(4)</sup>                   | Digital IOs referenced to VDD supply | −0.3     | VDD+0.3 | V    |
| Operating free-air temperature, T <sub>A</sub> |                                      | −40      | 85      | °C   |
| Operating junction temperature, T <sub>J</sub> |                                      | −40      | 150     | °C   |
| Storage temperature, T <sub>stg</sub>          |                                      | −65      | 150     | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
- (2) VBST-VBAT and PVDD-VBAT must be less than 16 V
- (3) PVDD can handle 19V transients for less than 10ns
- (4) All digital inputs and IOs are failsafe.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                  |                                      | MIN  | NOM | MAX  | UNIT |
|------------------|--------------------------------------|------|-----|------|------|
| VBAT             | Supply voltage(Internal Boost Mode)  | 2.7  | 3.6 | 5.5  | V    |
| VBAT             | Supply voltage(External Boost Mode)  | 3    | 3.6 | 5.5  | V    |
| VDD              | Supply voltage                       | 1.65 | 1.8 | 1.95 | V    |
| PVDD             | Supply voltage - external boost mode | VBAT |     | 16   | V    |
| V <sub>IH</sub>  | High-level digital input voltage     |      | VDD |      | V    |
| V <sub>IL</sub>  | Low-level digital input voltage      |      | 0   |      | V    |
| R <sub>SPK</sub> | Minimum speaker impedance            | 3.2  |     |      | Ω    |
| L <sub>SPK</sub> | Minimum speaker inductance           | 10   |     |      | μH   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | YFP (WCSP) | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | 36 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 47.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 17.0       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 13.1       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 12.7       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ , (External PVDD = 12 V),  $V_{DD} = 1.8\text{ V}$ ,  $R_L = 8\Omega + 33\text{ }\mu\text{H}$ ,  $f_{in} = 1\text{ kHz}$ , SSM,  $f_s = 48\text{ kHz}$ , Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

| PARAMETER                              |                                                                 | TEST CONDITIONS                                                                  | MIN          | TYP | MAX | UNIT |
|----------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------------------------|--------------|-----|-----|------|
| DIGITAL INPUT and OUTPUT               |                                                                 |                                                                                  |              |     |     |      |
| V <sub>IH</sub>                        | High-level digital input logic voltage threshold                | All digital pins except SDA and SCL                                              | 0.65 × VDD   |     |     | V    |
| V <sub>IL</sub>                        | Low-level digital input logic voltage threshold                 | All digital pins except SDA and SCL                                              | 0.35 × VDD   |     |     | V    |
| V <sub>IH(I2C)</sub>                   | High-level digital input logic voltage threshold                | SDA and SCL                                                                      | 0.7 × VDD    |     |     | V    |
| V <sub>IL(I2C)</sub>                   | Low-level digital input logic voltage threshold                 | SDA and SCL                                                                      | 0.3 × VDD    |     |     | V    |
| V <sub>OH</sub>                        | High-level digital output voltage                               | All digital pins except SDA, SCL and IRQZ; I <sub>OH</sub> = 2 mA.               | VDD – 0.45 V |     |     | V    |
| V <sub>OL</sub>                        | Low-level digital output voltage                                | All digital pins except SDA, SCL and IRQZ; I <sub>OL</sub> = –2 mA.              | 0.45         |     |     | V    |
| V <sub>OL(I2C)</sub>                   | Low-level digital output voltage                                | SDA and SCL; I <sub>OL(I2C)</sub> = –2 mA.                                       | 0.2 × VDD    |     |     | V    |
| V <sub>OL(IRQZ)</sub>                  | Low-level digital output voltage for IRQZ open drain Output     | IRQZ; I <sub>OL(IRQZ)</sub> = –2 mA.                                             | 0.45         |     |     | V    |
| I <sub>IH</sub>                        | Input logic-high leakage for digital inputs                     | All digital pins; Input = VDD.                                                   | –5           | 0.1 | 5   | μA   |
| I <sub>IL</sub>                        | Input logic-low leakage for digital inputs                      | All digital pins; Input = GND.                                                   | –5           | 0.1 | 5   | μA   |
| C <sub>IN</sub>                        | Input capacitance for digital inputs                            | All digital pins                                                                 | 5            |     |     | pF   |
| R <sub>PD</sub>                        | Pull down resistance for digital input/IO pins when asserted on | SDOUT, SDIN, FSYNC, SBCLK                                                        | 50           |     |     | kΩ   |
| AMPLIFIER PERFORMANCE - Internal Boost |                                                                 |                                                                                  |              |     |     |      |
|                                        | Output Voltage for Full-scale digital Input                     | Measured at -6 dB FS input                                                       | 6.32         |     |     | Vrms |
| P <sub>OUT</sub>                       | Maximum Continuous Output Power                                 | R <sub>L</sub> = 32Ω + 33 μH, THD+N = 0.03 %, f <sub>in</sub> = 1 kHz            | 1.25         |     |     | W    |
|                                        |                                                                 | R <sub>L</sub> = 8 Ω + 33 μH, THD+N = 0.03 %, f <sub>in</sub> = 1 kHz            | 5            |     |     | W    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, THD+N = 1 %, f <sub>in</sub> = 1 kHz               | 6.1          |     |     | W    |
|                                        | System efficiency at P <sub>OUT</sub> = 1 W                     | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz                            | 82.5         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz                            | 79.5         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz, VBAT = 4.2 V              | 83           |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz, VBAT = 4.2 V              | 85.2         |     |     | %    |
|                                        | System efficiency at P <sub>OUT</sub> =0.5 W                    | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz                            | 75.8         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz                            | 80.3         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz, VBAT = 4.2 V              | 84.9         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz, VBAT = 4.2 V              | 80.5         |     |     | %    |
|                                        | System efficiency at 0.1% THD+N power level                     | R <sub>L</sub> = 32 Ω + 33 μH, f <sub>in</sub> = 1 kHz,                          | 79.1         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz,                           | 81.2         |     |     | %    |
|                                        |                                                                 | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz                            | 75.7         |     |     | %    |
| THD+N                                  | Total harmonic distortion + noise                               | P <sub>OUT</sub> = 0.25 W, R <sub>L</sub> = 32Ω + 33 μH, f <sub>in</sub> = 1 kHz | 0.01         |     |     | %    |
|                                        |                                                                 | P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz    | 0.01         |     |     | %    |
|                                        |                                                                 | P <sub>OUT</sub> = 1 W, R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz    | 0.01         |     |     | %    |
| V <sub>N</sub>                         | Idle channel noise                                              | A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running                                | 14.8         |     |     | μV   |

## Electrical Characteristics (continued)

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ , (External PVDD = 12 V),  $V_{DD} = 1.8\text{ V}$ ,  $R_L = 8\Omega + 33\text{ }\mu\text{H}$ ,  $f_{in} = 1\text{ kHz}$ , SSM,  $f_s = 48\text{ kHz}$ , Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

| PARAMETER                             |                                                         | TEST CONDITIONS                                                                                                        | MIN | TYP   | MAX | UNIT |
|---------------------------------------|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------|
| F <sub>PWM</sub>                      | Class-D PWM switching frequency                         | Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0                                                               |     | 384   |     | kHz  |
|                                       |                                                         | Fixed Frequency Mode, CLASSD_SYNC=0                                                                                    |     | 384   |     | kHz  |
|                                       |                                                         | Fixed Frequency Mode, CLASSD_SYNC=1, f <sub>s</sub> = 44.1, 88.2, 174.6 kHz                                            |     | 352.8 |     | kHz  |
|                                       |                                                         | Fixed Frequency Mode, CLASSD_SYNC=1, f <sub>s</sub> = 48, 96, 192 kHz                                                  |     | 384   |     | kHz  |
| V <sub>OS</sub>                       | Output offset voltage                                   |                                                                                                                        | -1  |       | 1   | mV   |
| DNR                                   | Dynamic range                                           | A-Weighted, -60 dBFS Method                                                                                            |     | 106.5 |     | dB   |
| SNR                                   | Signal to noise ratio                                   | A-Weighted, Referenced to 1 % THD+N Output Level                                                                       |     | 112.5 |     | dB   |
| K <sub>CP</sub>                       | Click and pop performance                               | Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin. |     | 4     |     | mV   |
|                                       | Programmable output level range                         |                                                                                                                        | 8   |       | 18  | dBV  |
|                                       | Programmable output level step size                     |                                                                                                                        |     | 0.5   |     | dB   |
| AV <sub>ERROR</sub>                   | Amplifier gain error                                    | P <sub>OUT</sub> = 1 W                                                                                                 |     | ±0.1  |     | dB   |
|                                       | Mute attenuation                                        | Device in Shutdown or Muted in Normal Operation                                                                        |     | 110   |     | dB   |
|                                       | VBAT power-supply rejection ratio                       | VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz                                                     |     | 108   |     | dB   |
|                                       |                                                         | VBAT = 3.6 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz                                                     |     | 87.5  |     | dB   |
|                                       | AVDD power-supply rejection ratio                       | VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 217 Hz                                                      |     | 98    |     | dB   |
|                                       |                                                         | VDD = 1.8 V + 200 mV <sub>pp</sub> , f <sub>ripple</sub> = 20 kHz                                                      |     | 89    |     | dB   |
|                                       | Turn on time from release of SW shutdown                | No Volume Ramping                                                                                                      |     | 1.8   |     | ms   |
|                                       |                                                         | Volume Ramping                                                                                                         |     | 4.5   |     | ms   |
|                                       | Turn off time from assertion of SW shutdown to amp Hi-Z | No Volume Ramping                                                                                                      |     | 0.9   |     | ms   |
|                                       |                                                         | Volume Ramping                                                                                                         |     | 12.5  |     | ms   |
| AMPLIFIER PERFORMANCE - External PVDD |                                                         |                                                                                                                        |     |       |     |      |
|                                       | Output Voltage for Full-scale digital Input             | Measured at -6 dB FS input                                                                                             |     | 7.94  |     | Vrms |
| P <sub>OUT</sub>                      | Maximum Continuous Output Power                         | R <sub>L</sub> = 32Ω + 33 μH, THD+N = 1 %, f <sub>in</sub> = 1 kHz                                                     |     | 1.3   |     | W    |
|                                       |                                                         | R <sub>L</sub> = 8 Ω + 33 μH, THD+N = 1 %, f <sub>in</sub> = 1 kHz                                                     |     | 5.2   |     | W    |
|                                       |                                                         | R <sub>L</sub> = 4 Ω + 33 μH, THD+N = 1 %, f <sub>in</sub> = 1 kHz                                                     |     | 10.4  |     | W    |
|                                       |                                                         | R <sub>L</sub> = 32Ω + 33 μH, THD+N = 10 %, f <sub>in</sub> = 1 kHz                                                    |     | 1.6   |     | W    |
|                                       |                                                         | R <sub>L</sub> = 8 Ω + 33 μH, THD+N = 10 %, f <sub>in</sub> = 1 kHz                                                    |     | 6.3   |     | W    |
|                                       |                                                         | R <sub>L</sub> = 4 Ω + 33 μH, THD+N = 10%, f <sub>in</sub> = 1 kHz                                                     |     | 12.6  |     | W    |
|                                       | System efficiency at P <sub>OUT</sub> = 1 W             | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz                                                                  |     | 85.8  |     | %    |
|                                       |                                                         | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz                                                                  |     | 81.8  |     | %    |
|                                       |                                                         | R <sub>L</sub> = 8 Ω + 33 μH, f <sub>in</sub> = 1 kHz, External PVDD = 8.4 V                                           |     | 87.9  |     | %    |
|                                       |                                                         | R <sub>L</sub> = 4 Ω + 33 μH, f <sub>in</sub> = 1 kHz, External PVDD = 8.4 V                                           |     | 83.8  |     | %    |

## Electrical Characteristics (continued)

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ , (External PVDD = 12 V),  $V_{DD} = 1.8\text{ V}$ ,  $R_L = 8\Omega + 33\text{ }\mu\text{H}$ ,  $f_{in} = 1\text{ kHz}$ , SSM,  $f_s = 48\text{ kHz}$ , Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

| PARAMETER       |                                                         | TEST CONDITIONS                                                                                                        | MIN | TYP       | MAX | UNIT          |
|-----------------|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-----------|-----|---------------|
|                 | System efficiency at 0.1% THD+N power level             | $R_L = 32\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$ ,                                                      |     | 89.4      |     | %             |
|                 |                                                         | $R_L = 8\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$ ,                                                       |     | 91.2      |     | %             |
|                 |                                                         | $R_L = 4\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$                                                         |     | 87.2      |     | %             |
|                 |                                                         | $R_L = 32\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$ , External PVDD = 8.4 V                                |     | 83.9      |     | %             |
|                 |                                                         | $R_L = 8\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$ , External PVDD = 8.4 V                                 |     | 91.9      |     | %             |
|                 |                                                         | $R_L = 4\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$ , External PVDD = 8.4 V                                 |     | 88        |     | %             |
| THD+N           | Total harmonic distortion + noise                       | $P_{OUT} = 0.25\ \text{W}$ , $R_L = 32\Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$                             |     | 0.01      |     | %             |
|                 |                                                         | $P_{OUT} = 1\ \text{W}$ , $R_L = 8\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$                               |     | 0.01      |     | %             |
|                 |                                                         | $P_{OUT} = 1\ \text{W}$ , $R_L = 4\ \Omega + 33\ \mu\text{H}$ , $f_{in} = 1\ \text{kHz}$                               |     | 0.02      |     | %             |
| $V_N$           | Idle channel noise                                      | A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running                                                                      |     | 21.3      |     | $\mu\text{V}$ |
| $F_{PWM}$       | Class-D PWM switching frequency                         | Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0                                                               |     | 384       |     | kHz           |
|                 |                                                         | Fixed Frequency Mode, CLASSD_SYNC=0                                                                                    |     | 384       |     | kHz           |
|                 |                                                         | Fixed Frequency Mode, CLASSD_SYNC=1, $f_s = 44.1, 88.2, 174.6\ \text{kHz}$                                             |     | 352.8     |     | kHz           |
|                 |                                                         | Fixed Frequency Mode, CLASSD_SYNC=1, $f_s = 48, 96, 192\ \text{kHz}$                                                   |     | 384       |     | kHz           |
| $V_{OS}$        | Output offset voltage                                   |                                                                                                                        | -1  |           | 1   | mV            |
| DNR             | Dynamic range                                           | A-Weighted, -60 dBFS Method                                                                                            |     | 109       |     | dB            |
| SNR             | Signal to noise ratio                                   | A-Weighted, Referenced to 1 % THD+N Output Level                                                                       |     | 109.5     |     | dB            |
| $K_{CP}$        | Click and pop performance                               | Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin. |     | 3         |     | mV            |
|                 | Programmable output level range                         |                                                                                                                        | 8   |           | 18  | dBV           |
|                 | Programmable output level step size                     |                                                                                                                        |     | 0.5       |     | dB            |
| $AV_{ERROR}$    | Amplifier gain error                                    | $P_{OUT} = 1\ \text{W}$                                                                                                |     | $\pm 0.1$ |     | dB            |
|                 | Mute attenuation                                        | Device in Shutdown or Muted in Normal Operation                                                                        |     | 110       |     | dB            |
|                 | VBAT power-supply rejection ratio                       | $V_{BAT} = 3.6\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 217\ \text{Hz}$                                        |     | 110       |     | dB            |
|                 |                                                         | $V_{BAT} = 3.6\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 20\ \text{kHz}$                                        |     | 90        |     | dB            |
|                 | PVDD power-supply rejection ratio                       | $PVDD = 12\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 217\ \text{Hz}$                                            |     | 105       |     | dB            |
|                 |                                                         | $PVDD = 12\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 20\ \text{kHz}$                                            |     | 90        |     | dB            |
|                 | AVDD power-supply rejection ratio                       | $VDD = 1.8\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 217\ \text{Hz}$                                            |     | 86        |     | dB            |
|                 |                                                         | $VDD = 1.8\ \text{V} + 200\ \text{mV}_{pp}$ , $f_{ripple} = 20\ \text{kHz}$                                            |     | 73        |     | dB            |
|                 | Turn on time from release of SW shutdown                | No Volume Ramping                                                                                                      |     | 1.8       |     | ms            |
|                 |                                                         | Volume Ramping                                                                                                         |     | 4.5       |     | ms            |
|                 | Turn off time from assertion of SW shutdown to amp Hi-Z | No Volume Ramping                                                                                                      |     | 0.75      |     | ms            |
|                 |                                                         | Volume Ramping                                                                                                         |     | 12.5      |     | ms            |
| BOOST CONVERTER |                                                         |                                                                                                                        |     |           |     |               |
|                 | Max Output Voltage                                      | 0.1A DC load, Average voltage (w/o including ripple)                                                                   |     | 11        |     | V             |
|                 | Startup inrush current limit                            | Class-G Mode                                                                                                           |     | 1         |     | A             |
|                 | Startup inrush limit time                               | Class-G Mode                                                                                                           |     | 0.45      |     | ms            |

## Electrical Characteristics (continued)

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ , (External PVDD = 12 V),  $V_{DD} = 1.8\text{ V}$ ,  $R_L = 8\Omega + 33\text{ }\mu\text{H}$ ,  $f_{in} = 1\text{ kHz}$ , SSM,  $f_s = 48\text{ kHz}$ , Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

| PARAMETER                                                                  |                                                          | TEST CONDITIONS                                                               | MIN    | TYP      | MAX    | UNIT               |
|----------------------------------------------------------------------------|----------------------------------------------------------|-------------------------------------------------------------------------------|--------|----------|--------|--------------------|
|                                                                            | Switching Frequency                                      | PFM mode                                                                      |        | 50       |        | kHz                |
|                                                                            |                                                          | Current Control Mode                                                          |        | 4        |        | MHz                |
|                                                                            | Inductor Peak Current Limit                              | default setting                                                               |        | 4        |        | A                  |
| <b>DIE TEMPERATURE SENSOR</b>                                              |                                                          |                                                                               |        |          |        |                    |
|                                                                            | Resolution                                               |                                                                               |        | 8        |        | bits               |
|                                                                            | Die temperature measurement range                        |                                                                               | -40    |          | 150    | $^{\circ}\text{C}$ |
|                                                                            | Die temperature resolution                               |                                                                               |        | 1        |        | $^{\circ}\text{C}$ |
|                                                                            | Die temperature accuracy                                 |                                                                               |        | $\pm 5$  |        | $^{\circ}\text{C}$ |
| <b>VOLTAGE MONITOR</b>                                                     |                                                          |                                                                               |        |          |        |                    |
|                                                                            | Resolution                                               |                                                                               |        | 10       |        | bits               |
|                                                                            | VBAT measurement range                                   |                                                                               | 2      |          | 6      | V                  |
|                                                                            | VBAT resolution                                          |                                                                               |        | 15.6     |        | mV                 |
|                                                                            | VBAT accuracy                                            |                                                                               |        | $\pm 25$ |        | mV                 |
| <b>TDM SERIAL AUDIO PORT</b>                                               |                                                          |                                                                               |        |          |        |                    |
|                                                                            | PCM Sample Rates & FSYNC Input Frequency                 |                                                                               | 7.35   |          | 192    | kHz                |
|                                                                            | SBCLK Input Frequency                                    | I <sup>2</sup> S/TDM Operation                                                | 0.4704 |          | 24.576 | MHz                |
|                                                                            | SBCLK Maximum Input Jitter                               | RMS Jitter below 40 kHz that can be tolerated without performance degradation |        |          | 1      | ns                 |
|                                                                            |                                                          | RMS Jitter above 40 kHz that can be tolerated without performance degradation |        |          | 10     | ns                 |
|                                                                            | SBCLK Cycles per FSYNC in I <sup>2</sup> S and TDM Modes | Values: 64, 96, 128, 192, 256, 384 and 512                                    | 64     |          | 512    | Cycles             |
| <b>PCM PLAYBACK CHARACTERISTICS to <math>f_s \leq 48\text{ kHz}</math></b> |                                                          |                                                                               |        |          |        |                    |
| fs                                                                         | Sample Rates                                             |                                                                               | 7.35   |          | 48     | kHz                |
|                                                                            | Passband LPF Corner                                      |                                                                               |        | 0.454    |        | fs                 |
|                                                                            | Passband Ripple                                          | 20 Hz to LPF cutoff                                                           | -0.3   |          | 0.3    | dB                 |
|                                                                            | Stop Band Attenuation                                    | $\geq 0.55\text{ fs}$                                                         |        | 60       |        | dB                 |
|                                                                            |                                                          | $\geq 1\text{ fs}$                                                            |        | 65       |        | dB                 |
|                                                                            | Group Delay                                              | DC to 0.454 fs                                                                |        |          | 8.6    | 1/fs               |
| <b>PCM PLAYBACK CHARACTERISTICS <math>f_s &gt; 48\text{ kHz}</math></b>    |                                                          |                                                                               |        |          |        |                    |
| fs                                                                         | Sample Rates                                             |                                                                               | 88.2   |          | 192    | kHz                |
|                                                                            | Passband LPF Corner                                      | fs = 96 kHz                                                                   |        | 0.42     |        | fs                 |
|                                                                            |                                                          | fs = 192 kHz                                                                  |        | 0.21     |        | fs                 |
|                                                                            | Passband Ripple                                          | DC to LPF cutoff                                                              | -0.5   |          | 0.5    | dB                 |
|                                                                            | Stop Band Attenuation                                    | $\geq 0.55\text{ fs}$                                                         |        | 60       |        | dB                 |
|                                                                            |                                                          | $\geq 1\text{ fs}$                                                            |        | 65       |        | dB                 |
|                                                                            | Group Delay                                              | DC to 0.375 fs for 96 kHz                                                     |        |          | 8.6    | 1/fs               |
| <b>TYPICAL CURRENT CONSUMPTION</b>                                         |                                                          |                                                                               |        |          |        |                    |
|                                                                            | Current consumption in hardware shutdown                 | SDZ = 0, VBAT                                                                 |        | 0.1      |        | $\mu\text{A}$      |
|                                                                            |                                                          | SDZ = 0, VDD                                                                  |        | 1        |        | $\mu\text{A}$      |
|                                                                            | Current consumption in software shutdown                 | All Clocks Stopped, VBAT                                                      |        | 0.5      |        | $\mu\text{A}$      |
|                                                                            |                                                          | All Clocks Stopped, VDD                                                       |        | 10       |        | $\mu\text{A}$      |

## Electrical Characteristics (continued)

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ , (External PVDD = 12 V),  $V_{DD} = 1.8\text{ V}$ ,  $R_L = 8\Omega + 33\text{ }\mu\text{H}$ ,  $f_{in} = 1\text{ kHz}$ , SSM,  $f_s = 48\text{ kHz}$ , Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

| PARAMETER            |                                             | TEST CONDITIONS                                                         | MIN | TYP  | MAX  | UNIT |
|----------------------|---------------------------------------------|-------------------------------------------------------------------------|-----|------|------|------|
|                      | Current consumption in idle channel         | Clocking 0s PCM mode, VBAT                                              |     | 2.7  |      | mA   |
|                      |                                             | Clocking 0s PCM mode, VDD                                               |     | 7.9  |      | mA   |
|                      | Current consumption during active operation | f <sub>s</sub> = 48 kHz, VBAT                                           |     | 4.6  |      | mA   |
|                      |                                             | f <sub>s</sub> = 48 kHz, VDD                                            |     | 7.9  |      | mA   |
| PROTECTION CIRCUITRY |                                             |                                                                         |     |      |      |      |
|                      | Thermal shutdown temperature                |                                                                         |     | 140  |      | °C   |
|                      | Thermal shutdown retry                      |                                                                         |     | 1.5  |      | s    |
|                      | VBAT undervoltage lockout threshold (UVLO)  | UVLO is asserted                                                        | 2   |      |      | V    |
|                      |                                             | UVLO is released                                                        |     |      | 2.55 | V    |
|                      | Output short circuit limit                  | Output to Output, Output to GND, Output to VBST or Output to VBAT Short |     | 3.75 |      | A    |

## 6.6 I<sup>2</sup>C Timing Requirements

T<sub>A</sub> = 25 °C, VDD = 1.8 V (unless otherwise noted)

|                       |                                                                                              | MIN                       | NOM | MAX  | UNIT |
|-----------------------|----------------------------------------------------------------------------------------------|---------------------------|-----|------|------|
| <b>Standard-Mode</b>  |                                                                                              |                           |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency                                                                          | 0                         |     | 100  | kHz  |
| t <sub>HD;STA</sub>   | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4                         |     |      | μs   |
| t <sub>LOW</sub>      | LOW period of the SCL clock                                                                  | 4.7                       |     |      | μs   |
| t <sub>HIGH</sub>     | HIGH period of the SCL clock                                                                 | 4                         |     |      | μs   |
| t <sub>SU;STA</sub>   | Setup time for a repeated START condition                                                    | 4.7                       |     |      | μs   |
| t <sub>HD;DAT</sub>   | Data hold time: For I <sup>2</sup> C bus devices                                             | 0                         |     | 3.45 | μs   |
| t <sub>SU;DAT</sub>   | Data set-up time                                                                             | 250                       |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL rise time                                                                        |                           |     | 1000 | ns   |
| t <sub>f</sub>        | SDA and SCL fall time                                                                        |                           |     | 300  | ns   |
| t <sub>SU;STO</sub>   | Set-up time for STOP condition                                                               | 4                         |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition                                             | 4.7                       |     |      | μs   |
| C <sub>b</sub>        | Capacitive load for each bus line                                                            |                           |     | 400  | pF   |
| <b>Fast-Mode</b>      |                                                                                              |                           |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency                                                                          | 0                         |     | 400  | kHz  |
| t <sub>HD;STA</sub>   | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6                       |     |      | μs   |
| t <sub>LOW</sub>      | LOW period of the SCL clock                                                                  | 1.3                       |     |      | μs   |
| t <sub>HIGH</sub>     | HIGH period of the SCL clock                                                                 | 0.6                       |     |      | μs   |
| t <sub>SU;STA</sub>   | Setup time for a repeated START condition                                                    | 40.6                      |     |      | μs   |
| t <sub>HD;DAT</sub>   | Data hold time: For I <sup>2</sup> C bus devices                                             | 0                         |     | 0.9  | μs   |
| t <sub>SU;DAT</sub>   | Data set-up time                                                                             | 100                       |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL rise time                                                                        | 20 + 0.1 × C <sub>b</sub> |     | 300  | ns   |
| t <sub>f</sub>        | SDA and SCL fall time                                                                        | 20 + 0.1 × C <sub>b</sub> |     | 300  | ns   |
| t <sub>SU;STO</sub>   | Set-up time for STOP condition                                                               | 0.6                       |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition                                             | 1.3                       |     |      | μs   |
| C <sub>b</sub>        | Capacitive load for each bus line                                                            | 10                        |     | 400  | pF   |
| <b>Fast-Mode Plus</b> |                                                                                              |                           |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency                                                                          | 0                         |     | 1000 | kHz  |
| t <sub>HD;STA</sub>   | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26                      |     |      | μs   |
| t <sub>LOW</sub>      | LOW period of the SCL clock                                                                  | 0.5                       |     |      | μs   |
| t <sub>HIGH</sub>     | HIGH period of the SCL clock                                                                 | 0.26                      |     |      | μs   |
| t <sub>SU;STA</sub>   | Setup time for a repeated START condition                                                    | 0.26                      |     |      | μs   |
| t <sub>HD;DAT</sub>   | Data hold time: For I <sup>2</sup> C bus devices                                             | 0                         |     |      | μs   |
| t <sub>SU;DAT</sub>   | Data set-up time                                                                             | 50                        |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL Rise Time                                                                        |                           |     | 120  | ns   |
| t <sub>f</sub>        | SDA and SCL Fall Time                                                                        |                           |     | 120  | ns   |
| t <sub>SU;STO</sub>   | Set-up time for STOP condition                                                               |                           |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition                                             | 0.5                       |     |      | μs   |
| C <sub>b</sub>        | Capacitive load for each bus line                                                            | 10                        |     | 550  | pF   |

## 6.7 TDM Port Timing Requirements

T<sub>A</sub> = 25 °C, VDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

|                         |                   | MIN | NOM | MAX | UNIT |
|-------------------------|-------------------|-----|-----|-----|------|
| t <sub>H</sub> (SBCLK)  | SBCLK high period | 20  |     |     | ns   |
| t <sub>L</sub> (SBCLK)  | SBCLK low period  | 20  |     |     | ns   |
| t <sub>SU</sub> (FSYNC) | FSYNC setup time  | 8   |     |     | ns   |

## TDM Port Timing Requirements (continued)

$T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ , 20 pF load on all outputs (unless otherwise noted)

|                  |                      | MIN                          | NOM | MAX | UNIT |
|------------------|----------------------|------------------------------|-----|-----|------|
| $t_{HLD}(FSYNC)$ | FSYNC hold time      | 8                            |     |     | ns   |
| $t_{SU}(FSYNC)$  | SDIN setup time      | 8                            |     |     | ns   |
| $t_{HLD}(SDIN)$  | SDIN hold time       | 8                            |     |     | ns   |
| $t_d(DO-SBCLK)$  | SBCLK to SDOUT delay | 50% of FSYNC to 50% of SDOUT |     | 21  | ns   |
| $t_r(SBCLK)$     | SBCLK rise time      | 10% - 90 % Rise Time         |     | 8   | ns   |
| $t_f(SBCLK)$     | SBCLK fall time      | 90% - 10 % Fall Time         |     | 8   | ns   |

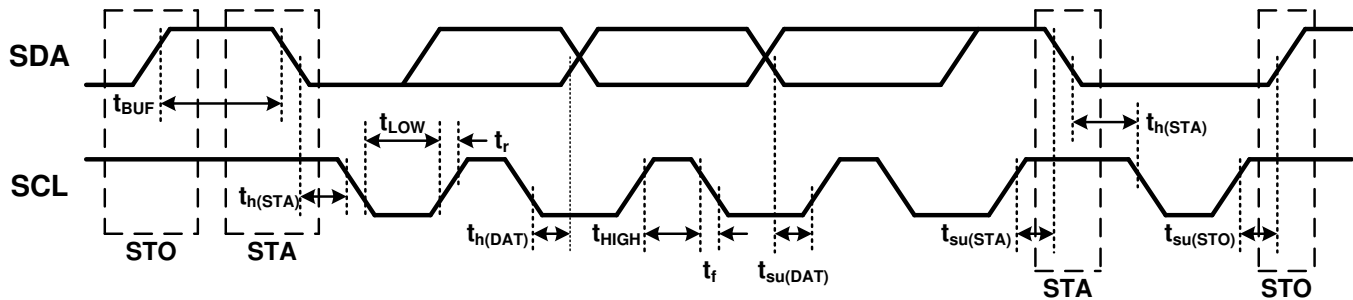


Figure 1. I<sup>2</sup>C Timing Diagram

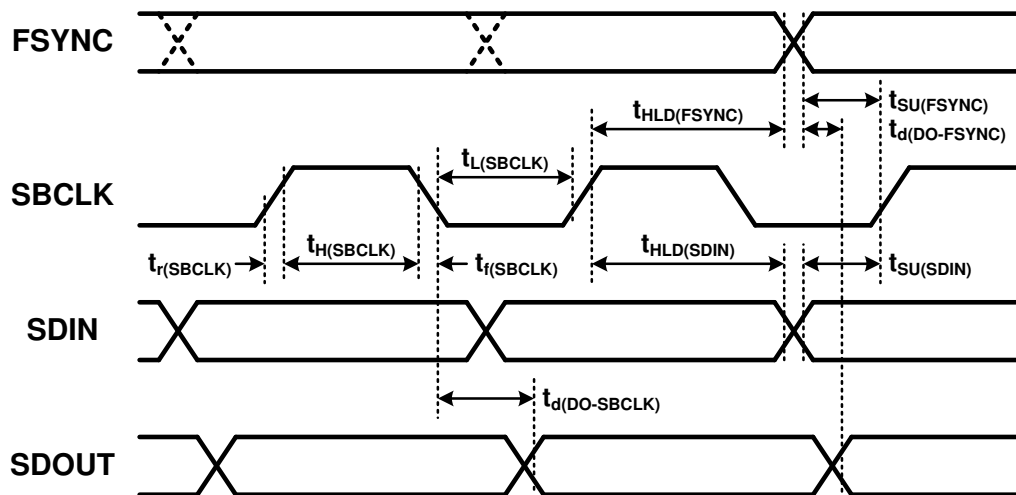
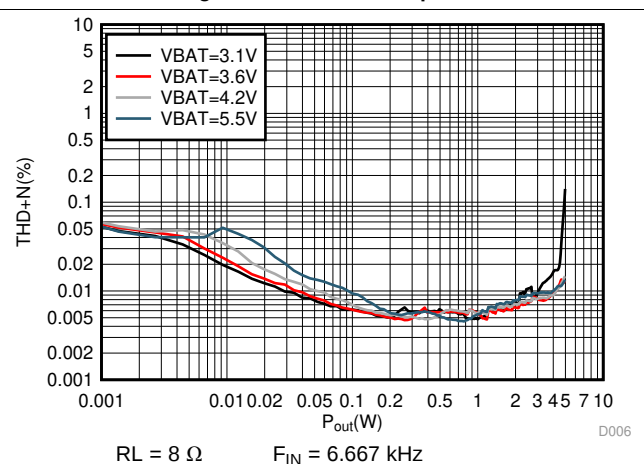
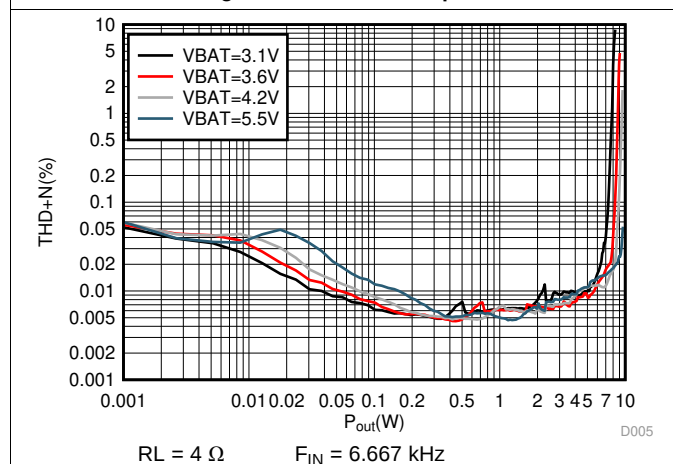
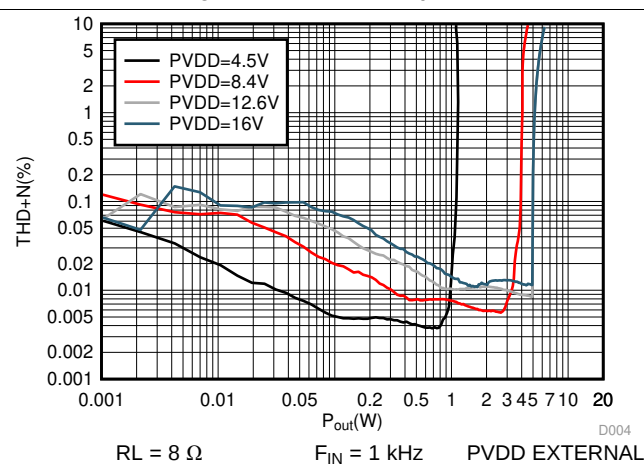
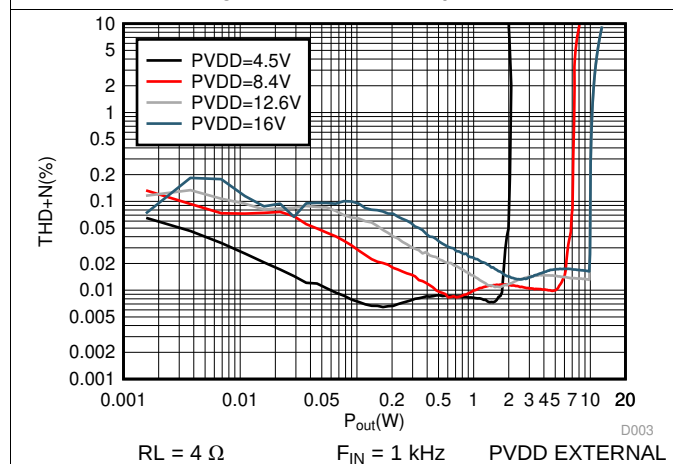
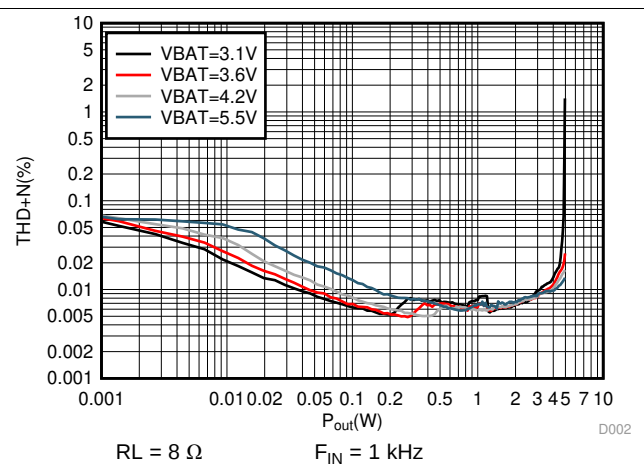
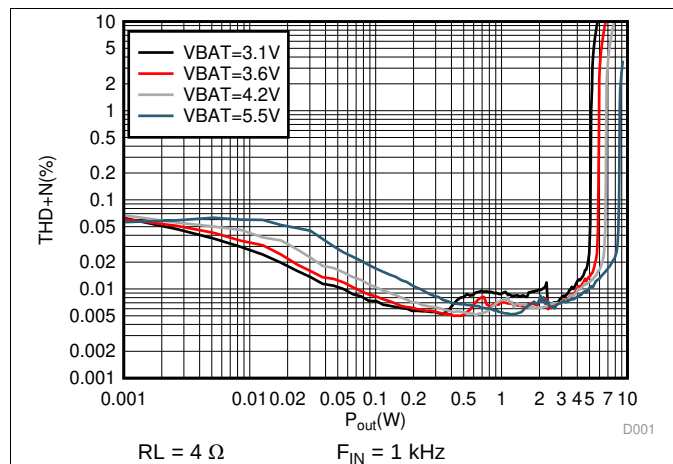


Figure 2. TDM Timing Diagram

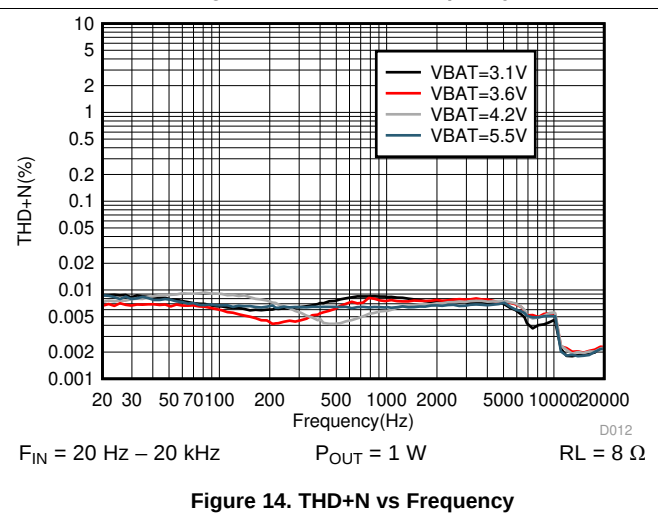
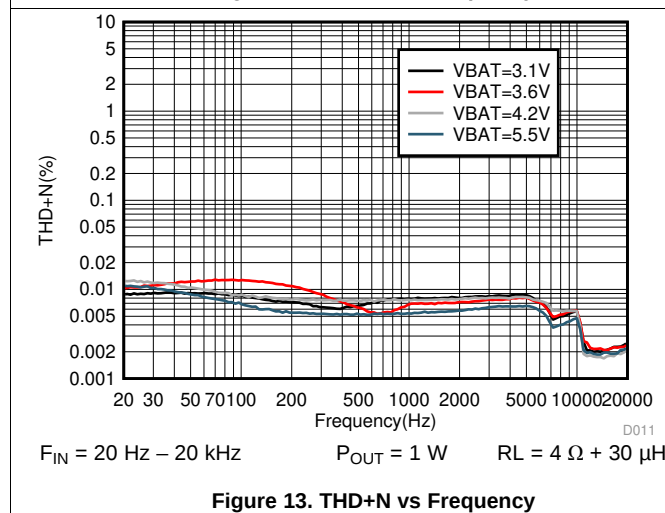
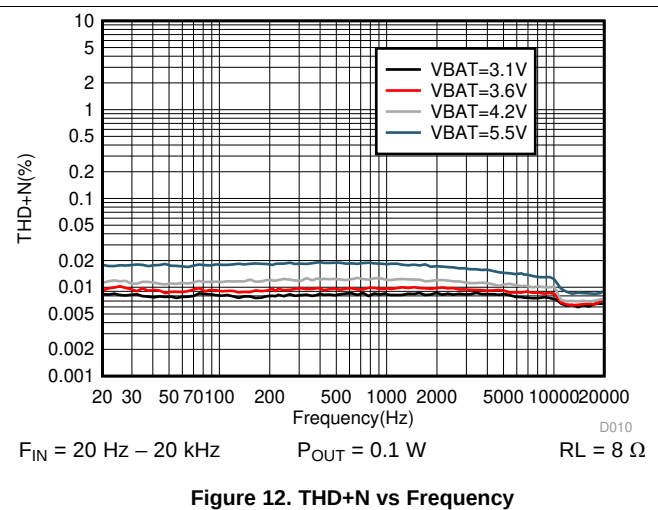
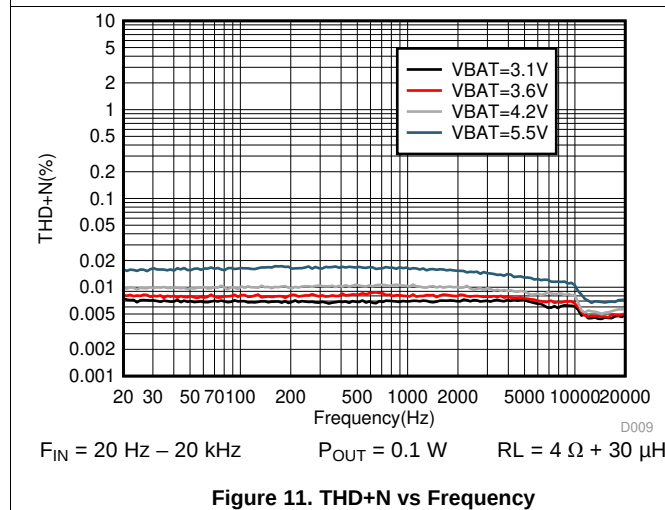
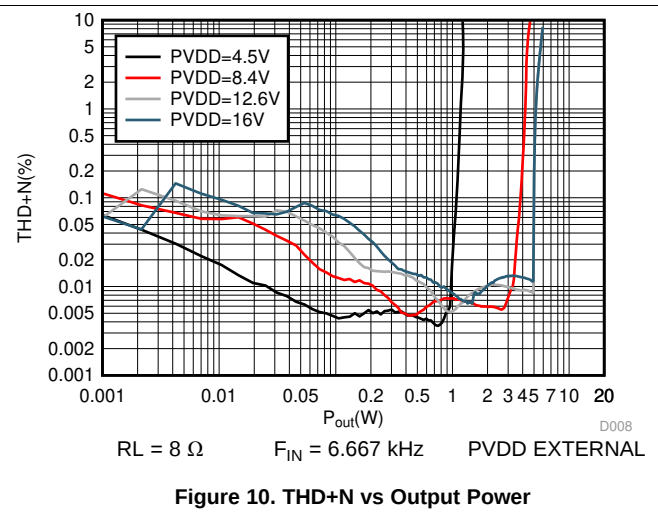
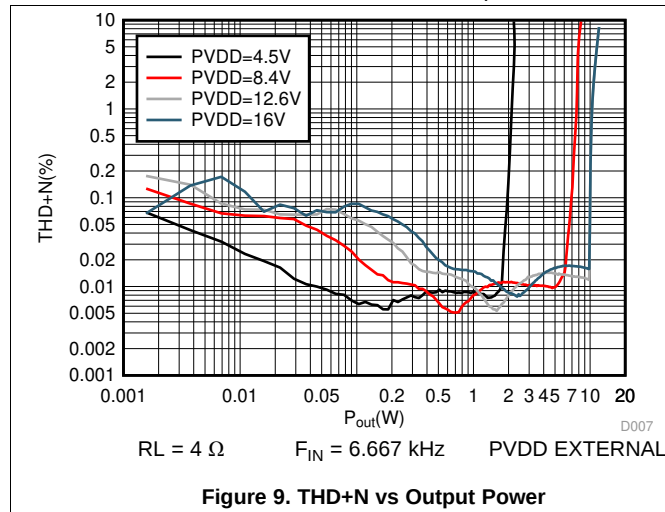
## 6.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $f_{\text{SPK\_AMP}} = 384 \text{ kHz}$ ,  $V_{\text{DD}} = 1.8\text{V}$ ,  $V_{\text{BAT}} = 3.6\text{V}$  (in external PVDD), input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30  $\mu\text{H}$ , unless otherwise noted.



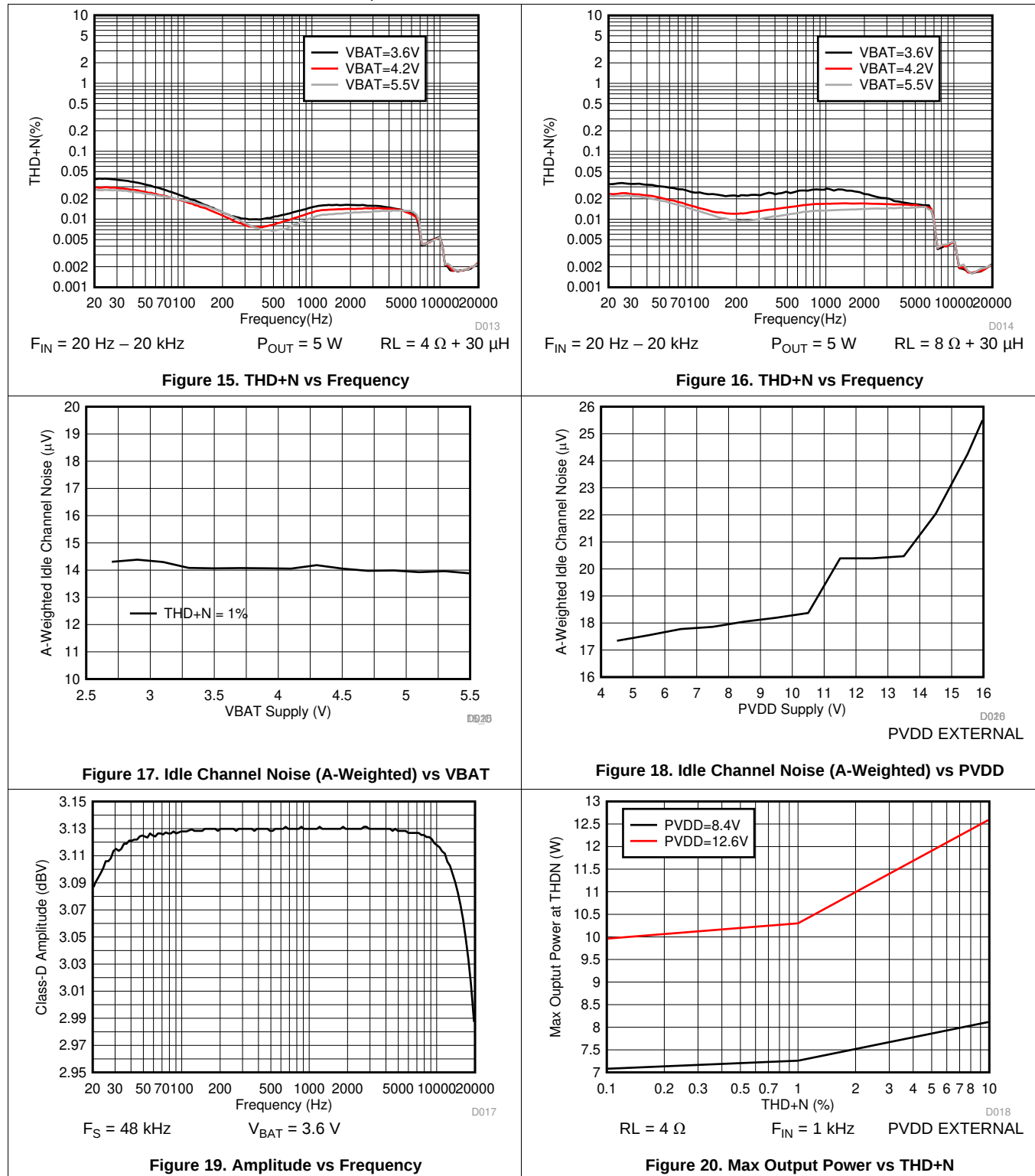
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $f_{\text{SPK\_AMP}} = 384 \text{ kHz}$ ,  $V_{\text{DD}} = 1.8\text{V}$ ,  $V_{\text{BAT}} = 3.6\text{V}$  (in external PVDD), input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30  $\mu\text{H}$ , unless otherwise noted.



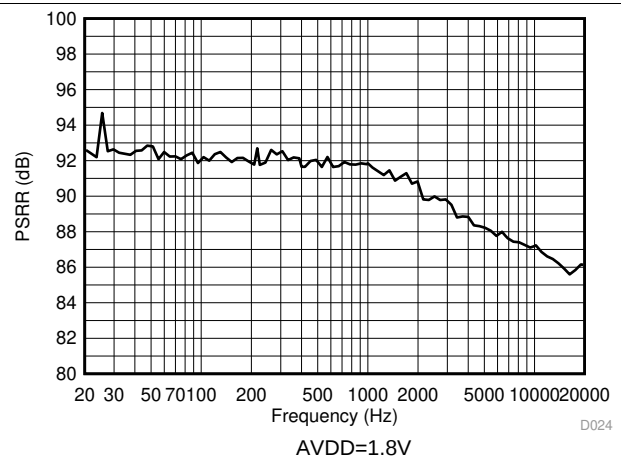
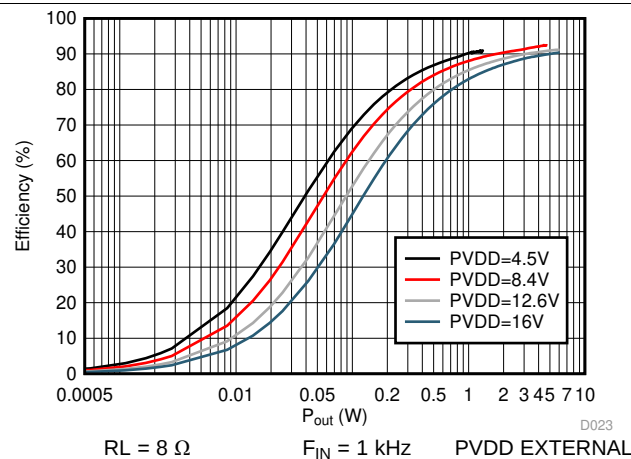
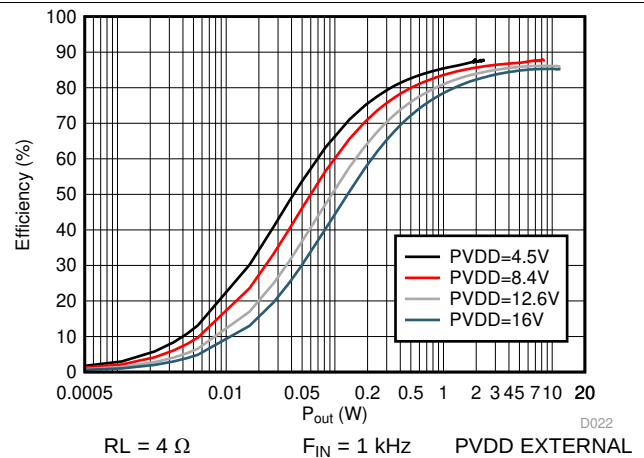
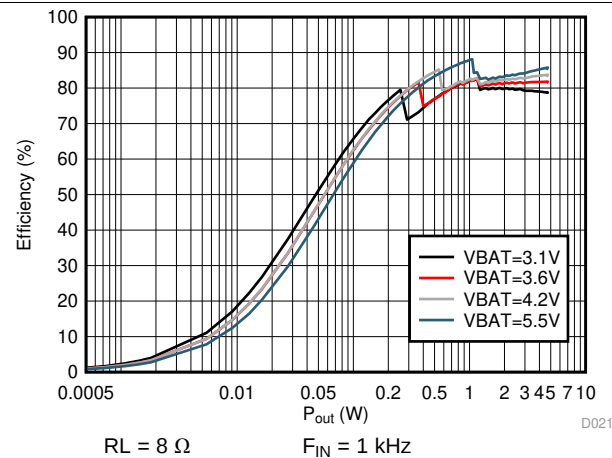
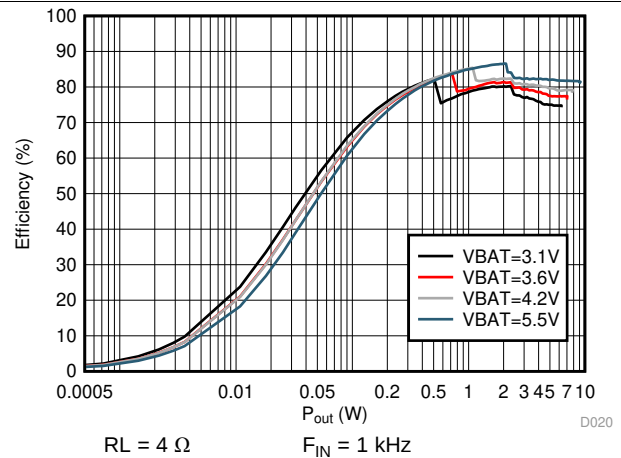
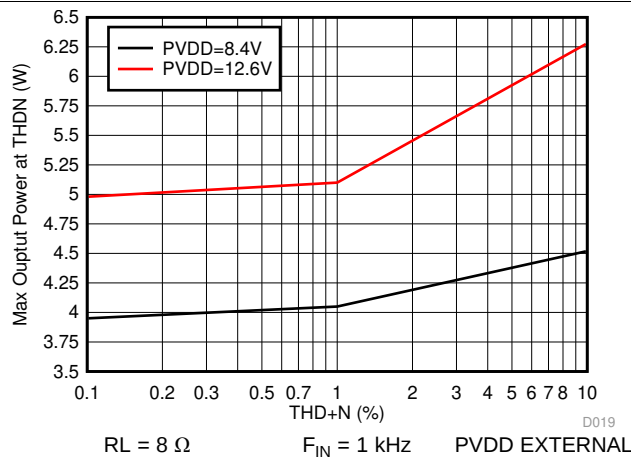
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $f_{\text{SPK\_AMP}} = 384 \text{ kHz}$ ,  $V_{\text{DD}} = 1.8\text{V}$ ,  $V_{\text{BAT}} = 3.6\text{V}$  (in external PVDD), input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30  $\mu\text{H}$ , unless otherwise noted.



## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $f_{\text{SPK\_AMP}} = 384 \text{ kHz}$ ,  $V_{\text{DD}} = 1.8\text{V}$ ,  $V_{\text{BAT}} = 3.6\text{V}$  (in external PVDD), input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30  $\mu\text{H}$ , unless otherwise noted.



## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $f_{\text{SPK\_AMP}} = 384\text{ kHz}$ ,  $V_{\text{DD}} = 1.8\text{V}$ ,  $V_{\text{BAT}} = 3.6\text{V}$  (in external PVDD), input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30  $\mu\text{H}$ , unless otherwise noted.

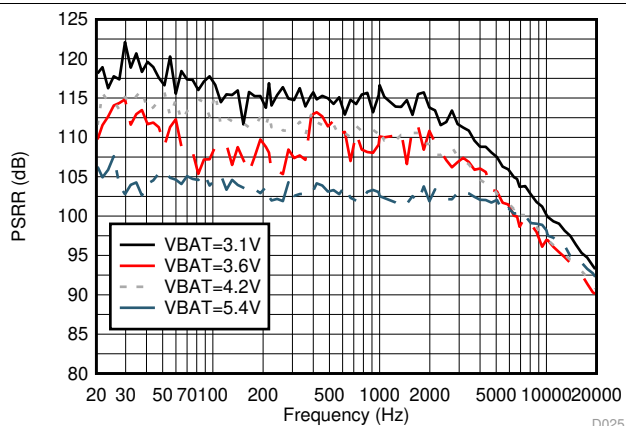


Figure 27. VBAT PSRR vs Frequency

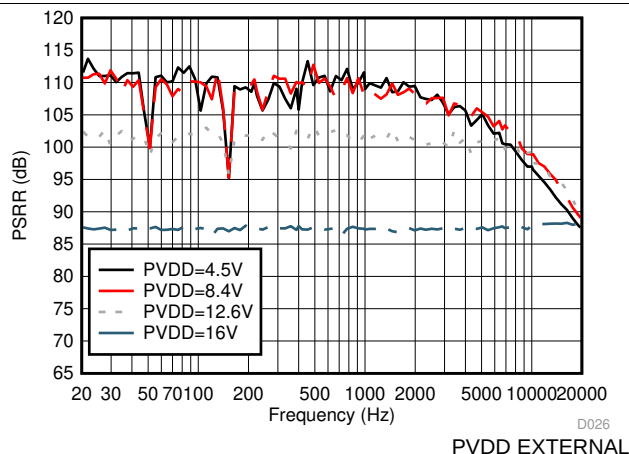


Figure 28. PVDD PSRR vs Frequency

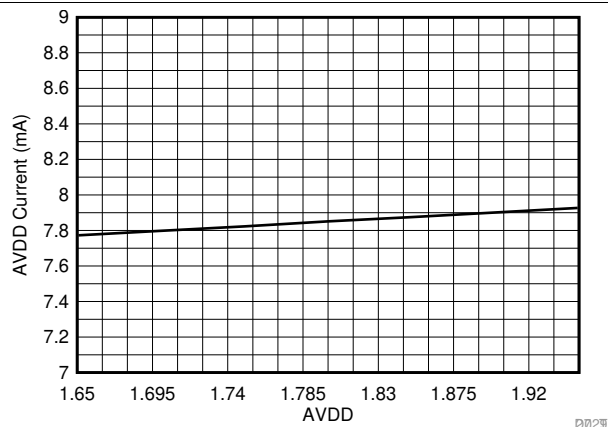


Figure 29. AVDD Idle Current vs AVDD

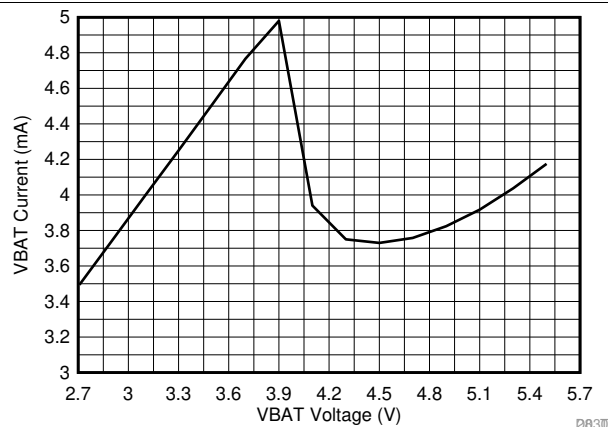


Figure 30. VBAT Idle Current vs VBAT

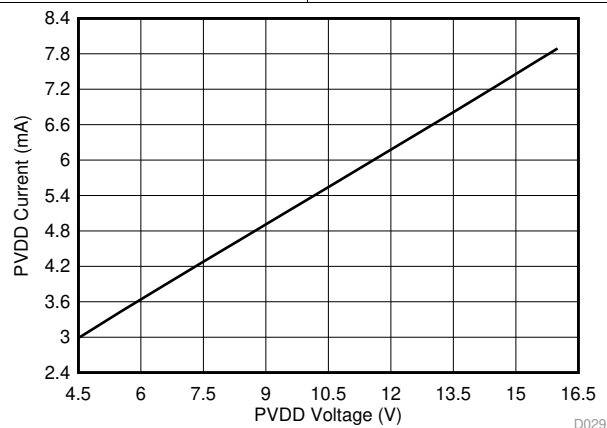
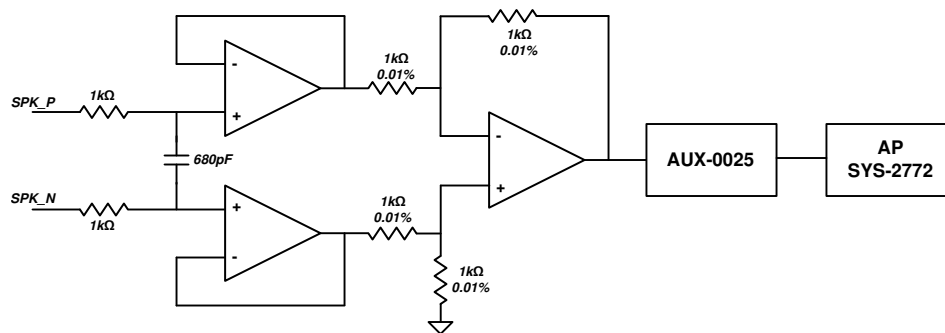


Figure 31. PVDD Idle Current vs PVDD

PVDD EXTERNAL

## 7 Parameter Measurement Information

All typical characteristics for the devices are measured using the Bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I<sup>2</sup>S interface to be driven directly into the SYS-2722. Speaker output terminals are connected to the Audio-Precision analyzer analog inputs through a differential-to-single ended (D2S) filter as shown below. The D2S filter contains a 1st order Passive pole at 120 kHz. The D2S filter ensures the TAS2110 high performance class-D amplifier sees a fully differential matched loading at its outputs. This prevents measurement errors due to loading effects of AUX-0025 filter on the class-D outputs.



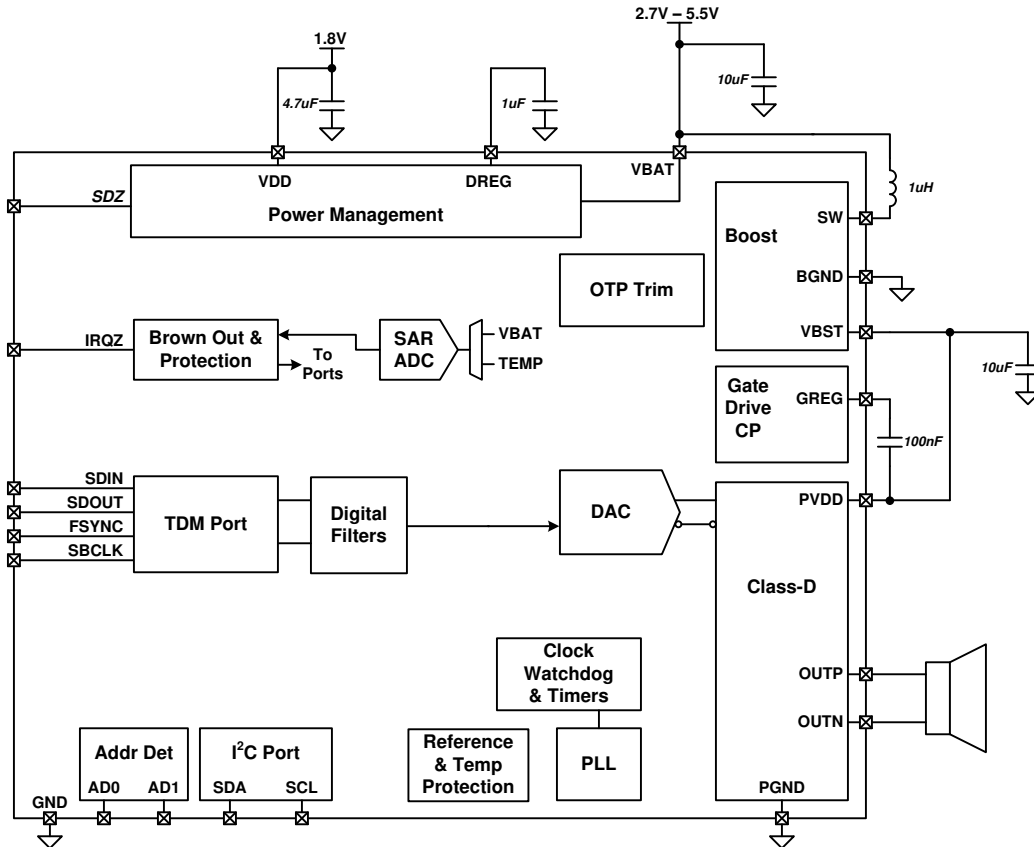
**Figure 32. Differential To Single Ended (D2S) Filter**

## 8 Detailed Description

### 8.1 Overview

The TAS2110 is a mono digital input Class-D amplifier optimized for mobile applications where efficient battery operation and small solution size are crucial. It integrates battery tracking limiting with brown out prevention.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 PurePath™ Console 3 Software

The TAS2110 advanced features and device configuration should be performed using PurePath Console 3 (PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2110 application can be download from with-in PPC3. The PCC3 tool will calculate necessary register coefficients that are described in the following sections. It is the recommended method to configure the device. Once the TAS2110 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

#### 8.3.2 Device Mode and Address Selection

The TAS2110 can operate using one of four selectable device addresses. In TDM/I<sup>2</sup>S Mode, audio input and output are provided via the FSYNC, SBCLK, SDIN and SDOUT pins using formats including I<sup>2</sup>S, Left Justified and TDM. Configuration and status are provided via the SDA and SCL pins using the I<sup>2</sup>C protocol. [Table 1](#) below illustrates how to select the device I<sup>2</sup>C address. I<sup>2</sup>C slave addresses are shown as 7-bit address format.

**Table 1. I<sup>2</sup>C Mode Address Selection**

| I <sup>2</sup> C SLAVE ADDRESS | AD1 PIN | AD0 PIN |
|--------------------------------|---------|---------|
| 0x48 (global address)          | NA      | NA      |
| 0x4C                           | GND     | GND     |
| 0x4D                           | GND     | VDD     |
| 0x4E                           | VDD     | GND     |
| 0x4F                           | VDD     | VDD     |

The TAS2110 has a global 7-bit I<sup>2</sup>C address 0x48. When enabled the device will additionally respond to I<sup>2</sup>C commands at this address regardless of the AD1 and AD0 pin settings. This is used to speed up device configuration when using multiple TAS2110 devices and programming similar settings across all devices. The I<sup>2</sup>C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I<sup>2</sup>C command. The I<sup>2</sup>C CRC function should be used to ensure each device properly received the I<sup>2</sup>C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C\_CKSUM* register should be checked on each device using the local address for a proper value. The global I<sup>2</sup>C address can be disabled using *I2C\_GBL\_EN* register. The I<sup>2</sup>C address is detected by sampling the address pins when SDZ pin is released. Additionally, the address may be re-detected by setting *I2C\_AD\_DET* high after power up and the pins will be resampled.

**Table 2. I<sup>2</sup>C Global Address Enable**

| <i>I2C_GBL_EN</i> | SETTING           |
|-------------------|-------------------|
| 0                 | Disabled          |
| 1                 | Enabled (default) |

**Table 3. I<sup>2</sup>C Global Address Enable**

| <i>I2C_AD_DET</i> | SETTING          |
|-------------------|------------------|
| 0                 | normal (default) |
| 1                 | Re-detect        |

### 8.3.3 General I<sup>2</sup>C Operation

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 2 kΩ and 4.7 kΩ. Do not allow the SDA and SCL voltages to exceed the device supply voltage, . The I<sup>2</sup>C pins are fault tolerant and will not load the I<sup>2</sup>C bus when the device is powered down.

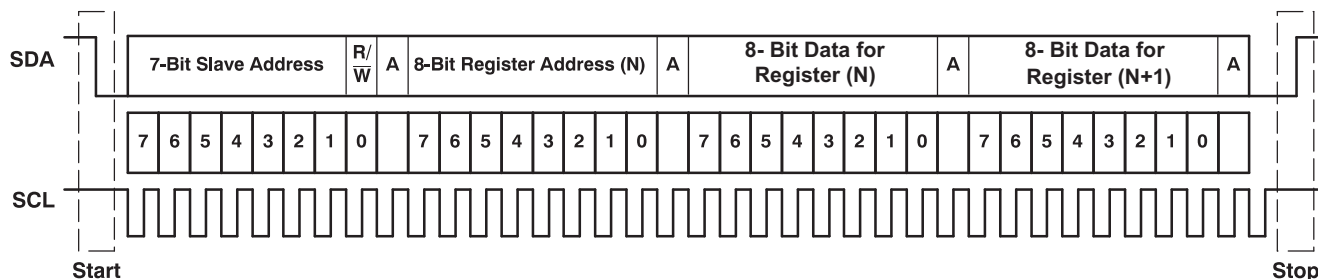


Figure 33. Typical I<sup>2</sup>C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 33 shows a generic data transfer sequence.

### 8.3.4 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2110 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2110 supports sequential I<sup>2</sup>C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I<sup>2</sup>C write transaction has taken place. For I<sup>2</sup>C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

### 8.3.5 Single-Byte Write

As shown in Figure 34, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the TAS2110 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

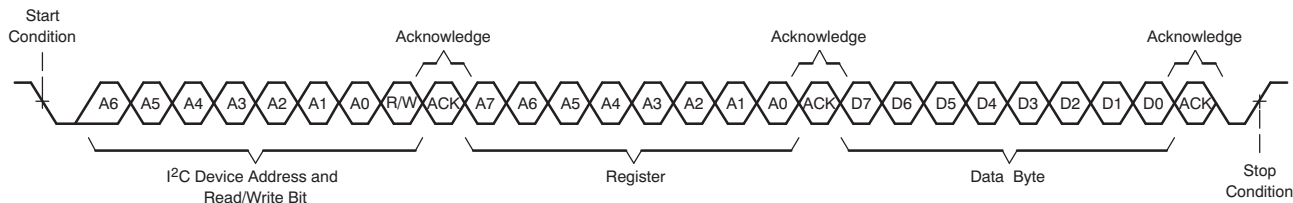
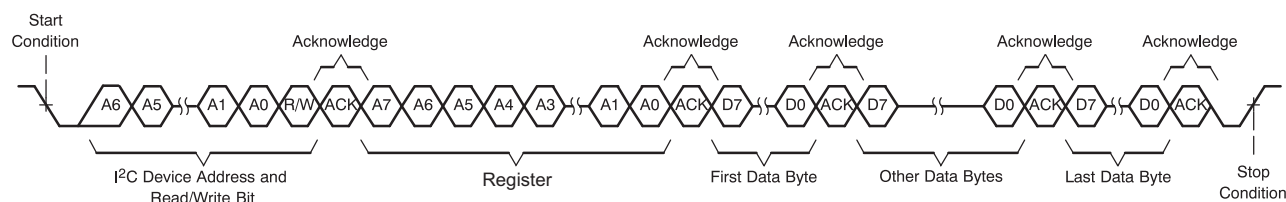


Figure 34. Single-Byte Write Transfer

### 8.3.6 Multiple-Byte Write and Incremental Multiple-Byte Write

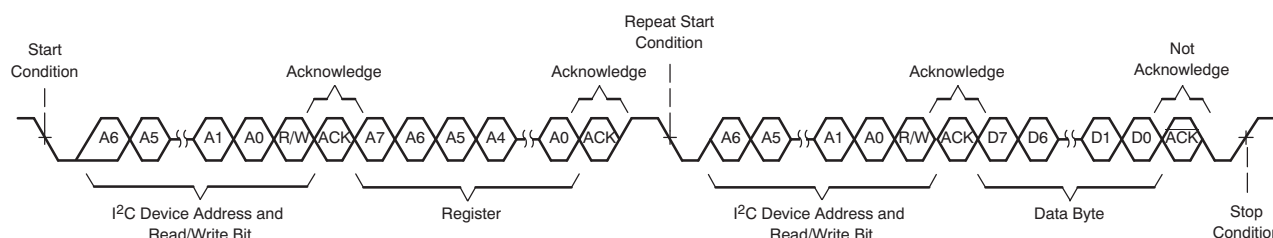
A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2110 as shown in Figure 35. After receiving each data byte, the device responds with an acknowledge bit.


**Figure 35. Multi-Byte Write Transfer**

### 8.3.7 Single-Byte Read

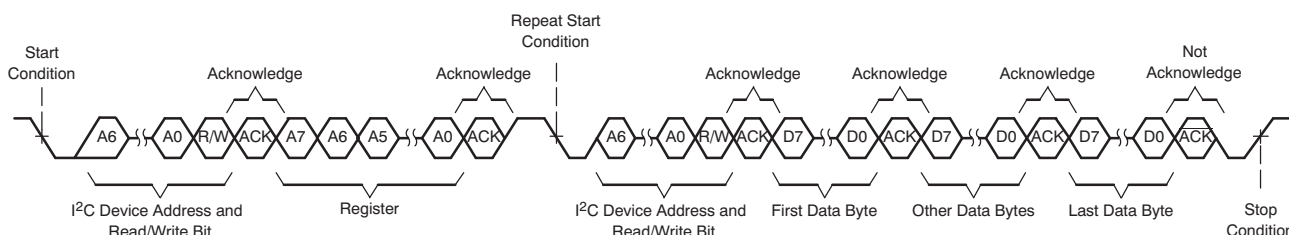
As shown in Figure 36, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2110 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2110 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2110 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.


**Figure 36. Single-Byte Read Transfer**

### 8.3.8 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2110 to the master device as shown in Figure 37. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.


**Figure 37. Multi-Byte Read Transfer**

### 8.3.9 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0, page 0, which is the default setting at power up (and after a software reset). The book and page can be set by the *BOOK*[7:0] and *PAGE*[7:0] registers respectively.

## 8.3.10 Operational Modes

### 8.3.10.1 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers loose state in this mode and I<sup>2</sup>C communication is disabled.

In normal shutdown mode if SDZ is asserted low while audio is playing, the device will ramp down volume on the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode. If configured in normal with timeout shutdown mode the device will force a hard shutdown after a timeout of the configurable shutdown timer. Finally the device can be configured for hard shutdown and will not attempt to gracefully stop the audio channel.

**Table 4. Shutdown Control**

| <i>SDZ_MODE[1:0]</i> | SETTING                              |
|----------------------|--------------------------------------|
| 00                   | Normal Shutdown with Timer (default) |
| 01                   | Immediate Shutdown                   |
| 10                   | Normal Shutdown                      |
| 11                   | Reserved                             |

**Table 5. Shutdown Control**

| <i>SDZ_TIMEOUT[1:0]</i> | SETTING        |
|-------------------------|----------------|
| 00                      | 2 ms           |
| 01                      | 4 ms           |
| 10                      | 6 ms (default) |
| 11                      | 23.8 ms        |

When SDZ is released, the device will sample the AD0 and AD1 pins and enter the software shutdown mode.

### 8.3.10.2 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to loose register state. Software Shutdown is enabled by asserting the *MODE[1:0]* register bits to 2'b10. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When deasserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

### 8.3.10.3 Mute

The TAS2110 will volume ramp down the Class-D amplifier to a mute state by setting the *MODE[1:0]* register bits to 2'b01. During mute the Class-D still switches, but transmits no audio content. If mute is deasserted, the device will volume ramp back to the programmed digital volume setting.

### 8.3.10.4 Active

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. Set the *MODE[1:0]* register bits to 2'b00 to enter active mode.

### 8.3.10.5 Mode Control and Software Reset

The TAS2110 mode can be configured by writing the *MODE[1:0]* bits.

**Table 6. Mode Control**

| <i>MODE[1:0]</i> | SETTING |
|------------------|---------|
| 00               | Active  |
| 01               | Mute    |

**Table 6. Mode Control (continued)**

| <i>MODE[1:0]</i> | <b>SETTING</b>              |
|------------------|-----------------------------|
| 10               | Software Shutdown (default) |
| 11               | Reserved                    |

A software reset can be accomplished by asserting the *SW\_RESET* bit, which is self clearing. This will restore all registers to their default values.

**Table 7. Software Reset**

| <i>SW_RESET</i> | <b>SETTING</b>        |
|-----------------|-----------------------|
| 0               | Don't reset (default) |
| 1               | Reset                 |

### 8.3.11 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the VDD and VBAT pins will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit hardware shutdown until VDD and VBAT are valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If VDD dips below the POR threshold, the device will immediately be forced into a reset state.

The device also monitors the VBAT supply and holds the analog core in power down if the supply is below the UVLO threshold. If the TAS2110 is in active operation and a UVLO fault occurs, the analog supplies will immediately power down to protect the device. These faults are latching and require a transition through HW/SW shutdown to clear the fault. The live and latched registers will report UVLO faults.

The device transitions into software shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into software shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit is set low (*INT\_MASK[2]*). The clock fault is also available for readback in the live or latched fault status registers (*INT\_LIVE[2]* and *INT\_LTCH[2]*). Reading the latched fault status register (*INT\_LTCH[7:0]*) clears the register.

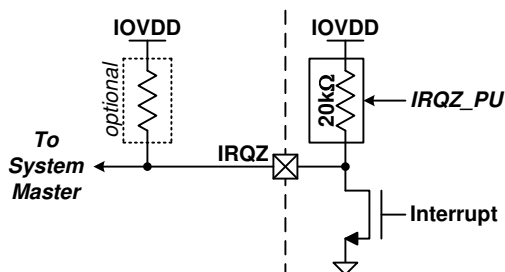
The TAS2110 also monitors die temperature and Class-D load current and will enter software shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the appropriate fault interrupt mask register bit is set low (*INT\_MASK[0]* for over temp and *INT\_MASK[1]* for over current). The fault status can also be monitored in the live and latched fault registers as with the TDM clock error.

Die over temp and Class-D over current errors can either be latching (for example the device will enter software shutdown until a HW/SW shutdown sequence is applied) or they can be configured to automatically retry after a prescribed time. This behavior can be configured in the *OTE\_RETRY* and *OCE\_RETRY* register bits (for over temp and over current respectively). Even in latched mode, the Class-D will not attempt to retry after an over temp or over current error until the retry time period (1.5 s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through SW/HW shutdown, the device will only begin to operate after the retry time period.

The status registers (and IRQZ pin if enabled via the status mask register) also indicates limiter behavior including when the limiter is activity, when VBAT is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

Interrupts can be queried using the *INT\_LIVE[9:0]* and *INT\_LTCH[13:0]* registers and correspond to the *INT\_MASK[10:0]* Interrupts. The latched registers are cleared by writing the self clearing register *INT\_CLR\_LTCH* high.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to . An internal pull up resistor is provided in the TAS2110 and can be accessed by setting the *IRQZ\_PU* register bit high. [Figure 38](#) below highlights the IRQZ pin circuit.



**Figure 38. IRQZ Pin**

**Table 8. Fault Interrupt Mask**

| INT_MASK[10:0] BIT | INTERRUPT                           | DEFAULT (1 = Mask) |
|--------------------|-------------------------------------|--------------------|
| 0                  | Over Temp Error                     | 0                  |
| 1                  | Over Current Error                  | 0                  |
| 2                  | TDM Clock Error                     | 1                  |
| 3                  | Limiter Active                      | 1                  |
| 4                  | Limiter Voltage < Inf Point         | 1                  |
| 5                  | Limiter Max Atten                   | 1                  |
| 6                  | Limiter Inf Hold                    | 1                  |
| 7                  | Limiter Mute                        | 1                  |
| 8                  | Brown Out on VBAT Supply            | 0                  |
| 9                  | Brown Out Protection Active         | 1                  |
| 10                 | Brown Out Power Down (Latched Only) | 1                  |

**Table 9. IRQ Clear Latched**

| INT_CLR_LTCH | STATE                 |
|--------------|-----------------------|
| 0            | Don't Clear           |
| 1            | Clear (self clearing) |

**Table 10. IRQZ Internal Pull Up Enable**

| IRQZ_PU | STATE              |
|---------|--------------------|
| 0       | Disabled (default) |
| 1       | Enabled            |

**Table 11. IRQZ Polarity**

| IRQZ_POL | STATE                |
|----------|----------------------|
| 0        | Active High          |
| 1        | Active Low (default) |

**Table 12. IRQZ Assert Interrupt Configuration**

| <i>IRQZ_PIN_CFG[1:0]</i> | VALUE                                                    |
|--------------------------|----------------------------------------------------------|
| 00                       | On any unmasked live interrupts                          |
| 01                       | On any unmasked latched interrupts (default)             |
| 10                       | For 2-4 ms one time on any unmasked live interrupt event |
| 11                       | For 2-4 ms every 4 ms on any unmasked latched interrupts |

**Table 13. Retry after Over Current Event**

| <i>OCE_RETRY</i> | STATE              |
|------------------|--------------------|
| 0                | Disabled (default) |
| 1                | Enabled            |

**Table 14. Retry after Over Temperature Event**

| <i>OTE_RETRY</i> | VALUE                  |
|------------------|------------------------|
| 0                | Do not retry (default) |
| 1                | Retry after 1.5 s      |

### 8.3.12 Power Sequencing Requirements

There are no other power sequencing requirements for order of rate of ramping up or down.

### 8.3.13 Digital Input Pull Downs

Each digital input and IO has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown.

**Table 15. Digital Input Pull Down Enables**

| REGISTER BIT     | DESCRIPTION                | BIT VALUE | STATE              |
|------------------|----------------------------|-----------|--------------------|
| <i>DIN_PD[0]</i> | Weak pull down for SBCLK.  | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[1]</i> | Weak pull down for FSYNC.  | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[2]</i> | Weak pull down for SDIN.   | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[3]</i> | Weak pull down for SDOOUT. | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[4]</i> | Weak pull down for AD0.    | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[5]</i> | Weak pull down for AD1.    | 0         | Disabled (default) |
|                  |                            | 1         | Enabled            |
| <i>DIN_PD[7]</i> | Weak pull down for GPIO.   | 0         | Disabled           |
|                  |                            | 1         | Enabled (default)  |

## 8.4 Device Functional Modes

### 8.4.1 TDM Port

The TAS2110 provides a flexible TDM serial audio port. The port can be configured to support a variety of formats including stereo I<sup>2</sup>S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOOUT pin is used to transmit sample streams including VBAT voltage, die temperature and channel gain.

## Device Functional Modes (continued)

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. Valid SBCLK to FSYNC ratios are 64, 96, 128, 192, 256, 384 and 512. The device will automatically detect the number of time slots and this does not need to be programmed.

By default, the TAS2110 will automatically detect the PCM playback sample rate. This can be disabled by setting the *AUTO\_RATE* register bit high and manually configuring the device.

The *SAMP\_RATE* register bits set the PCM audio sample rate when *AUTO\_RATE* is enabled. The TAS2110 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (*AUTO\_RATE* enabled) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

When using the auto rate detection the sampling rate and SBCLK to FSYNC ration detected on the TDM bus is reported back on the read-only register *FS\_RATE* and *FS\_RATIO* respectively.

While the sampling rate of 192 kHz is supported, it is internally down-sampled to 96 kHz. Therefore audio content greater than 40 kHz should not be applied to prevent aliasing. This additionally effects all processing blocks like BOP and limiter which should use 96 kHz fs when accepting 192 kHz audio. It is recommend to use [PurePath™ Console 3 Software](#) to configure the device.

**Table 16. PCM Auto Sample Rate Detection**

| <i>AUTO_RATE</i> | SETTING           |
|------------------|-------------------|
| 0                | Enabled (default) |
| 1                | Disabled          |

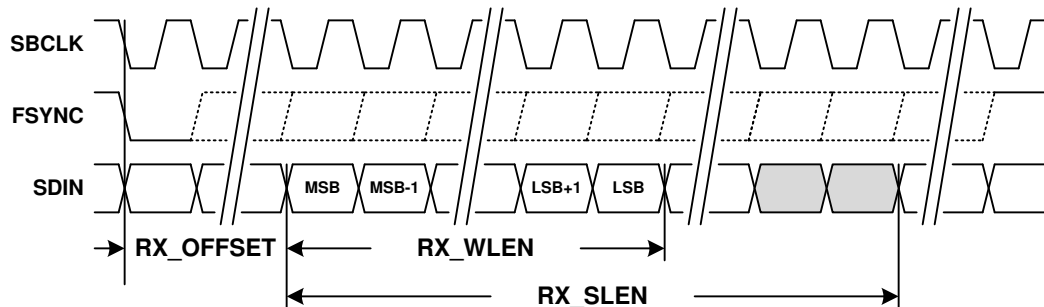
**Table 17. PCM Audio Sample Rates**

| <i>SAMP_RATE</i> [2:0] | <i>FS_RATE</i> (read only) | SAMPLE RATE                 |
|------------------------|----------------------------|-----------------------------|
| 000                    | 000                        | 7.35kHz / 8 kHz             |
| 001                    | 001                        | 14.7kHz / 16kHz             |
| 010                    | 010                        | 22.05 kHz / 24 kHz          |
| 011                    | 011                        | 29.4 kHz / 32 kHz           |
| 100                    | 100                        | 44.1 kHz / 48 kHz (default) |
| 101                    | 101                        | 88.2 kHz / 96 kHz           |
| 110                    | 110                        | 176.4 kHz / 192 kHz         |
| 111                    | 111                        | Reserved                    |

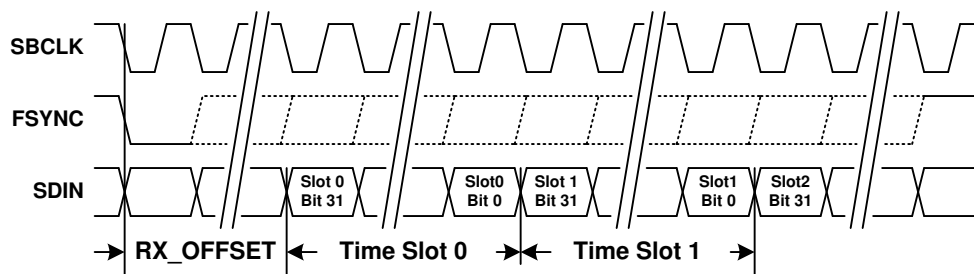
**Table 18. PCM SBCLK to FSYNC Ratio Rates**

| <i>FS_RATIO</i> [3:0] | SAMPLE RATE     |
|-----------------------|-----------------|
| 0x0 - 0x3             | Reserved        |
| 0x4                   | 64              |
| 0x5                   | 96              |
| 0x6                   | 128             |
| 0x7                   | 192             |
| 0x8                   | 256             |
| 0x9                   | 384             |
| 0xA                   | 512             |
| 0xB - 0xE             | Reserved        |
| 0xF                   | Error Condition |

Figure 39 and Figure 40 below illustrates the receiver frame parameters required to configure the port for playback. A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME\_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge (set by the *RX\_EDGE* register bit). The *RX\_OFFSET* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I<sup>2</sup>S format.



**Figure 39. TDM RX Time Slot with Left Justification**



**Figure 40. TDM RX Time Slots**

**Table 19. TDM Start of Frame Polarity**

| <i>FRAME_START</i> | <b>POLARITY</b>                               |
|--------------------|-----------------------------------------------|
| 0                  | Low to High on FSYNC <sup>(1)</sup>           |
| 1                  | High to Low on FSYNC (default) <sup>(2)</sup> |

(1) When Low to High is used *RX\_EDGE* and *TX\_EDGE* cannot both simultaneously be set to rising edge.

(2) When High to Low is used *RX\_EDGE* and *TX\_EDGE* cannot both simultaneously be set to falling edge.

**Table 20. TDM RX Capture Polarity**

| <i>RX_EDGE</i> | <b>FSYNC AND SDIN CAPTURE EDGE</b> |
|----------------|------------------------------------|
| 0              | Rising edge of SBCLK (default)     |
| 1              | Falling edge of SBCLK              |

**Table 21. TDM RX Start of Frame to Time Slot 0 Offset**

| <i>RX_OFFSET[4:0]</i> | <b>SBCLK CYCLES</b> |
|-----------------------|---------------------|
| 0x00                  | 0                   |
| 0x01                  | 1 (default)         |
| 0x02                  | 2                   |
| ...                   | ...                 |
| 0x1E                  | 30                  |
| 0x1F                  | 31                  |

The *RX\_SLEN[1:0]* register bits set the length of the RX time slot. The length of the audio sample word within the time slot is configured by the *RX\_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX\_JUSTIFY* register bit. The TAS2110 supports mono and stereo down mix playback ( $(L+R)/2$ ) via the left time slot, right time slot and time slot configuration register bits (*RX\_SLOT\_L[3:0]*, *RX\_SLOT\_R[3:0]* and *RX\_SCFG[1:0]* respectively). By default the device will playback mono from the time slot equal to the I<sup>2</sup>C base address offset for playback. The *RX\_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX\_SLOT\_L[3:0]* and *RX\_SLOT\_R[3:0]* register bits.

If time slot selections places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

**Table 22. TDM RX Time Slot Length**

| <i>RX_SLEN[1:0]</i> | TIME SLOT LENGTH  |
|---------------------|-------------------|
| 00                  | 16-bits           |
| 01                  | 24-bits           |
| 10                  | 32-bits (default) |
| 11                  | reserved          |

**Table 23. TDM RX Sample Word Length**

| <i>RX_WLEN[1:0]</i> | LENGTH            |
|---------------------|-------------------|
| 00                  | 16-bits           |
| 01                  | 20-bits           |
| 10                  | 24-bits (default) |
| 11                  | 32-bits           |

**Table 24. TDM RX Sample Justification**

| <i>RX_JUSTIFY</i> | JUSTIFICATION  |
|-------------------|----------------|
| 0                 | Left (default) |
| 1                 | Right          |

**Table 25. TDM RX Time Slot Select Configuration**

| <i>RX_SCFG[1:0]</i> | CONFIG ORIGIN                                                          |
|---------------------|------------------------------------------------------------------------|
| 00                  | Mono with Time Slot equal to I <sup>2</sup> C Address Offset (default) |
| 01                  | Mono Left Channel                                                      |
| 10                  | Mono Right Channel                                                     |
| 10                  | Stereo Down Mix $(L+R)/2$                                              |

**Table 26. TDM RX Left Channel Time Slot**

| <i>RX_SLOT_L[3:0]</i> | TIME SLOT   |
|-----------------------|-------------|
| 0x0                   | 0 (default) |
| 0x1                   | 1           |
| ...                   | ...         |
| 0xE                   | 14          |
| 0xF                   | 15          |

**Table 27. TDM RX Right Channel Time Slot**

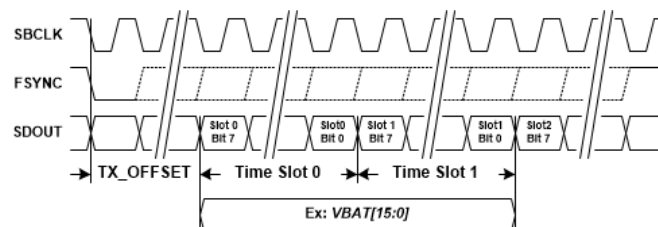
| <i>RX_SLOT_R[3:0]</i> | TIME SLOT   |
|-----------------------|-------------|
| 0x0                   | 0           |
| 0x1                   | 1 (default) |

**Table 27. TDM RX Right Channel Time Slot (continued)**

| <i>RX_SLOT_R[3:0]</i> | TIME SLOT |
|-----------------------|-----------|
| ...                   | ...       |
| 0xE                   | 14        |
| 0xF                   | 15        |

The TDM port can transmit a number sample streams on the SDOUT pin including, VBAT voltage, die temperature and channel gain. below illustrates the alignment of time slots to the beginning of a frame and how a given sample stream is mapped to time slots. Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin, which can be configured by setting the *TX\_EDGE* register bit. The *TX\_OFFSET* register defines the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This would typically be programmed to 0 for Left Justified format and 1 for I<sup>2</sup>S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX\_FILL* register bit setting. An optional bus keeper will weakly hold the state of SDOUT when all devices driving are Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX\_KEEPCY* register bit. The bus-keeper can additionally be configured to be enabled for only 1LSB cycle or always using *TX\_KEEPLN* and to drive the full or half cycle of the LSB using *TX\_KEEPCY*.

Each sample stream is composed of either one or two 8-bit time slots.. The VBAT voltage stream is 10-bit precision, and can either be transmitted left justified in a 16-bit word (using two time slots) or can be truncated to 8-bits (the top 8 MSBs) and be transmitted in a single time slot. This is configured by setting *VBAT\_SLEN* register bit. The Die temperature and gain are both 8-bit precision and are transmitted in a single time slot.


**Figure 41. TDM Port TX Diagram**
**Table 28. TDM TX Transmit Polarity**

| <i>TX_EDGE</i> | SDOUT TRANSMIT EDGE             |
|----------------|---------------------------------|
| 0              | Rising edge of SBCLK            |
| 1              | Falling edge of SBCLK (default) |

**Table 29. TDM TX Start of Frame to Time Slot 0 Offset**

| <i>TX_OFFSET[2:0]</i> | SBCLK CYCLES |
|-----------------------|--------------|
| 0x0                   | 0            |
| 0x1                   | 1 (default)  |
| 0x2                   | 2            |
| ...                   | ...          |
| 0x6                   | 6            |
| 0x7                   | 7            |

**Table 30. TDM TX Unused Bit Field Fill**

| <i>TX_FILL</i> | SDOUT UNUSED BIT FIELDS |
|----------------|-------------------------|
| 0              | Transmit 0              |
| 1              | Transmit Hi-Z (default) |

**Table 31. TDM TX SDOUT Bus Keeper Enable**

| <i>TX_KEEPE</i> | <b>SDOUT BUS KEEPER</b>     |
|-----------------|-----------------------------|
| 0               | Disable bus keeper          |
| 1               | Enable bus keeper (default) |

**Table 32. TDM TX SDOUT Bus Keeper Length**

| <i>TX_KEEPLN</i> | <b>SDOUT BUS KEEPER ENABLED FOR</b> |
|------------------|-------------------------------------|
| 0                | 1 LSB cycle (default)               |
| 1                | Always                              |

**Table 33. TDM TX SDOUT Bus Keeper LSB Cycle**

| <i>TX_KEEPCY</i> | <b>SDOUT BUS KEEPER DRIVEN</b> |
|------------------|--------------------------------|
| 0                | full-cycle (default)           |
| 1                | half-cycle                     |

The time slot register for each sample stream defines where the MSB transmission begins. Each sample stream can be individually enabled or disabled. This is useful to manage limited TDM bandwidth since it may not be necessary to transmit all streams for all devices on the bus.

It is important to ensure that time slot assignments for actively transmitted sample streams do not conflict. This will produce unpredictable transmission results in the conflicting bit slots

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

It is recommended to keep the following slot ordering:

VBAT\_SLOT<TEMP\_SLOT<GAIN\_SLOT.

**Table 34. TDM VBAT Time Slot**

| <i>VBAT_SLOT[5:0]</i> | <b>SLOT</b> |
|-----------------------|-------------|
| 0x00                  | 0           |
| 0x01                  | 1           |
| ...                   | ...         |
| 0x04                  | 4 (default) |
| ...                   | ...         |
| 0x3E                  | 62          |
| 0x3F                  | 63          |

**Table 35. TDM VBAT Time Slot Length**

| <i>VBAT_SLEN</i> | <b>SLOT LENGTH</b>           |
|------------------|------------------------------|
| 0                | Truncate to 8-bits (default) |
| 1                | Left justify to 16-bits      |

**Table 36. TDM VBAT Transmit Enable**

| <i>VBAT_TX</i> | <b>STATE</b>       |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

**Table 37. TDM Temp Sensor Time Slot**

| <i>TEMP_SLOT[5:0]</i> | <b>SLOT</b> |
|-----------------------|-------------|
| 0x00                  | 0           |
| 0x01                  | 1           |
| ...                   | ...         |
| 0x05                  | 5 (default) |
| ...                   | ...         |
| 0x3E                  | 62          |
| 0x3F                  | 63          |

**Table 38. TDM Temp Sensor Transmit Enable**

| <i>TEMP_TX</i> | <b>STATE</b>       |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

The following sample streams are part of the [Inter Chip Limiter Alignment](#) system. These data streams can be routed over the audio TDM bus.

**Table 39. TDM Limiter Gain Reduction Time Slot**

| <i>GAIN_SLOT[5:0]</i> | <b>SLOT</b> |
|-----------------------|-------------|
| 0x00                  | 0           |
| 0x01                  | 1           |
| ...                   | ...         |
| 0x06                  | 6 (default) |
| ...                   | ...         |
| 0x3E                  | 62          |
| 0x3F                  | 63          |

**Table 40. TDM Limiter Gain Reduction Transmit Enable**

| <i>GAIN_TX</i> | <b>STATE</b>       |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

**Table 41. TDM Boost Sync Time Slot**

| <i>BST_SLOT[5:0]</i> | <b>SLOT</b> |
|----------------------|-------------|
| 0x00                 | 0           |
| 0x01                 | 1           |
| ...                  | ...         |
| 0x07                 | 7 (default) |
| ...                  | ...         |
| 0x3E                 | 62          |
| 0x3F                 | 63          |

**Table 42. TDM Boost Sync Enable**

| <i>BST_TX</i> | <b>STATE</b>       |
|---------------|--------------------|
| 0             | Disabled (default) |
| 1             | Enabled            |

## 8.4.2 Playback Signal Path

### 8.4.2.1 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The TAS2110 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. The HPF can be disabled using register HPF\_EN. The HPF Bi-Quad filter coefficients can be changed from the default 2 Hz using the HPFC\_N0, HPFC\_N1, HPFC\_D1 registers using the equation  $[N, D] = \text{butter}(1, fc/(fs/2), 'high');$  round( $N(0)*2^{31}$ );. These coefficients should be calculated and set using [PurePath™ Console 3 Software](#).

**Table 43. HPF Enable**

| HPF_EN | STATE             |
|--------|-------------------|
| 0      | Enabled (default) |
| 1      | Disabled          |

### 8.4.2.2 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's output level and digital volume control (DVC).

Amplifier output level settings are presented in dBV (dB relative to 1 V<sub>rms</sub>) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only. [Table 44](#) below shows gain settings that can be programmed via the AMP\_LEVEL register.

**Table 44. Amplifier Output Level Settings**

| AMP_LEVEL[4:0] | FULL SCALE OUTPUT |                       |
|----------------|-------------------|-----------------------|
|                | dBV               | V <sub>PEAK</sub> (V) |
| 0x00           | 8                 | 3.55                  |
| 0x01           | 8.5               | 3.76                  |
| 0x02           | 9                 | 3.99                  |
| ...            | ...               | ...                   |
| 0x10           | 16                | 8.92                  |
| ...            | ...               | ...                   |
| 0x13           | 17.5              | 10.60                 |
| 0x14           | 18                | 11.23                 |
| 0x15-0x1F      | Reserved          | Reserved              |

[Equation 1](#) calculates the amplifiers output voltage.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \text{ dBV}$$

where

- V<sub>AMP</sub> is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A<sub>dvc</sub> is the digital volume control setting, 0 dB to -100 dB in 0.5 dB steps
- A<sub>AMP</sub> is the amplifier output level setting in dBV

(1)

Settings greater than 0xC8 are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the DVC\_RAMP register bits. If DVC\_RAMP is set to 0x0000 0000, volume ramping is disabled. This can be used to speed up startup, shutdown and digital volume changes when volume ramping is handled by the system master.

The digital volume control registers DVC\_PCM represent the volume in a 2.X format. To calculate the value to write to these 4 registers apply the following formula to the desired dB DVC\_PCM = round( $10^{(dB/20)*2^{30}}$ ).

A volume ramp rate can be set using DVC\_RAMP and represents a rate in 1.X format. To calculate the value to write to these 4 registers apply the following formula DVC\_RAMP = round( $((1 - \exp(-1/(0.2*fs*time \text{ in seconds}))) * 2^{31})$ ).

**Table 45. PCM Digital Volume Control**

| DVC_PCM[31:0]     | VOLUME (dB) |
|-------------------|-------------|
| 0x0000 0D43 (MIN) | -110        |
| ...               | ...         |
| 0x4000 0000       | 0 (default) |
| ...               | ...         |
| 0x5092 BEE4 (MAX) | 2           |

**Table 46. Digital Volume Ramp Rate**

| DVC_RAMP[31:0] | RAMP RATE @ 48kHz (s) |
|----------------|-----------------------|
| 0x0000 0D43    | 0                     |
| ...            | ...                   |
| 0x7FFC 963B    | 1 s                   |

### 8.4.2.3 Auto-Mute During Idle Channel Mode

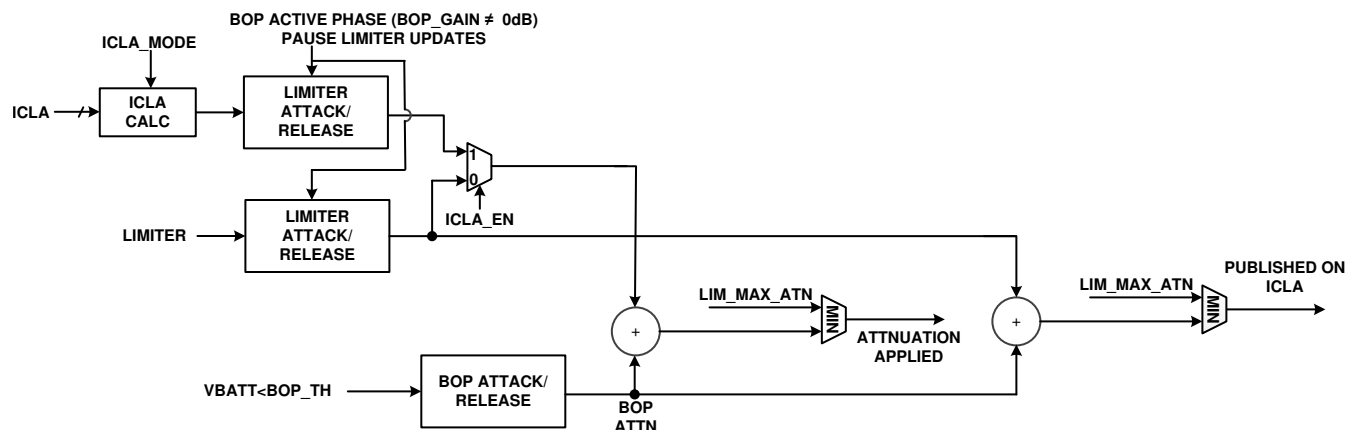
Device will stop playing audio if the input audio level drops below the programmable threshold for a programmable timer window. If this behavior is not preferred, threshold level can be kept at very low levels.

### 8.4.2.4 Auto-Start/Stop on Audio Clocks

The TAS2110 can enter low power software shutdown when the TDM clocks are stopped instead of going into clock error. The device will resume operation when the clocks resume.

### 8.4.2.5 Supply Tracking Limiters with Brown Out Prevention

The TAS2110 monitors battery voltage (VBAT) and along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiters threshold can be configured to track the monitored voltage below a programmable inflection point with a programmable slope. A minimum threshold sets the limit of threshold reduction from the voltage tracking. Configurable attack rate, hold time and release rate are provided to shape the dynamic response of each limiter. If the ICLA is enabled the actual attenuation is based on the ICLA configuration using the calculated attenuation value of all devices on the selected ICLA bus.


**Figure 42. Limiter and Brown Out Prevention Interaction Diagram**

A Brown Out Prevention (BOP) feature provides a priority input to provide a fast response to transient dips in the battery supply (VBAT) which at end of charge conditions that can cause system level brown out. When the selected supply dips below the brown-out threshold the BOP will begin reducing gain at a configurable attack rate. When the VBAT supply rises above the brownout threshold, the BOP will begin to release after the programmed hold time. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event. The VBAT limiter is enabled by setting the *LIMB\_EN* bit high.

**Table 47. VBAT Tracking Limiter Enable**

| <i>LIMB_EN</i> | VALUE              |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

The limiter has a configurable attack rate, hold time and release rate, which are available via the *LIMB\_ATK\_RT[2:0]*, *LIMB\_HLD\_TM[2:0]*, *LIMB\_RLS\_RT[2:0]* register bits. The limiter attack and release step sizes can be set by configuring the *LIMB\_ATK\_ST[1:0]* and *LIMB\_RLS\_ST[1:0]* register bits. The rates are based on the number of audio samples and actual time values can be calculated by multiplying by 1/fs. For example the attack rate of 4 samples at 48 ksps would be approximately 83  $\mu$ s.

**Table 48. Limiter Attack Rate**

| <i>LIMB_ATK_RT[2:0]</i> | ATTACK RATE (samples/step) | ATTACK RATE @ 48 ksps (~ $\mu$ s) |
|-------------------------|----------------------------|-----------------------------------|
| 0x0                     | 1                          | 20                                |
| 0x1                     | 2 (default)                | 42                                |
| 0x2                     | 4                          | 83                                |
| 0x3                     | 8                          | 167                               |
| 0x4                     | 16                         | 333                               |
| 0x5                     | 32                         | 666                               |
| 0x6                     | 64                         | 1300                              |
| 0x7                     | 128                        | 2700                              |

**Table 49. Limiter Hold Time**

| <i>LIMB_HLD_TM[2:0]</i> | HOLD TIME (samples) | HOLD TIME @ 48ksps (ms) |
|-------------------------|---------------------|-------------------------|
| 0x0                     | 0                   | 0                       |
| 0x1                     | 1920                | 40                      |
| 0x2                     | 4800                | 100                     |
| 0x3                     | 9600                | 200                     |
| 0x4                     | 19200               | 400                     |
| 0x5                     | 48000               | 1000                    |
| 0x6                     | 96000 (default)     | 2000                    |
| 0x7                     | 192000              | 4000                    |

**Table 50. Limiter Release Rate**

| <i>LIMB_RLS_RT[2:0]</i> | Release Rate (samples/step) | RELEASE RATE @ 48 ksps (ms) |
|-------------------------|-----------------------------|-----------------------------|
| 0x0                     | 10                          | 0.2                         |
| 0x1                     | 20                          | 0.4                         |
| 0x2                     | 40                          | 0.8                         |
| 0x3                     | 80                          | 1.7                         |
| 0x4                     | 160                         | 3.3                         |
| 0x5                     | 320                         | 6.7                         |
| 0x6                     | 640 (default)               | 13.3                        |
| 0x7                     | 1280                        | 26.7                        |

**Table 51. Limiter Attack Step Size**

| <i>LIMB_ATK_ST[1:0]</i> | STEP SIZE (dB) |
|-------------------------|----------------|
| 00                      | 0.25           |
| 01                      | 0.5 (default)  |

**Table 51. Limiter Attack Step Size (continued)**

| <i>LIMB_ATK_ST[1:0]</i> | STEP SIZE (dB) |
|-------------------------|----------------|
| 10                      | 1              |
| 11                      | 2              |

**Table 52. Limiter Release Step Size**

| <i>LIMB_RLS_ST[1:0]</i> | STEP SIZE (dB) |
|-------------------------|----------------|
| 00                      | 0.25           |
| 01                      | 0.5 (default)  |
| 10                      | 1              |
| 11                      | 2              |

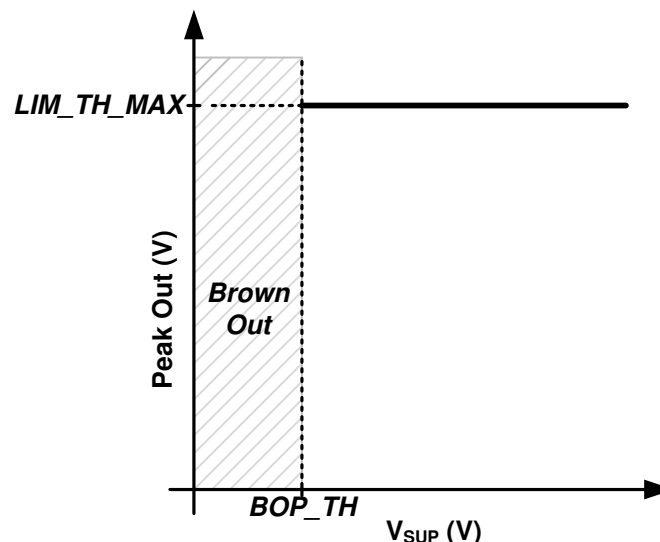
A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM\_MAX\_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

The limiter max attenuation *LIM\_MAX\_ATN* represent the limit in a 1.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired dB using equation  $LIM\_MAX\_ATN = \text{round}(10^{(-dB/20)*2^{31}})$ .

**Table 53. Limiter Max Attenuation**

| <i>LIM_MAX_ATN[31:0]</i> | ATTENUATION (dB) |
|--------------------------|------------------|
| 0x7214 82C0              | -1               |
| ...                      | ...              |
| 0x2D6A 866F              | -9 (default)     |
| ...                      | ...              |
| 0x1326 DD71              | -16.5            |

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. [Figure 43](#) below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM\_TH\_MAX*. Set the limiter inflection point using *LIM\_INF\_PT* below the minimum allowable supply setting. The limiter minimum threshold register *LIM\_TH\_MIN* does not impact limiter behavior in this use case.



**Figure 43. Limiter with Fixed Threshold**

The VBAT limiter threshold max *LIMB\_TH\_MAX* and min *LIMB\_TH\_MIN* registers represent the limit in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired threshold voltage using the equation *LIMB\_TH\_MAX* or *LIMB\_TH\_MIN* = round(Volts\*2<sup>27</sup>).

**Table 54. VBAT Limiter Maximum Threshold**

| <i>LIMB_TH_MAX</i> [31:0] | THRESHOLD (V) |
|---------------------------|---------------|
| 0x1400 0000               | 2.5           |
| ...                       | ...           |
| 0x4800 0000               | 9 (default)   |
| ...                       | ...           |
| 0x7C00 0000               | 15.5          |

**Table 55. VBAT Limiter Minimum Threshold**

| <i>LIMB_TH_MIN</i> [31:0] | THRESHOLD (V) |
|---------------------------|---------------|
| 0x1400 0000               | 2.5           |
| ...                       | ...           |
| 0x2000 0000               | 4 (default)   |
| ...                       | ...           |
| 0x7C00 0000               | 15.5          |

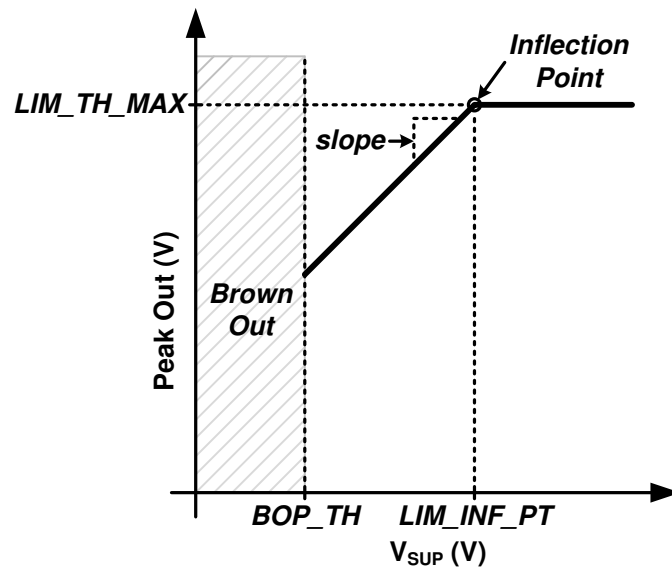
The VBAT limiter inflection point *LIMB\_INF\_PT* represent the limit in a format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using the equation *LIMB\_INF\_PT* = round(Volts\*2<sup>8</sup>).

**Table 56. VBAT Limiter Inflection Point**

| <i>LIMB_INF_PT</i> [31:0] | THRESHOLD (V) |
|---------------------------|---------------|
| 0x2000 0000               | 2             |
| ...                       | ...           |
| 0x34CC CCCC               | 3.3 (default) |
| ...                       | ...           |
| 0x3000 0000               | 6             |

Figure 44 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM\_TH\_MAX* register to the desired threshold and *LIM\_INF\_PT* register to the desired inflection point where the limiter will begin reducing the threshold with the selected supply. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in the supply voltage. More aggressive tracking slopes can be programmed if desired. Program the *LIM\_TH\_MIN* below the minimum the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

The VBAT limiter tracking slope *LIMB\_SLOPE*[31:0] represent the limit in a format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using equation *LIMB\_SLOPE* = round(slope(V/V)\*2<sup>8</sup>).

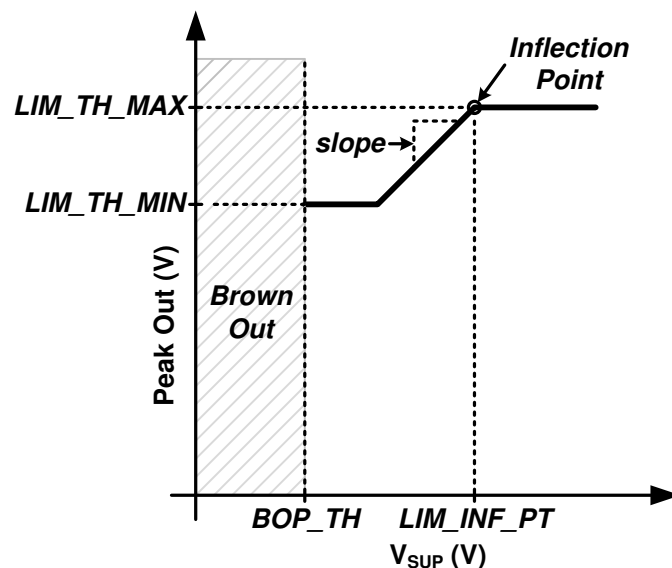


**Figure 44. Limiter with Inflection Point**

**Table 57. Limiter VBAT Tracking Slope**

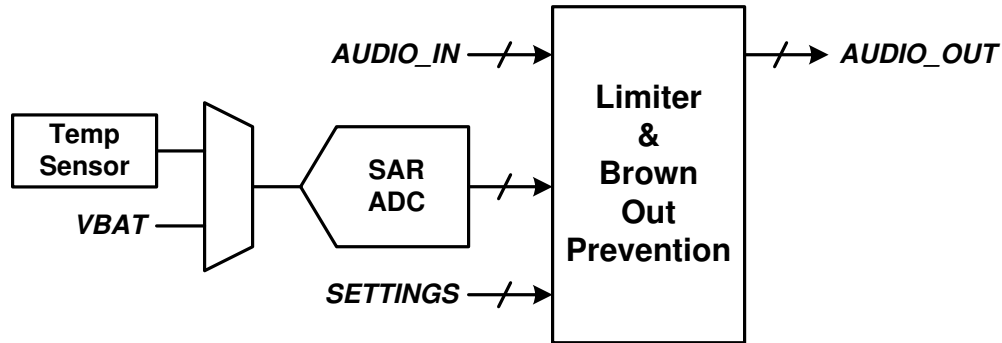
| <i>LIMB_SLOPE[31:0]</i> | <i>SLOPE (V/V)</i> |
|-------------------------|--------------------|
| 0x1000 0000             | 1 (default)        |
| ...                     | ...                |
| 0x4000 0000             | 4                  |

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the *LIM\_TH\_MIN* register to the desired minimum threshold. This is shown in [Figure 45](#) below.



**Figure 45. Limiter with Inflection Point and Minimum Threshold**

The TAS2110 also employs a Brown Out Prevention (BOP) feature that serves as a low latency priority input to the limiter engine that begins attacking the VBAT supply dipping below the programmed BOP threshold. This feature can be enabled by setting the *BOP\_EN* register bit high. It should be noted that the BOP feature is independent of the limiter and will function if enabled, even if the limiter is disabled. The BOP threshold is configured by setting the threshold with register bits *BOP\_TH*.



**Figure 46. Limiter Block Diagram**

**Table 58. Brown Out Prevention Enable**

| <i>BOP_EN</i> | VALUE             |
|---------------|-------------------|
| 0             | Disabled          |
| 1             | Enabled (default) |

The Brownout prevention threshold *BOP\_TH* represent a threshold in a 4.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation *BOP\_TH* = round(Volts\*2<sup>28</sup>).

**Table 59. Brown Out Prevention Threshold**

| <i>BOP_TH</i> [31:0]      | VBAT THRESHOLD (V) |
|---------------------------|--------------------|
| 0x0000 000 - 0x1FFF FFFF  | Reserved           |
| 0x2000 0000               | 2.5                |
| ...                       | ...                |
| 0x2E66 6666               | 2.9 (default)      |
| ...                       | ...                |
| 0x2000 0000               | 4                  |
| 0x2000 0001 - 0xFFFF FFFF | Reserved           |

The BOP feature has a separate attack rate *BOP\_ATK\_RT*, attack step size *BOP\_ATK\_ST* and hold time *BOP\_HLD\_TM* from the battery tracking limiter. The BOP feature uses the *LIMB\_RLS\_RT* register setting to release after a brown out event. The rates are based on the number of audio samples and actual time values can be calculated by multiplying by 1/fs. For example the attack rate of 4 samples at 48 ksp/s would be approximately 83  $\mu$ s.

**Table 60. Brown Out Prevention Attack Rate**

| <i>BOP_ATK_RT</i> [2:0] | ATTACK RATE (samples/step) | ATTACK RATE @ 48 ksp/s (~ $\mu$ s) |
|-------------------------|----------------------------|------------------------------------|
| 0x0                     | 1                          | 20                                 |
| 0x1                     | 2                          | 42                                 |
| 0x2                     | 4                          | 83                                 |
| 0x3                     | 8                          | 167                                |
| 0x4                     | 16                         | 333                                |
| 0x5                     | 32                         | 666                                |

**Table 60. Brown Out Prevention Attack Rate (continued)**

| <i>BOP_ATK_RT[2:0]</i> | ATTACK RATE (samples/step) | ATTACK RATE @ 48 ksps (~μs) |
|------------------------|----------------------------|-----------------------------|
| 0x6                    | 64                         | 1300                        |
| 0x7                    | 128                        | 2700                        |

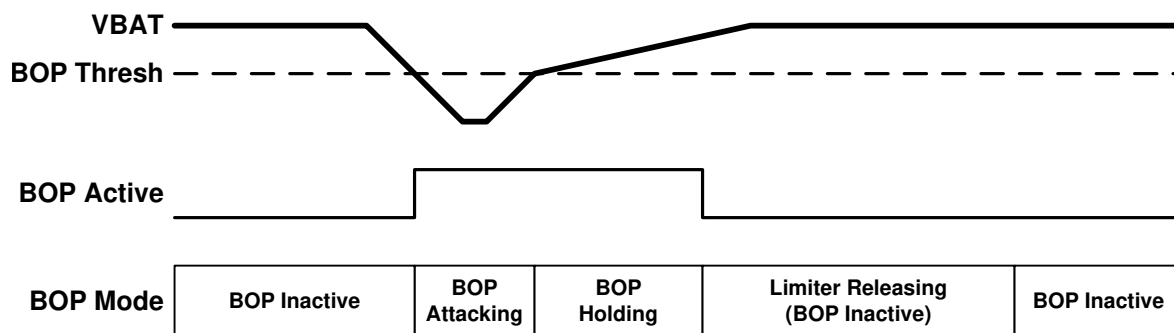
**Table 61. Brown Out Prevention Attack Step Size**

| <i>BOP_ATK_ST[1:0]</i> | STEP SIZE (dB) |
|------------------------|----------------|
| 00                     | 0.5            |
| 01                     | 1 (default)    |
| 10                     | 1.5            |
| 11                     | 2              |

**Table 62. Brown Out Prevention Hold Time**

| <i>BOP_HLD_TM[2:0]</i> | HOLD TIME (ms) |
|------------------------|----------------|
| 0x0                    | 0              |
| 0x1                    | 10             |
| 0x2                    | 25             |
| 0x3                    | 50             |
| 0x4                    | 100            |
| 0x5                    | 250            |
| 0x6                    | 500 (default)  |
| 0x7                    | 1000           |

The TAS2110 can also shutdown the device when a brown out event occurs if the *BOP\_MUTE* register bit is set high. For the device to continue playing audio again, the device must transition through a SW/HW shutdown state. Setting the *BOP\_INF\_HLD* high will cause the limiter to stay in the hold state (for example never release) after a cleared brown out event until either the device transitions through a mute or SW/HW shutdown state or the register bit *BOP\_HLD\_CLR* is written to a high value (which will cause the device to exit the hold state and begin releasing). This bit is self clearing and will always readback low. [Figure 47](#) below illustrates the entering and exiting from a brown out event.


**Figure 47. Brown Out Prevention Event**
**Table 63. Shutdown on Brown Out Event**

| <i>BOP_MUTE</i> | VALUE                    |
|-----------------|--------------------------|
| 0               | Don't Shutdown (default) |
| 1               | Mute then shutdown       |

**Table 64. Infinite Hold on Brown Out Event**

| <i>BOP_INF_HLD</i> | VALUE                                                    |
|--------------------|----------------------------------------------------------|
| 0                  | Use <i>BOP_HLD_TM</i> after Brown Out event (default)    |
| 1                  | Do not release until <i>BOP_HLD_CLR</i> is asserted high |

If the TAS2110 is configured to hold the brownout event until cleared the attenuation will remain until *BOP\_HLD\_CLR* register clear is performed. This should be performed by setting the *BOP\_HLR\_CLR* bit high, reading the register and then setting the *BOP\_HLD\_CLR* back to low.

**Table 65. BOP Infinite Hold Clear**

| <i>BOP_HLD_CLR</i> | VALUE                 |
|--------------------|-----------------------|
| 0                  | Don't clear (default) |
| 1                  | Clear event           |

A hard brownout level can be set to shutdown the TAS2110 if the BOP cannot mitigate the drop in battery voltage VBAT. This will shutdown the device and should not be used if the *BOP\_MUTE* is enable. The brownout shutdown will only function if brownout engine is enabled using *BOP\_EN*.

**Table 66. Brown Out Shutdown Enable**

| <i>BOSD_EN</i> | VALUE              |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

The Brownout prevention shutdown threshold *BOSD\_TH* represent a threshold in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation  $BOSD\_TH = \text{round}(\text{Volts} \times 2^{27})$ .

**Table 67. Brown Out Shutdown Threshold**

| <i>BOSD_TH</i> [31:0] | VBAT THRESHOLD (V) |
|-----------------------|--------------------|
| 0x2000 0000           | 2.5                |
| ...                   | ...                |
| 0x2B33 3333           | 2.7 (default)      |
| ...                   | ...                |
| 0x3FFF FFFF           | 3.99               |

#### 8.4.2.6 Inter Chip Limiter Alignment

##### 8.4.2.6.1 TDM Mode

The TAS2110 supports alignment of limiter (including brown out prevention) dynamics across devices that share the same TDM bus. This ensures consistent gain between channels during limiting or brown out events since these dynamics are dependent on audio content, which can vary across channels. Each device can be configured to align to a specified number of other devices, which allows creation of groupings of devices that align only to each other. All devices in the same group must use the same setting.

Limiter activity is communicated via the limiter gain reduction parameter that can be optionally transmitted by each device on SDOOUT in an 8-bit time slot. Gain reduction should be transmitted in adjacent time slots for all devices that are to be aligned beginning with the first slot that is specified by the *ICLA\_SLOT* register. The order of the devices is not important as long as they are adjacent. The time slot for limiter gain reduction is configured by the *GAIN\_SLOT* register and enabled by the *GAIN\_TX* register bit.

The *ICLA\_SEN* register specify which time slots should be listened to for gain alignment. This allows any number of devices between two and eight to be grouped together. At least two of these bits should be enabled for alignment to take place. The *ICLA\_USE\_MAX* register bit determines whether alignment is based on the maximum or minimum gain reduction value from the group of enabled devices. If the *BIL\_ICLA\_EN* is enabled the # of slots will be double what is selected. For example if time-slot 0,1, and 2 are used for gain alignment. Then time-slots 3, 4, and 5 will be used for brownout-current alignment.

To enable the inter chip limiter alignment feature, the *ICLA\_GAIN\_EN* register bit should be asserted high and all devices should be configured with identical limiter and brown out prevention settings. Limiter gain reduction transmission should be enabled on all devices as described above.

**Table 68. Inter Chip Limiter Alignment**

| <i>ICLA_GAIN_EN</i> | VALUE              |
|---------------------|--------------------|
| 0                   | Disabled (default) |
| 1                   | Enabled            |

**Table 69. ICLA Gain Alignment Configuration**

| <i>ICLA_MODE</i> | VALUE                                                      |
|------------------|------------------------------------------------------------|
| 00               | Use the maximum gain reduction of the ICLA group (default) |
| 01               | Use the minimum gain reduction of the ICLA group           |
| 10-11            | Reserved                                                   |

**Table 70. Inter Chip Limiter Gain Alignment Starting Time Slot**

| <i>ICLA_GAIN_SLOT[5:0]</i> | STARTING TIME SLOT |
|----------------------------|--------------------|
| 0x00                       | Time Slot 0        |
| 0x01                       | Time Slot 1        |
| 0x02                       | Time Slot 2        |
| ...                        | ...                |
| 0x3F                       | Time Slot 63       |

**Table 71. Inter Chip Limiter Alignment Time Slots Enable**

| REGISTER BIT            | DESCRIPTION                                                                                                          | BIT VALUE | STATE              |
|-------------------------|----------------------------------------------------------------------------------------------------------------------|-----------|--------------------|
| <i>ICLA_GAIN_SEN[0]</i> | Time Slot = <i>ICLA_GAIN_SLOT</i> . When enabled, the limiter will include this time slot in the alignment group.    | 0         | Disabled (default) |
|                         |                                                                                                                      | 1         | Enabled            |
| <i>ICLA_GAIN_SEN[1]</i> | Time Slot = <i>ICLA_GAIN_SLOT</i> + 1. When enabled, the limiter will include this time slot in the alignment group. | 0         | Disabled (default) |
|                         |                                                                                                                      | 1         | Enabled            |
| <i>ICLA_GAIN_SEN[2]</i> | Time Slot = <i>ICLA_GAIN_SLOT</i> + 2. When enabled, the limiter will include this time slot in the alignment group. | 0         | Disabled (default) |
|                         |                                                                                                                      | 1         | Enabled            |
| <i>ICLA_GAIN_SEN[3]</i> | Time Slot = <i>ICLA_GAIN_SLOT</i> + 3. When enabled, the limiter will include this time slot in the alignment group. | 0         | Disabled (default) |
|                         |                                                                                                                      | 1         | Enabled            |

#### 8.4.2.7 Class-D Settings

The TAS2110 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the *AMP\_SS* register bit high. This can help reduce EMI in some systems.

**Table 72. Low EMI Spread Spectrum Mode**

| <i>AMP_SS</i> | SPREAD SPECTRUM   |
|---------------|-------------------|
| 0             | Disabled          |
| 1             | Enabled (default) |

By default the Class-D amplifier's switching frequency is based on the device's trimmed internal oscillator. To synchronize switching to the audio sample rate, set the *CLASSD\_SYNC* register bit high. When the Class-D is synchronized to the audio sample rate, the *RATE\_RAMP* register bit must be set based whether the audio sample rate is based on a 44.1 kHz or 48 kHz frequency. For 44.1, 88.2 and 176.4 kHz, set this bit high. for 48, 96 and 192 kHz, set this bit low. This ensures that the internal ramp generator has the appropriate slope.

**Table 73. Class-D Synchronization Mode**

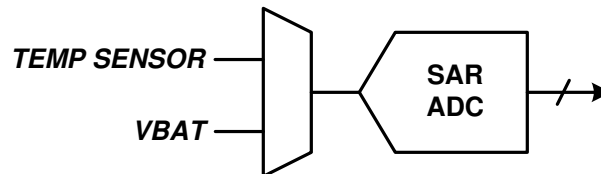
| <i>CLASSD_SYNC</i> | SYNCHRONIZATION MODE                       |
|--------------------|--------------------------------------------|
| 0                  | Not synchronized to audio clocks (default) |
| 1                  | Synchronized to audio clocks               |

**Table 74. Sample Rate for Class-D Synchronized Mode**

| <i>RAMP_RATE</i> | PLAYBACK SAMPLE RATE         |
|------------------|------------------------------|
| 0                | multiples of 48 kHz(default) |
| 1                | multiples of 44.1 kHz        |

### 8.4.3 SAR ADC

A 10-bit SAR ADC monitors VBAT voltage *VBAT\_CNV* and die temperature *TMP\_CNV*. VBAT voltage conversions are also used by the limiter and brown out prevention features.


**Figure 48. SAR Block Diagram**

Actual VBAT voltage is calculated by dividing the *VBAT\_CNV* register by 64. Actual die temperature is calculated by subtracting 93 from *TMP\_CNV* register. The battery voltage VBAT can be filtered using *VBAT\_FLT* register but will increase the latency. The *VBAT\_CNV* registers should be read *VBAT\_MSB* followed by *VBAT\_LSB*.

**Table 75. VBAT Filtering**

| <i>VBAT_FLT[0]</i> | FILTER POLE       |
|--------------------|-------------------|
| 0                  | 100 kHz (default) |
| 1                  | Bypass            |

**Table 76. ADC VBAT Voltage Conversion**

| <i>VBAT_CNV[9:0]</i> | VBAT VOLTAGE (V) |
|----------------------|------------------|
| 0x000                | 0 V              |
| 0x001                | 0.0156 V         |
| ...                  | ...              |
| 0x100                | 4.0 V            |
| ...                  | ...              |
| 0x17F                | 5.9844 V         |
| 0x180                | 6.0 V            |

**Table 77. ADC Die Temperature Conversion**

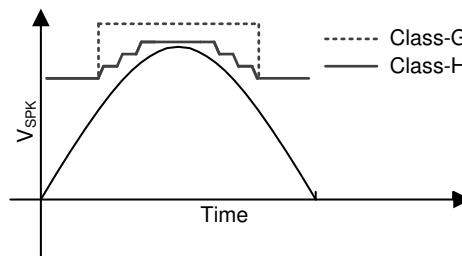
| <i>TMP_CNV[7:0]</i> | DIE TEMPERATURE (°C) |
|---------------------|----------------------|
| 0x00 - 0x52         | Invalid              |
| 0x53                | -40 °C               |

**Table 77. ADC Die Temperature Conversion (continued)**

| TMP_CNV[7:0] | DIE TEMPERATURE (°C) |
|--------------|----------------------|
| ...          | ...                  |
| 0x76         | 25 °C                |
| ...          | ...                  |
| 0xF3         | 150 °C               |
| 0xF4-0xFF    | Invalid              |

#### 8.4.4 Boost

The TAS2110 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using [Table 78](#).


**Figure 49. Boost Mode Signal Tracking Example**
**Table 78. Boost Mode**

| BST_MODE[1:0] | BOOST MODE                          |
|---------------|-------------------------------------|
| 00            | Class-H - High efficiency (default) |
| 01            | Class-G - Low in-rush               |
| 10            | Always On                           |
| 11            | Always Off - Pass-through           |

The boost can be enabled and disabled using *BST\_EN* register. When driving the Class-D amplifier using an external supply through the PVDD pin, the boost should be disabled and the VBST pin can be left floating. Do not drive an external voltage on the VBST pin. When supplying an external PVDD voltage the VBAT voltage must also be supplied to the device. While VBAT supply must be present it will not carry current to the speaker load.

**Table 79. Boost Enable**

| BST_EN | BOOST IS          |
|--------|-------------------|
| 0      | Disabled          |
| 1      | Enabled (default) |

**Table 80. Active Mode PFM Lower Frequency Limit**

| BST_PFML[1:0] | LOWER LIMIT (Hz) |
|---------------|------------------|
| 00            | No lower limit   |
| 01            | 25 kHz           |
| 10            | 50 kHz (default) |

**Table 80. Active Mode PFM Lower Frequency Limit (continued)**

| <i>BST_PFML[1:0]</i> | LOWER LIMIT (Hz) |
|----------------------|------------------|
| 11                   | 100 kHz          |

The boost has a soft-start to limit in-rush current during the initial charge. The current limit and soft-start timer are configurable to adjust to system component selection.

**Table 81. Soft-Start Current Limit**

| <i>BST_SSL[1:0]</i> | CURRENT LIMIT (A)             |
|---------------------|-------------------------------|
| 00                  | Disabled - Boost Normal Limit |
| 01                  | 1.0 A                         |
| 10                  | 1.5 A (default)               |
| 11                  | 2 A                           |

**Table 82. Class-G Soft-Start Timer**

| <i>BST_GSST[1:0]</i> | TIMEOUT (s)           |
|----------------------|-----------------------|
| 00                   | 1 * BST_HSTT          |
| 01                   | 2 * BST_HSTT          |
| 10                   | 4 * BST_HSTT(default) |
| 11                   | 8 * BST_HSTT          |

**Table 83. Class-H Soft-Start Timer**

| <i>BST_HSST[3:0]</i> | TIMEOUT (s)           |
|----------------------|-----------------------|
| 0x0                  | 9 $\mu$ S             |
| 0x1                  | 18 $\mu$ S            |
| 0x2                  | 36 $\mu$ S            |
| 0x3                  | 54 $\mu$ S            |
| 0x4                  | 72 $\mu$ S            |
| 0x5                  | 90 $\mu$ S            |
| 0x6                  | 108 $\mu$ S           |
| 0x7                  | 135 $\mu$ S (default) |
| 0x8                  | 162 $\mu$ S           |
| 0x9                  | 198 $\mu$ S           |
| 0xA                  | 252 $\mu$ S           |
| 0xB                  | 342 $\mu$ S           |
| 0xC                  | 477 $\mu$ S           |
| 0xD                  | 612 $\mu$ S           |
| 0xE                  | 792 $\mu$ S           |
| 0xF                  | 990 $\mu$ S           |

The boost inductor and decoupling capacitor range needs to be specified using *BST\_IR* and *BST\_LR* registers. These setting optimize the boost to ensure current limit accuracy and avoid clipping in class-H operation.

**Table 84. Boost Inductor Range**

| <i>BST_IR[1:0]</i> | INDUCTANCE (H)                    |
|--------------------|-----------------------------------|
| 00                 | < 0.6 $\mu$ H                     |
| 01                 | 0.6 $\mu$ H-1.3 $\mu$ H (default) |
| 10                 | 1.3 $\mu$ H - 2.5 $\mu$ H         |
| 11                 | Reserved                          |

**Table 85. Boost Load Regulation**

| BST_LR | VALUE                                |
|--------|--------------------------------------|
| 00     | Reserved                             |
| 01     | 3A/V; load regulation = 1V (default) |
| 10     | 2A/V; load regulation = 1.5V         |
| 11     | Reserved                             |

The maximum boost voltage regulation is set by BST\_VREG. When operating in class-G mode the boost when needed will be at this voltage. In class-H mode of operation the boost voltage is automatically selected based on the audio signal but, will not exceed this set value.

The peak current limits the boost current drawn from the VBAT supply. This setting allows flexibility in the inductor selection for various saturation currents. The current limit can be adjust in 45 mA steps with register BST\_ILIM[5:0]. The peak current limit setting is the maximum and may be temporarily reduced if the and ICLA current limit is active.

**Table 86. Peak Current Limit**

| BST_ILIM[5:0] | CURRENT (A)      |
|---------------|------------------|
| 0x00 - 0x08   | Reserved         |
| 0x09          | 1.48 A           |
| 0x0A          | 1.54 A           |
| ...           | ...              |
| 0x36          | 3.96 A (default) |
| 0x37          | 4 A              |
| 0x38 - 0x3F   | Reserved         |

For multiple parts the TAS2110 can shift the boost phase to ensure each device will contribute to the load sharing. The boost syncing among multiple devices is enabled using BST\_SYNC and then each part is configured to be on 0 or 180 phase using BST\_PA. This avoids peak current align on and clock edges and spreads out battery ripple. The phase of additional devices can be set relative to the master using register BST\_PA[1:0]. The phase align is performed over the Inter-chip Communication (ICC) bus and a slot for this feature needs to be configured if enabled.

**Table 87. Boost Sync**

| BST_SYNC |                      |
|----------|----------------------|
| 0        | Not Synced (default) |
| 1        | Synced to FSYNC      |

**Table 88. Boost Phase**

| BST_PA[0] | PHASE (Deg)   |
|-----------|---------------|
| 0         | ~0° (default) |
| 1         | ~180°         |

#### 8.4.5 Clocks and PLL

In TMD/I<sup>2</sup>C Mode, the device operates from SBCLK. [Table 89](#) and [Table 90](#) below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio (for 44.1 kHz and 48 kHz family frequencies respectively).

If the sample rate is properly configured via the SAMP\_RATE[1:0] bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts. After the clock error is detected the device will enter a low power halt mode after CLK\_HALT\_TIMER if CLK\_HALT\_EN is enabled. Additionally the device can automatically power up and down on valid clock signals if CLK\_ERR\_PWR\_EN is set. The device sampling rate should not be changed while this feature is enabled. Additionally, the CLK\_HALT\_EN should be set when CLK\_ERR\_PWR\_EN is set for this feature to work properly.

**Table 89. Supported SBCLK Frequencies (48 kHz based sample rates)**

| SAMPLE RATE (kHz) | SBCLK TO FSYNC RATIO |           |            |            |            |            |            |
|-------------------|----------------------|-----------|------------|------------|------------|------------|------------|
|                   | 64                   | 96        | 128        | 192        | 256        | 384        | 512        |
| 16 kHz            | 1.024 MHz            | 1.536 MHz | 2.048 MHz  | 3.072 MHz  | 4.096 MHz  | 6.144 MHz  | 8.192 MHz  |
| 32 kHz            | 2.048 MHz            | 3.072 MHz | 4.0960 MHz | 6.144 MHz  | 8.192 MHz  | 12.288 MHz | 16.384 MHz |
| 48 kHz            | 3.072 MHz            | 4.608 MHz | 6.144 MHz  | 9.216 MHz  | 12.288 MHz | 18.432 MHz | 24.576 MHz |
| 96 kHz            | 6.144 MHz            | 9.216 MHz | 12.288 MHz | 18.432 MHz | 24.576 MHz | -          | -          |

**Table 90. Supported SBCLK Frequencies (44.1 kHz based sample rates)**

| SAMPLE RATE (kHz) | SBCLK TO FSYNC RATIO |            |             |             |             |             |             |
|-------------------|----------------------|------------|-------------|-------------|-------------|-------------|-------------|
|                   | 64                   | 96         | 128         | 192         | 256         | 384         | 512         |
| 14.7 kHz          | 940.8 kHz            | 1.4112 MHz | 1.8816 MHz  | 2.8224 MHz  | 3.7632 MHz  | 5.6448 MHz  | 7.5264 MHz  |
| 29.4 kHz          | 1.8816 MHz           | 2.8224 MHz | 3.7632 MHz  | 5.6448 MHz  | 7.5264 MHz  | 11.2896 MHz | 15.0528 MHz |
| 44.1 kHz          | 2.8224 MHz           | 4.2336 MHz | 5.6448 MHz  | 8.4672 MHz  | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz |
| 88.2 kHz          | 5.6448 MHz           | 8.4672 MHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz | -           | -           |

**Table 91. Clock Power Up/Down on Valid ASI Clocks**

| CLK_ERR_PWR_EN | SETTING            |
|----------------|--------------------|
| 0              | Disabled (default) |
| 1              | Enabled            |

**Table 92. Clock Halt(Sleep) After Errors Longer Than Halt Timer**

| CLK_HALT_EN | SETTING           |
|-------------|-------------------|
| 0           | Enabled (default) |
| 1           | Disabled          |

**Table 93. Clock Halt Timer**

| CLK_HALT_TIMER[2:0] | SETTING            |
|---------------------|--------------------|
| 000                 | 1 ms               |
| 001                 | 3.27 ms            |
| 010                 | 26.21 ms           |
| 011                 | 52.42 ms (default) |
| 100                 | 104.85 ms          |
| 101                 | 209.71 ms          |
| 110                 | 419.43 ms          |
| 111                 | 838.86 ms          |

#### 8.4.6 Thermal Foldback

The TAS2110 monitors the die temperature and can automatically limit the audio signal when the die temperature reaches a set threshold. It is recommended to use [PurePath™ Console 3 Software](#) to configure the thermal foldback as the software will perform the necessary math for each register.

Thermal foldback can be disabled using *TF\_EN*. If the die temperature reaches *TF\_TEMP\_TH* this feature will begin to attenuate the audio signal to prevent the device from shutting down due to over-temperature. It will attenuate the audio signal by *TF\_LIMS* db per degree of temperature over *TF\_TEMP\_TH*. The thermal foldback with attack at a fixed rate of 0.25 dB per sample. A maximum attenuation of *TF\_MAX\_ATTN* can be specified. However if the device continue to heat up eventually the device over-temperature will be triggered. The attenuation will be held for *TF\_HOLD\_CNT* samples before the attenuation will begin releasing.

**Table 94. Thermal Foldback Enable**

| TF_EN | SETTING           |
|-------|-------------------|
| 0     | Disabled          |
| 1     | Enabled (default) |

**Table 95. Thermal Foldback Registers**

| REGISTER    | DESCRIPTION                                         | CALCULATION                                               |
|-------------|-----------------------------------------------------|-----------------------------------------------------------|
| TF_LIMS     | Thermal foldback limiter slope (in db/°C)           | $\text{round}(10^{(-\text{slope} / 20)} * 2^{31})$        |
| TF_HOLD_CNT | Thermal foldback hold count (samples)               | $\text{round}(\text{seconds} * 1000)$                     |
| TF_REL_RATE | Thermal foldback limiter release rate (db/samples)  | $\text{round}(10^{(\text{dB per sample} / 20)} * 2^{30})$ |
| TF_TEMP_TH  | Thermal foldback limiter temperature threshold (°C) | $\text{round}(\text{°C} * 2^{23})$                        |
| TF_MAX_ATTN | Thermal foldback max gain reduction (dB)            | $\text{round}(10^{(\text{max attn dB} / 20)} * 2^{31})$   |

#### 8.4.7 Internal Tone Generator

The TAS2110 has two internal tone generators that can be used for pilot tone, ultrasonic tone, or diagnostic purposes. It is recommended to use [PurePath™ Console 3 Software](#) to configure the tone generators as the software will perform the necessary math for each register.

The frequency and amplitude of each generator can be set independently. Each tone generator is enabled using TGx\_EN and will soft-ramp to the level set by registers TGx\_AMP if corresponding register TGx\_SR is set. The frequency using registers TGx\_FREQ and amplitude using registers TGx\_AMP. These amplitude and frequency should be set only when the tone generator is disabled. Additionally the first tone-generator can be configured to enable and disable the tone using a pin selected by TG1\_PINEN pin. When enabled the pin will be logically ORed with the TG1\_EN register to play the tone. This can be used for audible diagnostic tones or other alerting functions.

When the tone generator is configured to operate in pin-triggered mode, the sampling rate used in the TG1 equations should be 96 kHz. The range of frequencies that can be generated in this mode is 20 Hz to 38 kHz. For ASI bus sample rates of 192 kHz the tone generator 1 and 2 will run only at 96 kHz and this sampling rate should be used in the calculation. When not in pin trigger TG1 can generate tones up to fs/2.

The max frequency for tone generator 2 is based on the sampling rate and shown in [Table 102](#).

**Table 96. Tone Generator Clock Source**

| TG_CLK | SETTING                |
|--------|------------------------|
| 0      | External TDM (default) |
| 1      | Internal Oscillator    |

**Table 97. Tone Generator 1 Enable**

| TG1_EN | TONE GENERATOR OUTPUT            |
|--------|----------------------------------|
| 00     | disabled / pin trigger (default) |
| 01     | enabled - play tone always       |
| 10     | audio level enabled              |
| 11     | reserved                         |

**Table 98. Tone Generator 1 Pin Enable**

| TG1_PINEN[1:0] | TONE GENERATOR OUTPUT |
|----------------|-----------------------|
| 00             | disabled (default)    |
| 01             | SDIN pin              |
| 11             | AD1 pin               |

**Table 99. Tone Generator 1 Soft-Ramp**

| TG1_SR | SOFT RAMPUP       |
|--------|-------------------|
| 0      | disabled          |
| 1      | enabled (default) |

The pilot tone frequency and amplitude can be programmed using the following register. The equations are used to calculate the register settings for a given gain, frequency, and audio sampling rate.

fc = frequency of the tone

fs = sampling rate

$$TG1\_FREQ1[1-4] = 2 * \cos(2 * \pi * fc / fs)$$

$$TG1\_FREQ2[1-4] = \sin(2 * \pi * fc / fs)$$

$$TG1\_FREQ3[1-4] = (\text{lcm}(fs, fc) / fc) - 1$$

$$TG1\_AMP = 10 ^ { (dB/20)}$$

Equations for tone generator 2 are

$$TG2\_FREQ1[1-4] = 2 * \cos(2 * \pi * fc / (n*fs))$$

$$TG2\_FREQ2[1-4] = \sin(2 * \pi * fc / (n*fs))$$

$$TG2\_FREQ3[1-4] = (\text{lcm}(n*fs, fc) / fc) - n$$

$$TG2\_AMP = (10 ^ { (dB/20)}) / 4$$

**Table 100. Tone Generator Defaults**

| REGISTER       | DEFAULT VALUE | DEFAULT REGISTERVALUE |
|----------------|---------------|-----------------------|
| TG1_FREQ1[1-4] | 0             | 0x0000 0000           |
| TG1_FREQ2[1-4] | 0             | 0x0000 0000           |
| TG1_FREQ3[1-4] | 0             | 0x0000 0000           |
| TG1_AMP        | -40 dBFS      | 0x0147 AE14           |
| TG2_FREQ1[1-4] | 0             | 0x0000 0000           |
| TG2_FREQ2[1-4] | 0             | 0x0000 0000           |
| TG2_FREQ3[1-4] | 0             | 0x0000 0000           |
| TG2_AMP        | -12 dBFS      | 0x2026 F310           |

**Table 101. Tone Generator 2 Enable**

| TG2_EN | TONE GENERATOR OUTPUT |
|--------|-----------------------|
| 0      | disabled (default)    |
| 1      | enabled - play tone   |

**Table 102. Tone Generator 2 n Value and Range**

| fs             | n | MAX TONE FREQUENCY |
|----------------|---|--------------------|
| 96 kHz         | 1 | < fs /2            |
| 48 kHz, 32 kHz | 2 | < fs               |
| 24 kHz         | 4 | < 2*fs             |

**Table 102. Tone Generator 2 n Value and Range (continued)**

| fs            | n | MAX TONE FREQUENCY |
|---------------|---|--------------------|
| 16 kHz, 8 kHz | 8 | < 4 * fs           |

**Table 103. Tone Generator 2 Soft-Ramp**

| TG2_SR | SOFT RAMPUP       |
|--------|-------------------|
| 0      | disabled          |
| 1      | enabled (default) |

## 8.5 Register Maps

### 8.5.1 Register Summary Table Page=0x00

| Addr | Register       | Description                    | Section                                                            |
|------|----------------|--------------------------------|--------------------------------------------------------------------|
| 0x00 | PAGE0          | Device Page                    | <a href="#">PAGE0 (page=0x00 address=0x00) [reset=0h]</a>          |
| 0x01 | SW_RESET       | Software Reset                 | <a href="#">SW_RESET (page=0x00 address=0x01) [reset=0h]</a>       |
| 0x02 | PWR_CTL        | Power Control                  | <a href="#">PWR_CTL (page=0x00 address=0x02) [reset=Eh]</a>        |
| 0x03 | PB_CFG1        | Playback Configuration 1       | <a href="#">PB_CFG1 (page=0x00 address=0x03) [reset=20h]</a>       |
| 0x04 | MISC_CFG1      | Misc Configuration 1           | <a href="#">MISC_CFG1 (page=0x00 address=0x04) [reset=C6h]</a>     |
| 0x05 | MISC_CFG2      | Misc Configuration 2           | <a href="#">MISC_CFG2 (page=0x00 address=0x05) [reset=22h]</a>     |
| 0x06 | TDM_CFG0       | TDM Configuration 0            | <a href="#">TDM_CFG0 (page=0x00 address=0x06) [reset=9h]</a>       |
| 0x07 | TDM_CFG1       | TDM Configuration 1            | <a href="#">TDM_CFG1 (page=0x00 address=0x07) [reset=2h]</a>       |
| 0x08 | TDM_CFG2       | TDM Configuration 2            | <a href="#">TDM_CFG2 (page=0x00 address=0x08) [reset=Ah]</a>       |
| 0x09 | TDM_CFG3       | TDM Configuration 3            | <a href="#">TDM_CFG3 (page=0x00 address=0x09) [reset=10h]</a>      |
| 0x0A | TDM_CFG4       | TDM Configuration 4            | <a href="#">TDM_CFG4 (page=0x00 address=0x0A) [reset=13h]</a>      |
| 0x0D | TDM_CFG7       | TDM Configuration 7            | <a href="#">TDM_CFG7 (page=0x00 address=0x0D) [reset=4h]</a>       |
| 0x0E | TDM_CFG8       | TDM Configuration 8            | <a href="#">TDM_CFG8 (page=0x00 address=0x0E) [reset=5h]</a>       |
| 0x0F | TDM_CFG9       | TDM Configuration 9            | <a href="#">TDM_CFG9 (page=0x00 address=0x0F) [reset=6h]</a>       |
| 0x10 | TDM_CFG10      | TDM Configuration 10           | <a href="#">TDM_CFG10 (page=0x00 address=0x10) [reset=7h]</a>      |
| 0x11 | TDM_DET        | TDM Clock detection monitor    | <a href="#">TDM_DET (page=0x00 address=0x11) [reset=7Fh]</a>       |
| 0x12 | LIM_CFG_0      | Limiter Configuration 0        | <a href="#">LIM_CFG_0 (page=0x00 address=0x12) [reset=12h]</a>     |
| 0x13 | LIM_CFG_1      | Limiter Configuration 1        | <a href="#">LIM_CFG_1 (page=0x00 address=0x13) [reset=76h]</a>     |
| 0x14 | BOP_CFG_0      | Brown Out Prevention 0         | <a href="#">BOP_CFG_0 (page=0x00 address=0x14) [reset=1h]</a>      |
| 0x15 | BOP_CFG_1      | Brown Out Prevention 1         | <a href="#">BOP_CFG_1 (page=0x00 address=0x15) [reset=2Eh]</a>     |
| 0x16 | ICLA_CFG       | ICLA gain alignment mode       | <a href="#">ICLA_CFG (page=0x00 address=0x16) [reset=60h]</a>      |
| 0x18 | GAIN_ICLA_CFG0 | Inter Chip Limiter Alignment 0 | <a href="#">GAIN_ICLA_CFG0 (page=0x00 address=0x18) [reset=Ch]</a> |
| 0x19 | ICLA_CFG1      | Inter Chip Limiter Alignment 1 | <a href="#">ICLA_CFG1 (page=0x00 address=0x19) [reset=0h]</a>      |
| 0x1A | INT_MASK0      | Interrupt Mask 0               | <a href="#">INT_MASK0 (page=0x00 address=0x1A) [reset=FCh]</a>     |
| 0x1B | INT_MASK1      | Interrupt Mask 1               | <a href="#">INT_MASK1 (page=0x00 address=0x1B) [reset=A6h]</a>     |
| 0x1F | INT_LIVE0      | Live Interrupt Readback 0      | <a href="#">INT_LIVE0 (page=0x00 address=0x1F) [reset=0h]</a>      |
| 0x20 | INT_LIVE1      | Live Interrupt Readback 1      | <a href="#">INT_LIVE1 (page=0x00 address=0x20) [reset=0h]</a>      |
| 0x24 | INT_LTCH0      | Latched Interrupt Readback 0   | <a href="#">INT_LTCH0 (page=0x00 address=0x24) [reset=0h]</a>      |
| 0x25 | INT_LTCH1      | Latched Interrupt Readback 1   | <a href="#">INT_LTCH1 (page=0x00 address=0x25) [reset=0h]</a>      |
| 0x2A | VBAT_MSB       | SAR ADC Conversion 0           | <a href="#">VBAT_MSB (page=0x00 address=0x2A) [reset=0h]</a>       |
| 0x2B | VBAT_LSB       | SAR ADC Conversion 1           | <a href="#">VBAT_LSB (page=0x00 address=0x2B) [reset=0h]</a>       |
| 0x2C | TEMP           | SAR ADC Conversion 2           | <a href="#">TEMP (page=0x00 address=0x2C) [reset=0h]</a>           |
| 0x30 | INT_CLK        | Interrupt and Clock Error      | <a href="#">INT_CLK (page=0x00 address=0x30) [reset=19h]</a>       |
| 0x31 | DIN_PD         | Digital Input Pin Pull Down    | <a href="#">DIN_PD (page=0x00 address=0x31) [reset=40h]</a>        |
| 0x32 | MISC_CFG3      | Misc Configuration 3           | <a href="#">MISC_CFG3 (page=0x00 address=0x32) [reset=80h]</a>     |
| 0x33 | BOOST_CFG1     | Boost Configure 1              | <a href="#">BOOST_CFG1 (page=0x00 address=0x33) [reset=34h]</a>    |
| 0x34 | BOOST_CFG2     | Boost Configure 2              | <a href="#">BOOST_CFG2 (page=0x00 address=0x34) [reset=4Bh]</a>    |

## Register Maps (continued)

|      |            |                      |                                                                 |
|------|------------|----------------------|-----------------------------------------------------------------|
| 0x35 | BOOST_CFG3 | Boost Configure 3    | <a href="#">BOOST_CFG3 (page=0x00 address=0x35) [reset=74h]</a> |
| 0x3D | MISC_CFG4  | Misc Configuration 4 | <a href="#">MISC_CFG4 (page=0x00 address=0x3D) [reset=8h]</a>   |
| 0x3F | TG_CFG0    | Tone Generator       | <a href="#">TG_CFG0 (page=0x00 address=0x3F) [reset=0h]</a>     |
| 0x40 | BOOST_CFG4 | Boost Configure 4    | <a href="#">BOOST_CFG4 (page=0x00 address=0x40) [reset=36h]</a> |
| 0x7D | REV_ID     | Revision and PG ID   | <a href="#">REV_ID (page=0x00 address=0x7D) [reset=0h]</a>      |
| 0x7E | I2C_CKSUM  | I2C Checksum         | <a href="#">I2C_CKSUM (page=0x00 address=0x7E) [reset=0h]</a>   |
| 0x7F | BOOK       | Device Book          | <a href="#">BOOK (page=0x00 address=0x7F) [reset=0h]</a>        |

### 8.5.2 Register Summary Table Page=0x01

| Addr | Register | Description              | Section                                                       |
|------|----------|--------------------------|---------------------------------------------------------------|
| 0x00 | PAGE1    | Device Page              | <a href="#">PAGE1 (page=0x01 address=0x00) [reset=0h]</a>     |
| 0x08 | TF_CFG21 | Thermal Folder Configure | <a href="#">TF_CFG21 (page=0x01 address=0x08) [reset=40h]</a> |

### 8.5.3 Register Summary Table Page=0x02

| Addr | Register  | Description                                           | Section                                                        |
|------|-----------|-------------------------------------------------------|----------------------------------------------------------------|
| 0x00 | PAGE2     | Device Page                                           | <a href="#">PAGE2 (page=0x02 address=0x00) [reset=0h]</a>      |
| 0x0C | DVC_CFG1  | Digital Volume Control 1                              | <a href="#">DVC_CFG1 (page=0x02 address=0x0C) [reset=40h]</a>  |
| 0x0D | DVC_CFG2  | Digital Volume Control 2                              | <a href="#">DVC_CFG2 (page=0x02 address=0x0D) [reset=40h]</a>  |
| 0x0E | DVC_CFG3  | Digital Volume Control 3                              | <a href="#">DVC_CFG3 (page=0x02 address=0x0E) [reset=0h]</a>   |
| 0x0F | DVC_CFG4  | Digital Volume Control 4                              | <a href="#">DVC_CFG4 (page=0x02 address=0x0F) [reset=0h]</a>   |
| 0x10 | DVC_CFG5  | Digital Volume Control 5                              | <a href="#">DVC_CFG5 (page=0x02 address=0x10) [reset=3h]</a>   |
| 0x11 | DVC_CFG6  | Digital Volume Control 6                              | <a href="#">DVC_CFG6 (page=0x02 address=0x11) [reset=4Ah]</a>  |
| 0x12 | DVC_CFG7  | Digital Volume Control 7                              | <a href="#">DVC_CFG7 (page=0x02 address=0x12) [reset=6Ch]</a>  |
| 0x13 | DVC_CFG7  | Digital Volume Control 8                              | <a href="#">DVC_CFG7 (page=0x02 address=0x13) [reset=6Ch]</a>  |
| 0x14 | LIM_CFG1  | Limiter Configuration 1                               | <a href="#">LIM_CFG1 (page=0x02 address=0x14) [reset=2Dh]</a>  |
| 0x15 | LIM_CFG2  | Limiter Configuration 2- Sets limiter max attenuation | <a href="#">LIM_CFG2 (page=0x02 address=0x15) [reset=6Ah]</a>  |
| 0x16 | LIM_CFG3  | Limiter Configuration 3- Sets limiter max attenuation | <a href="#">LIM_CFG3 (page=0x02 address=0x16) [reset=86h]</a>  |
| 0x17 | LIM_CFG4  | Limiter Configuration 4- Sets limiter max attenuation | <a href="#">LIM_CFG4 (page=0x02 address=0x17) [reset=6Fh]</a>  |
| 0x18 | LIM_CFG5  | Limiter Configuration 5                               | <a href="#">LIM_CFG5 (page=0x02 address=0x18) [reset=47h]</a>  |
| 0x19 | LIM_CFG6  | Limiter Configuration 6                               | <a href="#">LIM_CFG6 (page=0x02 address=0x19) [reset=5Ch]</a>  |
| 0x1A | LIM_CFG7  | Limiter Configuration 7                               | <a href="#">LIM_CFG7 (page=0x02 address=0x1A) [reset=28h]</a>  |
| 0x1B | LIM_CFG8  | Limiter Configuration 8                               | <a href="#">LIM_CFG8 (page=0x02 address=0x1B) [reset=F6h]</a>  |
| 0x1C | LIM_CFG9  | Limiter Configuration 9                               | <a href="#">LIM_CFG9 (page=0x02 address=0x1C) [reset=16h]</a>  |
| 0x1D | LIM_CFG10 | Limiter Configuration 10                              | <a href="#">LIM_CFG10 (page=0x02 address=0x1D) [reset=66h]</a> |
| 0x1E | LIM_CFG11 | Limiter Configuration 11                              | <a href="#">LIM_CFG11 (page=0x02 address=0x1E) [reset=66h]</a> |
| 0x1F | LIM_CFG12 | Limiter Configuration 12                              | <a href="#">LIM_CFG12 (page=0x02 address=0x1F) [reset=66h]</a> |
| 0x20 | LIM_CFG13 | Limiter Configuration 13                              | <a href="#">LIM_CFG13 (page=0x02 address=0x20) [reset=34h]</a> |
| 0x21 | LIM_CFG14 | Limiter Configuration 14                              | <a href="#">LIM_CFG14 (page=0x02 address=0x21) [reset=CCh]</a> |
| 0x22 | LIM_CFG15 | Limiter Configuration 15                              | <a href="#">LIM_CFG15 (page=0x02 address=0x22) [reset=CCh]</a> |
| 0x23 | LIM_CFG16 | Limiter Configuration 16                              | <a href="#">LIM_CFG16 (page=0x02 address=0x23) [reset=CDh]</a> |
| 0x24 | LIM_CFG17 | Limiter Configuration 1                               | <a href="#">LIM_CFG17 (page=0x02 address=0x24) [reset=10h]</a> |
| 0x25 | LIM_CFG18 | Limiter Configuration 2                               | <a href="#">LIM_CFG18 (page=0x02 address=0x25) [reset=0h]</a>  |
| 0x26 | LIM_CFG19 | Limiter Configuration 3                               | <a href="#">LIM_CFG19 (page=0x02 address=0x26) [reset=0h]</a>  |
| 0x27 | LIM_CFG20 | Limiter Configuration 4                               | <a href="#">LIM_CFG20 (page=0x02 address=0x27) [reset=0h]</a>  |
| 0x28 | BOP_CFG1  | Brown Out Prevention 1                                | <a href="#">BOP_CFG1 (page=0x02 address=0x28) [reset=2Eh]</a>  |
| 0x29 | BOP_CFG2  | Brown Out Prevention 2                                | <a href="#">BOP_CFG2 (page=0x02 address=0x29) [reset=66h]</a>  |
| 0x2A | BOP_CFG3  | Brown Out Prevention 3                                | <a href="#">BOP_CFG3 (page=0x02 address=0x2A) [reset=66h]</a>  |
| 0x2B | BOP_CFG4  | Brown Out Prevention 4                                | <a href="#">BOP_CFG4 (page=0x02 address=0x2B) [reset=66h]</a>  |
| 0x2C | BOP_CFG5  | Brown Out Prevention 5                                | <a href="#">BOP_CFG5 (page=0x02 address=0x2C) [reset=2Bh]</a>  |

|      |            |                                             |                                                                 |
|------|------------|---------------------------------------------|-----------------------------------------------------------------|
| 0x2D | BOP_CFG6   | Brown Out Prevention 6                      | <a href="#">BOP_CFG6 (page=0x02 address=0x2D) [reset=33h]</a>   |
| 0x2E | BOP_CFG7   | Brown Out Prevention 7                      | <a href="#">BOP_CFG7 (page=0x02 address=0x2E) [reset=33h]</a>   |
| 0x2F | BOP_CFG8   | Brown Out Prevention 8                      | <a href="#">BOP_CFG8 (page=0x02 address=0x2F) [reset=33h]</a>   |
| 0x30 | HPFC_CFG1  | HPF Coefficient 1                           | <a href="#">HPFC_CFG1 (page=0x02 address=0x30) [reset=7Fh]</a>  |
| 0x31 | HPFC_CFG2  | HPF Coefficient 2                           | <a href="#">HPFC_CFG2 (page=0x02 address=0x31) [reset=FBh]</a>  |
| 0x32 | HPFC_CFG3  | HPF Coefficient 3                           | <a href="#">HPFC_CFG3 (page=0x02 address=0x32) [reset=B6h]</a>  |
| 0x33 | HPFC_CFG4  | HPF Coefficient 4                           | <a href="#">HPFC_CFG4 (page=0x02 address=0x33) [reset=14h]</a>  |
| 0x34 | HPFC_CFG5  | HPF Coefficient 5                           | <a href="#">HPFC_CFG5 (page=0x02 address=0x34) [reset=80h]</a>  |
| 0x35 | HPFC_CFG6  | HPF Coefficient 6                           | <a href="#">HPFC_CFG6 (page=0x02 address=0x35) [reset=4h]</a>   |
| 0x36 | HPFC_CFG7  | HPF Coefficient 7                           | <a href="#">HPFC_CFG7 (page=0x02 address=0x36) [reset=49h]</a>  |
| 0x37 | HPFC_CFG8  | HPF Coefficient 8                           | <a href="#">HPFC_CFG8 (page=0x02 address=0x37) [reset=ECh]</a>  |
| 0x38 | HPFC_CFG9  | HPF Coefficient 9                           | <a href="#">HPFC_CFG9 (page=0x02 address=0x38) [reset=7Fh]</a>  |
| 0x39 | HPFC_CFG10 | HPF Coefficient 10                          | <a href="#">HPFC_CFG10 (page=0x02 address=0x39) [reset=7Fh]</a> |
| 0x3A | HPFC_CFG11 | HPF Coefficient 11                          | <a href="#">HPFC_CFG11 (page=0x02 address=0x3A) [reset=6Ch]</a> |
| 0x3B | HPFC_CFG12 | HPF Coefficient 12                          | <a href="#">HPFC_CFG12 (page=0x02 address=0x3B) [reset=28h]</a> |
| 0x3C | TG_CFG1    | Tone Generator 1 Freq Calc 1                | <a href="#">TG_CFG1 (page=0x02 address=0x3C) [reset=3Fh]</a>    |
| 0x3D | TG_CFG2    | Tone Generator 1 Freq Calc 1                | <a href="#">TG_CFG2 (page=0x02 address=0x3D) [reset=FFh]</a>    |
| 0x3E | TG_CFG3    | Tone Generator 1 Freq Calc 1                | <a href="#">TG_CFG3 (page=0x02 address=0x3E) [reset=7Ah]</a>    |
| 0x3F | TG_CFG4    | Tone Generator 1 Freq Calc 1                | <a href="#">TG_CFG4 (page=0x02 address=0x3F) [reset=E3h]</a>    |
| 0x40 | TG_CFG5    | Tone Generator 1 Freq Calc 2                | <a href="#">TG_CFG5 (page=0x02 address=0x40) [reset=1h]</a>     |
| 0x41 | TG_CFG6    | Tone Generator 1 Freq Calc 2                | <a href="#">TG_CFG6 (page=0x02 address=0x41) [reset=1h]</a>     |
| 0x42 | TG_CFG7    | Tone Generator 1 Freq Calc 2                | <a href="#">TG_CFG7 (page=0x02 address=0x42) [reset=5Bh]</a>    |
| 0x43 | TG_CFG8    | Tone Generator 1 Freq Calc 2                | <a href="#">TG_CFG8 (page=0x02 address=0x43) [reset=4Ch]</a>    |
| 0x44 | TG_CFG9    | Tone Generator 1 Freq Calc 3                | <a href="#">TG_CFG9 (page=0x02 address=0x44) [reset=0h]</a>     |
| 0x45 | TG_CFG10   | Tone Generator 1 Freq Calc 3                | <a href="#">TG_CFG10 (page=0x02 address=0x45) [reset=0h]</a>    |
| 0x46 | TG_CFG11   | Tone Generator 1 Freq Calc 3                | <a href="#">TG_CFG11 (page=0x02 address=0x46) [reset=3h]</a>    |
| 0x47 | TG_CFG12   | Tone Generator 1 Freq Calc 3                | <a href="#">TG_CFG12 (page=0x02 address=0x47) [reset=1Fh]</a>   |
| 0x48 | TG_CFG13   | Tone Generator 1 Amplitude Calc             | <a href="#">TG_CFG13 (page=0x02 address=0x48) [reset=2h]</a>    |
| 0x49 | TG_CFG14   | Tone Generator 1 Amplitude Calc             | <a href="#">TG_CFG14 (page=0x02 address=0x49) [reset=46h]</a>   |
| 0x4A | TG_CFG15   | Tone Generator 1 Amplitude Calc             | <a href="#">TG_CFG15 (page=0x02 address=0x4A) [reset=B4h]</a>   |
| 0x4B | TG_CFG16   | Tone Generator 1 Amplitude Calc             | <a href="#">TG_CFG16 (page=0x02 address=0x4B) [reset=E4h]</a>   |
| 0x4C | TG_CFG17   | Tone Generator 2 Freq Calc 1                | <a href="#">TG_CFG17 (page=0x02 address=0x4C) [reset=E0h]</a>   |
| 0x4D | TG_CFG18   | Tone Generator 2 Freq Calc 1                | <a href="#">TG_CFG18 (page=0x02 address=0x4D) [reset=0h]</a>    |
| 0x4E | TG_CFG19   | Tone Generator 2 Freq Calc 1                | <a href="#">TG_CFG19 (page=0x02 address=0x4E) [reset=0h]</a>    |
| 0x4F | TG_CFG20   | Tone Generator 2 Freq Calc 1                | <a href="#">TG_CFG20 (page=0x02 address=0x4F) [reset=0h]</a>    |
| 0x50 | TG_CFG21   | Tone Generator 2 Freq Calc 2                | <a href="#">TG_CFG21 (page=0x02 address=0x50) [reset=6Eh]</a>   |
| 0x51 | TG_CFG22   | Tone Generator 2 Freq Calc 2                | <a href="#">TG_CFG22 (page=0x02 address=0x51) [reset=D9h]</a>   |
| 0x52 | TG_CFG23   | Tone Generator 2 Freq Calc 2                | <a href="#">TG_CFG23 (page=0x02 address=0x52) [reset=EBh]</a>   |
| 0x53 | TG_CFG24   | Tone Generator 2 Freq Calc 2                | <a href="#">TG_CFG24 (page=0x02 address=0x53) [reset=A1h]</a>   |
| 0x54 | TG_CFG25   | Tone Generator 2 Freq Calc 3                | <a href="#">TG_CFG25 (page=0x02 address=0x54) [reset=0h]</a>    |
| 0x55 | TG_CFG26   | Tone Generator 2 Freq Calc 3                | <a href="#">TG_CFG26 (page=0x02 address=0x55) [reset=0h]</a>    |
| 0x56 | TG_CFG27   | Tone Generator 2 Freq Calc 3                | <a href="#">TG_CFG27 (page=0x02 address=0x56) [reset=0h]</a>    |
| 0x57 | TG_CFG28   | Tone Generator 2 Freq Calc 3                | <a href="#">TG_CFG28 (page=0x02 address=0x57) [reset=2Ch]</a>   |
| 0x58 | TG_CFG29   | Tone Generator 2 Amplitude Calc             | <a href="#">TG_CFG29 (page=0x02 address=0x58) [reset=8h]</a>    |
| 0x59 | TG_CFG30   | Tone Generator 2 Amplitude Calc             | <a href="#">TG_CFG30 (page=0x02 address=0x59) [reset=9h]</a>    |
| 0x5A | TG_CFG31   | Tone Generator 2 Amplitude Calc             | <a href="#">TG_CFG31 (page=0x02 address=0x5A) [reset=BCh]</a>   |
| 0x5B | TG_CFG32   | Tone Generator 2 Amplitude Calc             | <a href="#">TG_CFG32 (page=0x02 address=0x5B) [reset=C4h]</a>   |
| 0x5C | LD_CFG0    | Load Diagnostics Resistance Upper Threshold | <a href="#">LD_CFG0 (page=0x02 address=0x5C) [reset=64h]</a>    |
| 0x5D | LD_CFG1    | Load Diagnostics Resistance Upper Threshold | <a href="#">LD_CFG1 (page=0x02 address=0x5D) [reset=0h]</a>     |
| 0x5E | LD_CFG2    | Load Diagnostics Resistance Upper Threshold | <a href="#">LD_CFG2 (page=0x02 address=0x5E) [reset=0h]</a>     |
| 0x5F | LD_CFG3    | Load Diagnostics Resistance Upper Threshold | <a href="#">LD_CFG3 (page=0x02 address=0x5F) [reset=0h]</a>     |
| 0x60 | LD_CFG4    | Load Diagnostics Resistance Lower Threshold | <a href="#">LD_CFG4 (page=0x02 address=0x60) [reset=0h]</a>     |
| 0x61 | LD_CFG5    | Load Diagnostics Resistance Lower Threshold | <a href="#">LD_CFG5 (page=0x02 address=0x61) [reset=80h]</a>    |
| 0x62 | LD_CFG6    | Load Diagnostics Resistance Lower Threshold | <a href="#">LD_CFG6 (page=0x02 address=0x62) [reset=0h]</a>     |

|      |           |                                             |                                                                |
|------|-----------|---------------------------------------------|----------------------------------------------------------------|
| 0x63 | LD_CFG7   | Load Diagnostics Resistance Lower Threshold | <a href="#">LD_CFG7 (page=0x02 address=0x63) [reset=0h]</a>    |
| 0x64 | IDC_CFG0  | Idle channel detection threshold            | <a href="#">IDC_CFG0 (page=0x02 address=0x64) [reset=0h]</a>   |
| 0x65 | IDC_CFG1  | Idle channel detection threshold            | <a href="#">IDC_CFG1 (page=0x02 address=0x65) [reset=20h]</a>  |
| 0x66 | IDC_CFG2  | Idle channel detection threshold            | <a href="#">IDC_CFG2 (page=0x02 address=0x66) [reset=C4h]</a>  |
| 0x67 | IDC_CFG3  | Idle channel detection threshold            | <a href="#">IDC_CFG3 (page=0x02 address=0x67) [reset=9Ch]</a>  |
| 0x6C | IDC_CFG7  | Hysteresis for idle channel detection       | <a href="#">IDC_CFG7 (page=0x02 address=0x6C) [reset=0h]</a>   |
| 0x6D | IDC_CFG8  | Hysteresis for idle channel detection       | <a href="#">IDC_CFG8 (page=0x02 address=0x6D) [reset=0h]</a>   |
| 0x6E | IDC_CFG9  | Hysteresis for idle channel detection       | <a href="#">IDC_CFG9 (page=0x02 address=0x6E) [reset=12h]</a>  |
| 0x6F | IDC_CFG10 | Hysteresis for idle channel detection       | <a href="#">IDC_CFG10 (page=0x02 address=0x6F) [reset=C0h]</a> |
| 0x7C | TF_CFG_1  | Thermal foldback limiter slope (in db/C)    | <a href="#">TF_CFG_1 (page=0x02 address=0x7C) [reset=72h]</a>  |
| 0x7D | TF_CFG_2  | Thermal foldback limiter slope (in db/C)    | <a href="#">TF_CFG_2 (page=0x02 address=0x7D) [reset=14h]</a>  |
| 0x7E | TF_CFG_3  | Thermal foldback limiter slope (in db/C)    | <a href="#">TF_CFG_3 (page=0x02 address=0x7E) [reset=82h]</a>  |
| 0x7F | TF_CFG_4  | Thermal foldback limiter slope (in db/C)    | <a href="#">TF_CFG_4 (page=0x02 address=0x7F) [reset=C0h]</a>  |

#### 8.5.4 Register Summary Table Page=0x04

| Addr | Register | Description                                               | Section                                                       |
|------|----------|-----------------------------------------------------------|---------------------------------------------------------------|
| 0x00 | PAGE4    | Device Page                                               | <a href="#">PAGE4 (page=0x04 address=0x00) [reset=0h]</a>     |
| 0x18 | LD_CFG8  | Load Resistance Value after load diagnostics is completed | <a href="#">LD_CFG8 (page=0x04 address=0x18) [reset=0h]</a>   |
| 0x19 | LD_CFG9  | Load Resistance Value after load diagnostics is completed | <a href="#">LD_CFG9 (page=0x04 address=0x19) [reset=0h]</a>   |
| 0x1A | LD_CFG10 | Load Resistance Value after load diagnostics is completed | <a href="#">LD_CFG10 (page=0x04 address=0x1A) [reset=0h]</a>  |
| 0x1B | LD_CFG11 | Load Resistance Value after load diagnostics is completed | <a href="#">LD_CFG11 (page=0x04 address=0x1B) [reset=0h]</a>  |
| 0x58 | TF_CFG4  | Thermal foldback hold count (samples)                     | <a href="#">TF_CFG4 (page=0x04 address=0x58) [reset=0h]</a>   |
| 0x59 | TF_CFG5  | Thermal foldback hold count (samples)                     | <a href="#">TF_CFG5 (page=0x04 address=0x59) [reset=0h]</a>   |
| 0x5A | TF_CFG6  | Thermal foldback hold count (samples)                     | <a href="#">TF_CFG6 (page=0x04 address=0x5A) [reset=0h]</a>   |
| 0x5B | TF_CFG7  | Thermal foldback hold count (samples)                     | <a href="#">TF_CFG7 (page=0x04 address=0x5B) [reset=64h]</a>  |
| 0x5C | TF_CFG8  | Thermal foldback limiter release rate (db/samples)        | <a href="#">TF_CFG8 (page=0x04 address=0x5C) [reset=40h]</a>  |
| 0x5D | TF_CFG9  | Thermal foldback limiter release rate (db/samples)        | <a href="#">TF_CFG9 (page=0x04 address=0x5D) [reset=BDh]</a>  |
| 0x5E | TF_CFG10 | Thermal foldback limiter release rate (db/samples)        | <a href="#">TF_CFG10 (page=0x04 address=0x5E) [reset=B7h]</a> |
| 0x5F | TF_CFG11 | Thermal foldback limiter release rate (db/samples)        | <a href="#">TF_CFG11 (page=0x04 address=0x5F) [reset=B0h]</a> |
| 0x60 | TF_CFG12 | Thermal foldback limiter temperature threshold            | <a href="#">TF_CFG12 (page=0x04 address=0x60) [reset=39h]</a> |
| 0x61 | TF_CFG13 | Thermal foldback limiter temperature threshold            | <a href="#">TF_CFG13 (page=0x04 address=0x61) [reset=82h]</a> |
| 0x62 | TF_CFG14 | Thermal foldback limiter temperature threshold            | <a href="#">TF_CFG14 (page=0x04 address=0x62) [reset=60h]</a> |
| 0x63 | TF_CFG16 | Thermal foldback limiter temperature threshold            | <a href="#">TF_CFG16 (page=0x04 address=0x63) [reset=7Fh]</a> |
| 0x64 | TF_CFG17 | Thermal foldback max gain reduction (dB)                  | <a href="#">TF_CFG17 (page=0x04 address=0x64) [reset=2Dh]</a> |
| 0x65 | TF_CFG18 | Thermal foldback max gain reduction (dB)                  | <a href="#">TF_CFG18 (page=0x04 address=0x65) [reset=6Ah]</a> |
| 0x66 | TF_CFG19 | Thermal foldback max gain reduction (dB)                  | <a href="#">TF_CFG19 (page=0x04 address=0x66) [reset=86h]</a> |
| 0x67 | TF_CFG20 | Thermal foldback max gain reduction (dB)                  | <a href="#">TF_CFG20 (page=0x04 address=0x67) [reset=6Fh]</a> |

### 8.5.5 PAGE0 (page=0x00 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

**Table 104. Device Page Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------|
| 7-0 | PAGE[7:0] | RW   | 0h    | Sets the device page.<br>00h = Page 0<br>01h = Page 1<br>...<br>FFh = Page 255 |

### 8.5.6 SW\_RESET (page=0x00 address=0x01) [reset=0h]

Asserting Software Reset will place all register values in their default POR (Power on Reset) state.

**Table 105. Software Reset Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                             |
|-----|----------|------|-------|-------------------------------------------------------------------------|
| 7-1 | Reserved | R    | 0h    | Reserved                                                                |
| 0   | SW_RESET | RW   | 0h    | Software reset. Bit is self clearing.<br>0b = Don't reset<br>1b = Reset |

### 8.5.7 PWR\_CTL (page=0x00 address=0x02) [reset=Eh]

Sets device's mode of operation and power down of IV sense blocks.

**Table 106. Power Control Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                 |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 7   | Reserved  | R    | 0h    | Reserved                                                                                                    |
| 6   | LDG_MODE  | RW   | 0h    | Load Diagnostic is<br>0b = Not Running<br>1b = Running (self clearing)                                      |
| 5   | Reserved  | RW   | 0h    | Reserved                                                                                                    |
| 4   | Reserved  | RW   | 0h    | Reserved                                                                                                    |
| 3   | Reserved  | RW   | 1h    | Reserved                                                                                                    |
| 2   | Reserved  | RW   | 1h    | Reserved                                                                                                    |
| 1-0 | MODE[1:0] | RW   | 2h    | Device operational mode.<br>00b = Active<br>01b = Mute<br>10b = Software Shutdown<br>11b = Load Diagnostics |

### 8.5.8 PB\_CFG1 (page=0x00 address=0x03) [reset=20h]

Sets playback high pass filter corner (PCM playback only).

**Table 107. Playback Configuration 1 Field Descriptions**

| Bit | Field    | Type | Reset | Description                                         |
|-----|----------|------|-------|-----------------------------------------------------|
| 7   | Reserved | R    | 0h    | Reserved                                            |
| 6   | HPF_EN   | RW   | 0h    | Disable DC Blocker<br>0b = Enabled<br>1b = Disabled |

**Table 107. Playback Configuration 1 Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5-1 | AMP_LEVEL[4:0] | RW   | 10h   | 15h-1Fh - Reserved<br>01h = 8.5 dBV(3.76Vpk)<br>02h = 9.0 dBV(3.99Vpk)<br>03h = 9.5 dBV(4.22Vpk)<br>04h = 10.0 dBV(4.47Vpk)<br>05h = 10.5 dBV(4.74Vpk)<br>06h = 11.0 dBV (5.02 Vpk)<br>07h = 11.5 dBV (5.32 Vpk)<br>08h = 12.0 dBV (5.63 Vpk)<br>09h = 12.5 dBV (5.96 Vpk)<br>0Ah = 13.0 dBV (6.32 Vpk)<br>0Bh = 13.5 dBV (6.69 Vpk)<br>0Ch = 14.0 dBV (7.09 Vpk)<br>0Dh = 14.5 dBV (7.51 Vpk)<br>0Eh = 15.0 dBV (7.95 Vpk)<br>0Fh = 15.5 dBV (8.42 Vpk)<br>10h = 16.0 dBV (8.92 Vpk)<br>11h = 16.5 dBV (9.45 Vpk)<br>12h = 17.0 dBV (10.01 Vpk)<br>13h = 17.5 dBV (10.61 Vpk)<br>14h = 18.0 dBV (11.23 Vpk)<br>15h = Reserved<br>16h = Reserved<br>17h = Reserved<br>18h = Reserved<br>19h = Reserved<br>1Ah = Reserved<br>1Bh = Reserved<br>15h-1Fh - Reserved |
| 0   | Reserved       | RW   | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

### 8.5.9 MISC\_CFG1 (page=0x00 address=0x04) [reset=C6h]

Sets OTE/OCE retry, IRQZ pull up, and amp spread spectrum.

**Table 108. Misc Configuration 1 Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                        |
|-----|-----------|------|-------|------------------------------------------------------------------------------------|
| 7   | Reserved  | RW   | 1h    | Reserved                                                                           |
| 6   | Reserved  | RW   | 1h    | Reserved                                                                           |
| 5   | OCE_RETRY | RW   | 0h    | Retry after over current event.<br>0b = Do not retry<br>1b = Retry after 1.5 s     |
| 4   | OTE_RETRY | RW   | 0h    | Retry after over temperature event.<br>0b = Do not retry<br>1b = Retry after 1.5 s |
| 3   | IRQZ_PU   | RW   | 0h    | IRQZ internal pull up enable.<br>0b = Disabled<br>1b = Enabled                     |
| 2   | AMP_SS    | RW   | 1h    | Low EMI spread spectrum enable.<br>0b = Disabled<br>1b = Enabled                   |
| 1-0 | Reserved  | RW   | 2h    | Reserved                                                                           |

### 8.5.10 MISC\_CFG2 (page=0x00 address=0x05) [reset=22h]

Set shutdown, VBAT filter, and I2C options.

**Table 109. Misc Configuration 2 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                |
|-----|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | SDZ_MODE[1:0]    | RW   | 0h    | SDZ Mode configuration.<br>00b = Initiates normal shutdown; force shutdown after timeout<br>01b = Immediate force shutdown<br>10b = Normal shutdown only<br>11b = Reserved |
| 5-4 | SDZ_TIMEOUT[1:0] | RW   | 2h    | SDZ Timeout value<br>00b = 2 ms<br>01b = 4 ms<br>10b = 6 ms<br>11b = 23.8 ms                                                                                               |
| 3   | Reserved         | RW   | 0h    | Reserved                                                                                                                                                                   |
| 2   | VBAT_FLT         | RW   | 0h    | VBAT filter into SAR ADC.<br>0b = 100kHz cut off<br>1b = Bypass                                                                                                            |
| 1   | I2C_GBL_EN       | RW   | 1h    | I2C global address is<br>0b = Disabled<br>1b = Enabled                                                                                                                     |
| 0   | I2C_AD_DET       | RW   | 0h    | Re-detect I2C slave address (self clearing bit).<br>0b = normal<br>1b = Re-detect address                                                                                  |

### 8.5.11 TDM\_CFG0 (page=0x00 address=0x06) [reset=9h]

Sets the TDM frame start, TDM sample rate, TDM auto rate detection and whether rate is based on 44.1 kHz or 48 kHz frequency.

**Table 110. TDM Configuration 0 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                                                                                                                                                                   |
| 6   | CLASSD_SYNC    | RW   | 0h    | Class-D synchronization mode.<br>0b = Not synchronized to audio clocks<br>1b = Synchronized to audio clocks                                                                                                |
| 5   | RAMP_RATE      | RW   | 0h    | Sample rate based on 44.1kHz or 48kHz when CLASSD_SYNC=1.<br>0b = 48kHz<br>1b = 44.1kHz                                                                                                                    |
| 4   | AUTO_RATE      | RW   | 0h    | Auto detection of TDM sample rate.<br>0b = Enabled<br>1b = Disabled                                                                                                                                        |
| 3-1 | SAMP_RATE[2:0] | RW   | 4h    | Sample rate of the TDM bus.<br>000b = 7.35/8 kHz<br>001b = 14.7/16 kHz<br>010b = 22.05/24 kHz<br>011b = 29.4/32 kHz<br>100b = 44.1/48 kHz<br>101b = 88.2/96 kHz<br>110b = 176.4/192 kHz<br>111b = Reserved |
| 0   | FRAME_START    | RW   | 1h    | TDM frame start polarity.<br>0b = Low to High on FSYNC<br>1b = High to Low on FSYNC                                                                                                                        |

### 8.5.12 TDM\_CFG1 (page=0x00 address=0x07) [reset=2h]

Sets TDM RX justification, offset and capture edge.

**Table 111. TDM Configuration 1 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                               |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                                                  |
| 6   | RX_JUSTIFY     | RW   | 0h    | TDM RX sample justification within the time slot.<br>0b = Left<br>1b = Right              |
| 5-1 | RX_OFFSET[4:0] | RW   | 1h    | TDM RX start of frame to time slot 0 offset (SBCLK cycles).                               |
| 0   | RX_EDGE        | RW   | 0h    | TDM RX capture clock polarity.<br>0b = Rising edge of SBCLK<br>1b = Falling edge of SBCLK |

### 8.5.13 TDM\_CFG2 (page=0x00 address=0x08) [reset=Ah]

Sets TDM RX time slot select, word length and time slot length.

**Table 112. TDM Configuration 2 Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                     |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | Reserved     | RW   | 0h    | Reserved                                                                                                                                                                        |
| 5-4 | RX_SCFG[1:0] | RW   | 0h    | TDM RX time slot select config.<br>00b = Mono with time slot equal to I2C address offset<br>01b = Mono left channel<br>10b = Mono right channel<br>11b = Stereo downmix (L+R)/2 |
| 3-2 | RX_WLEN[1:0] | RW   | 2h    | TDM RX word length.<br>00b = 16-bits<br>01b = 20-bits<br>10b = 24-bits<br>11b = 32-bits                                                                                         |
| 1-0 | RX_SLEN[1:0] | RW   | 2h    | TDM RX time slot length.<br>00b = 16-bits<br>01b = 24-bits<br>10b = 32-bits<br>11b = Reserved                                                                                   |

### 8.5.14 TDM\_CFG3 (page=0x00 address=0x09) [reset=10h]

Sets TDM RX left and right time slots.

**Table 113. TDM Configuration 3 Field Descriptions**

| Bit | Field          | Type | Reset | Description                     |
|-----|----------------|------|-------|---------------------------------|
| 7-4 | RX_SLOT_R[3:0] | RW   | 1h    | TDM RX Right Channel Time Slot. |
| 3-0 | RX_SLOT_L[3:0] | RW   | 0h    | TDM RX Left Channel Time Slot.  |

### 8.5.15 TDM\_CFG4 (page=0x00 address=0x0A) [reset=13h]

Sets TDM TX bus keeper, fill, offset and transmit edge.

**Table 114. TDM Configuration 4 Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                      |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------|
| 7   | TX_KEEPCY | RW   | 0h    | TDM TX SDOUT LSB data will be driven for<br>0b = full-cycle<br>1b = half-cycle                                   |
| 6   | TX_KEEPLN | RW   | 0h    | TDM TX SDOUT will hold the bus for the following when<br>TX_KEEPCY is enabled<br>0b = 1 LSB cycle<br>1b = always |

**Table 114. TDM Configuration 4 Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                              |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------|
| 5   | TX_KEEPE       | RW   | 0h    | TDM TX SDOOUT bus keeper enable.<br>0b = Disable bus keeper<br>1b = Enable bus keeper    |
| 4   | TX_FILL        | RW   | 1h    | TDM TX SDOOUT unused bitfield fill.<br>0b = Transmit 0<br>1b = Transmit Hi-Z             |
| 3-1 | TX_OFFSET[2:0] | RW   | 1h    | TDM TX start of frame to time slot 0 offset.                                             |
| 0   | TX_EDGE        | RW   | 1h    | TDM TX launch clock polarity.<br>0b = Rising edge of SBCLK<br>1b = Falling edge of SBCLK |

#### 8.5.16 TDM\_CFG7 (page=0x00 address=0x0D) [reset=4h]

Sets TDM TX VBAT time slot and enable.

**Table 115. TDM Configuration 7 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                              |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------|
| 7   | VBAT_SLEN      | RW   | 0h    | TDM TX VBAT time slot length.<br>0b = Truncate to 8-bits<br>1b = Left justify to 16-bits |
| 6   | VBAT_TX        | RW   | 0h    | TDM TX VBAT transmit enable.<br>0b = Disabled<br>1b = Enabled                            |
| 5-0 | VBAT_SLOT[5:0] | RW   | 4h    | TDM TX VBAT time slot.                                                                   |

#### 8.5.17 TDM\_CFG8 (page=0x00 address=0x0E) [reset=5h]

Sets TDM TX temp time slot and enable.

**Table 116. TDM Configuration 8 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                          |
|-----|----------------|------|-------|----------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                             |
| 6   | TEMP_TX        | RW   | 0h    | TDM TX temp sensor transmit enable.<br>0b = Disabled<br>1b = Enabled |
| 5-0 | TEMP_SLOT[5:0] | RW   | 5h    | TDM TX temp sensor time slot.                                        |

#### 8.5.18 TDM\_CFG9 (page=0x00 address=0x0F) [reset=6h]

Sets ICLA bus, TDM TX limiter gain reduction time slot and enable.

**Table 117. TDM Configuration 9 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                     |
|-----|----------------|------|-------|---------------------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                                        |
| 6   | GAIN_TX        | RW   | 0h    | TDM TX limiter gain reduction transmit enable.<br>0b = Disabled<br>1b = Enabled |
| 5-0 | GAIN_SLOT[5:0] | RW   | 6h    | TDM TX limiter gain reduction time slot.                                        |

### 8.5.19 TDM\_CFG10 (page=0x00 address=0x10) [reset=7h]

Sets boost current limiter slot and enable

**Table 118. TDM Configuration 10 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                           |
|-----|---------------|------|-------|-----------------------------------------------------------------------|
| 7   | BST_TX        | RW   | 0h    | TDM TX boost current limiter enable.<br>0b = Disabled<br>1b = Enabled |
| 6   | BST_SYNC_TX   | RW   | 0h    | TDM TX boost clock sync enable.<br>0b = Disabled<br>1b = Enabled      |
| 5-0 | BST_SLOT[5:0] | RW   | 7h    | TDM TX boost sync and current limit time slot.                        |

### 8.5.20 TDM\_DET (page=0x00 address=0x11) [reset=7Fh]

Readback of internal auto-rate detection.

**Table 119. TDM Clock detection monitor Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                            |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved      | R    | 0h    | Reserved                                                                                                                                                                                                               |
| 6-3 | FS_RATIO[3:0] | R    | Fh    | Detected SBCLK to FSYNC ratio.<br>00h = 16<br>01h = 24<br>02h = 32<br>03h = 48<br>04h = 64<br>05h = 96<br>06h = 128<br>07h = 192<br>08h = 256<br>09h = 384<br>0Ah = 512<br>0Bh-0Eh = Reserved<br>0F = Invalid ratio    |
| 2-0 | FS_RATE[2:0]  | R    | 7h    | Detected sample rate of TDM bus.<br>000b = 7.35/8 KHz<br>001b = 14.7/16 KHz<br>010b = 22.05/24 KHz<br>011b = 29.4/32 KHz<br>100b = 44.1/48 KHz<br>101b = 88.2/96 KHz<br>110b = 176.4/192 KHz<br>111b = Error condition |

### 8.5.21 LIM\_CFG\_0 (page=0x00 address=0x12) [reset=12h]

Sets Limiter attack step size, attack rate and enable.

**Table 120. Limiter Configuration 0 Field Descriptions**

| Bit | Field                 | Type | Reset | Description                                                                                                         |
|-----|-----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved              | R    | 0h    | Reserved                                                                                                            |
| 6   | VBAT_LIM_TH_SELECTION | RW   | 0h    | Select source of threshold for VBAT based limiting<br>0b = User configured Thresholds<br>1b = PVDD based thresholds |
| 5-4 | LIMB_ATK_ST[1:0]      | RW   | 1h    | VBAT Limiter/ICLA attack step size.<br>00b = 0.25 dB<br>01b = 0.5 dB<br>10b = 1 dB<br>11b = 2 dB                    |

**Table 120. Limiter Configuration 0 Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3-1 | LIMB_ATK_RT[2:0] | RW   | 1h    | VBAT Limiter/ICLA attack rate.<br>000b = 1 step in 1 sample<br>001b = 1 step in 2 samples<br>010b = 1 step in 4 samples<br>011b = 1 step in 8 samples<br>100b = 1 step in 16 samples<br>101b = 1 step in 32 samples<br>110b = 1 step in 64 samples<br>111b = 1 step in 128 samples |
| 0   | LIMB_EN          | RW   | 0h    | Limiter enable.<br>0b = Disabled<br>1b = Enabled                                                                                                                                                                                                                                   |

### 8.5.22 LIM\_CFG\_1 (page=0x00 address=0x13) [reset=76h]

Sets VBAT limiter release step size, release rate and hold time.

**Table 121. Limiter Configuration 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                      |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | LIMB_RLS_ST[1:0] | RW   | 1h    | VBAT Limiter/BOP/ICLA release step size.<br>00b = 0.25 dB<br>01b = 0.5 dB<br>10b = 1 dB<br>11b = 2 dB                                                                                                                                                                                            |
| 5-3 | LIMB_RLS_RT[2:0] | RW   | 6h    | VBAT Limiter/BOP/ICLA release rate.<br>000b = 1 step in 10 samples<br>001b = 1 step in 20 samples<br>010b = 1 step in 40 samples<br>011b = 1 step in 80 samples<br>100b = 1 step in 160 samples<br>101b = 1 step in 320 samples<br>110b = 1 step in 640 samples<br>111b = 1 step in 1280 samples |
| 2-0 | LIMB_HLD_TM[2:0] | RW   | 6h    | VBAT Limiter hold time in samples.<br>000b = 0 samples<br>001b = 1920 samples<br>010b = 4800 samples<br>011b = 9600 samples<br>100b = 19200 samples<br>101b = 48000 samples<br>110b = 96000 samples<br>111b = 192000 samples                                                                     |

### 8.5.23 BOP\_CFG\_0 (page=0x00 address=0x14) [reset=1h]

Sets BOP infinite hold clear, infinite hold enable, mute on brown out and enable.

**Table 122. Brown Out Prevention 0 Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                             |
|-----|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 7-5 | Reserved    | R    | 0h    | Reserved                                                                                                                                |
| 4   | BOSD_EN     | RW   | 0h    | Brown out prevention shutdown enable.<br>0b = Disabled<br>1b = Enabled                                                                  |
| 3   | BOP_HLD_CLR | RW   | 0h    | BOP infinite hold clear (self clearing).<br>0b = Don't clear<br>1b = Clear                                                              |
| 2   | BOP_INF_HLD | RW   | 0h    | Infinite hold on brown out event.<br>0b = Use BOP_HLD_TM after brown out event<br>1b = Don't release until BOP_HLD_CLR is asserted high |

**Table 122. Brown Out Prevention 0 Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                          |
|-----|----------|------|-------|--------------------------------------------------------------------------------------|
| 1   | BOP_MUTE | RW   | 0h    | Mute on brown out event.<br>0b = Don't mute<br>1b = Mute followed by device shutdown |
| 0   | BOP_EN   | RW   | 1h    | Brown out prevention enable.<br>0b = Disabled<br>1b = Enabled                        |

#### 8.5.24 BOP\_CFG\_1 (page=0x00 address=0x15) [reset=2Eh]

BOP attack rate, attack step size and hold time.

**Table 123. Brown Out Prevention 1 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-----|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-5 | BOP_ATK_RT[2:0] | RW   | 1h    | Brown out prevention attack rate.<br>000b = 1 step in 1 sample<br>001b = 1 step in 2 samples<br>010b = 1 step in 4 samples<br>011b = 1 step in 8 samples<br>100b = 1 step in 16 samples<br>101b = 1 step in 32 samples<br>110b = 1 step in 64 samples<br>111b = 1 step in 128 samples |
| 4-3 | BOP_ATK_ST[1:0] | RW   | 1h    | Brown out prevention attack step size.<br>00b = 0.5 dB<br>01b = 1 dB<br>10b = 1.5 dB<br>11b = 2 dB                                                                                                                                                                                    |
| 2-0 | BOP_HLD_TM[2:0] | RW   | 6h    | Brown out prevention hold time.<br>000b = 0 ms<br>001b = 10 ms<br>010b = 25 ms<br>011b = 50 ms<br>100b = 100 ms<br>101b = 250 ms<br>110b = 500 ms<br>111b = 1000 ms                                                                                                                   |

#### 8.5.25 ICLA\_CFG (page=0x00 address=0x16) [reset=60h]

ICLA gain alignment mode

**Table 124. ICLA gain alignment mode Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                     |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                                                                                                                                                        |
| 6-4 | Reserved       | RW   | 6h    | Reserved                                                                                                                                                                                        |
| 3-2 | ICLA_MODE[1:0] | RW   | 0h    | Inter chip limiter alignment gain mode.<br>00b = Use the maximum of the ICLA group gain reduction<br>01b = Use the minimum of the ICLA group gain reduction<br>10b = Reserved<br>11b = Reserved |
| 1-0 | Reserved       | R    | 0h    | Reserved                                                                                                                                                                                        |

#### 8.5.26 GAIN\_ICLA\_CFG0 (page=0x00 address=0x18) [reset=Ch]

ICLA starting time slot and enable.

**Table 125. Inter Chip Limiter Alignment 0 Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7   | Reserved | R    | 0h    | Reserved    |

**Table 125. Inter Chip Limiter Alignment 0 Field Descriptions (continued)**

| Bit | Field               | Type | Reset | Description                                                                |
|-----|---------------------|------|-------|----------------------------------------------------------------------------|
| 6-1 | ICLA_GAIN_SLOT[5:0] | RW   | 6h    | Inter chip limiter alignment gain starting time slot.                      |
| 0   | ICLA_GAIN_EN        | RW   | 0h    | Inter chip limiter alignment gain enable.<br>0b = Disabled<br>1b = Enabled |

### 8.5.27 ICLA\_CFG1 (page=0x00 address=0x19) [reset=0h]

ICLA time slot enables.

**Table 126. Inter Chip Limiter Alignment 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ICLA_GAIN_SEN[3] | RW   | 0h    | Time slot equals ICLA_GAIN_SLOT[5:0]+3. When enabled, the limiter will include this time slot in the alignment group.<br>0b = Disabled<br>1b = Enabled |
| 6   | ICLA_GAIN_SEN[2] | RW   | 0h    | Time slot equals ICLA_GAIN_SLOT[5:0]+2. When enabled, the limiter will include this time slot in the alignment group.<br>0b = Disabled<br>1b = Enabled |
| 5   | ICLA_GAIN_SEN[1] | RW   | 0h    | Time slot equals ICLA_GAIN_SLOT[5:0]+1. When enabled, the limiter will include this time slot in the alignment group.<br>0b = Disabled<br>1b = Enabled |
| 4   | ICLA_GAIN_SEN[0] | RW   | 0h    | Time slot equals ICLA_GAIN_SLOT[5:0]+0. When enabled, the limiter will include this time slot in the alignment group.<br>0b = Disabled<br>1b = Enabled |
| 3   | Reserved         | RW   | 0h    | Reserved                                                                                                                                               |
| 2   | Reserved         | RW   | 0h    | Reserved                                                                                                                                               |
| 1   | Reserved         | RW   | 0h    | Reserved                                                                                                                                               |
| 0   | Reserved         | RW   | 0h    | Reserved                                                                                                                                               |

### 8.5.28 INT\_MASK0 (page=0x00 address=0x1A) [reset=FCh]

Interrupt masks.

**Table 127. Interrupt Mask 0 Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                               |
|-----|-------------|------|-------|---------------------------------------------------------------------------|
| 7   | INT_MASK[7] | RW   | 1h    | Limiter mute mask.<br>0b = Don't Mask<br>1b = Mask                        |
| 6   | INT_MASK[6] | RW   | 1h    | Limiter infinite hold mask.<br>0b = Don't Mask<br>1b = Mask               |
| 5   | INT_MASK[5] | RW   | 1h    | Limiter max attenuation mask.<br>0b = Don't Mask<br>1b = Mask             |
| 4   | INT_MASK[4] | RW   | 1h    | VBAT below limiter inflection point mask.<br>0b = Don't Mask<br>1b = Mask |
| 3   | INT_MASK[3] | RW   | 1h    | Limiter active mask.<br>0b = Don't Mask<br>1b = Mask                      |
| 2   | INT_MASK[2] | RW   | 1h    | TDM clock error mask.<br>0b = Don't Mask<br>1b = Mask                     |

**Table 127. Interrupt Mask 0 Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                              |
|-----|-------------|------|-------|----------------------------------------------------------|
| 1   | INT_MASK[1] | RW   | 0h    | Over current error mask.<br>0b = Don't Mask<br>1b = Mask |
| 0   | INT_MASK[0] | RW   | 0h    | Over temp error mask.<br>0b = Don't Mask<br>1b = Mask    |

### 8.5.29 INT\_MASK1 (page=0x00 address=0x1B) [reset=A6h]

Interrupt masks.

**Table 128. Interrupt Mask 1 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                   |
|-----|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved        | RW   | 1h    | Reserved                                                                                                                                                      |
| 6   | Reserved        | RW   | 0h    | Reserved                                                                                                                                                      |
| 5   | INT_MASK[13]    | RW   | 1h    | Load Diagnostic Completion Mask<br>0b = Don't Mask<br>1b = Masked                                                                                             |
| 4-3 | INT_MASK[12:11] | RW   | 0h    | Speaker open load mask<br>00b = Don't Mask<br>01b = Mask open Load detection<br>10b = Mask Short Load detection<br>11b = Mask both Open, Short Load detection |
| 2   | INT_MASK[10]    | RW   | 1h    | Brownout device power down start mask<br>0b = Don't Mask<br>1b = Mask                                                                                         |
| 1   | INT_MASK[9]     | RW   | 1h    | Brownout Protection Active mask<br>0b = Don't Mask<br>1b = Mask                                                                                               |
| 0   | INT_MASK[8]     | RW   | 0h    | VBAT Brown out detected mask<br>0b = Don't Mask<br>1b = Mask                                                                                                  |

### 8.5.30 INT\_LIVE0 (page=0x00 address=0x1F) [reset=0h]

Live interrupt readback.

**Table 129. Live Interrupt Readback 0 Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                  |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------|
| 7   | INT_LIVE[7] | R    | 0h    | Interrupt due to limiter mute.<br>0b = No interrupt<br>1b = Interrupt                        |
| 6   | INT_LIVE[6] | R    | 0h    | Interrupt due to limiter infinite hold.<br>0b = No interrupt<br>1b = Interrupt               |
| 5   | INT_LIVE[5] | R    | 0h    | Interrupt due to limiter max attenuation.<br>0b = No interrupt<br>1b = Interrupt             |
| 4   | INT_LIVE[4] | R    | 0h    | Interrupt due to VBAT below limiter inflection point.<br>0b = No interrupt<br>1b = Interrupt |
| 3   | INT_LIVE[3] | R    | 0h    | Interrupt due to limiter active.<br>0b = No interrupt<br>1b = Interrupt                      |
| 2   | INT_LIVE[2] | R    | 0h    | Interrupt due to TDM clock error.<br>0b = No interrupt<br>1b = Interrupt                     |

**Table 129. Live Interrupt Readback 0 Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                 |
|-----|-------------|------|-------|-----------------------------------------------------------------------------|
| 1   | INT_LIVE[1] | R    | 0h    | Interrupt due to over current error.<br>0b = No interrupt<br>1b = Interrupt |
| 0   | INT_LIVE[0] | R    | 0h    | Interrupt due to over temp error.<br>0b = No interrupt<br>1b = Interrupt    |

**8.5.31 INT\_LIVE1 (page=0x00 address=0x20) [reset=0h]**

Live interrupt readback.

**Table 130. Live Interrupt Readback 1 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                           |
|-----|-----------------|------|-------|---------------------------------------------------------------------------------------|
| 7   | Reserved        | R    | 0h    | Reserved                                                                              |
| 6   | Reserved        | R    | 0h    | Reserved                                                                              |
| 5-2 | INT_LIVE[13:10] | R    | 0h    | Reserved                                                                              |
| 1   | INT_LIVE[9]     | R    | 0h    | Brownout Protection Active flag<br>0b = No interrupt<br>1b = Interrupt                |
| 0   | INT_LIVE[8]     | R    | 0h    | Interrupt due to VBAT brown out detected flag.<br>0b = No interrupt<br>1b = Interrupt |

**8.5.32 INT\_LTCH0 (page=0x00 address=0x24) [reset=0h]**

Latched interrupt readback.

**Table 131. Latched Interrupt Readback 0 Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                  |
|-----|--------------|------|-------|----------------------------------------------------------------------------------------------|
| 7   | INT_LTCH0[7] | R    | 0h    | Interrupt due to limiter mute.<br>0b = No interrupt<br>1b = Interrupt                        |
| 6   | INT_LTCH0[6] | R    | 0h    | Interrupt due to limiter infinite hold.<br>0b = No interrupt<br>1b = Interrupt               |
| 5   | INT_LTCH0[5] | R    | 0h    | Interrupt due to limiter max attenuation.<br>0b = No interrupt<br>1b = Interrupt             |
| 4   | INT_LTCH0[4] | R    | 0h    | Interrupt due to VBAT below limiter inflection point.<br>0b = No interrupt<br>1b = Interrupt |
| 3   | INT_LTCH0[3] | R    | 0h    | Interrupt due to limiter active<br>0b = No interrupt<br>1b = Interrupt                       |
| 2   | INT_LTCH0[2] | R    | 0h    | Interrupt due to TDM clock error<br>0b = No interrupt<br>1b = Interrupt                      |
| 1   | INT_LTCH0[1] | R    | 0h    | Interrupt due to over current error<br>0b = No interrupt<br>1b = Interrupt                   |
| 0   | INT_LTCH0[0] | R    | 0h    | Interrupt due to over temp error<br>0b = No interrupt<br>1b = Interrupt                      |

### 8.5.33 INT\_LTCH1 (page=0x00 address=0x25) [reset=0h]

Latched interrupt readback.

**Table 132. Latched Interrupt Readback 1 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                         |
|-----|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved       | R    | 0h    | Reserved                                                                                                                                            |
| 6   | Reserved       | R    | 0h    | Reserved                                                                                                                                            |
| 5   | INT_LTCH1[5]   | R    | 0h    | Interrupt due to load diagnostic completion.<br>0b = Not completed<br>1b = Completed                                                                |
| 4-3 | INT_LTCH1[4:3] | R    | 0h    | Interrupt due to Load Diagnostic Mode Fault Status.<br>00b = Normal Load<br>01b = Open Load Detected<br>10b = Short Load Detected<br>11b = Reserved |
| 2   | INT_LTCH1[2]   | R    | 0h    | Interrupt due to Brownout Protection Triggered shutdown.<br>0b = No interrupt<br>1b = Interrupt                                                     |
| 1   | INT_LTCH1[1]   | R    | 0h    | Interrupt due to Brownout Protection Active flag.<br>0b = No interrupt<br>1b = Interrupt                                                            |
| 0   | INT_LTCH1[0]   | R    | 0h    | Interrupt due to VBAT brown out detected flag.<br>0b = No interrupt<br>1b = Interrupt                                                               |

### 8.5.34 VBAT\_MSB (page=0x00 address=0x2A) [reset=0h]

MSBs of SAR ADC VBAT conversion.

**Table 133. SAR ADC Conversion 0 Field Descriptions**

| Bit | Field         | Type | Reset | Description                           |
|-----|---------------|------|-------|---------------------------------------|
| 7-0 | VBAT_CNV[9:2] | R    | 0h    | Returns SAR ADC VBAT conversion MSBs. |

### 8.5.35 VBAT\_LSB (page=0x00 address=0x2B) [reset=0h]

LSBs of SAR ADC VBAT conversion.

**Table 134. SAR ADC Conversion 1 Field Descriptions**

| Bit | Field         | Type | Reset | Description                           |
|-----|---------------|------|-------|---------------------------------------|
| 7-6 | VBAT_CNV[1:0] | R    | 0h    | Returns SAR ADC VBAT conversion LSBs. |
| 5-0 | Reserved      | R    | 0h    | Reserved                              |

### 8.5.36 TEMP (page=0x00 address=0x2C) [reset=0h]

SAR ADC Temp conversion.

**Table 135. SAR ADC Conversion 2 Field Descriptions**

| Bit | Field        | Type | Reset | Description                             |
|-----|--------------|------|-------|-----------------------------------------|
| 7-0 | TMP_CNV[7:0] | R    | 0h    | Returns SAR ADC temp sensor conversion. |

### 8.5.37 INT\_CLK (page=0x00 address=0x30) [reset=19h]

Sets ASI clock error handling and interrupt configuration.

**Table 136. Interrupt and Clock Error Field Descriptions**

| Bit | Field               | Type | Reset | Description                                                                                                                                                                                                                                                          |
|-----|---------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CLK_ERR_PWR_EN      | RW   | 0h    | Power up/down based on valid ASI clocks is<br>0b = Disable<br>1b = Enabled                                                                                                                                                                                           |
| 6   | CLK_HALT_EN         | RW   | 0h    | Put device to sleep(halt) after clock error lasts longer than CLK_HALT_TIMER is<br>0b = Enable<br>1b = Disable                                                                                                                                                       |
| 5-3 | CLK_HALT_TIMER[2:0] | RW   | 3h    | If CLK_HALT_EN device will goto sleep after<br>000b = 1 ms<br>001b = 3.27 ms<br>010b = 26.21ms<br>011b = 52.42ms<br>100b = 104.85ms<br>101b = 209.71ms<br>110b = 419.43ms<br>111b = 838.86ms                                                                         |
| 2   | INT_CLR_LTCH        | RW   | 0h    | Clear INT_LTCH registers<br>0b = Don't clear<br>1b = Clear (self clearing bit)                                                                                                                                                                                       |
| 1-0 | IRQZ_PIN_CFG[1:0]   | RW   | 1h    | IRQZ interrupt configuration. IRQZ will assert<br>00b = on any unmasked live interrupts<br>01b = on any unmasked latched interrupts<br>10b = for 2-4ms one time on any unmasked live interrupt event<br>11b = for 2-4ms every 4ms on any unmasked latched interrupts |

### 8.5.38 DIN\_PD (page=0x00 address=0x31) [reset=40h]

Sets enables of input pin weak pull down.

**Table 137. Digital Input Pin Pull Down Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                |
|-----|-----------|------|-------|------------------------------------------------------------|
| 7   | Reserved  | R    | 0h    | Reserved                                                   |
| 6   | DIN_PD[6] | RW   | 1h    | Weak pull down for GPIO.<br>0b = Disabled<br>1b = Enabled  |
| 5   | DIN_PD[5] | RW   | 0h    | Weak pull down for AD1.<br>0b = Disabled<br>1b = Enabled   |
| 4   | DIN_PD[4] | RW   | 0h    | Weak pull down for AD0.<br>0b = Disabled<br>1b = Enabled   |
| 3   | DIN_PD[3] | RW   | 0h    | Weak pull down for SDOUT.<br>0b = Disabled<br>1b = Enabled |
| 2   | DIN_PD[2] | RW   | 0h    | Weak pull down for SDIN.<br>0b = Disabled<br>1b = Enabled  |
| 1   | DIN_PD[1] | RW   | 0h    | Weak pull down for FSYNC.<br>0b = Disabled<br>1b = Enabled |
| 0   | DIN_PD[0] | RW   | 0h    | Weak pull down for SBCLK.<br>0b = Disabled<br>1b = Enabled |

### 8.5.39 MISC\_CFG3 (page=0x00 address=0x32) [reset=80h]

Set IRQZ pin active state

**Table 138. Misc Configuration 3 Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                          |
|-----|----------|------|-------|--------------------------------------------------------------------------------------|
| 7   | IRQZ_POL | RW   | 1h    | IRQZ pin polarity for interrupt.<br>0b = Active high (IRQ)<br>1b = Active low (IRQZ) |
| 6-4 | Reserved | RW   | 0h    | Reserved                                                                             |
| 3-2 | Reserved | R    | 0h    | Reserved                                                                             |
| 1   | Reserved | RW   | 0h    | Reserved                                                                             |
| 0   | Reserved | R    | 0h    | Reserved                                                                             |

### 8.5.40 BOOST\_CFG1 (page=0x00 address=0x33) [reset=34h]

Boost Configure 1

**Table 139. Boost Configure 1 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                        |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | BST_MODE      | RW   | 0h    | Boost Mode                                                                                                                                                                         |
| 6   | BST_MODE      | RW   | 0h    | Boost Mode<br>00b = Class-H<br>01b = Class-G<br>10b = Always ON<br>11b = Always OFF(Passthrough)                                                                                   |
| 5   | BST_EN        | RW   | 1h    | Boost enable<br>0b = Disabled<br>1b = Enabled                                                                                                                                      |
| 4-3 | BST_GSST[1:0] | RW   | 2h    | Boost soft-start timer in Class-G mode<br>00b = 1 x Class-H power-up time<br>01b = 2 x Class-H power-up time<br>10b = 4 x Class-H power-up time<br>11b = 8 x Class-H power-up time |
| 2-1 | BST_PFML[1:0] | RW   | 2h    | Boost active mode PFM lower limit<br>00b = No lower limit<br>01b = 25 kHz<br>10b = 50 kHz<br>11b = 100 kHz                                                                         |
| 0   | Reserved      | RW   | 0h    | Reserved                                                                                                                                                                           |

### 8.5.41 BOOST\_CFG2 (page=0x00 address=0x34) [reset=4Bh]

Boost Configure 2

**Table 140. Boost Configure 2 Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                          |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 7-6 | BST_IR[1:0] | RW   | 1h    | Boost inductor range<br>00b = less than 0.6 uH<br>01b = 0.6 uH to 1.3 uH<br>10b = 1.3 uH to 2.5 uH<br>11b = Reserved |
| 5   | BST_SYNC    | RW   | 0h    | Boost sync to clock<br>0b = Not synced<br>1b = Synced                                                                |
| 4   | BST_PA      | RW   | 0h    | Boost sync phase<br>0b = 0 deg<br>1b = 180 deg                                                                       |

**Table 140. Boost Configure 2 Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                               |
|-----|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3-0 | BST_VREG[3:0] | RW   | Bh    | Boost Maximum Voltage<br>0000b = Reserved<br>0001b = 6.5 V<br>0010b = 7.0 V<br>....<br>1011b = 11.5 V<br>....<br>1101b = 12.5 V<br>1110b-1111b = Reserved |

#### 8.5.42 BOOST\_CFG3 (page=0x00 address=0x35) [reset=74h]

Boost Configure 3

**Table 141. Boost Configure 3 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                     |
|-----|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | BST_HSST[3:0] | RW   | 7h    | Step Time for Boost if in Class-H mode<br>0000b = 9us<br>0001b = 18us<br>0010b = 36us<br>0011b = 54us<br>0100b = 72us<br>0101b = 90us<br>0110b = 108us<br>0111b = 135us<br>1000b = 162us<br>1001b = 198us<br>1010b = 252us<br>1011b = 342us<br>1100b = 477us<br>1101b = 612us<br>1110b = 792us<br>1111b = 990us |
| 3-2 | BST_LR[1:0]   | RW   | 1h    | Slope of boost load regulation.<br>00b = Reserved<br>01b = 3A/V; load regulation = 1V (default)<br>10b = 2A/V; load regulation = 1.5V<br>11b = Reserved                                                                                                                                                         |
| 1   | Reserved      | RW   | 0h    | Reserved                                                                                                                                                                                                                                                                                                        |
| 0   | Reserved      | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                        |

#### 8.5.43 MISC\_CFG4 (page=0x00 address=0x3D) [reset=8h]

Tone gen clocking, load diagnostic clocking, VI averaging.

**Table 142. Misc Configuration 4 Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------|
| 7-4 | Reserved | R    | 0h    | Clock source for tone generator beep mode<br>0b = External TDM<br>1b = Internal Oscillator |
| 3   | LDG_CLK  | RW   | 0h    | Clock source for load diagnostic<br>0b = External TDM<br>1b = Internal Oscillator          |
| 2-1 | Reserved | RW   | 1h    | Reserved                                                                                   |
| 0   | Reserved | RW   | 0h    | Reserved                                                                                   |

#### 8.5.44 TG\_CFG0 (page=0x00 address=0x3F) [reset=0h]

Tone Generator

**Table 143. Tone Generator Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                        |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | TG1_EN[1:0]    | RW   | 0h    | Tone Generator 1 is<br>00b = Disabled or pin triggered<br>01b = Enabled - play tone<br>10b = audio level enabled<br>11b = reserved |
| 5-4 | TG1_PINEN[1:0] | RW   | 0h    | Tone pin trigger<br>00b = Disabled<br>01b = SDIN<br>10b = GPIO<br>11b = AD1                                                        |
| 3   | TG2_EN         | RW   | 0h    | Tone Generator 2 is<br>0b = Disabled<br>1b = Enabled                                                                               |
| 2-0 | Reserved       | R    | 0h    | Reserved                                                                                                                           |

#### 8.5.45 BOOST\_CFG4 (page=0x00 address=0x40) [reset=36h]

Boost Configure 4

**Table 144. Boost Configure 4 Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                |
|-----|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | BST_SSL[7:0] | RW   | 0h    | Boost peak current limit<br>00h = 0.99 A<br>01h = 1.045 A<br>02h = 1.1 A<br>...<br>0x36h = 3.96 A<br>0x37h = 4 A<br>0x38h-0x3Fh = Reserved |

#### 8.5.46 REV\_ID (page=0x00 address=0x7D) [reset=0h]

Returns REV and PG ID.

**Table 145. Revision and PG ID Field Descriptions**

| Bit | Field       | Type | Reset | Description              |
|-----|-------------|------|-------|--------------------------|
| 7-4 | REV_ID[3:0] | R    | 0h    | Returns the revision ID. |
| 3-0 | PG_ID[3:0]  | R    | 0h    | Returns the PG ID.       |

#### 8.5.47 I2C\_CKSUM (page=0x00 address=0x7E) [reset=0h]

Returns I2C checksum.

**Table 146. I2C Checksum Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                |
|-----|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | I2C_CKSUM[7:0] | RW   | 0h    | Returns I2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages. |

### 8.5.48 BOOK (page=0x00 address=0x7F) [reset=0h]

Device's memory map is divided into pages and books. This register sets the book.

**Table 147. Device Book Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------|
| 7-0 | BOOK[7:0] | RW   | 0h    | Sets the device book.<br>00h = Book 0<br>01h = Book 1<br>...<br>FFh = Book 255 |

### 8.5.49 PAGE1 (page=0x01 address=0x00) [reset=0h]

Device Page

**Table 148. Device Page Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------|
| 7-0 | PAGE[7:0] | RW   | 0h    | Sets the device page.<br>00h = Page 0<br>01h = Page 1<br>...<br>FFh = Page 255 |

### 8.5.50 TF\_CFG21 (page=0x01 address=0x08) [reset=40h]

Set the enable for thermal foldback

**Table 149. Thermal Folder Configure Field Descriptions**

| Bit | Field    | Type | Reset | Description                                        |
|-----|----------|------|-------|----------------------------------------------------|
| 7   | Reserved | R    | 0h    | Reserved                                           |
| 6   | TF_EN    | RW   | 1h    | Thermal Foldback is<br>0 = Disabled<br>1 = Enabled |
| 5-0 | Reserved | RW   | 0h    | Reserved                                           |

### 8.5.51 PAGE2 (page=0x02 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

**Table 150. Device Page Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------|
| 7-0 | PAGE[7:0] | RW   | 0h    | Sets the device page.<br>00h = Page 0<br>01h = Page 1<br>...<br>FFh = Page 255 |

### 8.5.52 DVC\_CFG1 (page=0x02 address=0x0C) [reset=40h]

Sets playback volume for PCM playback path.

**Table 151. Digital Volume Control 1 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                |
|-----|----------------|------|-------|------------------------------------------------------------|
| 7-0 | DVC_PCM[31:24] | RW   | 40h   | $\text{round}(10^{(\text{volume in dB}/20)} \cdot 2^{30})$ |

### 8.5.53 DVC\_CFG2 (page=0x02 address=0x0D) [reset=40h]

Sets playback volume for PCM playback path.

**Table 152. Digital Volume Control 2 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                |
|-----|----------------|------|-------|------------------------------------------------------------|
| 7-0 | DVC_PCM[23:16] | RW   | 40h   | $\text{round}(10^{(\text{volume in dB}/20)} \cdot 2^{30})$ |

### 8.5.54 DVC\_CFG3 (page=0x02 address=0x0E) [reset=0h]

Sets playback volume for PCM playback path.

**Table 153. Digital Volume Control 3 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                |
|-----|---------------|------|-------|------------------------------------------------------------|
| 7-0 | DVC_PCM[15:8] | RW   | 0h    | $\text{round}(10^{(\text{volume in dB}/20)} \cdot 2^{30})$ |

### 8.5.55 DVC\_CFG4 (page=0x02 address=0x0F) [reset=0h]

Sets playback volume for PCM playback path.

**Table 154. Digital Volume Control 4 Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                |
|-----|--------------|------|-------|------------------------------------------------------------|
| 7-0 | DVC_PCM[7:0] | RW   | 0h    | $\text{round}(10^{(\text{volume in dB}/20)} \cdot 2^{30})$ |

### 8.5.56 DVC\_CFG5 (page=0x02 address=0x10) [reset=3h]

Sets ramp rate for volume control

**Table 155. Digital Volume Control 5 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                              |
|-----|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 7-0 | DVC_RAMP[31:24] | RW   | 3h    | $\text{round}((1 - \exp(-1/(0.2 \cdot f_s \cdot \text{time in seconds}))) \cdot 2^{31})$ |

### 8.5.57 DVC\_CFG6 (page=0x02 address=0x11) [reset=4Ah]

Sets ramp rate for volume control

**Table 156. Digital Volume Control 6 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                              |
|-----|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 7-0 | DVC_RAMP[23:16] | RW   | 4Ah   | $\text{round}((1 - \exp(-1/(0.2 \cdot f_s \cdot \text{time in seconds}))) \cdot 2^{31})$ |

### 8.5.58 DVC\_CFG7 (page=0x02 address=0x12) [reset=51h]

Sets ramp rate for volume control

**Table 157. Digital Volume Control 7 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                              |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------|
| 7-0 | DVC_RAMP[15:8] | RW   | 51h   | $\text{round}((1 - \exp(-1/(0.2 \cdot f_s \cdot \text{time in seconds}))) \cdot 2^{31})$ |

### 8.5.59 DVC\_CFG7 (page=0x02 address=0x13) [reset=6Ch]

Sets ramp rate for volume control

**Table 158. Digital Volume Control 8 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                              |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------|
| 7-0 | DVC_RAMP[7:0] | RW   | 6Ch   | $\text{round}((1 - \exp(-1/(0.2 \cdot f_s \cdot \text{time in seconds}))) \cdot 2^{31})$ |

### 8.5.60 LIM\_CFG1 (page=0x02 address=0x14) [reset=2Dh]

Sets limiter max attenuation

**Table 159. Limiter Configuration 1 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                               |
|-----|--------------------|------|-------|-----------------------------------------------------------|
| 7-0 | LIM_MAX_ATN[31:24] | RW   | 2Dh   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

### 8.5.61 LIM\_CFG2 (page=0x02 address=0x15) [reset=6Ah]

Limiter Configuration 2- Sets limiter max attenuation

**Table 160. Limiter Configuration 2- Sets limiter max attenuation Field Descriptions**

| Bit | Field              | Type | Reset | Description                                               |
|-----|--------------------|------|-------|-----------------------------------------------------------|
| 7-0 | LIM_MAX_ATN[23:16] | RW   | 6Ah   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

### 8.5.62 LIM\_CFG3 (page=0x02 address=0x16) [reset=86h]

Limiter Configuration 3- Sets limiter max attenuation

**Table 161. Limiter Configuration 3- Sets limiter max attenuation Field Descriptions**

| Bit | Field             | Type | Reset | Description                                               |
|-----|-------------------|------|-------|-----------------------------------------------------------|
| 7-0 | LIM_MAX_ATN[15:8] | RW   | 86h   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

### 8.5.63 LIM\_CFG4 (page=0x02 address=0x17) [reset=6Fh]

Limiter Configuration 4- Sets limiter max attenuation

**Table 162. Limiter Configuration 4- Sets limiter max attenuation Field Descriptions**

| Bit | Field            | Type | Reset | Description                                               |
|-----|------------------|------|-------|-----------------------------------------------------------|
| 7-0 | LIM_MAX_ATN[7:0] | RW   | 6Fh   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

### 8.5.64 LIM\_CFG5 (page=0x02 address=0x18) [reset=47h]

Sets VBAT Limiter max threshold.

**Table 163. Limiter Configuration 5 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                              |
|-----|--------------------|------|-------|----------------------------------------------------------|
| 7-0 | LIMB_TH_MAX[31:24] | RW   | 47h   | $\text{round}(\text{lim max peak voltage} \cdot 2^{27})$ |

### 8.5.65 LIM\_CFG6 (page=0x02 address=0x19) [reset=5Ch]

Sets VBAT Limiter max threshold.

**Table 164. Limiter Configuration 6 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                              |
|-----|--------------------|------|-------|----------------------------------------------------------|
| 7-0 | LIMB_TH_MAX[23:16] | RW   | 5Ch   | $\text{round}(\text{lim max peak voltage} \cdot 2^{27})$ |

### 8.5.66 LIM\_CFG7 (page=0x02 address=0x1A) [reset=28h]

Sets VBAT Limiter max threshold.

**Table 165. Limiter Configuration 7 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                              |
|-----|-------------------|------|-------|----------------------------------------------------------|
| 7-0 | LIMB_TH_MAX[15:8] | RW   | 28h   | $\text{round}(\text{lim max peak voltage} \cdot 2^{27})$ |

### 8.5.67 LIM\_CFG8 (page=0x02 address=0x1B) [reset=F6h]

Sets VBAT Limiter max threshold.

**Table 166. Limiter Configuration 8 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                  |
|-----|------------------|------|-------|----------------------------------------------|
| 7-0 | LIMB_TH_MAX[7:0] | RW   | F6h   | round(lim max peak voltage*2 <sup>27</sup> ) |

### 8.5.68 LIM\_CFG9 (page=0x02 address=0x1C) [reset=16h]

Sets VBAT limiter min threshold.

**Table 167. Limiter Configuration 9 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                  |
|-----|--------------------|------|-------|----------------------------------------------|
| 7-0 | LIMB_TH_MIN[31:24] | RW   | 16h   | round(lim min peak voltage*2 <sup>27</sup> ) |

### 8.5.69 LIM\_CFG10 (page=0x02 address=0x1D) [reset=66h]

Sets VBAT limiter min threshold.

**Table 168. Limiter Configuration 10 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                  |
|-----|--------------------|------|-------|----------------------------------------------|
| 7-0 | LIMB_TH_MIN[23:16] | RW   | 66h   | round(lim min peak voltage*2 <sup>27</sup> ) |

### 8.5.70 LIM\_CFG11 (page=0x02 address=0x1E) [reset=66h]

Sets VBAT limiter min threshold.

**Table 169. Limiter Configuration 11 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                  |
|-----|-------------------|------|-------|----------------------------------------------|
| 7-0 | LIMB_TH_MIN[15:8] | RW   | 66h   | round(lim min peak voltage*2 <sup>27</sup> ) |

### 8.5.71 LIM\_CFG12 (page=0x02 address=0x1F) [reset=66h]

Sets VBAT limiter min threshold.

**Table 170. Limiter Configuration 12 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                  |
|-----|------------------|------|-------|----------------------------------------------|
| 7-0 | LIMB_TH_MIN[7:0] | RW   | 66h   | round(lim min peak voltage*2 <sup>27</sup> ) |

### 8.5.72 LIM\_CFG13 (page=0x02 address=0x20) [reset=34h]

Sets VBAT limiter inflection point.

**Table 171. Limiter Configuration 13 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                      |
|-----|--------------------|------|-------|--------------------------------------------------|
| 7-0 | LIMB_INF_PT[31:24] | RW   | 34h   | round(Vbat at inflection point*2 <sup>28</sup> ) |

### 8.5.73 LIM\_CFG14 (page=0x02 address=0x21) [reset=CCh]

Sets VBAT limiter inflection point.

**Table 172. Limiter Configuration 14 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                      |
|-----|--------------------|------|-------|--------------------------------------------------|
| 7-0 | LIMB_INF_PT[23:16] | RW   | CCh   | round(Vbat at inflection point*2 <sup>28</sup> ) |

**8.5.74 LIM\_CFG15 (page=0x02 address=0x22) [reset=CCh]**

Sets VBAT limiter inflection point.

**Table 173. Limiter Configuration 15 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                      |
|-----|-------------------|------|-------|--------------------------------------------------|
| 7-0 | LIMB_INF_PT[15:8] | RW   | CCh   | round(Vbat at inflection point*2 <sup>28</sup> ) |

**8.5.75 LIM\_CFG16 (page=0x02 address=0x23) [reset=CDh]**

Sets VBAT limiter inflection point.

**Table 174. Limiter Configuration 16 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                      |
|-----|------------------|------|-------|--------------------------------------------------|
| 7-0 | LIMB_INF_PT[7:0] | RW   | CDh   | round(Vbat at inflection point*2 <sup>28</sup> ) |

**8.5.76 LIM\_CFG17 (page=0x02 address=0x24) [reset=10h]**

Sets VBAT limiter slope

**Table 175. Limiter Configuration 1 Field Descriptions**

| Bit | Field             | Type | Reset | Description                   |
|-----|-------------------|------|-------|-------------------------------|
| 7-0 | LIMB_SLOPE[31:24] | RW   | 10h   | round(slope*2 <sup>28</sup> ) |

**8.5.77 LIM\_CFG18 (page=0x02 address=0x25) [reset=0h]**

Sets VBAT limiter slope

**Table 176. Limiter Configuration 2 Field Descriptions**

| Bit | Field             | Type | Reset | Description                   |
|-----|-------------------|------|-------|-------------------------------|
| 7-0 | LIMB_SLOPE[23:16] | RW   | 0h    | round(slope*2 <sup>28</sup> ) |

**8.5.78 LIM\_CFG19 (page=0x02 address=0x26) [reset=0h]**

Sets VBAT limiter slope

**Table 177. Limiter Configuration 3 Field Descriptions**

| Bit | Field            | Type | Reset | Description                   |
|-----|------------------|------|-------|-------------------------------|
| 7-0 | LIMB_SLOPE[15:8] | RW   | 0h    | round(slope*2 <sup>28</sup> ) |

**8.5.79 LIM\_CFG20 (page=0x02 address=0x27) [reset=0h]**

Sets VBAT limiter slope

**Table 178. Limiter Configuration 4 Field Descriptions**

| Bit | Field           | Type | Reset | Description                   |
|-----|-----------------|------|-------|-------------------------------|
| 7-0 | LIMB_SLOPE[7:0] | RW   | 0h    | round(slope*2 <sup>28</sup> ) |

**8.5.80 BOP\_CFG1 (page=0x02 address=0x28) [reset=2Eh]**

BOP threshold.

**Table 179. Brown Out Prevention 1 Field Descriptions**

| Bit | Field         | Type | Reset | Description                                |
|-----|---------------|------|-------|--------------------------------------------|
| 7-0 | BOP_TH[31:24] | RW   | 2Eh   | round(Vbat BOP threshold*2 <sup>28</sup> ) |

### 8.5.81 BOP\_CFG2 (page=0x02 address=0x29) [reset=66h]

BOP threshold.

**Table 180. Brown Out Prevention 2 Field Descriptions**

| Bit | Field         | Type | Reset | Description                    |
|-----|---------------|------|-------|--------------------------------|
| 7-0 | BOP_TH[23:16] | RW   | 66h   | round(Vbat BOP threshold*2^28) |

### 8.5.82 BOP\_CFG3 (page=0x02 address=0x2A) [reset=66h]

BOP threshold.

**Table 181. Brown Out Prevention 3 Field Descriptions**

| Bit | Field        | Type | Reset | Description                    |
|-----|--------------|------|-------|--------------------------------|
| 7-0 | BOP_TH[15:8] | RW   | 66h   | round(Vbat BOP threshold*2^28) |

### 8.5.83 BOP\_CFG4 (page=0x02 address=0x2B) [reset=66h]

BOP threshold.

**Table 182. Brown Out Prevention 4 Field Descriptions**

| Bit | Field       | Type | Reset | Description                    |
|-----|-------------|------|-------|--------------------------------|
| 7-0 | BOP_TH[7:0] | RW   | 66h   | round(Vbat BOP threshold*2^28) |

### 8.5.84 BOP\_CFG5 (page=0x02 address=0x2C) [reset=2Bh]

BOSD threshold.

**Table 183. Brown Out Prevention 5 Field Descriptions**

| Bit | Field          | Type | Reset | Description                     |
|-----|----------------|------|-------|---------------------------------|
| 7-0 | BOSD_TH[31:24] | RW   | 2Bh   | round(Vbat BOSD threshold*2^28) |

### 8.5.85 BOP\_CFG6 (page=0x02 address=0x2D) [reset=33h]

BOSD threshold.

**Table 184. Brown Out Prevention 6 Field Descriptions**

| Bit | Field          | Type | Reset | Description                     |
|-----|----------------|------|-------|---------------------------------|
| 7-0 | BOSD_TH[23:16] | RW   | 33h   | round(Vbat BOSD threshold*2^28) |

### 8.5.86 BOP\_CFG7 (page=0x02 address=0x2E) [reset=33h]

BOSD threshold.

**Table 185. Brown Out Prevention 7 Field Descriptions**

| Bit | Field         | Type | Reset | Description                     |
|-----|---------------|------|-------|---------------------------------|
| 7-0 | BOSD_TH[15:8] | RW   | 33h   | round(Vbat BOSD threshold*2^28) |

### 8.5.87 BOP\_CFG8 (page=0x02 address=0x2F) [reset=33h]

BOSD threshold.

**Table 186. Brown Out Prevention 8 Field Descriptions**

| Bit | Field        | Type | Reset | Description                     |
|-----|--------------|------|-------|---------------------------------|
| 7-0 | BOSD_TH[7:0] | RW   | 33h   | round(Vbat BOSD threshold*2^28) |

**8.5.88 HPFC\_CFG1 (page=0x02 address=0x30) [reset=7Fh]**

HPF Biquad coefficients

**Table 187. HPF Coefficient 1 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                              |
|-----|---------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N0[31:24] | RW   | 7Fh   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31); |

**8.5.89 HPFC\_CFG2 (page=0x02 address=0x31) [reset=FBh]**

HPF Biquad coefficients

**Table 188. HPF Coefficient 2 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                              |
|-----|---------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N0[23:16] | RW   | FBh   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31); |

**8.5.90 HPFC\_CFG3 (page=0x02 address=0x32) [reset=B6h]**

HPF Biquad coefficients

**Table 189. HPF Coefficient 3 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                              |
|-----|--------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N0[15:8] | RW   | B6h   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31); |

**8.5.91 HPFC\_CFG4 (page=0x02 address=0x33) [reset=14h]**

HPF Biquad coefficients

**Table 190. HPF Coefficient 4 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                              |
|-----|-------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N0[7:0] | RW   | 14h   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31); |

**8.5.92 HPFC\_CFG5 (page=0x02 address=0x34) [reset=80h]**

HPF Biquad coefficients

**Table 191. HPF Coefficient 5 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                              |
|-----|---------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N1[31:24] | RW   | 80h   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31); |

**8.5.93 HPFC\_CFG6 (page=0x02 address=0x35) [reset=4h]**

HPF Biquad coefficients

**Table 192. HPF Coefficient 6 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                              |
|-----|---------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N1[23:16] | RW   | 4h    | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31); |

**8.5.94 HPFC\_CFG7 (page=0x02 address=0x36) [reset=49h]**

HPF Biquad coefficients

**Table 193. HPF Coefficient 7 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                              |
|-----|--------------------|------|-------|----------------------------------------------------------|
| 7-0 | HPF_COEFF_N1[15:8] | RW   | 49h   | [N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31); |

### 8.5.95 HPFC\_CFG8 (page=0x02 address=0x37) [reset=ECh]

HPF Biquad coefficients

**Table 194. HPF Coefficient 8 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                                |
|-----|-------------------|------|-------|----------------------------------------------------------------------------|
| 7-0 | HPF_COEFF_N1[7:0] | RW   | ECh   | $[N, D] = \text{butter}(1, fc/(fs/2), 'high'); \text{round}(N(2)*2^{31});$ |

### 8.5.96 HPFC\_CFG9 (page=0x02 address=0x38) [reset=7Fh]

HPF Biquad coefficients

**Table 195. HPF Coefficient 9 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                                                 |
|-----|---------------------|------|-------|-----------------------------------------------------------------------------|
| 7-0 | HPF_COEFF_D1[31:24] | RW   | 7Fh   | $[N, D] = \text{butter}(1, fc/(fs/2), 'high'); \text{round}(-D(2)*2^{31});$ |

### 8.5.97 HPFC\_CFG10 (page=0x02 address=0x39) [reset=7Fh]

HPF Biquad coefficients

**Table 196. HPF Coefficient 10 Field Descriptions**

| Bit | Field               | Type | Reset | Description                                                                 |
|-----|---------------------|------|-------|-----------------------------------------------------------------------------|
| 7-0 | HPF_COEFF_D1[23:16] | RW   | 7Fh   | $[N, D] = \text{butter}(1, fc/(fs/2), 'high'); \text{round}(-D(2)*2^{31});$ |

### 8.5.98 HPFC\_CFG11 (page=0x02 address=0x3A) [reset=6Ch]

HPF Biquad coefficients

**Table 197. HPF Coefficient 11 Field Descriptions**

| Bit | Field              | Type | Reset | Description                                                                 |
|-----|--------------------|------|-------|-----------------------------------------------------------------------------|
| 7-0 | HPF_COEFF_D1[15:8] | RW   | 6Ch   | $[N, D] = \text{butter}(1, fc/(fs/2), 'high'); \text{round}(-D(2)*2^{31});$ |

### 8.5.99 HPFC\_CFG12 (page=0x02 address=0x3B) [reset=28h]

HPF Biquad coefficients

**Table 198. HPF Coefficient 12 Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                                 |
|-----|-------------------|------|-------|-----------------------------------------------------------------------------|
| 7-0 | HPF_COEFF_D1[7:0] | RW   | 28h   | $[N, D] = \text{butter}(1, fc/(fs/2), 'high'); \text{round}(-D(2)*2^{31});$ |

### 8.5.100 TG\_CFG1 (page=0x02 address=0x3C) [reset=3Fh]

Tone Generator 1 Freq Calc 1

**Table 199. Tone Generator 1 Freq Calc 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                        |
|-----|------------------|------|-------|----------------------------------------------------|
| 7-0 | TG1_FREQ1[31:24] | RW   | 3Fh   | $\text{round}((2*\cos(2*\pi*f\_tone/fs))^*2^{29})$ |

### 8.5.101 TG\_CFG2 (page=0x02 address=0x3D) [reset=FFh]

Tone Generator 1 Freq Calc 1

**Table 200. Tone Generator 1 Freq Calc 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                        |
|-----|------------------|------|-------|----------------------------------------------------|
| 7-0 | TG1_FREQ1[23:16] | RW   | FFh   | $\text{round}((2*\cos(2*\pi*f\_tone/fs))^*2^{29})$ |

**8.5.102 TG\_CFG3 (page=0x02 address=0x3E) [reset=7Ah]**

Tone Generator 1 Freq Calc 1

**Table 201. Tone Generator 1 Freq Calc 1 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                      |
|-----|-----------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG1_FREQ1[15:8] | RW   | 7Ah   | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.103 TG\_CFG4 (page=0x02 address=0x3F) [reset=E3h]**

Tone Generator 1 Freq Calc 1

**Table 202. Tone Generator 1 Freq Calc 1 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                      |
|-----|----------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG1_FREQ1[7:0] | RW   | E3h   | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.104 TG\_CFG5 (page=0x02 address=0x40) [reset=1h]**

Tone Generator 1 Freq Calc 2

**Table 203. Tone Generator 1 Freq Calc 2 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                              |
|-----|------------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG1_FREQ2[31:24] | RW   | 1h    | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.105 TG\_CFG6 (page=0x02 address=0x41) [reset=1h]**

Tone Generator 1 Freq Calc 2

**Table 204. Tone Generator 1 Freq Calc 2 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                              |
|-----|------------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG1_FREQ2[23:16] | RW   | 1h    | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.106 TG\_CFG7 (page=0x02 address=0x42) [reset=5Bh]**

Tone Generator 1 Freq Calc 2

**Table 205. Tone Generator 1 Freq Calc 2 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                              |
|-----|-----------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG1_FREQ2[15:8] | RW   | 5Bh   | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.107 TG\_CFG8 (page=0x02 address=0x43) [reset=4Ch]**

Tone Generator 1 Freq Calc 2

**Table 206. Tone Generator 1 Freq Calc 2 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                              |
|-----|----------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG1_FREQ2[7:0] | RW   | 4Ch   | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.108 TG\_CFG9 (page=0x02 address=0x44) [reset=0h]**

Tone Generator 1 Freq Calc 3

**Table 207. Tone Generator 1 Freq Calc 3 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                              |
|-----|------------------|------|-------|----------------------------------------------------------|
| 7-0 | TG1_FREQ3[31:24] | RW   | 0h    | $(\text{LCM}(f_s, f_{\text{tone}})/f_{\text{tone}}) - 1$ |

### 8.5.109 TG\_CFG10 (page=0x02 address=0x45) [reset=0h]

Tone Generator 1 Freq Calc 3

**Table 208. Tone Generator 1 Freq Calc 3 Field Descriptions**

| Bit | Field            | Type | Reset | Description                       |
|-----|------------------|------|-------|-----------------------------------|
| 7-0 | TG1_FREQ3[23:16] | RW   | 0h    | $(LCM(f_s, f\_tone)/f\_tone) - 1$ |

### 8.5.110 TG\_CFG11 (page=0x02 address=0x46) [reset=3h]

Tone Generator 1 Freq Calc 3

**Table 209. Tone Generator 1 Freq Calc 3 Field Descriptions**

| Bit | Field           | Type | Reset | Description                       |
|-----|-----------------|------|-------|-----------------------------------|
| 7-0 | TG1_FREQ3[15:8] | RW   | 3h    | $(LCM(f_s, f\_tone)/f\_tone) - 1$ |

### 8.5.111 TG\_CFG12 (page=0x02 address=0x47) [reset=1Fh]

Tone Generator 1 Freq Calc 3

**Table 210. Tone Generator 1 Freq Calc 3 Field Descriptions**

| Bit | Field          | Type | Reset | Description                       |
|-----|----------------|------|-------|-----------------------------------|
| 7-0 | TG1_FREQ3[7:0] | RW   | 1Fh   | $(LCM(f_s, f\_tone)/f\_tone) - 1$ |

### 8.5.112 TG\_CFG13 (page=0x02 address=0x48) [reset=2h]

Tone Generator 1 Amplitude Calc

**Table 211. Tone Generator 1 Amplitude Calc Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                 |
|-----|----------------|------|-------|-------------------------------------------------------------|
| 7-0 | TG1_AMP[31:24] | RW   | 2h    | $\text{round}(10^{(\text{tone amplitude dB}/20)} * 2^{31})$ |

### 8.5.113 TG\_CFG14 (page=0x02 address=0x49) [reset=46h]

Tone Generator 1 Amplitude Calc

**Table 212. Tone Generator 1 Amplitude Calc Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                 |
|-----|----------------|------|-------|-------------------------------------------------------------|
| 7-0 | TG1_AMP[23:16] | RW   | 46h   | $\text{round}(10^{(\text{tone amplitude dB}/20)} * 2^{31})$ |

### 8.5.114 TG\_CFG15 (page=0x02 address=0x4A) [reset=B4h]

Tone Generator 1 Amplitude Calc

**Table 213. Tone Generator 1 Amplitude Calc Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                 |
|-----|---------------|------|-------|-------------------------------------------------------------|
| 7-0 | TG1_AMP[15:8] | RW   | B4h   | $\text{round}(10^{(\text{tone amplitude dB}/20)} * 2^{31})$ |

### 8.5.115 TG\_CFG16 (page=0x02 address=0x4B) [reset=E4h]

Tone Generator 1 Amplitude Calc

**Table 214. Tone Generator 1 Amplitude Calc Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                 |
|-----|--------------|------|-------|-------------------------------------------------------------|
| 7-0 | TG1_AMP[7:0] | RW   | E4h   | $\text{round}(10^{(\text{tone amplitude dB}/20)} * 2^{31})$ |

**8.5.116 TG\_CFG17 (page=0x02 address=0x4C) [reset=E0h]**

Tone Generator 2 Freq Calc 1

**Table 215. Tone Generator 2 Freq Calc 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                      |
|-----|------------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG2_FREQ1[31:24] | RW   | E0h   | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.117 TG\_CFG18 (page=0x02 address=0x4D) [reset=0h]**

Tone Generator 2 Freq Calc 1

**Table 216. Tone Generator 2 Freq Calc 1 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                      |
|-----|------------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG2_FREQ1[23:16] | RW   | 0h    | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.118 TG\_CFG19 (page=0x02 address=0x4E) [reset=0h]**

Tone Generator 2 Freq Calc 1

**Table 217. Tone Generator 2 Freq Calc 1 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                      |
|-----|-----------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG2_FREQ1[15:8] | RW   | 0h    | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.119 TG\_CFG20 (page=0x02 address=0x4F) [reset=0h]**

Tone Generator 2 Freq Calc 1

**Table 218. Tone Generator 2 Freq Calc 1 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                      |
|-----|----------------|------|-------|----------------------------------------------------------------------------------|
| 7-0 | TG2_FREQ1[7:0] | RW   | 0h    | $\text{round}((2 \cdot \cos(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 29)$ |

**8.5.120 TG\_CFG21 (page=0x02 address=0x50) [reset=6Eh]**

Tone Generator 2 Freq Calc 2

**Table 219. Tone Generator 2 Freq Calc 2 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                              |
|-----|------------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG2_FREQ2[31:24] | RW   | 6Eh   | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.121 TG\_CFG22 (page=0x02 address=0x51) [reset=D9h]**

Tone Generator 2 Freq Calc 2

**Table 220. Tone Generator 2 Freq Calc 2 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                              |
|-----|------------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG2_FREQ2[23:16] | RW   | D9h   | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

**8.5.122 TG\_CFG23 (page=0x02 address=0x52) [reset=EBh]**

Tone Generator 2 Freq Calc 2

**Table 221. Tone Generator 2 Freq Calc 2 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                              |
|-----|-----------------|------|-------|--------------------------------------------------------------------------|
| 7-0 | TG2_FREQ2[15:8] | RW   | EBh   | $\text{round}((\sin(2 \cdot \pi \cdot f_{\text{tone}}/f_s))^2 \cdot 31)$ |

### 8.5.123 TG\_CFG24 (page=0x02 address=0x53) [reset=A1h]

Tone Generator 2 Freq Calc 2

**Table 222. Tone Generator 2 Freq Calc 2 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                         |
|-----|----------------|------|-------|---------------------------------------------------------------------|
| 7-0 | TG2_FREQ2[7:0] | RW   | A1h   | $\text{round}((\sin(2\pi \cdot f_{\text{tone}}/f_s)) \cdot 2^{31})$ |

### 8.5.124 TG\_CFG25 (page=0x02 address=0x54) [reset=0h]

Tone Generator 2 Freq Calc 3

**Table 223. Tone Generator 2 Freq Calc 3 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                      |
|-----|------------------|------|-------|------------------------------------------------------------------|
| 7-0 | TG2_FREQ3[31:24] | RW   | 0h    | $(\text{LCM}(2 \cdot f_s, f_{\text{tone}})/f_{\text{tone}}) - 2$ |

### 8.5.125 TG\_CFG26 (page=0x02 address=0x55) [reset=0h]

Tone Generator 2 Freq Calc 3

**Table 224. Tone Generator 2 Freq Calc 3 Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                      |
|-----|------------------|------|-------|------------------------------------------------------------------|
| 7-0 | TG2_FREQ3[23:16] | RW   | 0h    | $(\text{LCM}(2 \cdot f_s, f_{\text{tone}})/f_{\text{tone}}) - 2$ |

### 8.5.126 TG\_CFG27 (page=0x02 address=0x56) [reset=0h]

Tone Generator 2 Freq Calc 3

**Table 225. Tone Generator 2 Freq Calc 3 Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                      |
|-----|-----------------|------|-------|------------------------------------------------------------------|
| 7-0 | TG2_FREQ3[15:8] | RW   | 0h    | $(\text{LCM}(2 \cdot f_s, f_{\text{tone}})/f_{\text{tone}}) - 2$ |

### 8.5.127 TG\_CFG28 (page=0x02 address=0x57) [reset=2Ch]

Tone Generator 2 Freq Calc 3

**Table 226. Tone Generator 2 Freq Calc 3 Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                      |
|-----|----------------|------|-------|------------------------------------------------------------------|
| 7-0 | TG2_FREQ3[7:0] | RW   | 2Ch   | $(\text{LCM}(2 \cdot f_s, f_{\text{tone}})/f_{\text{tone}}) - 2$ |

### 8.5.128 TG\_CFG29 (page=0x02 address=0x58) [reset=8h]

Tone Generator 2 Amplitude Calc

**Table 227. Tone Generator 2 Amplitude Calc Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                     |
|-----|----------------|------|-------|-----------------------------------------------------------------|
| 7-0 | TG2_AMP[31:24] | RW   | 8h    | $\text{round}(10^{(\text{tone amplitude dB}/20)} \cdot 2^{31})$ |

### 8.5.129 TG\_CFG30 (page=0x02 address=0x59) [reset=9h]

Tone Generator 2 Amplitude Calc

**Table 228. Tone Generator 2 Amplitude Calc Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                     |
|-----|----------------|------|-------|-----------------------------------------------------------------|
| 7-0 | TG2_AMP[23:16] | RW   | 9h    | $\text{round}(10^{(\text{tone amplitude dB}/20)} \cdot 2^{31})$ |

**8.5.130 TG\_CFG31 (page=0x02 address=0x5A) [reset=BCh]**

Tone Generator 2 Amplitude Calc

**Table 229. Tone Generator 2 Amplitude Calc Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                     |
|-----|---------------|------|-------|-----------------------------------------------------------------|
| 7-0 | TG2_AMP[15:8] | RW   | BCh   | $\text{round}(10^{(\text{tone amplitude dB}/20)} \cdot 2^{31})$ |

**8.5.131 TG\_CFG32 (page=0x02 address=0x5B) [reset=C4h]**

Tone Generator 2 Amplitude Calc

**Table 230. Tone Generator 2 Amplitude Calc Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                     |
|-----|--------------|------|-------|-----------------------------------------------------------------|
| 7-0 | TG2_AMP[7:0] | RW   | C4h   | $\text{round}(10^{(\text{tone amplitude dB}/20)} \cdot 2^{31})$ |

**8.5.132 LD\_CFG0 (page=0x02 address=0x5C) [reset=64h]**

Load Diagnostics Resistance Upper Threshold

**Table 231. Load Diagnostics Resistance Upper Threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                               |
|-----|-------------------|------|-------|-------------------------------------------|
| 7-0 | LDG_RES_UT[31:24] | RW   | 64h   | $\text{round}(\text{ohm}/7 \cdot 2^{22})$ |

**8.5.133 LD\_CFG1 (page=0x02 address=0x5D) [reset=0h]**

Load Diagnostics Resistance Upper Threshold

**Table 232. Load Diagnostics Resistance Upper Threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                               |
|-----|-------------------|------|-------|-------------------------------------------|
| 7-0 | LDG_RES_UT[23:16] | RW   | 0h    | $\text{round}(\text{ohm}/7 \cdot 2^{22})$ |

**8.5.134 LD\_CFG2 (page=0x02 address=0x5E) [reset=0h]**

Load Diagnostics Resistance Upper Threshold

**Table 233. Load Diagnostics Resistance Upper Threshold Field Descriptions**

| Bit | Field            | Type | Reset | Description                               |
|-----|------------------|------|-------|-------------------------------------------|
| 7-0 | LDG_RES_UT[15:8] | RW   | 0h    | $\text{round}(\text{ohm}/7 \cdot 2^{22})$ |

**8.5.135 LD\_CFG3 (page=0x02 address=0x5F) [reset=0h]**

Load Diagnostics Resistance Upper Threshold

**Table 234. Load Diagnostics Resistance Upper Threshold Field Descriptions**

| Bit | Field           | Type | Reset | Description                               |
|-----|-----------------|------|-------|-------------------------------------------|
| 7-0 | LDG_RES_UT[7:0] | RW   | 0h    | $\text{round}(\text{ohm}/7 \cdot 2^{22})$ |

**8.5.136 LD\_CFG4 (page=0x02 address=0x60) [reset=0h]**

Load Diagnostics Resistance Lower Threshold

**Table 235. Load Diagnostics Resistance Lower Threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                               |
|-----|-------------------|------|-------|-------------------------------------------|
| 7-0 | LDG_RES_LT[31:24] | RW   | 0h    | $\text{round}(\text{ohm}/7 \cdot 2^{22})$ |

### 8.5.137 LD\_CFG5 (page=0x02 address=0x61) [reset=80h]

Load Diagnostics Resistance Lower Threshold

**Table 236. Load Diagnostics Resistance Lower Threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                   |
|-----|-------------------|------|-------|-------------------------------|
| 7-0 | LDG_RES_LT[23:16] | RW   | 80h   | round(ohm/7*2 <sup>22</sup> ) |

### 8.5.138 LD\_CFG6 (page=0x02 address=0x62) [reset=0h]

Load Diagnostics Resistance Lower Threshold

**Table 237. Load Diagnostics Resistance Lower Threshold Field Descriptions**

| Bit | Field            | Type | Reset | Description                   |
|-----|------------------|------|-------|-------------------------------|
| 7-0 | LDG_RES_LT[15:8] | RW   | 0h    | round(ohm/7*2 <sup>22</sup> ) |

### 8.5.139 LD\_CFG7 (page=0x02 address=0x63) [reset=0h]

Load Diagnostics Resistance Lower Threshold

**Table 238. Load Diagnostics Resistance Lower Threshold Field Descriptions**

| Bit | Field           | Type | Reset | Description                   |
|-----|-----------------|------|-------|-------------------------------|
| 7-0 | LDG_RES_LT[7:0] | RW   | 0h    | round(ohm/7*2 <sup>22</sup> ) |

### 8.5.140 IDC\_CFG0 (page=0x02 address=0x64) [reset=0h]

Idle channel detection threshold

**Table 239. Idle channel detection threshold Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                            |
|-----|----------------|------|-------|------------------------------------------------------------------------|
| 7-0 | IDC_DTH[31:24] | RW   | 0h    | round(10 <sup>^(idle channel threshold dB/20)</sup> *2 <sup>31</sup> ) |

### 8.5.141 IDC\_CFG1 (page=0x02 address=0x65) [reset=20h]

Idle channel detection threshold

**Table 240. Idle channel detection threshold Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                            |
|-----|----------------|------|-------|------------------------------------------------------------------------|
| 7-0 | IDC_DTH[23:16] | RW   | 20h   | round(10 <sup>^(idle channel threshold dB/20)</sup> *2 <sup>31</sup> ) |

### 8.5.142 IDC\_CFG2 (page=0x02 address=0x66) [reset=C4h]

Idle channel detection threshold

**Table 241. Idle channel detection threshold Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                            |
|-----|---------------|------|-------|------------------------------------------------------------------------|
| 7-0 | IDC_DTH[15:8] | RW   | C4h   | round(10 <sup>^(idle channel threshold dB/20)</sup> *2 <sup>31</sup> ) |

### 8.5.143 IDC\_CFG3 (page=0x02 address=0x67) [reset=9Ch]

Idle channel detection threshold

**Table 242. Idle channel detection threshold Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                            |
|-----|--------------|------|-------|------------------------------------------------------------------------|
| 7-0 | IDC_DTH[7:0] | RW   | 9Ch   | round(10 <sup>^(idle channel threshold dB/20)</sup> *2 <sup>31</sup> ) |

**8.5.144 IDC\_CFG7 (page=0x02 address=0x6C) [reset=0h]**

Hysteresis for idle channel detection

**Table 243. Hysteresis for idle channel detection Field Descriptions**

| Bit | Field           | Type | Reset | Description               |
|-----|-----------------|------|-------|---------------------------|
| 7-0 | IDC_HYST[31:24] | RW   | 0h    | round(time in seconds*fs) |

**8.5.145 IDC\_CFG8 (page=0x02 address=0x6D) [reset=0h]**

Hysteresis for idle channel detection

**Table 244. Hysteresis for idle channel detection Field Descriptions**

| Bit | Field           | Type | Reset | Description               |
|-----|-----------------|------|-------|---------------------------|
| 7-0 | IDC_HYST[23:16] | RW   | 0h    | round(time in seconds*fs) |

**8.5.146 IDC\_CFG9 (page=0x02 address=0x6E) [reset=12h]**

Hysteresis for idle channel detection

**Table 245. Hysteresis for idle channel detection Field Descriptions**

| Bit | Field          | Type | Reset | Description               |
|-----|----------------|------|-------|---------------------------|
| 7-0 | IDC_HYST[15:8] | RW   | 12h   | round(time in seconds*fs) |

**8.5.147 IDC\_CFG10 (page=0x02 address=0x6F) [reset=C0h]**

Hysteresis for idle channel detection

**Table 246. Hysteresis for idle channel detection Field Descriptions**

| Bit | Field         | Type | Reset | Description               |
|-----|---------------|------|-------|---------------------------|
| 7-0 | IDC_HYST[7:0] | RW   | C0h   | round(time in seconds*fs) |

**8.5.148 TF\_CFG\_1 (page=0x02 address=0x7C) [reset=72h]**

Thermal foldback limiter slope (in db/C)

**Table 247. Thermal foldback limiter slope (in db/C) Field Descriptions**

| Bit | Field          | Type | Reset | Description                                     |
|-----|----------------|------|-------|-------------------------------------------------|
| 7-0 | TF_LIMS[31:24] | RW   | 72h   | round( $10^{(-\text{slope}/20)} \cdot 2^{31}$ ) |

**8.5.149 TF\_CFG\_2 (page=0x02 address=0x7D) [reset=14h]**

Thermal foldback limiter slope (in db/C)

**Table 248. Thermal foldback limiter slope (in db/C) Field Descriptions**

| Bit | Field          | Type | Reset | Description                                     |
|-----|----------------|------|-------|-------------------------------------------------|
| 7-0 | TF_LIMS[23:16] | RW   | 14h   | round( $10^{(-\text{slope}/20)} \cdot 2^{31}$ ) |

**8.5.150 TF\_CFG\_3 (page=0x02 address=0x7E) [reset=82h]**

Thermal foldback limiter slope (in db/C)

**Table 249. Thermal foldback limiter slope (in db/C) Field Descriptions**

| Bit | Field         | Type | Reset | Description                                     |
|-----|---------------|------|-------|-------------------------------------------------|
| 7-0 | TF_LIMS[15:8] | RW   | 82h   | round( $10^{(-\text{slope}/20)} \cdot 2^{31}$ ) |

**8.5.151 TF\_CFG\_4 (page=0x02 address=0x7F) [reset=C0h]**

Thermal foldback limiter slope (in db/C)

**Table 250. Thermal foldback limiter slope (in db/C) Field Descriptions**

| Bit | Field        | Type | Reset | Description                                          |
|-----|--------------|------|-------|------------------------------------------------------|
| 7-0 | TF_LIMS[7:0] | RW   | C0h   | $\text{round}(10^{-(\text{slope}/20)} \cdot 2^{31})$ |

**8.5.152 PAGE4 (page=0x04 address=0x00) [reset=0h]**

The device's memory map is divided into pages and books. This register sets the page.

**Table 251. Device Page Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------|
| 7-0 | PAGE[7:0] | RW   | 0h    | Sets the device page.<br>00h = Page 0<br>01h = Page 1<br>...<br>FFh = Page 255 |

**8.5.153 LD\_CFG8 (page=0x04 address=0x18) [reset=0h]**

Load Resistance Value after load diagnostics is completed

**Table 252. Load Resistance Value after load diagnostics is completed Field Descriptions**

| Bit | Field              | Type | Reset | Description                                  |
|-----|--------------------|------|-------|----------------------------------------------|
| 7-0 | LD_RES_VAL1[31:24] | RW   | 0h    | $7 * ((\text{LD\_RES\_VAL1}) / 2^{22})$ ohms |

**8.5.154 LD\_CFG9 (page=0x04 address=0x19) [reset=0h]**

Load Resistance Value after load diagnostics is completed

**Table 253. Load Resistance Value after load diagnostics is completed Field Descriptions**

| Bit | Field              | Type | Reset | Description                                  |
|-----|--------------------|------|-------|----------------------------------------------|
| 7-0 | LD_RES_VAL1[23:16] | RW   | 0h    | $7 * ((\text{LD\_RES\_VAL1}) / 2^{22})$ ohms |

**8.5.155 LD\_CFG10 (page=0x04 address=0x1A) [reset=0h]**

Load Resistance Value after load diagnostics is completed

**Table 254. Load Resistance Value after load diagnostics is completed Field Descriptions**

| Bit | Field             | Type | Reset | Description                                  |
|-----|-------------------|------|-------|----------------------------------------------|
| 7-0 | LD_RES_VAL1[15:8] | RW   | 0h    | $7 * ((\text{LD\_RES\_VAL1}) / 2^{22})$ ohms |

**8.5.156 LD\_CFG11 (page=0x04 address=0x1B) [reset=0h]**

Load Resistance Value after load diagnostics is completed

**Table 255. Load Resistance Value after load diagnostics is completed Field Descriptions**

| Bit | Field            | Type | Reset | Description                                  |
|-----|------------------|------|-------|----------------------------------------------|
| 7-0 | LD_RES_VAL1[7:0] | RW   | 0h    | $7 * ((\text{LD\_RES\_VAL1}) / 2^{22})$ ohms |

**8.5.157 TF\_CFG4 (page=0x04 address=0x58) [reset=0h]**

Thermal foldback hold count (samples)

**Table 256. Thermal foldback hold count (samples) Field Descriptions**

| Bit | Field              | Type | Reset | Description           |
|-----|--------------------|------|-------|-----------------------|
| 7-0 | TF_HOLD_CNT[31:24] | RW   | 0h    | round(seconds * 1000) |

**8.5.158 TF\_CFG5 (page=0x04 address=0x59) [reset=0h]**

Thermal foldback hold count (samples)

**Table 257. Thermal foldback hold count (samples) Field Descriptions**

| Bit | Field              | Type | Reset | Description           |
|-----|--------------------|------|-------|-----------------------|
| 7-0 | TF_HOLD_CNT[23:16] | RW   | 0h    | round(seconds * 1000) |

**8.5.159 TF\_CFG6 (page=0x04 address=0x5A) [reset=0h]**

Thermal foldback hold count (samples)

**Table 258. Thermal foldback hold count (samples) Field Descriptions**

| Bit | Field             | Type | Reset | Description           |
|-----|-------------------|------|-------|-----------------------|
| 7-0 | TF_HOLD_CNT[15:8] | RW   | 0h    | round(seconds * 1000) |

**8.5.160 TF\_CFG7 (page=0x04 address=0x5B) [reset=64h]**

Thermal foldback hold count (samples)

**Table 259. Thermal foldback hold count (samples) Field Descriptions**

| Bit | Field            | Type | Reset | Description           |
|-----|------------------|------|-------|-----------------------|
| 7-0 | TF_HOLD_CNT[7:0] | RW   | 64h   | round(seconds * 1000) |

**8.5.161 TF\_CFG8 (page=0x04 address=0x5C) [reset=40h]**

Thermal foldback limiter release rate (db/samples)

**Table 260. Thermal foldback limiter release rate (db/samples) Field Descriptions**

| Bit | Field              | Type | Reset | Description                                       |
|-----|--------------------|------|-------|---------------------------------------------------|
| 7-0 | TF_REL_RATE[31:24] | RW   | 40h   | round( $10^{(dB \text{ per sample}/20)*2^{30}}$ ) |

**8.5.162 TF\_CFG9 (page=0x04 address=0x5D) [reset=BDh]**

Thermal foldback limiter release rate (db/samples)

**Table 261. Thermal foldback limiter release rate (db/samples) Field Descriptions**

| Bit | Field              | Type | Reset | Description                                       |
|-----|--------------------|------|-------|---------------------------------------------------|
| 7-0 | TF_REL_RATE[23:16] | RW   | BDh   | round( $10^{(dB \text{ per sample}/20)*2^{30}}$ ) |

**8.5.163 TF\_CFG10 (page=0x04 address=0x5E) [reset=B7h]**

Thermal foldback limiter release rate (db/samples)

**Table 262. Thermal foldback limiter release rate (db/samples) Field Descriptions**

| Bit | Field             | Type | Reset | Description                                       |
|-----|-------------------|------|-------|---------------------------------------------------|
| 7-0 | TF_REL_RATE[15:8] | RW   | B7h   | round( $10^{(dB \text{ per sample}/20)*2^{30}}$ ) |

#### 8.5.164 TF\_CFG11 (page=0x04 address=0x5F) [reset=B0h]

Thermal foldback limiter release rate (db/samples)

**Table 263. Thermal foldback limiter release rate (db/samples) Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                 |
|-----|------------------|------|-------|-------------------------------------------------------------|
| 7-0 | TF_REL_RATE[7:0] | RW   | B0h   | $\text{round}(10^{(\text{dB per sample}/20)} \cdot 2^{30})$ |

#### 8.5.165 TF\_CFG12 (page=0x04 address=0x60) [reset=39h]

Thermal foldback limiter temperature threshold

**Table 264. Thermal foldback limiter temperature threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                 |
|-----|-------------------|------|-------|-------------------------------------------------------------|
| 7-0 | TF_TEMP_TH[31:24] | RW   | 39h   | $\text{round}(\text{temperature in degree C} \cdot 2^{23})$ |

#### 8.5.166 TF\_CFG13 (page=0x04 address=0x61) [reset=82h]

Thermal foldback limiter temperature threshold

**Table 265. Thermal foldback limiter temperature threshold Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                 |
|-----|-------------------|------|-------|-------------------------------------------------------------|
| 7-0 | TF_TEMP_TH[23:16] | RW   | 82h   | $\text{round}(\text{temperature in degree C} \cdot 2^{23})$ |

#### 8.5.167 TF\_CFG14 (page=0x04 address=0x62) [reset=60h]

Thermal foldback limiter temperature threshold

**Table 266. Thermal foldback limiter temperature threshold Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                 |
|-----|------------------|------|-------|-------------------------------------------------------------|
| 7-0 | TF_TEMP_TH[15:8] | RW   | 60h   | $\text{round}(\text{temperature in degree C} \cdot 2^{23})$ |

#### 8.5.168 TF\_CFG16 (page=0x04 address=0x63) [reset=7Fh]

Thermal foldback limiter temperature threshold

**Table 267. Thermal foldback limiter temperature threshold Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                 |
|-----|-----------------|------|-------|-------------------------------------------------------------|
| 7-0 | TF_TEMP_TH[7:0] | RW   | 7Fh   | $\text{round}(\text{temperature in degree C} \cdot 2^{23})$ |

#### 8.5.169 TF\_CFG17 (page=0x04 address=0x64) [reset=2Dh]

Thermal foldback max gain reduction (dB)

**Table 268. Thermal foldback max gain reduction (dB) Field Descriptions**

| Bit | Field               | Type | Reset | Description                                               |
|-----|---------------------|------|-------|-----------------------------------------------------------|
| 7-0 | TF_MAX_ATTEN[31:24] | RW   | 2Dh   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

#### 8.5.170 TF\_CFG18 (page=0x04 address=0x65) [reset=6Ah]

Thermal foldback max gain reduction (dB)

**Table 269. Thermal foldback max gain reduction (dB) Field Descriptions**

| Bit | Field               | Type | Reset | Description                                               |
|-----|---------------------|------|-------|-----------------------------------------------------------|
| 7-0 | TF_MAX_ATTEN[23:16] | RW   | 6Ah   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

**8.5.171 TF\_CFG19 (page=0x04 address=0x66) [reset=86h]**

Thermal foldback max gain reduction (dB)

**Table 270. Thermal foldback max gain reduction (dB) Field Descriptions**

| Bit | Field              | Type | Reset | Description                                               |
|-----|--------------------|------|-------|-----------------------------------------------------------|
| 7-0 | TF_MAX_ATTEN[15:8] | RW   | 86h   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

**8.5.172 TF\_CFG20 (page=0x04 address=0x67) [reset=6Fh]**

Thermal foldback max gain reduction (dB)

**Table 271. Thermal foldback max gain reduction (dB) Field Descriptions**

| Bit | Field             | Type | Reset | Description                                               |
|-----|-------------------|------|-------|-----------------------------------------------------------|
| 7-0 | TF_MAX_ATTEN[7:0] | RW   | 6Fh   | $\text{round}(10^{(\text{max attn dB}/20)} \cdot 2^{31})$ |

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TAS2110 is a digital input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-H boost converter. In auto passthrough mode, the Class-H boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. It is recommended to configure the TAS2110 using [PurePath™ Console 3 Software](#).

### 9.2 Typical Application

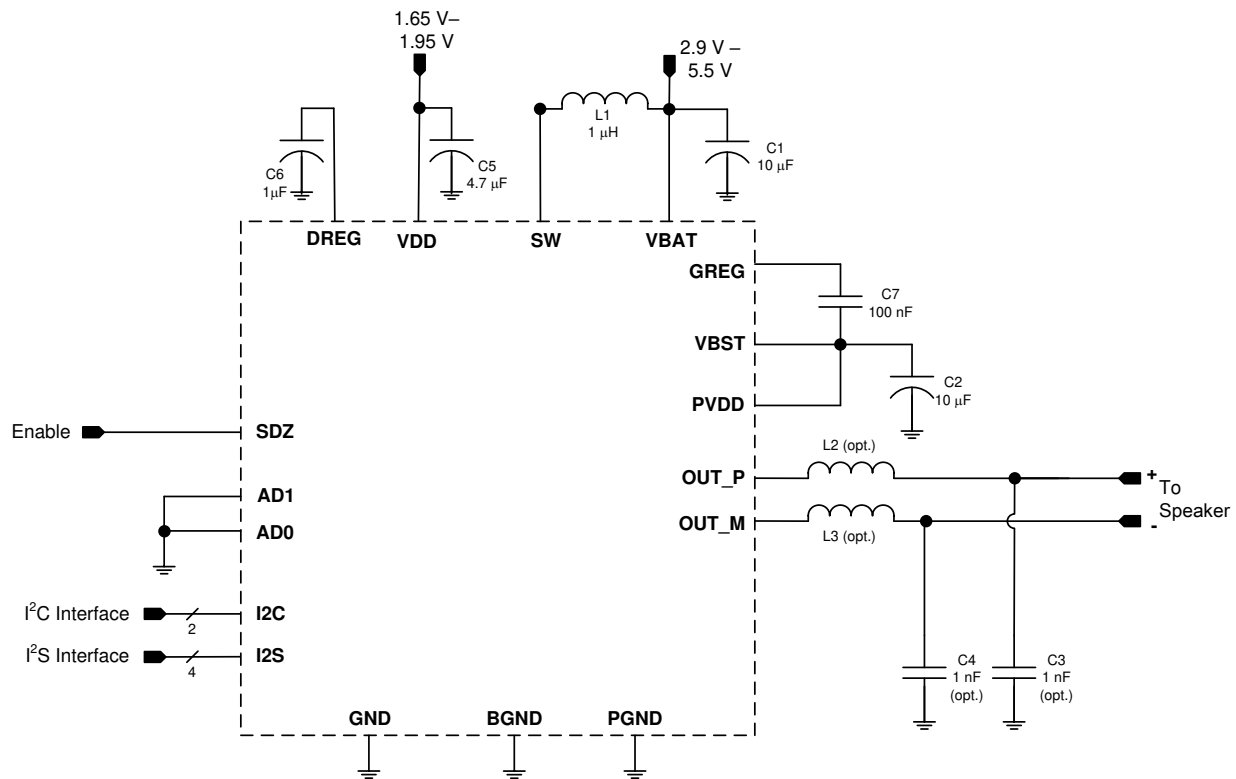


Figure 50. Typical Application - Digital Audio Input

Table 272. Recommended External Components

| COMPONENT | DESCRIPTION                             | SPECIFICATION             | MIN  | TYP | MAX | UNIT |
|-----------|-----------------------------------------|---------------------------|------|-----|-----|------|
| L1        | Boost Converter Inductor <sup>(1)</sup> | Inductance, 20% Tolerance | 0.47 | 1   |     | µH   |
|           |                                         | Saturation Current        |      | 4.5 |     | A    |

(1) See section [Boost Converter Passive Devices](#) for additional requirements on derating, stability, and inductor value trade-offs.

## Typical Application (continued)

**Table 272. Recommended External Components (continued)**

| COMPONENT        | DESCRIPTION                                                                                                                                                              | SPECIFICATION                  | MIN | TYP  | MAX   | UNIT          |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----|------|-------|---------------|
| R2,R3            | EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. TAS2110 is a filter-less Class-D and does not require these bead inductors. | Impedance at 100 MHz           |     | 120  |       | $\Omega$      |
|                  |                                                                                                                                                                          | DC Resistance                  |     |      | 0.095 | $\Omega$      |
|                  |                                                                                                                                                                          | DC Current                     |     |      | 2     | A             |
|                  |                                                                                                                                                                          | Size                           |     | 0402 |       | EIA           |
| C1,C2,C3,C4      | Boost Converter Input Capacitor <sup>(1)</sup>                                                                                                                           | Capacitance, 20% Tolerance     | 10  |      |       | $\mu\text{F}$ |
| C6,C7,C9,C15,C16 | Boost Converter Output Capacitor                                                                                                                                         | Type                           | X5R |      |       |               |
|                  |                                                                                                                                                                          | Capacitance, 20% Tolerance     | 10  |      | 47    | $\mu\text{F}$ |
|                  |                                                                                                                                                                          | Rated Voltage                  | 16  |      |       | V             |
|                  |                                                                                                                                                                          | Capacitance at 11.5 V derating | 3.3 |      |       | $\mu\text{F}$ |
| C13,C14          | EMI Filter Capacitors (optional, must use R2, R3 if C13, C14 used)                                                                                                       | Capacitance                    |     | 1    |       | nF            |
| C5,C8            | VDD Decoupling Capacitor                                                                                                                                                 | Capacitance                    | 4.7 |      |       | $\mu\text{F}$ |
| C11,C12          | DREG Decoupling Capacitor                                                                                                                                                | Capacitance                    | 1   |      |       | $\mu\text{F}$ |
| C10              | GREG Fly Capacitor                                                                                                                                                       | Capacitance                    | 100 |      |       | nF            |

### 9.2.1 Design Requirements

For given design example, use the parameters shown in [Table 273](#)

**Table 273. Design Parameters**

| DESIGN PARAMETER             | EXAMPLE VALUE                   |
|------------------------------|---------------------------------|
| Audio Input                  | Digital Audio, I <sup>2</sup> S |
| Mono or Stereo Configuration | Mono                            |
| Max Output Power at 1% THD+N | 5.0 W                           |

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See [Device Mode and Address Selection](#) for information on changing the I<sup>2</sup>C address of the TAS2110 to support stereo operation. Mono or stereo configuration does not impact the device performance.

#### 9.2.2.2 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in [Figure 50](#) and whose specifications are provided in [Table 272](#). These specifications are based on the design of the TAS2110 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

Additionally, the ratio of L1/C2 (the derated value of C2 at 11.5 V should be used in this ratio) has to be lesser than 1/3 for boost stability. This 1/3 ratio should be maintained including the worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be  $\geq 0.47 \mu\text{H}$  at the boost switching frequency (100 kHz to 4 MHz). Using a  $0.47 \mu\text{H}$  will have more boost ripple than a  $1.0 \mu\text{H}$  or  $2.2 \mu\text{H}$  but the high PSRR should minimize the effect from the additional ripple. Finally, the minimum C2 (derated value at programmed boost voltage) should be >  $3.3 \mu\text{F}$  for Class-D power delivery specification.

#### 9.2.2.3 EMI Passive Devices

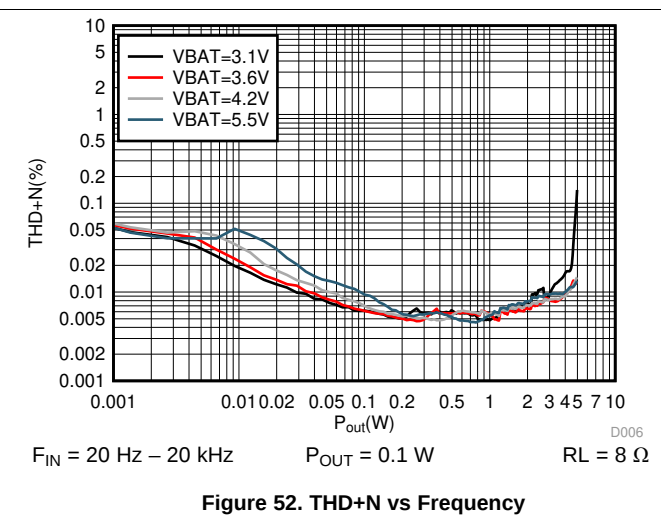
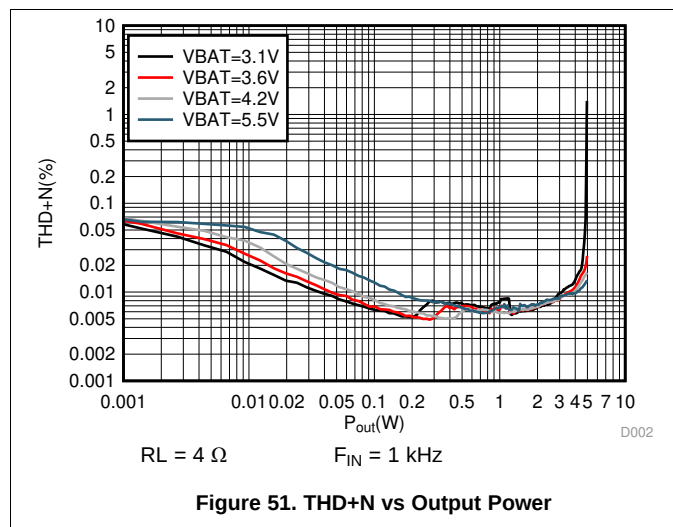
The system designer may want to include passive devices on the Class-D output . These passive devices that are labeled L2, L3, C3 and C4 in [Figure 50](#) and their recommended specifications are provided in [Table 272](#). If C3 and C4 are used, L2 and L3 must also be installed, and C3 and C4 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

### 9.2.2.4 Miscellaneous Passive Devices

The GREG Capacitor requires 100 nF to meet boost and Class-D power delivery and efficiency specs. For best device performance, the GREG capacitor should be placed very close to the device, star connected to PVDD and be routed with wide traces to minimize the impact of PCB parasitic effects.

DREG Capacitor should be placed and Ground Loop closed next to device. DREG is internal supply(1.5V typical, functional min of 1.35V) generated from external VDD supply. For best performance, noise on VDD should be reduced by wide traces or higher caps on VDD next to device based on board routings.

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

### 10.1 Power Supplies

The TAS2110 requires four power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 2.9 V to 5.5 V
  - Max Current: 5 A for ILIM = 4.0 A (default)
- Analog Supply (terminal: VDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- Internal Supplies
  - Digital Supply (terminal: DREG): 1.35 V to 1.65 V
  - Boost Output (terminal: VBST) : VBAT to 13V
  - Class-D Power Supply (terminal: PVDD): Short to VBST

The decoupling capacitors for the power supplies should be placed close to the device terminals.

### 10.2 Power Supply Sequencing

The power rail may be brought up and down in any order. There is no requirement on sequencing. However if VDD is present without VBAT an additional rise in VDD current will be observed until VBAT is present.

When the supplies have settled, the SDZ terminal can be set HIGH to operate the device. Additionally the SDZ pin can be tied to VDD and the internal POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100  $\mu$ s to allow the OTP to load. The above sequence should be completed before any I<sup>2</sup>C operation.

In External PVDD Case, User need to ensure that PVDD does not drop below VBAT-0.7V.

#### 10.2.1 Boost Supply Details

The boost supply (VBAT) and associated passives need to be able to support the current requirements of the device. By default, the peak current limit of the boost is set to 4 A. Refer to [Table 86](#) for information on changing the current limit. A minimum of a 10  $\mu$ F capacitor is recommended on the boost supply to quickly support changes in required current. Refer to [Figure 50](#) for the schematic.

The current requirements can also be reduced by lowering the gain of the amplifier, or in response to decreasing battery through the use of the battery-tracking feature of the TAS2110 described in [Supply Tracking Limiters with Brown Out Prevention](#).

## 11 Layout

### 11.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VBST and Ground close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBAT and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Minimize trace inductance between the GREG capacitor and TAS2564. This can be done by using multiple vias in parallel and by using wide routes where possible. This capacitor should have a star connection to PVDD.
- Do not use VIAS for traces that carry high current. These include the traces for VBST, SW, VBAT, PGND and the speaker OUT\_P, OUT\_M.
- SW, OUT\_P and OUT\_M are high switching nets and keep out should be kept from these signals to prevent corruption of digital signals.
- Use epoxy filled vias for the interior pads.
- EMI ferrites must be used if EMI capacitors are used on OUT\_P, OUT\_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in [Figure 50](#) and described in [Power Supplies](#).
- Place EMI ferrites, if used, close to the device.

**Table 274. Pin Layout Guidelines**

| PIN                   | MAX PARASITIC INDUCTANCE | LAYOUT RECOMMENDATIONS                                                                                                                                                                                                                                                                                                        |
|-----------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BGND, GND, PGND, GNDD | 150 pH                   | Short BGND, GND, GNDD, PGND below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible                                                                                                                                                                    |
| DREG                  | 500 pH                   | Bypass to GND with capacitor recommended in <a href="#">Table 272</a> . Do not connect to external load. Both ends of decoupling cap should see as low inductance as possible between this pin and gnd pins.                                                                                                                  |
| GREG                  | 200 pH                   | Connect it to PVDD with a star connection and not to boost plane with recommended in <a href="#">Table 272</a> . Do not connect to external load.                                                                                                                                                                             |
| PVDD                  | 100 pH                   | Short it to VBST(boost) plane through strong connection. Connect it to GREG with a star connection and not to boost plane.                                                                                                                                                                                                    |
| SW                    |                          | Connect to VBAT with boost inductor recommended in <a href="#">Table 272</a> . Reduce parasitic capacitor and resistance for efficiency. Boost inductor should be as close as possible to the SW pin. Inductor should be connected to SW through thick plane. Traces should support currents up to device over-current limit. |
| VBAT                  | 500 pH                   | Bypass to GND with capacitor recommended in <a href="#">Table 272</a> . Should be connected to inductor through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBAT pin and PGND pin.                                                                                        |
| VBST                  | 100 pH                   | Do not connect to external load. Bypass to GND with capacitor recommended in <a href="#">Table 272</a> . Connect to PVDD through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBST pin and BGND pin. Traces should support currents up to device over-current limit.       |
| VDD                   | 200 pH                   | Bypass to GND with capacitor recommended in <a href="#">Table 272</a> . Both the end of decoupling cap should see as low inductance as possible between this pin and GND pin                                                                                                                                                  |

## 11.2 Layout Example

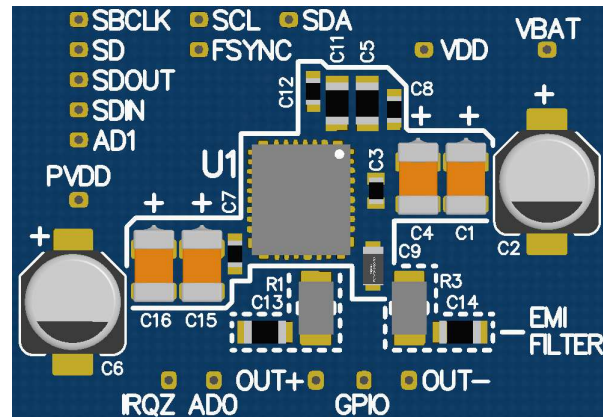


Figure 53. Board Layout- Top

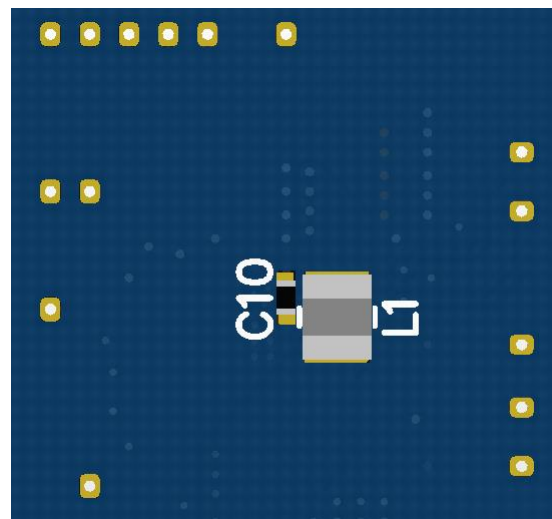


Figure 54. Board Layout- Bottom

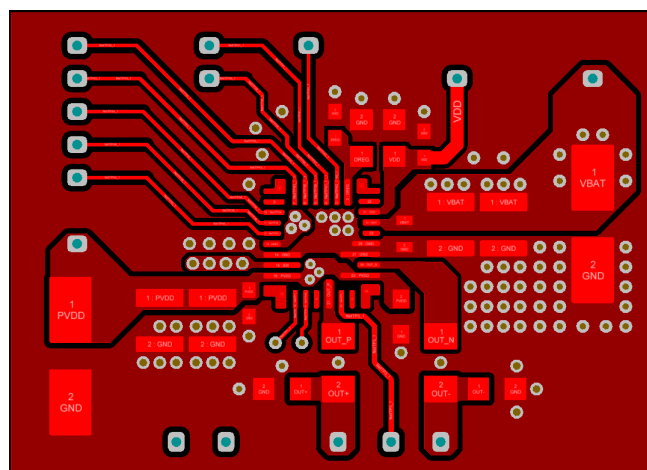


Figure 55. Top Copper

## Layout Example (continued)

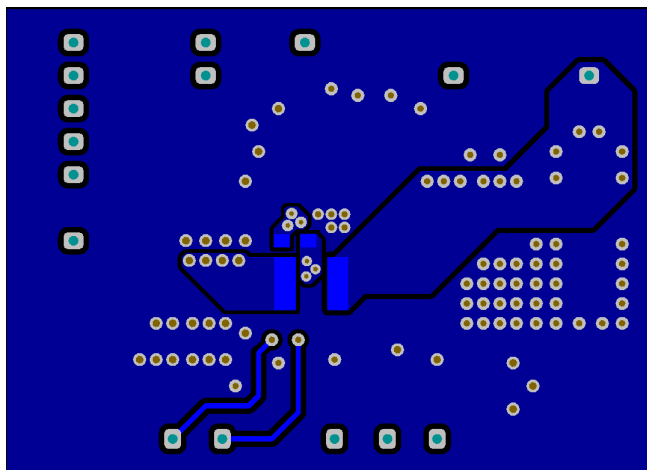


Figure 56. Bottom Copper

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following: [TAS2563YBGEVM-DC Evaluation module user's guide](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

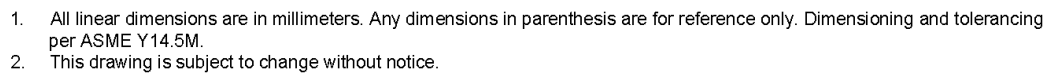
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PLASTIC QUAD FLAT PACK- NO LEAD



## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins     | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TAS2110RPPR</a> | Active        | Production           | VQFN-HR (RPP)   32 | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | TAS2110             |
| TAS2110RPPR.A               | Active        | Production           | VQFN-HR (RPP)   32 | 3000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | TAS2110             |
| <a href="#">TAS2110RPPT</a> | Active        | Production           | VQFN-HR (RPP)   32 | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | TAS2110             |
| TAS2110RPPT.A               | Active        | Production           | VQFN-HR (RPP)   32 | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | TAS2110             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

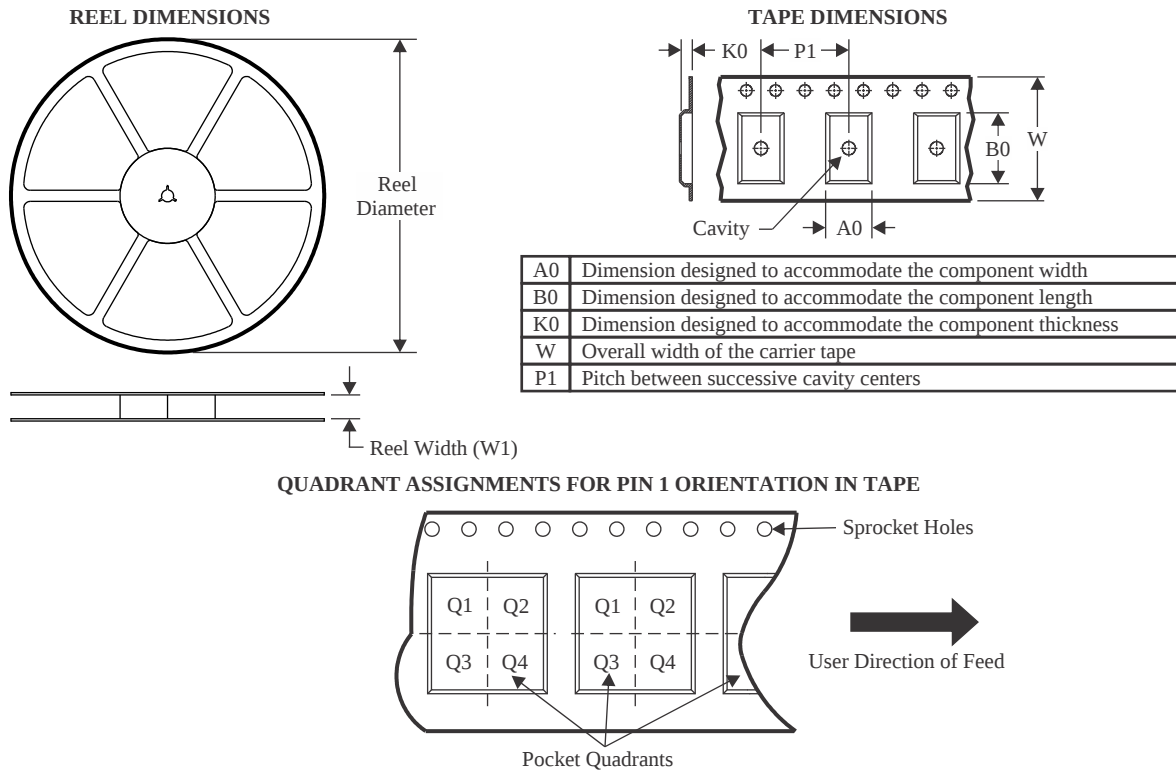
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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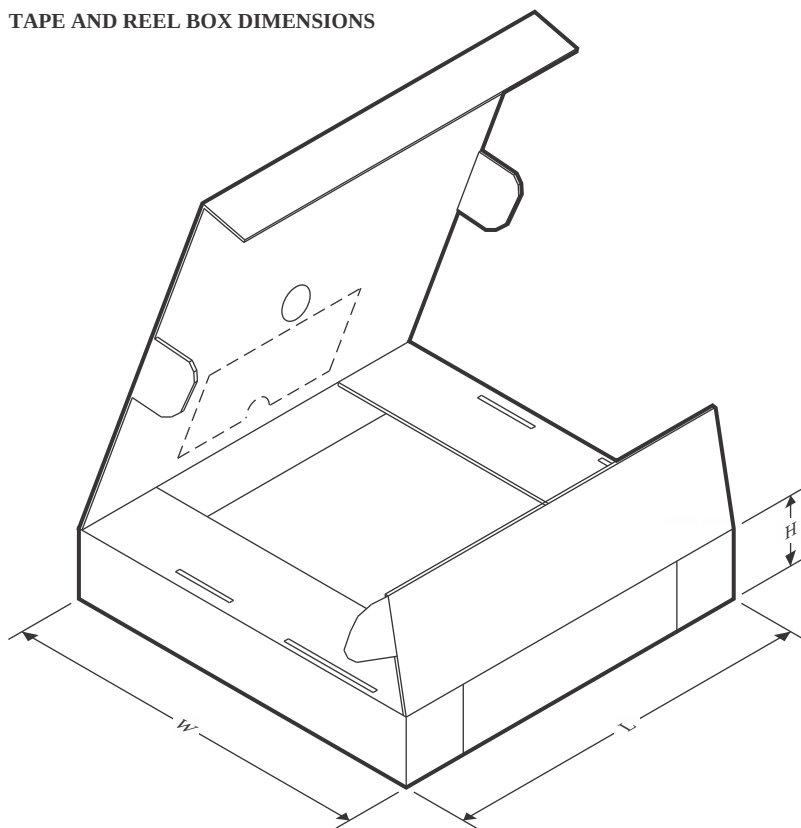
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS2110RPPR | VQFN-HR      | RPP             | 32   | 3000 | 330.0              | 12.4               | 4.3     | 4.8     | 1.2     | 8.0     | 12.0   | Q2            |
| TAS2110RPPT | VQFN-HR      | RPP             | 32   | 250  | 180.0              | 12.4               | 4.3     | 4.8     | 1.2     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS2110RPPR | VQFN-HR      | RPP             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TAS2110RPPT | VQFN-HR      | RPP             | 32   | 250  | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

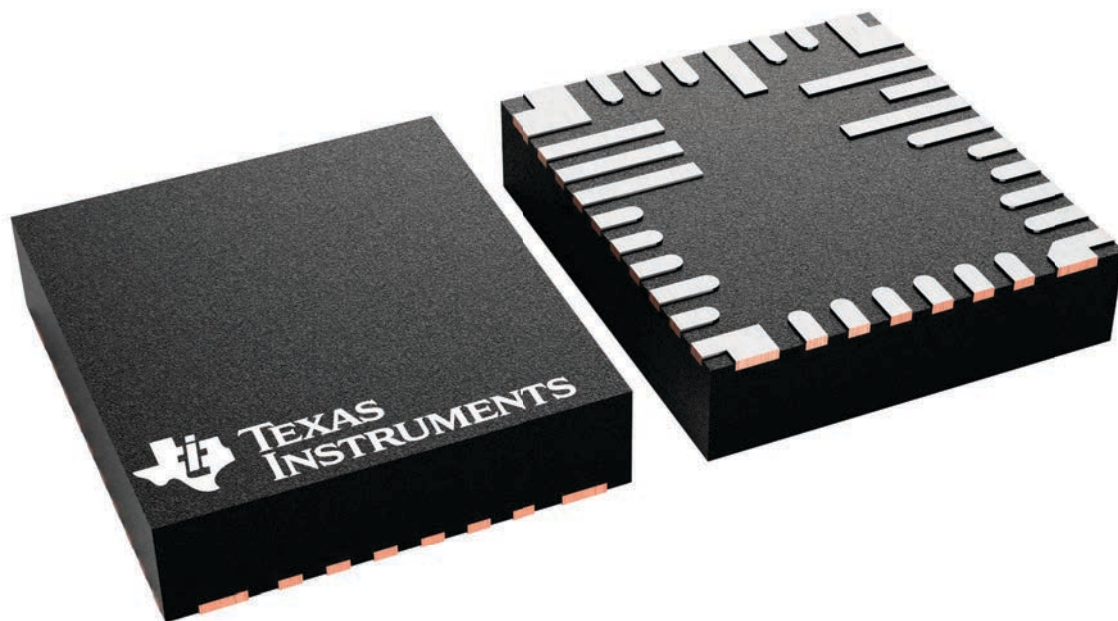
**RPP 32**

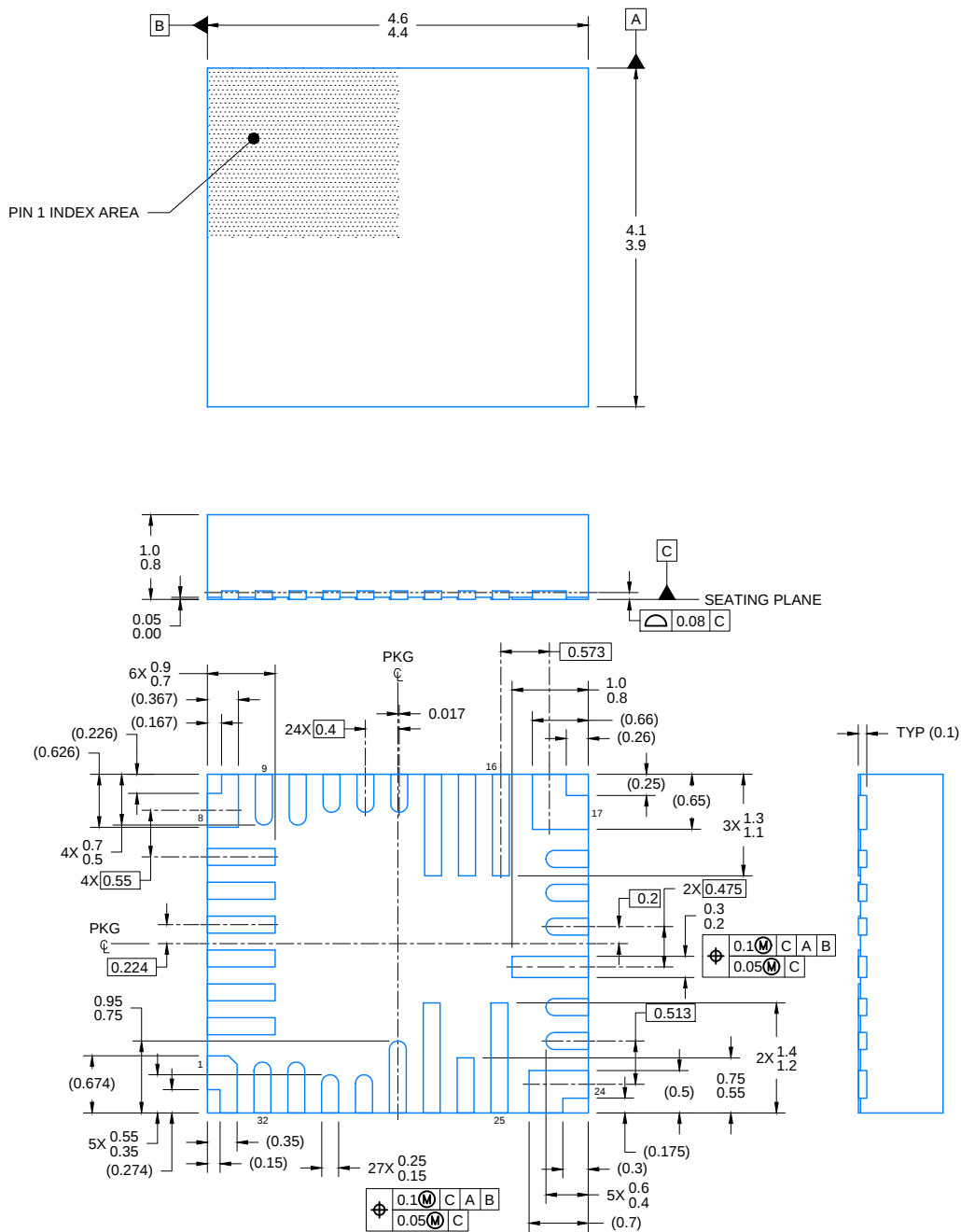
**VQFN-HR - 1.0 mm max height**

4.5 x 4, 0.4 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

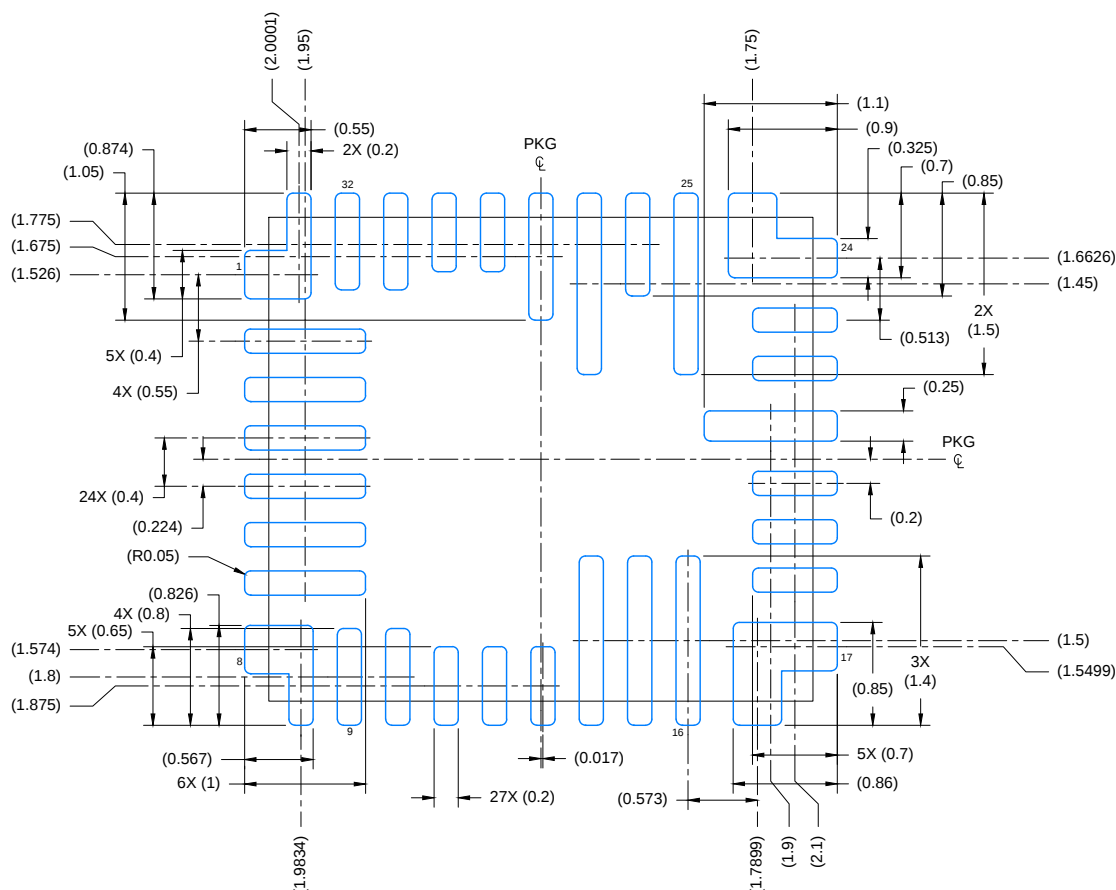




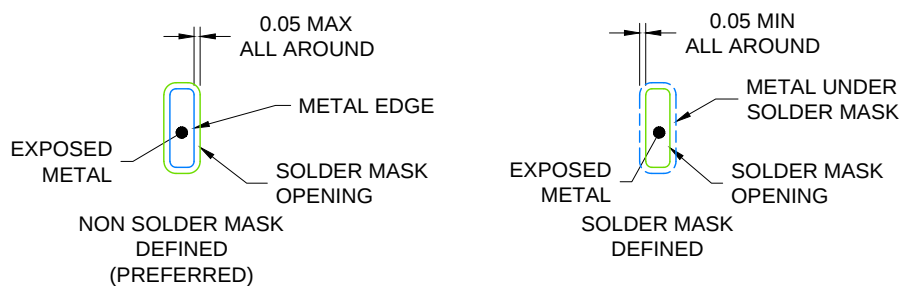
4224769/A 01/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 16X



## SOLDER MASK DETAILS

4224769/A 01/2019

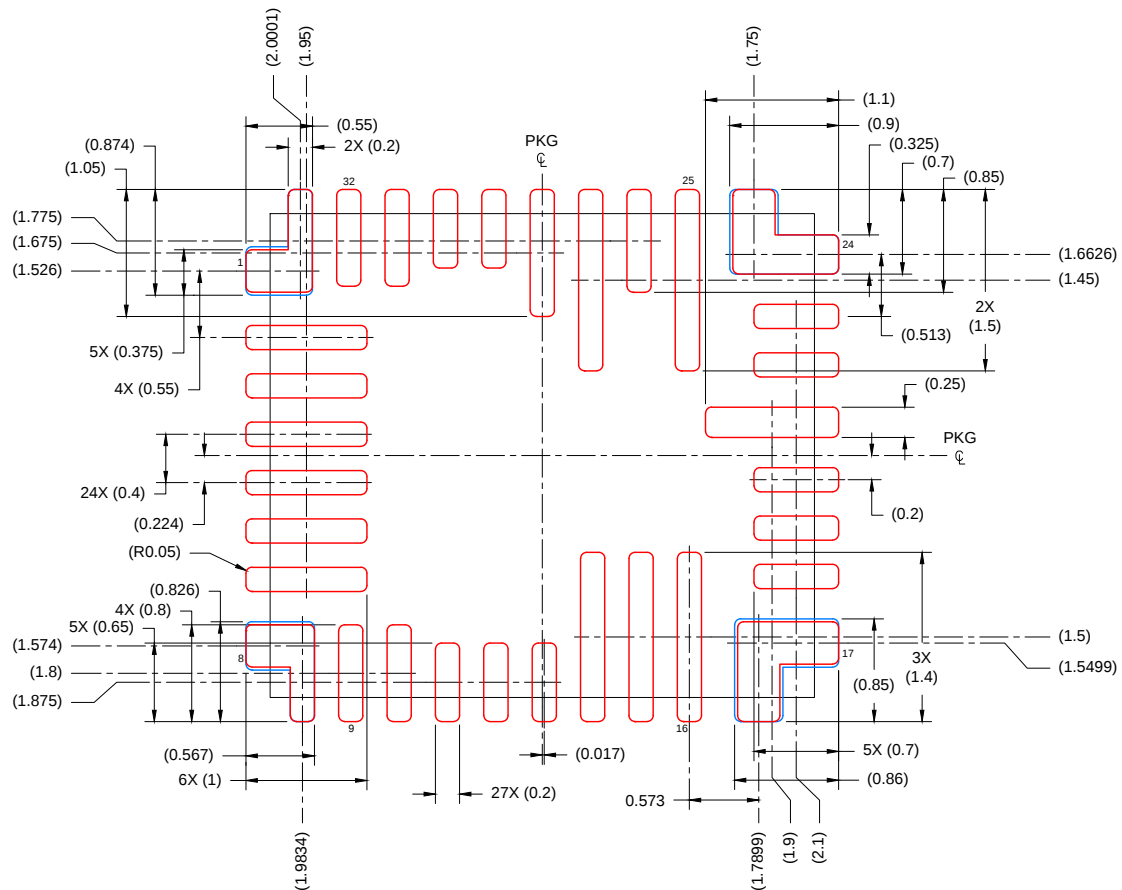
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).

**RPP0032A**

## VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.100mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

PAD 1: 93% , PAD 8: 92%, PAD 17: 87%, PAD 24: 94%

SCALE: 16X

4224769/A 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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