

# TAA3020 2 チャンネル、768kHz、104dB ダイナミックレンジのオーディオ ADC

## 1 特長

- マルチチャンネルの高性能 ADC:
  - 2 チャンネルのアナログ マイクロフォンまたはライン入力
  - 4 チャンネルのデジタル PDM マイクロフォン
  - 最大 2 つのアナログおよび最大 2 つのデジタル マイクロフォン チャンネル
- ADC ラインおよびマイクロフォンの差動入力性能:
  - ダイナミックレンジ (DR) 104 dB
  - THD+N: -95 dB
- ADC チャンネル合計モード、DR 性能:
  - 107dB (2 チャンネル加算)
- ADC 入力電圧:
  - 差動、 $2V_{RMS}$  フルスケール入力
  - シングルエンド、 $1V_{RMS}$  フルスケール入力
- ADC サンプル・レート ( $f_S$ ): 8kHz ~ 768kHz
- プログラム可能なチャンネル設定:
  - チャンネル ゲイン: 0.5dB 刻みで 0dB ~ 42dB
  - デジタル ボリューム制御: -100dB ~ 27dB
  - 0.1dB 分解能のゲイン較正
  - 163ns 分解能の位相較正
- マイクロフォンのバイアスまたは電源電圧の生成をプログラム可能
- 低遅延信号処理フィルタの選択
- HPF およびバイカッド デジタル フィルタをプログラム可能
- 自動ゲイン コントローラ (AGC)
- 音声アクティビティ検出 (VAD)
- I<sup>2</sup>C 制御インターフェイス
- 高性能オーディオ PLL を内蔵
- クロック分周器の設定を自動的に構成
- オーディオ シリアル データ インターフェイス
  - フォーマット: TDM、I<sup>2</sup>S、左揃え (LJ)
  - ワード長: 16 ビット、20 ビット、24 ビット、32 ビット
  - マスタまたはスレーブ インターフェイス
- 単一電源動作: 3.3V または 1.8V
- I/O 電源動作: 3.3V または 1.8V
- 1.8A VDD 電源での消費電力:
  - 9.5mW/チャンネル (サンプル レート: 48kHz)

## 3 概要

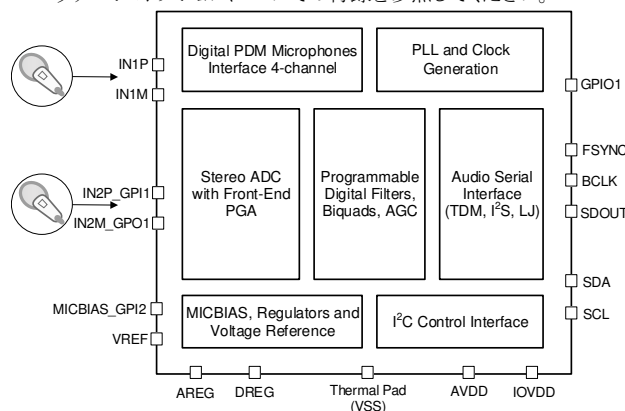
TAA3020 は、パルス密度変調 (PDM) マイクロフォン入力用の最大 2 つのアナログ チャンネル、または 4 つのデジタル チャンネルを同時にサンプリングできる、高性能オーディオ A/D コンバータ (ADC) です。このデバイスは、ラインおよびマイクロフォン入力をサポートし、シングルエンドおよび差動入力構成が可能です。このデバイスには、プログラム可能なチャンネル ゲイン、デジタル ボリューム制御、プログラム可能なマイクロフォン バイアス電圧、フェーズ ロック ループ (PLL)、プログラム可能なハイパス フィルタ (HPF)、バイカッド フィルタ、低遅延フィルタ モードが搭載されており、最高 768kHz のサンプル レートに対応できます。このデバイスは時分割多重化 (TDM)、I<sup>2</sup>S、左揃え (LJ) オーディオ フォーマットに対応し、I<sup>2</sup>C インターフェイスで制御可能です。これらの高性能機能を搭載しており、1.8V または 3.3V の単一電源で動作できることから、遠距離マイクロフォン録音アプリケーションの、スペースの制約が厳しいオーディオ システムに最適です。

TAA3020 は -40°C ~ +105°C で動作が規定されており、20 ピンの WQFN パッケージで供給されます。

### 製品情報 (1)

| 部品番号    | パッケージ     | 本体サイズ (公称)                |
|---------|-----------|---------------------------|
| TAA3020 | WQFN (20) | 3.00mm × 3.00mm、0.5mm ピッチ |

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。



### 概略ブロック図

## 2 アプリケーション

- スマート スピーカ
- IP ネットワーク カメラ
- 業務用マイク / ワイヤレス システム
- テレビ会議システム



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## 4 Pin Configuration and Functions

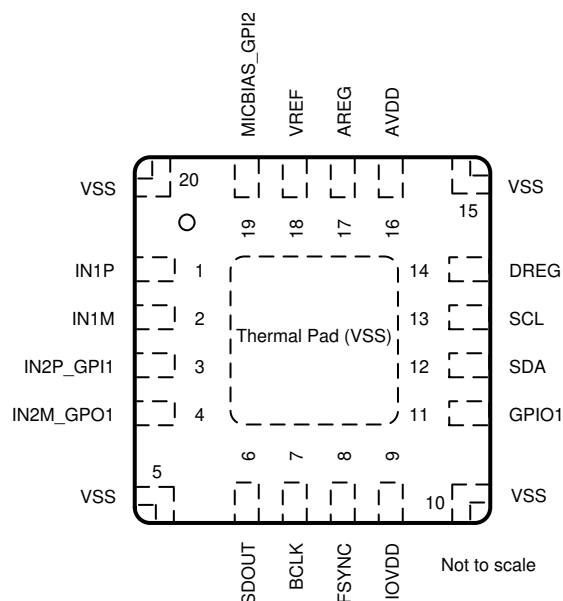


図 4-1. RTE Package, 20-Pin WQFN With Exposed Thermal Pad, Top View

表 4-1. Pin Functions

| NO. | PIN<br>NAME | TYPE                        | DESCRIPTION  |
|-----|-------------|-----------------------------|--|
|     |             |                             |  |
| 1   | IN1P        | Analog input                | Analog input 1P pin  |
| 2   | IN1M        | Analog input                | Analog input 1M pin  |
| 3   | IN2P_GPI1   | Analog input/digital input  | Analog input 2P pin or general-purpose digital input 1 (multipurpose functions such as digital microphones data, PLL input clock source, and so forth).  |
| 4   | IN2M_GPO1   | Analog input/digital output | Analog input 2M pin or general-purpose digital output 1 (multipurpose functions such as digital microphone clock, interrupt, and so forth).  |
| 5   | VSS         | Ground supply               | Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions. |
| 6   | SDOUT       | Digital output              | Audio serial data interface bus output   |
| 7   | BCLK        | Digital I/O                 | Audio serial data interface bus bit clock  |
| 8   | FSYNC       | Digital I/O                 | Audio serial data interface bus frame synchronization signal   |
| 9   | IOVDD       | Digital supply              | Digital I/O power supply (1.8V or 3.3V, nominal)   |
| 10  | VSS         | Ground supply               | Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions. |
| 11  | GPIO1       | Digital I/O                 | General-purpose digital input/output 1 (multipurpose functions such as digital microphones clock or data, PLL input clock source, interrupt, and so forth).  |
| 12  | SDA         | Digital I/O                 | Data pin for I <sup>2</sup> C control bus  |
| 13  | SCL         | Digital input               | Clock pin for I <sup>2</sup> C control bus   |
| 14  | DREG        | Digital supply              | Digital regulator output voltage for digital core supply (1.5V, nominal). Connect a 10-μF and 0.1μF low ESR capacitor in parallel to device ground (VSS).  |
| 15  | VSS         | Ground supply               | Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions. |
| 16  | AVDD        | Analog supply               | Analog power (1.8V or 3.3V, nominal)   |

表 4-1. Pin Functions (続き)

| PIN         |                   | TYPE                        | DESCRIPTION   |
|-------------|-------------------|-----------------------------|---|
| NO.         | NAME              |                             |   |
| 17          | AREG              | Analog supply               | Analog on-chip regulator output voltage for analog supply (1.8V, nominal) or external analog power (1.8V, nominal). Connect a 10μF and 0.1μF low ESR capacitor in parallel to analog ground (AVSS).                                 |
| 18          | VREF              | Analog                      | Analog reference voltage filter output. Connect a 1μF capacitor to analog ground (AVSS).  |
| 19          | MICBIAS_GPI2      | Analog output/digital input | MICBIAS output or general-purpose digital input 2 (multipurpose functions such as digital microphones data, PLL input clock source, and so forth). If used as MICBIAS output, then connect a 1μF capacitor to analog ground (AVSS). |
| 20          | VSS               | Ground supply               | Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions.                                  |
| Thermal Pad | Thermal Pad (VSS) | Ground supply               | Thermal pad shorted to internal device ground. Short the thermal pad directly to the board ground plane.  |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|                            |   | MIN  | MAX         | UNIT |
|----------------------------|---|------|-------------|------|
| Supply voltage             | AVDD to AVSS  | −0.3 | 3.9         | V    |
|                            | AREG to AVSS  | −0.3 | 2.0         |      |
|                            | IOVDD to VSS (thermal pad)  | −0.3 | 3.9         |      |
| Ground voltage differences | AVSS to VSS (thermal pad)   | −0.3 | 0.3         | V    |
| Analog input voltage       | Analog input pins voltage to AVSS   | −0.3 | AVDD + 0.3  | V    |
| Digital input voltage      | Digital input except IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad) | −0.3 | IOVDD + 0.3 | V    |
|                            | Digital input IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)        | −0.3 | AVDD + 0.3  |      |
| Temperature                | Operating ambient, T <sub>A</sub>   | −40  | 105         | °C   |
|                            | Junction, T <sub>J</sub>  | −40  | 150         |      |
|                            | Storage, T <sub>slg</sub>   | −65  | 150         |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

|                           |   | MIN  | NOM | MAX    | UNIT |
|---------------------------|---|------|-----|--------|------|
| POWER                     |   |      |     |        |      |
| AVDD, AREG <sup>(1)</sup> | Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator): AVDD 3.3-V operation     | 3.0  | 3.3 | 3.6    | V    |
|                           | Analog supply voltage AVDD and AREG to AVSS (AREG internal regulator is shutdown): AVDD 1.8-V operation | 1.7  | 1.8 | 1.9    |      |
| IOVDD                     | IO supply voltage to VSS (thermal pad): IOVDD 3.3-V operation   | 3.0  | 3.3 | 3.6    | V    |
|                           | IO supply voltage to VSS (thermal pad): IOVDD 1.8-V operation   | 1.65 | 1.8 | 1.95   |      |
| INPUTS                    |   |      |     |        |      |
|                           | Analog input pins voltage to AVSS   | 0    |     | AVDD   | V    |
|                           | Digital input except IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)                       | 0    |     | IOVDD  | V    |
|                           | Digital input IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)                              | 0    |     | AVDD   | V    |
| TEMPERATURE               |   |      |     |        |      |
| T <sub>A</sub>            | Operating ambient temperature   | −40  |     | 105    | °C   |
| OTHERS                    |   |      |     |        |      |
|                           | GPIOx or GPIx (used as MCLK input) clock frequency  |      |     | 36.864 | MHz  |
| C <sub>b</sub>            | SCL and SDA bus capacitance for I <sup>2</sup> C interface supports standard-mode and fast-mode         |      |     | 400    | pF   |
|                           | SCL and SDA bus capacitance for I <sup>2</sup> C interface supports fast-mode plus                      |      |     | 550    |      |
| C <sub>L</sub>            | Digital output load capacitance   |      | 20  | 50     | pF   |

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TAA3020    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RTE (WQFN) |      |
|                               |  | 20 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 55.9       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 33.1       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 23.4       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.6        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 23.3       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 16.7       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $IOVDD = 3.3\text{ V}$ ,  $f_{IN} = 1\text{-kHz}$  sinusoidal signal,  $f_S = 48\text{ kHz}$ , 32-bit audio data, BCLK =  $256 \times f_S$ , TDM slave mode, and PLL on (unless otherwise noted)

| PARAMETER  |  | TEST CONDITIONS  | MIN  | TYP  | MAX | UNIT             |
|--|--|--|------|------|-----|------------------|
| ADC CONFIGURATION  |  |  |      |      |     |                  |
|  | AC input impedance                                   | Input pins INxP or INxM, 10-kΩ input impedance selection   | 10   |      |     | kΩ               |
|  |  | Input pins INxP or INxM, 20-kΩ input impednace selection   | 20   |      |     |                  |
|  | Channel gain range                                   | Programmable range with 0.5-dB steps   | 0    |      | 42  | dB               |
| ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 3.3-V OPERATION |  |  |      |      |     |                  |
|  | Differential input full-scale AC signal voltage      | AC-coupled input   | 2    |      |     | V <sub>RMS</sub> |
|  | Single-ended input full-scale AC signal voltage      | AC-coupled input   | 1    |      |     | V <sub>RMS</sub> |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | IN1 differential input selected and AC signal shorted to ground, 10-kΩ input impedance selection, 0-dB channel gain        | 98   | 104  |     | dB               |
|  |  | IN1 differential input selected and AC signal shorted to ground, 10-kΩ input impedance selection, 12-dB channel gain       |      | 98   |     |                  |
| DR   | Dynamic range, A-weighted <sup>(2)</sup>             | IN1 differential input selected and –60-dB full-scale AC signal input, 10-kΩ input impedance selection, 0-dB channel gain  |      | 104  |     | dB               |
|  |  | IN1 differential input selected and –72-dB full-scale AC signal input, 10-kΩ input impedance selection, 12-dB channel gain |      | 98   |     |                  |
| THD+N  | Total harmonic distortion <sup>(2) (3)</sup>         | IN1 differential input selected and –1-dB full-scale AC signal input, 10-kΩ input impedance selection, 0-dB channel gain   |      | –95  | –80 | dB               |
|  |  | IN1 differential input selected and –13-dB full-scale AC signal input, 10-kΩ input impedance selection, 12-dB channel gain |      | –93  |     |                  |
| ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 1.8-V OPERATION |  |  |      |      |     |                  |
|  | Differential input full-scale AC signal voltage      | AC-coupled Input   | 1    |      |     | V <sub>RMS</sub> |
|  | Single-ended input full-scale AC signal voltage      | AC-coupled Input   | 0.5  |      |     | V <sub>RMS</sub> |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | IN1 differential input selected and AC signal shorted to ground, 10-kΩ input impedance selection, 0-dB channel gain        |      | 98   |     | dB               |
| DR   | Dynamic range, A-weighted <sup>(2)</sup>             | IN1 differential input selected and –60-dB full-scale AC signal input, 10-kΩ input impedance selection, 0-dB channel gain  |      | 99   |     | dB               |
| THD+N  | Total harmonic distortion <sup>(2) (3)</sup>         | IN1 differential input selected and –2-dB full-scale AC signal Input, 10-kΩ input impedance selection, 0 dB channel gain   |      | –90  |     | dB               |
| ADC OTHER PARAMETERS   |  |  |      |      |     |                  |
|  | Digital volume control range                         | Programmable 0.5-dB steps  | –100 |      | 27  | dB               |
|  | Output data sample rate                              | Programmable   | 7.35 |      | 768 | kHz              |
|  | Output data sample word length                       | Programmable   | 16   |      | 32  | Bits             |
|  | Digital high-pass filter cutoff frequency            | First-order IIR filter with programmable coefficients, –3-dB point (default setting)                                       |      | 12   |     | Hz               |
|  | Interchannel isolation                               | –1-dB full-scale AC-signal input to non measurement channel  |      | –124 |     | dB               |
|  | Interchannel gain mismatch                           | –6-dB full-scale AC-signal input and 0-dB channel gain   |      | 0.1  |     | dB               |
|  | Gain drift <sup>(4)</sup>                            | 0-dB channel gain, across temperature range –40°C to 105°C   |      | 36.8 |     | ppm/°C           |

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $IOVDD = 3.3\text{ V}$ ,  $f_{IN} = 1\text{-kHz}$  sinusoidal signal,  $f_S = 48\text{ kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM slave mode, and PLL on (unless otherwise noted)

| PARAMETER              |  | TEST CONDITIONS   | MIN          | TYP          | MAX          | UNIT              |
|------------------------|--|---|--------------|--------------|--------------|-------------------|
|                        | Interchannel phase mismatch                      | 1-kHz sinusoidal signal   |              | 0.02         |              | Degrees           |
|                        | Phase drift <sup>(5)</sup>                       | 1-kHz sinusoidal signal, across temperature range –40°C to 105°C  |              | 0.0005       |              | Degrees/°C        |
| PSRR                   | Power-supply rejection ratio                     | 100-mV <sub>PP</sub> , 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain                                  |              | 102          |              | dB                |
| CMRR                   | Common-mode rejection ratio                      | Differential microphone input selected, 0-dB channel gain, 100-mV <sub>PP</sub> , 1-kHz signal on both pins and measure level at output |              | 60           |              | dB                |
| <b>MICROPHONE BIAS</b> |  |   |              |              |              |                   |
|                        | MICBIAS noise                                    | BW = 20 Hz to 20 kHz, A-weighted, 1-μF capacitor between MICBIAS and AVSS   |              | 2.1          |              | μV <sub>RMS</sub> |
|                        | MICBIAS voltage                                  | MICBIAS programmed to VREF and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V  |              | VREF         |              | V                 |
|                        |  | MICBIAS programmed to VREF × 1.096 and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V  |              | VREF × 1.096 |              |                   |
|                        |  | Bypass to AVDD with 5-mA load   |              | AVDD – 0.2   |              |                   |
|                        | MICBIAS current drive                            |   |              |              | 5            | mA                |
|                        | MICBIAS load regulation                          | MICBIAS programmed to either VREF or VREF × 1.096, measured up to max load  | 0            | 0.6          | 1            | %                 |
|                        | MICBIAS over current protection threshold        |   | 6.1          |              |              | mA                |
| <b>DIGITAL I/O</b>     |  |   |              |              |              |                   |
| V <sub>IL</sub>        | Low-level digital input logic voltage threshold  | All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 1.8-V operation  | –0.3         |              | 0.35 × IOVDD | V                 |
|                        |  | All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 3.3-V operation  | –0.3         |              | 0.8          |                   |
| V <sub>IH</sub>        | High-level digital input logic voltage threshold | All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 1.8-V operation  | 0.65 × IOVDD |              | IOVDD + 0.3  | V                 |
|                        |  | All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 3.3-V operation  | 2            |              | IOVDD + 0.3  |                   |
| V <sub>OL</sub>        | Low-level digital output voltage                 | All digital pins except IN2M_GPO1, SDA and SCL, I <sub>OL</sub> = –2 mA, IOVDD 1.8-V operation  |              |              | 0.45         | V                 |
|                        |  | All digital pins except IN2M_GPO1, SDA and SCL, I <sub>OL</sub> = –2 mA, IOVDD 3.3-V operation  |              |              | 0.4          |                   |
| V <sub>OH</sub>        | High-level digital output voltage                | All digital pins except IN2M_GPO1, SDA and SCL, I <sub>OH</sub> = 2 mA, IOVDD 1.8-V operation   | IOVDD – 0.45 |              |              | V                 |
|                        |  | All digital pins except IN2M_GPO1, SDA and SCL, I <sub>OH</sub> = 2 mA, IOVDD 3.3-V operation   | 2.4          |              |              |                   |
| V <sub>IL(I2C)</sub>   | Low-level digital input logic voltage threshold  | SDA and SCL   | –0.5         |              | 0.3 × IOVDD  | V                 |
| V <sub>IH(I2C)</sub>   | High-level digital input logic voltage threshold | SDA and SCL   | 0.7 × IOVDD  |              | IOVDD + 0.5  | V                 |
| V <sub>OL1(I2C)</sub>  | Low-level digital output voltage                 | SDA, I <sub>OL(I2C)</sub> = –3 mA, IOVDD > 2 V  |              |              | 0.4          | V                 |
| V <sub>OL2(I2C)</sub>  | Low-level digital output voltage                 | SDA, I <sub>OL(I2C)</sub> = –2 mA, IOVDD ≤ 2 V  |              |              | 0.2 × IOVDD  | V                 |
| I <sub>OL(I2C)</sub>   | Low-level digital output current                 | SDA, V <sub>OL(I2C)</sub> = 0.4 V, standard-mode or fast-mode   | 3            |              |              | mA                |
|                        |  | SDA, V <sub>OL(I2C)</sub> = 0.4 V, fast-mode plus   | 20           |              |              |                   |
| I <sub>IH</sub>        | Input logic-high leakage for digital inputs      | All digital pins except IN2P_GPI1 and MICBIAS_GPI2 pins, input = IOVDD  | –5           | 0.1          | 5            | μA                |
| I <sub>IL</sub>        | Input logic-low leakage for digital inputs       | All digital pins except IN2P_GPI1 and MICBIAS_GPI2 pins, input = 0 V  | –5           | 0.1          | 5            | μA                |
| V <sub>IL(GPIx)</sub>  | Low-level digital input logic voltage threshold  | IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 1.8-V operation   | –0.3         |              | 0.35 × AVDD  | V                 |
|                        |  | IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 3.3-V operation   | –0.3         |              | 0.8          |                   |



at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $IOVDD = 3.3\text{ V}$ ,  $f_{IN} = 1\text{-kHz}$  sinusoidal signal,  $f_S = 48\text{ kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM slave mode, and PLL on (unless otherwise noted)

| PARAMETER      |   | TEST CONDITIONS   | MIN                | TYP | MAX          | UNIT          |
|----------------|---|---|--------------------|-----|--------------|---------------|
| $V_{IH(GPIx)}$ | High-level digital input logic voltage threshold          | IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 1.8-V operation         | $0.65 \times AVDD$ |     | $AVDD + 0.3$ | V             |
|                |   | IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 3.3-V operation         | 2                  |     | $AVDD + 0.3$ |               |
| $V_{OL(GPOx)}$ | Low-level digital output voltage                          | IN2M_GPO2 digital pin, $I_{OL} = -2\text{ mA}$ , AVDD 1.8-V operation |                    |     | 0.45         | V             |
|                |   | IN2M_GPO2 digital pin, $I_{OL} = -2\text{ mA}$ , AVDD 3.3-V operation |                    |     | 0.4          |               |
| $V_{OH(GPOx)}$ | High-level digital output voltage                         | IN2M_GPO2 digital pin, $I_{OH} = 2\text{ mA}$ , AVDD 1.8-V operation  | $AVDD - 0.45$      |     |              | V             |
|                |   | IN2M_GPO2 digital pin, $I_{OH} = 2\text{ mA}$ , AVDD 3.3-V operation  | 2.4                |     |              |               |
| $I_{IH(GPIx)}$ | Input logic-high leakage for digital inputs               | IN2P_GPI1 and MICBIAS_GPI2 digital pins, input = AVDD                 | -5                 | 0.1 | 5            | $\mu\text{A}$ |
| $I_{IL(GPIx)}$ | Input logic-high leakage for digital inputs               | IN2P_GPI1 and MICBIAS_GPI2 digital pins, input = 0 V                  | -5                 | 0.1 | 5            | $\mu\text{A}$ |
| $C_{IN}$       | Input capacitance for digital inputs                      | All digital pins  |                    | 5   |              | pF            |
| $R_{PD}$       | Pulldown resistance for digital I/O pins when asserted on |   |                    | 20  |              | k $\Omega$    |

#### TYPICAL SUPPLY CURRENT CONSUMPTION

|                    |  |  |      |    |
|--------------------|--|--|------|----|
| I <sub>AVDD</sub>  | Current consumption in sleep mode (software shutdown mode)   | All external clocks stopped, AVDD = 3.3 V, internal AREG                               | 5    | μA |
| I <sub>AVDD</sub>  |  | All external clocks stopped, AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD) | 10   |    |
| I <sub>IOVDD</sub> |  | All external clocks stopped, IOVDD = 3.3 V   | 0.5  |    |
| I <sub>IOVDD</sub> |  | All external clocks stopped, IOVDD = 1.8 V   | 0.5  |    |
| I <sub>AVDD</sub>  | Current consumption with ADC 2-channel operating at f <sub>S</sub> 48-kHz, PLL off and BCLK = 512 × f <sub>S</sub> | AVDD = 3.3 V, internal AREG  | 11.1 | mA |
| I <sub>AVDD</sub>  |  | AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)                              | 10.5 |    |
| I <sub>IOVDD</sub> |  | IOVDD = 3.3 V  | 0.1  |    |
| I <sub>IOVDD</sub> |  | IOVDD = 1.8 V  | 0.05 |    |
| I <sub>AVDD</sub>  | Current consumption with ADC 2-channel operating at f <sub>S</sub> 16-kHz, PLL on and BCLK = 256 × f <sub>S</sub>  | AVDD = 3.3 V, internal AREG  | 11.3 | mA |
| I <sub>AVDD</sub>  |  | AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)                              | 10.6 |    |
| I <sub>IOVDD</sub> |  | IOVDD = 3.3 V  | 0.05 |    |
| I <sub>IOVDD</sub> |  | IOVDD = 1.8 V  | 0.02 |    |
| I <sub>AVDD</sub>  | Current consumption with ADC 2-channel operating at f <sub>S</sub> 48-kHz, PLL on and BCLK = 256 × f <sub>S</sub>  | AVDD = 3.3 V, internal AREG  | 12.2 | mA |
| I <sub>AVDD</sub>  |  | AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)                              | 11.6 |    |
| I <sub>IOVDD</sub> |  | IOVDD = 3.3 V  | 0.1  |    |
| I <sub>IOVDD</sub> |  | IOVDD = 1.8 V  | 0.05 |    |

- (1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
- (2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
- (3) For best distortion performance, use input AC-coupling capacitors with low-voltage coefficient.
- (4) Gain drift = gain variation (in temperature range) / typical gain value (gain at room temperature) / temperature range  $\times 10^6$  measured with gain in linear scale.
- (5) Phase drift = phase deviation (in temperature range) / (temperature range).



## 5.6 Timing Requirements: I<sup>2</sup>C Interface

at T<sub>A</sub> = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see [Figure 5-1](#) for timing diagram

|                       |   | MIN                  | NOM | MAX  | UNIT |
|-----------------------|---|----------------------|-----|------|------|
| <b>STANDARD-MODE</b>  |   |                      |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency   | 0                    |     | 100  | kHz  |
| t <sub>HD,STA</sub>   | Hold time (repeated) START condition.<br>After this period, the first clock pulse is generated. | 4                    |     |      | μs   |
| t <sub>LOW</sub>      | Low period of the SCL clock   | 4.7                  |     |      | μs   |
| t <sub>HIGH</sub>     | High period of the SCL clock  | 4                    |     |      | μs   |
| t <sub>SU,STA</sub>   | Setup time for a repeated START condition   | 4.7                  |     |      | μs   |
| t <sub>HD,DAT</sub>   | Data hold time  | 0                    |     | 3.45 | μs   |
| t <sub>SU,DAT</sub>   | Data setup time   | 250                  |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL rise time   |                      |     | 1000 | ns   |
| t <sub>f</sub>        | SDA and SCL fall time   |                      |     | 300  | ns   |
| t <sub>SU,STO</sub>   | Setup time for STOP condition   | 4                    |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition  | 4.7                  |     |      | μs   |
| <b>FAST-MODE</b>      |   |                      |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency   | 0                    |     | 400  | kHz  |
| t <sub>HD,STA</sub>   | Hold time (repeated) START condition.<br>After this period, the first clock pulse is generated. | 0.6                  |     |      | μs   |
| t <sub>LOW</sub>      | Low period of the SCL clock   | 1.3                  |     |      | μs   |
| t <sub>HIGH</sub>     | High period of the SCL clock  | 0.6                  |     |      | μs   |
| t <sub>SU,STA</sub>   | Setup time for a repeated START condition   | 0.6                  |     |      | μs   |
| t <sub>HD,DAT</sub>   | Data hold time  | 0                    |     | 0.9  | μs   |
| t <sub>SU,DAT</sub>   | Data setup time   | 100                  |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL rise time   | 20                   |     | 300  | ns   |
| t <sub>f</sub>        | SDA and SCL fall time   | 20 × (IOVDD / 5.5 V) |     | 300  | ns   |
| t <sub>SU,STO</sub>   | Setup time for STOP condition   | 0.6                  |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition  | 1.3                  |     |      | μs   |
| <b>FAST-MODE PLUS</b> |   |                      |     |      |      |
| f <sub>SCL</sub>      | SCL clock frequency   | 0                    |     | 1000 | kHz  |
| t <sub>HD,STA</sub>   | Hold time (repeated) START condition.<br>After this period, the first clock pulse is generated. | 0.26                 |     |      | μs   |
| t <sub>LOW</sub>      | Low period of the SCL clock   | 0.5                  |     |      | μs   |
| t <sub>HIGH</sub>     | High period of the SCL clock  | 0.26                 |     |      | μs   |
| t <sub>SU,STA</sub>   | Setup time for a repeated START condition   | 0.26                 |     |      | μs   |
| t <sub>HD,DAT</sub>   | Data hold time  | 0                    |     |      | μs   |
| t <sub>SU,DAT</sub>   | Data setup time   | 50                   |     |      | ns   |
| t <sub>r</sub>        | SDA and SCL rise time   |                      |     | 120  | ns   |
| t <sub>f</sub>        | SDA and SCL fall time   | 20 × (IOVDD / 5.5 V) |     | 120  | ns   |
| t <sub>SU,STO</sub>   | Setup time for STOP condition   | 0.26                 |     |      | μs   |
| t <sub>BUF</sub>      | Bus free time between a STOP and START condition  | 0.5                  |     |      | μs   |

## 5.7 Switching Characteristics: I<sup>2</sup>C Interface

at T<sub>A</sub> = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see [Figure 5-1](#) for timing diagram

| PARAMETER            |                  | TEST CONDITIONS | MIN | TYP | MAX  | UNIT |
|----------------------|------------------|-----------------|-----|-----|------|------|
| t <sub>d</sub> (SDA) | SCL to SDA delay | Standard-mode   | 250 |     | 1250 | ns   |
|                      |                  | Fast-mode       | 250 |     | 850  |      |
|                      |                  | Fast-mode plus  |     |     | 400  |      |

## 5.8 Timing Requirements: TDM, I<sup>2</sup>S or LJ Interface

at T<sub>A</sub> = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see [Figure 5-2](#) for timing diagram

|                          |   |                                    | MIN | NOM | MAX | UNIT |
|--------------------------|---|------------------------------------|-----|-----|-----|------|
| t <sub>(BCLK)</sub>      | BCLK period                             |                                    | 40  |     |     | ns   |
| t <sub>H</sub> (BCLK)    | BCLK high pulse duration <sup>(1)</sup> |                                    | 25  |     |     | ns   |
| t <sub>L</sub> (BCLK)    | BCLK low pulse duration <sup>(1)</sup>  |                                    | 25  |     |     | ns   |
| t <sub>SU</sub> (FSYNC)  | FSYNC setup time                        |                                    | 8   |     |     | ns   |
| t <sub>HLD</sub> (FSYNC) | FSYNC hold time                         |                                    | 8   |     |     | ns   |
| t <sub>r</sub> (BCLK)    | BCLK rise time                          | 10% - 90% rise time <sup>(2)</sup> |     |     | 10  | ns   |
| t <sub>f</sub> (BCLK)    | BCLK fall time                          | 90% - 10% fall time <sup>(2)</sup> |     |     | 10  | ns   |

(1) The BCLK minimum high or low pulse duration can be relaxed to 14 ns (to meet the timing specifications), if the SDOUT data line is latched on the same BCLK edge polarity as the edge used by the device to transmit SDOUT data.

(2) The BCLK maximum rise and fall time can be relaxed to 13 ns if the BCLK frequency used in the system is below 20 MHz. Relaxing the BCLK rise and fall time can cause noise to increase because of higher clock jitter.

## 5.9 Switching Characteristics: TDM, I<sup>2</sup>S or LJ Interface

at T<sub>A</sub> = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see [Figure 5-2](#) for timing diagram

| PARAMETER                    |  | TEST CONDITIONS              | MIN | TYP | MAX    | UNIT |
|------------------------------|--|------------------------------|-----|-----|--------|------|
| t <sub>d</sub> (SDOUT-BCLK)  | BCLK to SDOUT delay  | 50% of BCLK to 50% of SDOUT  | 3   |     | 18     | ns   |
| t <sub>d</sub> (SDOUT-FSYNC) | FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0) | 50% of FSYNC to 50% of SDOUT |     |     | 18     | ns   |
| f <sub>(BCLK)</sub>          | BCLK output clock frequency: master mode <sup>(1)</sup>                  |                              |     |     | 24.576 | MHz  |
| t <sub>H</sub> (BCLK)        | BCLK high pulse duration: master mode                                    |                              | 14  |     |        | ns   |
| t <sub>L</sub> (BCLK)        | BCLK low pulse duration: master mode                                     |                              | 14  |     |        | ns   |
| t <sub>d</sub> (FSYNC)       | BCLK to FSYNC delay: master mode   | 50% of BCLK to 50% of FSYNC  | 3   |     | 18     | ns   |
| t <sub>r</sub> (BCLK)        | BCLK rise time: master mode  | 10% - 90% rise time          |     |     | 8      | ns   |
| t <sub>f</sub> (BCLK)        | BCLK fall time: master mode  | 90% - 10% fall time          |     |     | 8      | ns   |

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

## 5.10 Timing Requirements: PDM Digital Microphone Interface

at T<sub>A</sub> = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see [Figure 5-3](#) for timing diagram

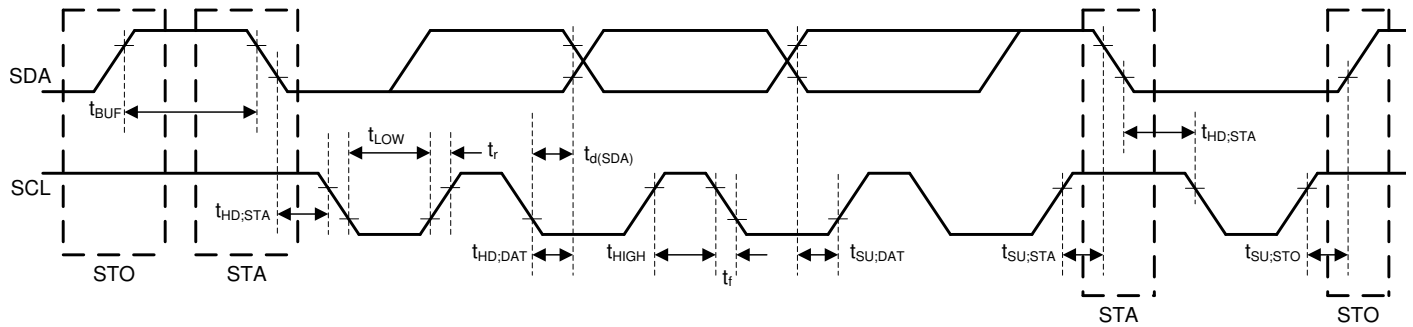
|                             |                     | MIN | NOM | MAX | UNIT |
|-----------------------------|---------------------|-----|-----|-----|------|
| t <sub>SU</sub> (PDM DINx)  | PDM DINx setup time | 30  |     |     | ns   |
| t <sub>HLD</sub> (PDM DINx) | PDM DINx hold time  | 0   |     |     | ns   |

## 5.11 Switching Characteristics: PDM Digital Microphone Interface

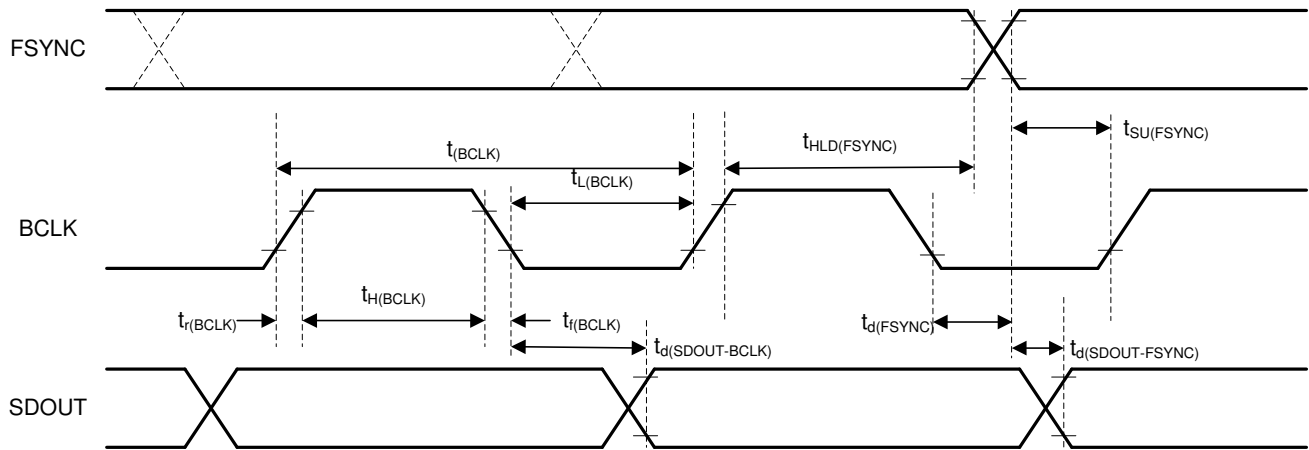
at  $T_A = 25^\circ\text{C}$ , IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see 5-3 for timing diagram

| PARAMETER              | TEST CONDITIONS            | MIN                 | TYP | MAX   | UNIT |
|------------------------|----------------------------|---------------------|-----|-------|------|
| $f_{\text{(PDMCLK)}}$  | PDMCLK clock frequency     | 0.768               |     | 6.144 | MHz  |
| $t_{\text{H(PDMCLK)}}$ | PDMCLK high pulse duration | 72                  |     |       | ns   |
| $t_{\text{L(PDMCLK)}}$ | PDMCLK low pulse duration  | 72                  |     |       | ns   |
| $t_{\text{r(PDMCLK)}}$ | PDMCLK rise time           | 10% - 90% rise time |     | 18    | ns   |
| $t_{\text{f(PDMCLK)}}$ | PDMCLK fall time           | 90% - 10% fall time |     | 18    | ns   |

## 5.12 Timing Diagrams



5-1. I²C Interface Timing Diagram



5-2. TDM (With BCLK\_POL = 1), I²S, and LJ Interface Timing Diagram

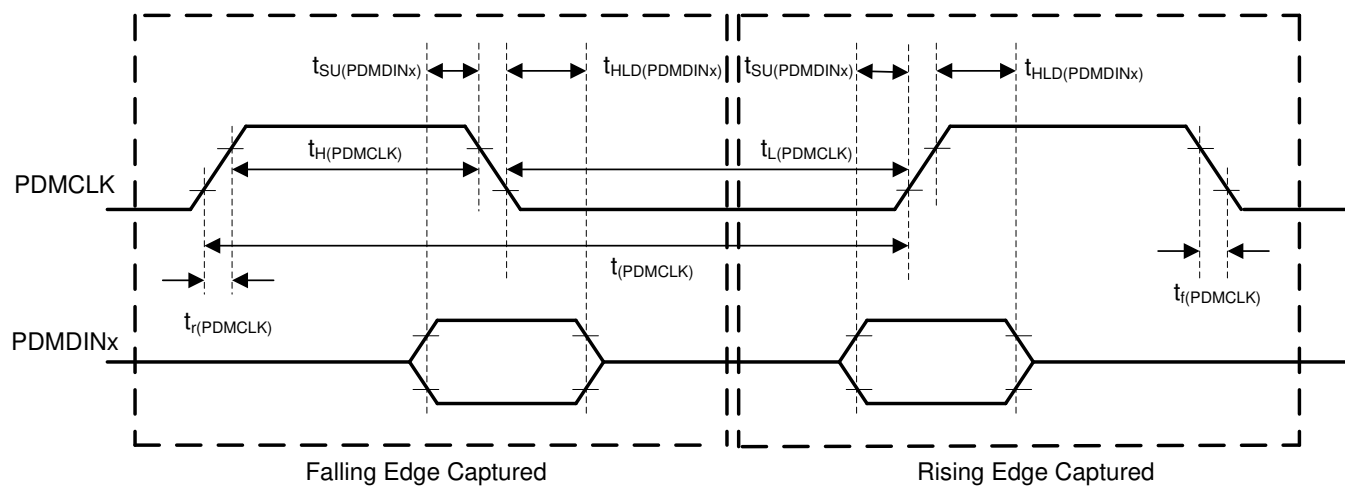


図 5-3. PDM Digital Microphone Interface Timing Diagram

## 6 Detailed Description

### 6.1 Overview

The TAA3020 is a high-performance, low-power, flexible, 2-channel, audio analog-to-digital converter (ADC) with extensive feature integration. This device is intended for applications in voice-activated systems, professional microphones, audio conferencing, portable computing, communication, and entertainment applications. The high dynamic range of the device enables far-field audio recording with high fidelity. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications.

The TAA3020 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma ( $\Delta\Sigma$ ) ADC
- Configurable single-ended or differential audio inputs
- Low-noise, programmable microphone bias output
- Automatic gain controller (AGC)
- Programmable decimation filters with a linear-phase filter or a low-latency filter
- Programmable channel gain, volume control, biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF), and digital channel mixer
- Pulse density modulation (PDM) microphone 4-channel interface with a high-performance decimation filter
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the TAA3020 for configuring the control registers is supported using an I<sup>2</sup>C interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I<sup>2</sup>S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

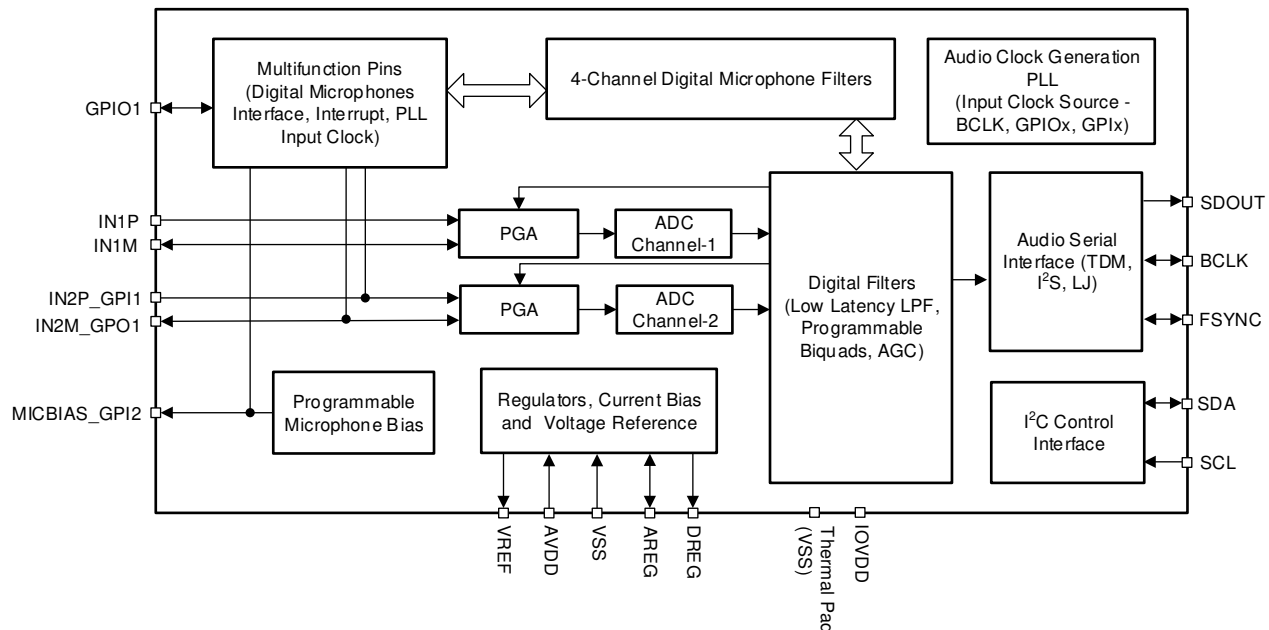
The TAA3020 can support multiple devices by sharing the common TDM bus across devices. Moreover, the device includes a daisy-chain feature as well. These features relax the shared TDM bus timing requirements and board design complexities when operating multiple devices for applications requiring high audio data bandwidth.

表 6-1 lists the reference abbreviations used throughout this document to registers that control the device.

**表 6-1. Abbreviations for Register References**

| REFERENCE                    | ABBREVIATION | DESCRIPTION  | EXAMPLE                                       |
|------------------------------|--------------|--|---|
| Page y, register z, bit k    | Py_Rz_Dk     | Single data bit. The value of a single bit in a register.      | Page 4, register 36, bit 0 = P4_R36_D0        |
| Page y, register z, bits k-m | Py_Rz_D[k:m] | Range of data bits. A range of data bits (inclusive).          | Page 4, register 36, bits 3-0 = P4_R36_D[3:0] |
| Page y, register z           | Py_Rz        | One entire register. All eight bits in the register as a unit. | Page 4, register 36 = P4_R36                  |
| Page y, registers z-n        | Py_Rz-Rn     | Range of registers. A range of registers in the same page.     | Page 4, registers 36, 37, 38 = P4_R36-R38     |

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

#### 6.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All registers can be accessed using I<sup>2</sup>C communication to the device. For more information, see the [セクション 6.5](#) section.

#### 6.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAA3020 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I<sup>2</sup>S or left-justified protocols format, programmable data length options, very flexible master-slave configurability for bus clock lines and the ability to communicate with multiple devices within a system directly.

The bus protocol TDM, I<sup>2</sup>S, or left-justified (LJ) format can be selected by using the ASI\_FORMAT[1:0] (P0\_R7\_D[7:6]) register bits. As shown in 表 6-2 and 表 6-3, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the ASI\_WLEN[1:0] (P0\_R7\_D[5:4]) register bits.

**表 6-2. Audio Serial Interface Format**

| P0_R7_D[7:6] : ASI_FORMAT[1:0] | AUDIO SERIAL INTERFACE FORMAT          |
|--------------------------------|--|
| 00 (default)                   | Time division multiplexing (TDM) mode  |
| 01                             | Inter IC sound (I <sup>2</sup> S) mode |
| 10                             | Left-justified (LJ) mode               |
| 11                             | Reserved (do not use this setting)     |

**表 6-3. Audio Output Channel Data Word-Length**

| P0_R7_D[5:4] : ASI_WLEN[1:0] | AUDIO OUTPUT CHANNEL DATA WORD-LENGTH          |
|------------------------------|--|
| 00                           | Output channel data word-length set to 16 bits |
| 01                           | Output channel data word-length set to 20 bits |
| 10                           | Output channel data word-length set to 24 bits |
| 11 (default)                 | Output channel data word-length set to 32 bits |

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 64) to allow all output channel audio data transmissions to complete on the audio bus by a device or multiple TAA3020 devices sharing the same audio bus. The device supports up to four output channels that can be configured to place their audio data on bus slot 0 to slot 63. 表 6-4 lists the output channel slot configuration settings. In I<sup>2</sup>S and LJ mode, the slots are divided into two sets, left-channel slots and right-channel slots, as described in the [Inter IC Sound \(I<sup>2</sup>S\) Interface](#) and [Left-Justified \(LJ\) Interface](#) sections.

**表 6-4. Output Channel Slot Assignment Settings**

| P0_R11_D[5:0] : CH1_SLOT[5:0] | OUTPUT CHANNEL 1 SLOT ASSIGNMENT                           |
|-------------------------------|--|
| 00 0000 = 0d (default)        | Slot 0 for TDM or left slot 0 for I <sup>2</sup> S, LJ.    |
| 00 0001 = 1d                  | Slot 1 for TDM or left slot 1 for I <sup>2</sup> S, LJ.    |
| ...                           | ...  |
| 01 1111 = 31d                 | Slot 31 for TDM or left slot 31 for I <sup>2</sup> S, LJ.  |
| 10 0000 = 32d                 | Slot 32 for TDM or right slot 0 for I <sup>2</sup> S, LJ.  |
| ...                           | ...  |
| 11 1110 = 62d                 | Slot 62 for TDM or right slot 30 for I <sup>2</sup> S, LJ. |
| 11 1111 = 63d                 | Slot 63 for TDM or right slot 31 for I <sup>2</sup> S, LJ. |

Similarly, the slot assignment setting for output channel 2 to channel 8 can be done using the CH2\_SLOT (P0\_R12) to CH8\_SLOT (P0\_R18) registers, respectively.

The slot word length is the same as the output channel data word length set for the device. The output channel data word length must be set to the same value for all TAA3020 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.



The device also includes a feature that offsets the start of the slot data transfer with respect to the frame sync by up to 31 cycles of the bit clock. 表 6-5 lists the programmable offset configuration settings.

**表 6-5. Programmable Offset Settings for the ASI Slot Start**

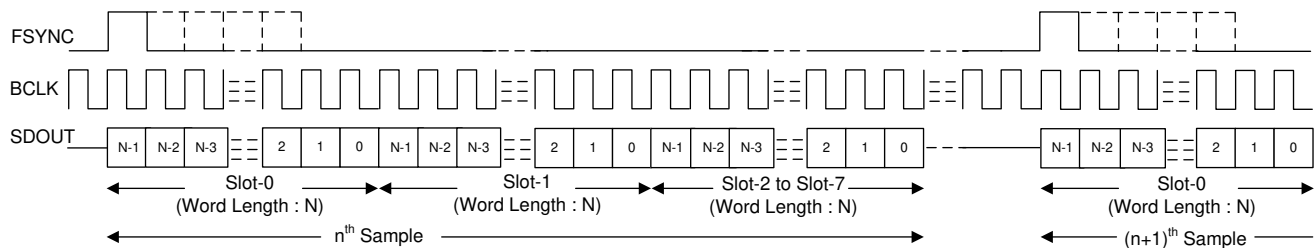
| P0_R8_D[4:0] : TX_OFFSET[4:0] | PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START  |
|-------------------------------|---|
| 0 0000 = 0d (default)         | The device follows the standard protocol timing without any offset.   |
| 0 0001 = 1d                   | Slot start is offset by one BCLK cycle, as compared to standard protocol timing.<br>For I <sup>2</sup> S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing. |
| .....                         | .....   |
| 1 1110 = 30d                  | Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.<br>For I <sup>2</sup> S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. |
| 1 1111 = 31d                  | Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.<br>For I <sup>2</sup> S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. |

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the FSYNC\_POL (P0\_R7\_D3) register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the BCLK\_POL (P0\_R7\_D2) register bit.

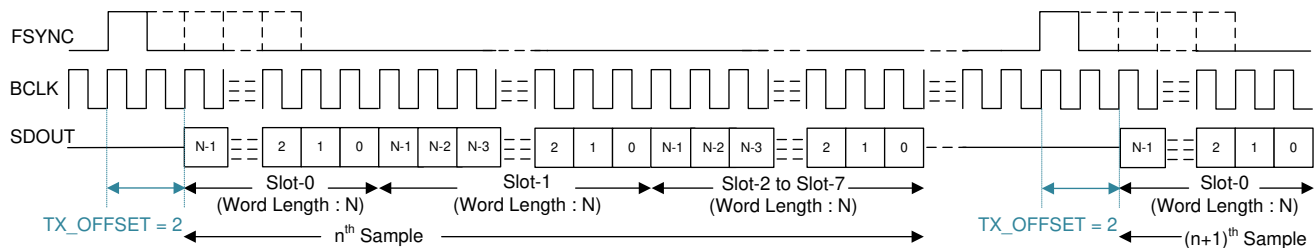
#### 6.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX\_OFFSET equals 0) is transmitted on the rising edge of BCLK.

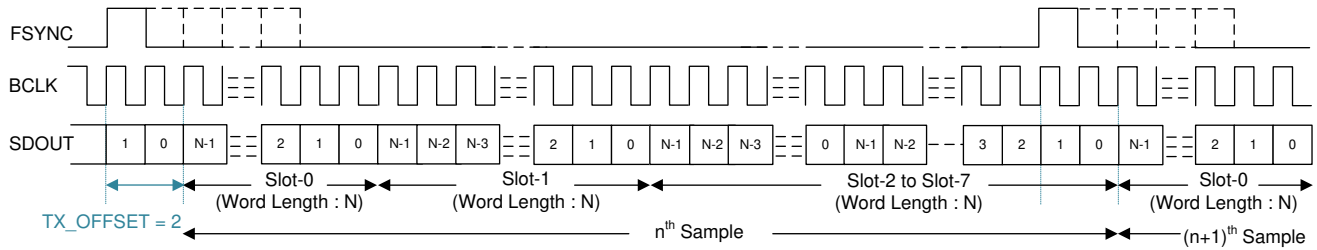
図 6-1 to 図 6-4 illustrate the protocol timing for TDM operation with various configurations.



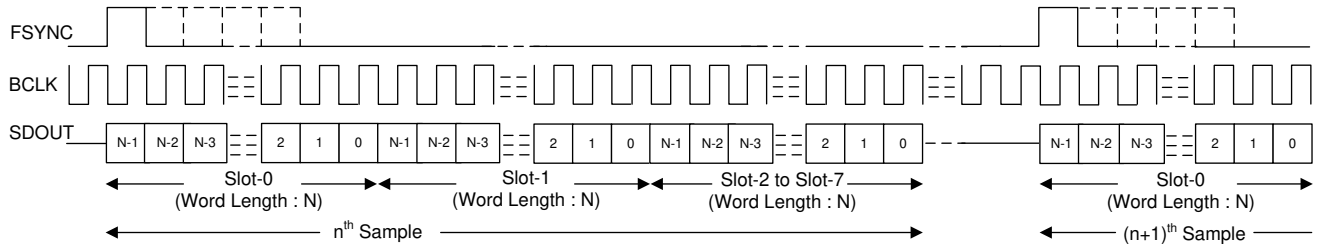
**図 6-1. TDM Mode Standard Protocol Timing (TX\_OFFSET = 0)**



**図 6-2. TDM Mode Protocol Timing (TX\_OFFSET = 2)**



**図 6-3. TDM Mode Protocol Timing (No Idle BCLK Cycles, TX\_OFFSET = 2)**

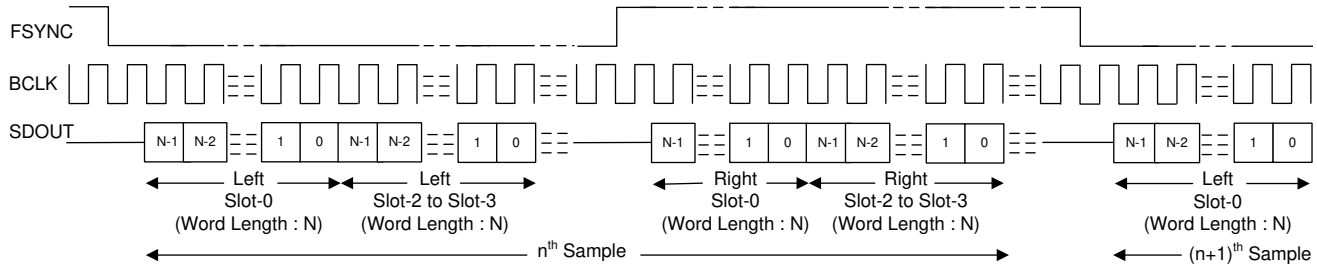


**図 6-4. TDM Mode Protocol Timing (TX\_OFFSET = 0 and BCLK\_POL = 1)**

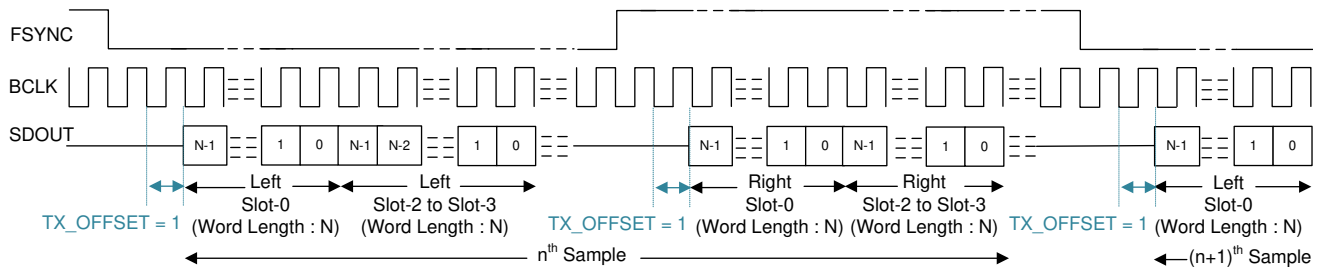
For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a TX\_OFFSET value higher than 0 is recommended.

#### 6.3.1.2.2 Inter IC Sound (I<sup>2</sup>S) Interface

The standard I<sup>2</sup>S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I<sup>2</sup>S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. 図 6-5 to 図 6-8 illustrate the protocol timing for I<sup>2</sup>S operation with various configurations.



**図 6-5. I<sup>2</sup>S Mode Standard Protocol Timing (TX\_OFFSET = 0)**



**図 6-6. I<sup>2</sup>S Protocol Timing (TX\_OFFSET = 1)**

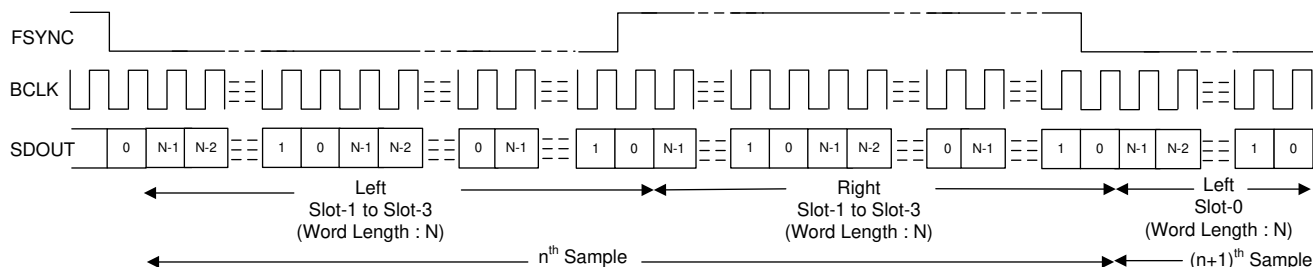


図 6-7. I²S Protocol Timing (No Idle BCLK Cycles, TX\_OFFSET = 0)

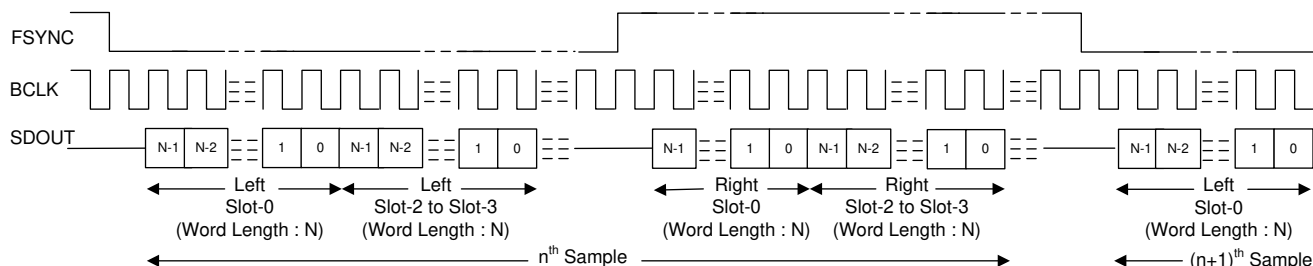


図 6-8. I²S Protocol Timing (TX\_OFFSET = 0 and BCLK\_POL = 1)

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

### 6.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. 図 6-9 to 図 6-12 illustrate the protocol timing for LJ operation with various configurations.

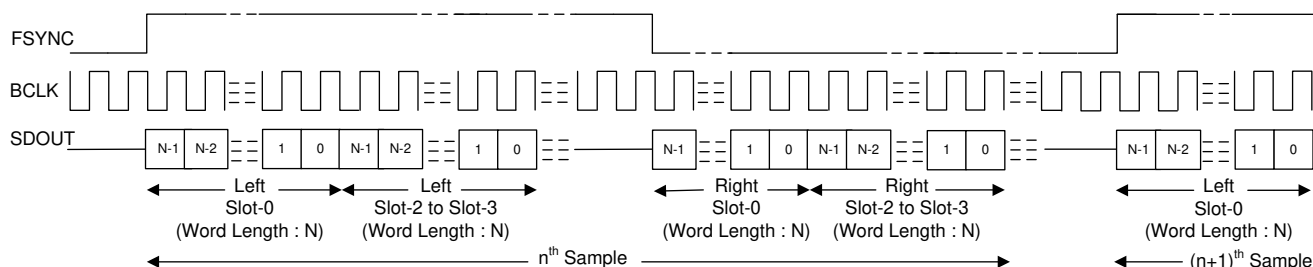
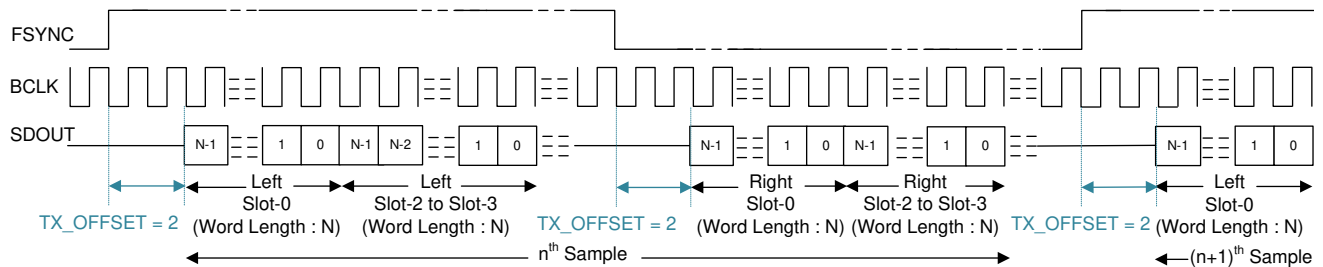
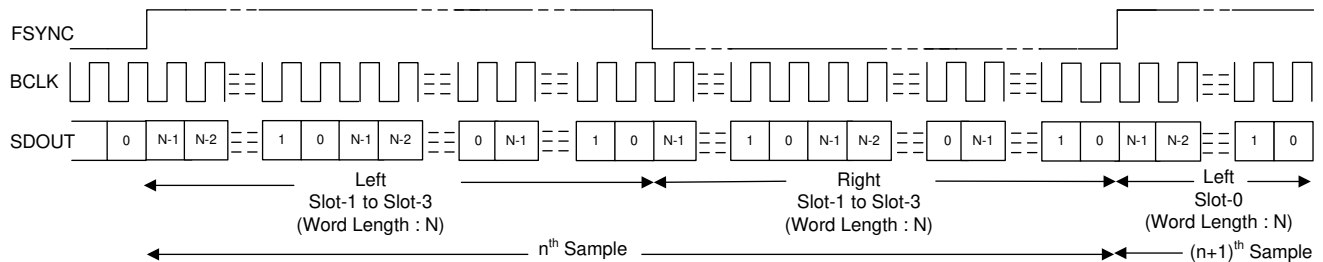


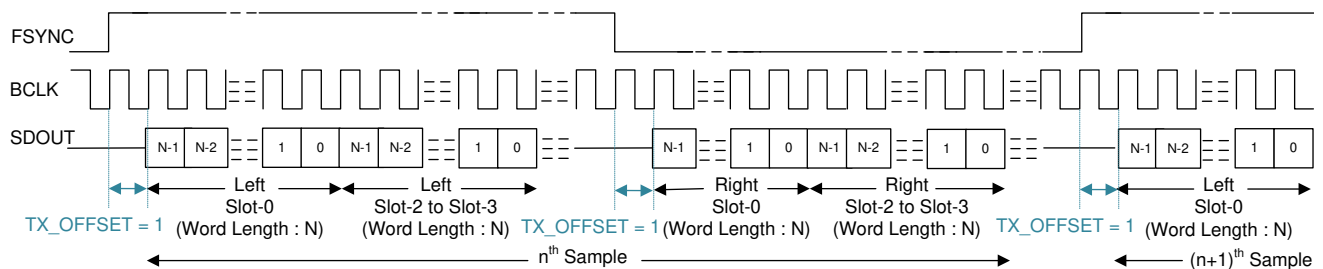
図 6-9. LJ Mode Standard Protocol Timing (TX\_OFFSET = 0)



**図 6-10. LJ Protocol Timing (TX\_OFFSET = 2)**



**図 6-11. LJ Protocol Timing (No Idle BCLK Cycles, TX\_OFFSET = 0)**

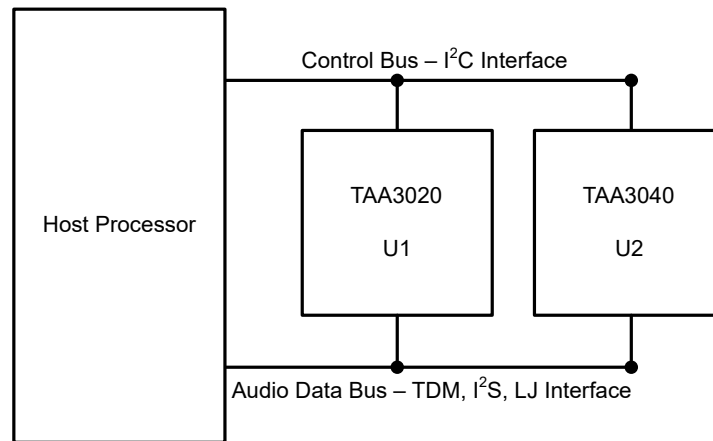


**図 6-12. LJ Protocol Timing (TX\_OFFSET = 1 and BCLK\_POL = 1)**

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX\_OFFSET value higher than 0 is recommended.

### 6.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect the TAA3020 and any other audio device by sharing a single common I<sup>2</sup>C control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone array for beam-forming operations, audio conferencing, noise cancellation, and so forth. [Figure 6-13](#) shows a diagram of the TAA3020 and TLV320ADCx140 devices in a configuration where the control and audio data buses are shared.



**Figure 6-13. Multiple Devices With Shared Control and Audio Data Buses**

The TAA3020 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- I<sup>2</sup>C broadcast simultaneously writes to (or triggers) all TAA3020 and TLV320ADCx140 devices
- Supports up to 64 configuration output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIO1 or GPOx pin can be configured as a secondary output data lane for the audio serial interface
- The GPIO1 or GPIx pin can be used in a daisy-chain configuration of multiple devices
- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable master and slave options for the audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices

See the [Multiple TLV320ADCx140 Devices With Shared TDM and I<sup>2</sup>C Bus application report](#) for further details.

### 6.3.2 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the ADC modulator and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio bus.

The device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 6-6 and 表 6-7 list the supported FSYNC and BCLK frequencies.

**表 6-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies**

| BCLK TO<br>FSYNC<br>RATIO | BCLK (MHz)       |                   |                   |                   |                   |                   |                    |                    |                    |
|---------------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|
|                           | FSYNC<br>(8 kHz) | FSYNC<br>(16 kHz) | FSYNC<br>(24 kHz) | FSYNC<br>(32 kHz) | FSYNC<br>(48 kHz) | FSYNC<br>(96 kHz) | FSYNC (192<br>kHz) | FSYNC (384<br>kHz) | FSYNC (768<br>kHz) |
| 16                        | Reserved         | 0.256             | 0.384             | 0.512             | 0.768             | 1.536             | 3.072              | 6.144              | 12.288             |
| 24                        | Reserved         | 0.384             | 0.576             | 0.768             | 1.152             | 2.304             | 4.608              | 9.216              | 18.432             |
| 32                        | 0.256            | 0.512             | 0.768             | 1.024             | 1.536             | 3.072             | 6.144              | 12.288             | 24.576             |
| 48                        | 0.384            | 0.768             | 1.152             | 1.536             | 2.304             | 4.608             | 9.216              | 18.432             | Reserved           |
| 64                        | 0.512            | 1.024             | 1.536             | 2.048             | 3.072             | 6.144             | 12.288             | 24.576             | Reserved           |
| 96                        | 0.768            | 1.536             | 2.304             | 3.072             | 4.608             | 9.216             | 18.432             | Reserved           | Reserved           |
| 128                       | 1.024            | 2.048             | 3.072             | 4.096             | 6.144             | 12.288            | 24.576             | Reserved           | Reserved           |
| 192                       | 1.536            | 3.072             | 4.608             | 6.144             | 9.216             | 18.432            | Reserved           | Reserved           | Reserved           |
| 256                       | 2.048            | 4.096             | 6.144             | 8.192             | 12.288            | 24.576            | Reserved           | Reserved           | Reserved           |
| 384                       | 3.072            | 6.144             | 9.216             | 12.288            | 18.432            | Reserved          | Reserved           | Reserved           | Reserved           |
| 512                       | 4.096            | 8.192             | 12.288            | 16.384            | 24.576            | Reserved          | Reserved           | Reserved           | Reserved           |
| 1024                      | 8.192            | 16.384            | 24.576            | Reserved          | Reserved          | Reserved          | Reserved           | Reserved           | Reserved           |
| 2048                      | 16.384           | Reserved          | Reserved          | Reserved          | Reserved          | Reserved          | Reserved           | Reserved           | Reserved           |

**表 6-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies**

| BCLK TO<br>FSYNC<br>RATIO | BCLK (MHz)          |                     |                      |                     |                     |                     |                      |                      |                      |
|---------------------------|---------------------|---------------------|----------------------|---------------------|---------------------|---------------------|----------------------|----------------------|----------------------|
|                           | FSYNC<br>(7.35 kHz) | FSYNC<br>(14.7 kHz) | FSYNC<br>(22.05 kHz) | FSYNC<br>(29.4 kHz) | FSYNC<br>(44.1 kHz) | FSYNC<br>(88.2 kHz) | FSYNC (176.4<br>kHz) | FSYNC (352.8<br>kHz) | FSYNC (705.6<br>kHz) |
| 16                        | Reserved            | Reserved            | 0.3528               | 0.4704              | 0.7056              | 1.4112              | 2.8224               | 5.6448               | 11.2896              |
| 24                        | Reserved            | 0.3528              | 0.5292               | 0.7056              | 1.0584              | 2.1168              | 4.2336               | 8.4672               | 16.9344              |
| 32                        | Reserved            | 0.4704              | 0.7056               | 0.9408              | 1.4112              | 2.8224              | 5.6448               | 11.2896              | 22.5792              |
| 48                        | 0.3528              | 0.7056              | 1.0584               | 1.4112              | 2.1168              | 4.2336              | 8.4672               | 16.9344              | Reserved             |
| 64                        | 0.4704              | 0.9408              | 1.4112               | 1.8816              | 2.8224              | 5.6448              | 11.2896              | 22.5792              | Reserved             |
| 96                        | 0.7056              | 1.4112              | 2.1168               | 2.8224              | 4.2336              | 8.4672              | 16.9344              | Reserved             | Reserved             |
| 128                       | 0.9408              | 1.8816              | 2.8224               | 3.7632              | 5.6448              | 11.2896             | 22.5792              | Reserved             | Reserved             |
| 192                       | 1.4112              | 2.8224              | 4.2336               | 5.6448              | 8.4672              | 16.9344             | Reserved             | Reserved             | Reserved             |
| 256                       | 1.8816              | 3.7632              | 5.6448               | 7.5264              | 11.2896             | 22.5792             | Reserved             | Reserved             | Reserved             |
| 384                       | 2.8224              | 5.6448              | 8.4672               | 11.2896             | 16.9344             | Reserved            | Reserved             | Reserved             | Reserved             |
| 512                       | 3.7632              | 7.5264              | 11.2896              | 15.0528             | 22.5792             | Reserved            | Reserved             | Reserved             | Reserved             |
| 1024                      | 7.5264              | 15.0528             | 22.5792              | Reserved            | Reserved            | Reserved            | Reserved             | Reserved             | Reserved             |
| 2048                      | 15.0528             | Reserved            | Reserved             | Reserved            | Reserved            | Reserved            | Reserved             | Reserved             | Reserved             |

The status register ASI\_STS (P0\_R21), captures the device auto detect result for the FSYNC frequency and the BCLK to FSYNC ratio. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes the record channels accordingly.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks. The device also supports an option to use BCLK, GPIO1, or the GPIx pin (as MCLK) as the audio clock source without using the PLL to reduce power consumption. However, the ADC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the [TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios application report](#).

The device also supports an audio bus master mode operation using the GPIO1 or GPIx pin (as MCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on master mode configuration and operation are discussed in the [Configuring and Operating TLV320ADCx120 as an Audio Bus Master application report](#).

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the ASI\_ERR (P0\_R9\_D5) and AUTO\_CLK\_CFG (P0\_R19\_D6) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the [ADCx120EVM-PDK Evaluation module user's guide](#) and the [PurePath™ console graphical development suite](#).

### 6.3.3 Input Channel Configurations

The device consists of two pairs of analog input pins (INxP and INxM) that can be configured as differential inputs or single-ended inputs for the recording channel. The device supports simultaneous recording of up to two channels using the high-performance multichannel ADC. The input source for the analog pins can be from electret condenser analog microphones, micro-electro-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board. Additionally, if the application uses digital PDM microphones for the recording, then the IN2P\_GPI1, IN2M\_GPO1, GPIO1, and MICBIAS\_GPI2 pins can be reconfigured in the device to support up to four channels for the digital microphone recording. The device can also support simultaneous recording on two analog and two digital microphone channels. 表 6-8 shows the input source selection for the record channel.

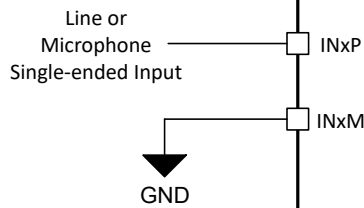
**表 6-8. Input Source Selection for the Record Channel**

| P0_R60_D[6:5] : CH1_INSRC[1:0] | INPUT CHANNEL 1 RECORD SOURCE SELECTION  |
|--------------------------------|--|
| 00 (default)                   | Analog differential input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled) |
| 01                             | Analog single-ended input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled) |
| 10                             | Digital PDM input for channel 1 (configure the GPIx and GPOx pin accordingly for PDMIN1 and PDMCLK)                    |
| 11                             | Reserved (do not use this setting)   |

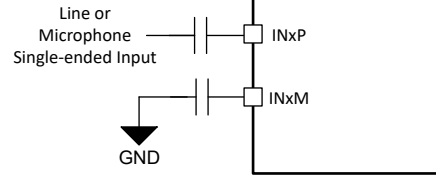
Similarly, the input source selection setting for input channel 2, channel 3, and channel 4 can be configured using the CH2\_INSRC[1:0] (P0\_R65\_D[6:5]), CH3\_INSRC[1:0] (P0\_R70\_D[6:5]), and CH4\_INSRC[1:0] (P0\_R75\_D[6:5]) register bits, respectively.

Typically, voice or audio signal inputs are capacitively coupled (AC coupled) to the device; however, the device also supports an option for DC-coupled inputs to save board space. This configuration can be done independently for each channel by setting the CH1\_DC (P0\_R60\_D4), CH2\_DC (P0\_R65\_D4), CH3\_DC (P0\_R70\_D4), and CH4\_DC (P0\_R75\_D4) register bits. The INxM pin can be directly grounded in DC-coupled mode (see 図 6-14), but the INxM pin must be grounded after the AC-coupling capacitor in AC-coupled mode (see 図 6-15) for the single-ended input configuration. For the best dynamic range performance, the differential AC-coupled input must be used .





**図 6-14. Single-Ended, DC-Coupled Input Connection**



**図 6-15. Single-Ended, AC-Coupled Input Connection**

The device allows for flexibility in choosing the typical input impedance on INxP or INxM from 2.5 k $\Omega$  (default), 10 k $\Omega$ , and 20 k $\Omega$  based on the input source impedance. The higher input impedance results in slightly higher noise or lower dynamic range. 表 6-9 lists the configuration register settings for the input impedance for the record channel.

**表 6-9. Input Impedance Selection for the Record Channel**

| P0_R60_D[3:2] : CH1_IMP[1:0] | CHANNEL 1 INPUT IMPEDANCE SELECTION                                       |
|------------------------------|---|
| 00 (default)                 | Channel 1 input impedance typical value is 2.5 k $\Omega$ on INxP or INxM |
| 01                           | Channel 1 input impedance typical value is 10 k $\Omega$ on INxP or INxM  |
| 10                           | Channel 1 input impedance typical value is 20 k $\Omega$ on INxP or INxM  |
| 11                           | Reserved (do not use this setting)  |

Similarly, the input impedance selection setting for input channel 2 can be configured using the CH2\_IMP[1:0] (P0\_R65\_D[3:2]) register bits.

The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power up. To enable quick charging, the device has modes to speed up the charging of the coupling capacitor. The default value of the quick-charge timing is set for a coupling capacitor up to 1  $\mu$ F. However, if a higher-value capacitor is used in the system, then the quick-charging timing can be increased by using the INCAP\_QCHG (P0\_R5\_D[5:4]) register bits. For best distortion performance, use the low-voltage coefficient capacitors for AC coupling.

The TAA3020 can also support a higher input common-mode tolerance at the expense of noise performance by a few decibels. The device supports three different modes with different common-mode tolerances, which can be configured using the CH1\_INP\_CM\_TOL\_CFG[1:0] (P0\_R58\_D[7:6]) register bits. 表 6-10 lists the configuration register settings for the input impedance for the record channel.

**表 6-10. Common-Mode Tolerance Mode Selection for Record Channel**

| P0_R58_D[7:6] : CH1_INP_CM_TOL_CFG[1:0] | CHANNEL 1 INPUT COMMON-MODE TOLERANCE   |
|---|---|
| 00 (default)                            | Channel 1 input common-mode tolerance of: AC-coupled input = 100 mV <sub>pp</sub> , DC-coupled input = 2.82 V <sub>pp</sub> .   |
| 01                                      | Channel 1 input common-mode tolerance of: AC/DC-coupled input = 1 V <sub>pp</sub> .   |
| 10 (high CMRR mode)                     | Channel 1 input common-mode tolerance of: AC/DC-coupled input = 0-AVDD (supported only with an input impedance of 10 k $\Omega$ and 20 k $\Omega$ ). For input impedance of 2.5 k $\Omega$ , the input common-mode tolerance is 0.4 V to 2.6 V. |
| 11                                      | Reserved (do not use this setting)  |

Similarly, the common-mode tolerance setting for input channel 2 can be configured using the CH2\_INP\_CM\_TOL\_CFG[1:0] (P0\_R58\_D[5:4]) register bits. See the [Input Common Mode Tolerance and High CMRR modes for TLV320ADCx120 Devices application report](#) for further details.

### 6.3.4 Reference Voltage

All audio data converters require a DC reference voltage. The TAA3020 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1- $\mu$ F capacitor connected from the VREF pin to analog ground (AVSS).

The value of this reference voltage can be configured using the P0\_R59\_D[1:0] register bits and must be set to an appropriate value based on the desired full-scale input for the device and the AVDD supply voltage available in the system. The default VREF value is set to 2.75 V, which in turn supports a 2- $V_{RMS}$  differential full-scale input to the device. The required minimum AVDD voltage for this mode is 3 V. 表 6-11 lists the various VREF settings supported along with required AVDD range and the supported full-scale input signal for that configuration.

**表 6-11. VREF Programmable Settings**

| P0_R59_D[1:0] :<br>ADC_FSCALE[1:0] | VREF OUTPUT<br>VOLTAGE (Same as<br>Internal ADC VREF) | DIFFERENTIAL FULL-<br>SCALE INPUT<br>SUPPORTED | SINGLE-ENDED FULL-<br>SCALE INPUT<br>SUPPORTED | AVDD RANGE<br>REQUIREMENT |
|------------------------------------|---|--|--|---------------------------|
| 00 (default)                       | 2.75 V  | 2 $V_{RMS}$                                    | 1 $V_{RMS}$                                    | 3 V to 3.6 V              |
| 01                                 | 2.5 V   | 1.818 $V_{RMS}$                                | 0.909 $V_{RMS}$                                | 2.8 V to 3.6 V            |
| 10                                 | 1.375 V   | 1 $V_{RMS}$                                    | 0.5 $V_{RMS}$                                  | 1.7 V to 1.9 V            |
| 11                                 | Reserved  | Reserved                                       | Reserved                                       | Reserved                  |

To achieve low-power consumption, this audio reference block is powered down as described in the [Sleep Mode or Software Shutdown](#) section. When exiting sleep mode, the audio reference block is powered up using the internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1- $\mu$ F decoupling capacitor. If a higher-value decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF\_QCHG (P0\_R2\_D[4:3]) register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

### 6.3.5 Programmable Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 5 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine tuned for specific microphone combinations.

When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. 表 6-12 shows the available microphone bias programmable options.

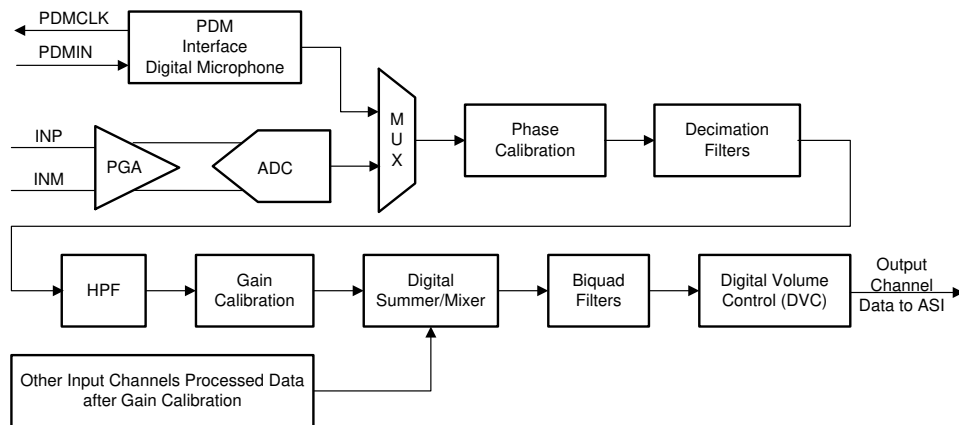
**表 6-12. MICBIAS Programmable Settings**

| P0_R59_D[6:4] : MBIAS_VAL[2:0] | P0_R59_D[1:0] : ADC_FSCALE[1:0] | MICBIAS OUTPUT VOLTAGE                |
|--------------------------------|---------------------------------|---------------------------------------|
| 000 (default)                  | 00 (default)                    | 2.75 V (same as the VREF output)      |
|                                | 01                              | 2.5 V (same as the VREF output)       |
|                                | 10                              | 1.375 V (same as the VREF output)     |
| 001                            | 00 (default)                    | 3.014 V (1.096 times the VREF output) |
|                                | 01                              | 2.740 V (1.096 times the VREF output) |
|                                | 10                              | 1.507 V (1.096 times the VREF output) |
| 010 to 101                     | XX                              | Reserved (do not use these settings)  |
| 110                            | XX                              | Same as AVDD                          |
| 111                            | XX                              | Reserved (do not use this setting)    |

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS\_PDZ (P0\_R117\_D7) register bit. Additionally, the device provides an option to configure the GPIO1 or GPIx pin to directly control the microphone bias output powering on or off. This feature is useful to control the microphone directly without engaging the host for I<sup>2</sup>C communication. The MICBIAS\_PDZ (P0\_R117\_D7) register bit value is ignored if the GPIO1 or GPIx pin is configured to set the microphone bias on or off.

### 6.3.6 Signal-Chain Processing

The TAA3020 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the TAA3020 optimized for a variety of end-equipments and applications that require multichannel audio capture. [Figure 6-16](#) shows a conceptual block diagram that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.



**Figure 6-16. Signal-Chain Processing Flowchart**

The front-end PGA is very low noise, with a 120-dB dynamic range performance. Along with a low-noise and low-distortion, multibit, delta-sigma ADC, the front-end PGA enables the TAA3020 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device also has an integrated programmable biquad filter that allows for custom low-pass, high-pass, or any other desired frequency shaping. Thus, the overall signal chain architecture removes the requirement to add external components for antialiasing low-pass filtering, and thus saves drastically on the external system component cost and board space. See the [TLV320ADCx140 Integrated Analog Anti-Aliasing Filter and Flexible Digital Filter application report](#) for further details.

The signal chain also consists of various highly programmable digital processing blocks such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, and volume control. The details on these processing blocks are discussed further in this section. The device also supports up to four digital PDM microphone recording channels when the analog record channels are not used. Channels 1 to 2 in the signal chain block diagram of [Figure 6-16](#) are as described in this section, however, channels 3 to 4 only support the digital microphone recording option and do not support the digital summer or mixer option.

The desired input channels for recording can be enabled or disabled by using the IN\_CH\_EN (P0\_R115) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI\_OUT\_EN (P0\_R116) register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application needs, if some channels must be

powered-up or powered-down dynamically when the other channel recording is on, then that use case is supported by setting the DYN\_CH\_PUPD\_EN (P0\_R117\_D4) register bit to 1'b1.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

For output sample rates of 48 kHz or lower, the device supports all features for 4-channel recording and various programmable processing blocks. However, for output sample rates higher than 48 kHz, there are limitations in the number of simultaneous channel recordings supported and the number of biquad filters and such. See the [TLV320ADCx140 Sampling Rates and Programmable Processing Blocks Supported application report](#) for further details.

### 6.3.6.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each input channel that can be set to the appropriate value based on the maximum input signal expected in the system and the ADC VREF setting used (see the [Reference Voltage](#) section), which determines the ADC full-scale signal level.

Configure the desired channel gain setting before powering up the ADC channel and do not change this setting when the ADC is powered on. The programmable range supported for each channel gain is from 0 dB to 42 dB in steps of 0.5 dB. To achieve low-noise performance, the device internal logic first maximizes the gain for the front-end, low-noise analog PGA, which supports a dynamic range of 120 dB, and then applies any residual programmed channel gain in the digital processing block.

表 6-13 shows the programmable options available for the channel gain.

**表 6-13. Channel Gain Programmable Settings**

| P0_R61_D[7:1] : CH1_GAIN[6:0]      | CHANNEL GAIN SETTING FOR INPUT CHANNEL 1 |
|------------------------------------|--|
| 000 0000 = 0d (default)            | Input channel 1 gain is set to 0 dB      |
| 000 0001 = 1d                      | Input channel 1 gain is set to 0.5 dB    |
| 000 0010 = 2d                      | Input channel 1 gain is set to 1 dB      |
| ...                                | ...                                      |
| 101 0011 = 83d                     | Input channel 1 gain is set to 41.5 dB   |
| 101 0100 = 84d                     | Input channel 1 gain is set to 42 dB     |
| 101 0101 to 111 1111 = 85d to 127d | Reserved (do not use these settings)     |

Similarly, the channel gain setting for input channel 2 can be configured using the CH2\_GAIN (P0\_R66\_D[7:1]) register bits. The channel gain feature is not available for the digital microphone record path.

The device also supports gain change when the ADC is enabled. The device supports multiple configurations to limit the audible artifacts during dynamic gain change. This feature can be configured by using the OTF\_GAIN\_CHANGE\_CFG (P0\_R113\_D[7:6]) register bits.

The device also has a programmable digital volume control with a range from –100 dB to +27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically when the ADC channel is powered up and recording. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DISABLE\_SOFT\_STEP (P0\_R108\_D4) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang-up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the DVOL\_GANG (P0\_R108\_D7) register bit.

表 6-14 shows the programmable options available for the digital volume control.

**表 6-14. Digital Volume Control (DVC) Programmable Settings**

| P0_R62_D[7:0] : CH1_DVOL[7:0] | DVC SETTING FOR OUTPUT CHANNEL 1        |
|-------------------------------|---|
| 0000 0000 = 0d                | Output channel 1 DVC is set to mute     |
| 0000 0001 = 1d                | Output channel 1 DVC is set to –100 dB  |
| 0000 0010 = 2d                | Output channel 1 DVC is set to –99.5 dB |
| 0000 0011 = 3d                | Output channel 1 DVC is set to –99 dB   |
| ...                           | ...                                     |
| 1100 1000 = 200d              | Output channel 1 DVC is set to –0.5 dB  |
| 1100 1001 = 201d (default)    | Output channel 1 DVC is set to 0 dB     |
| 1100 1010 = 202d              | Output channel 1 DVC is set to 0.5 dB   |
| ...                           | ...                                     |
| 1111 1101 = 253d              | Output channel 1 DVC is set to 26 dB    |
| 1111 1110 = 254d              | Output channel 1 DVC is set to 26.5 dB  |
| 1111 1111 = 255d              | Output channel 1 DVC is set to 27 dB    |

Similarly, the digital volume control setting for output channel 2 to channel 4 can be configured using the CH2\_DVOL (P0\_R67) to CH4\_DVOL (P0\_R77) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the DISABLE\_SOFT\_STEP (P0\_R108\_D4) register bit.

#### 6.3.6.2 Programmable Channel Gain Calibration

Along with the programmable channel gain and digital volume, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. 表 6-15 shows the programmable options available for the channel gain calibration.

**表 6-15. Channel Gain Calibration Programmable Settings**

| P0_R63_D[7:4] : CH1_GCAL[3:0] | CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1 |
|-------------------------------|--|
| 0000 = 0d                     | Input channel 1 gain calibration is set to –0.8 dB   |
| 0001 = 1d                     | Input channel 1 gain calibration is set to –0.7 dB   |
| ...                           | ...  |
| 1000 = 8d (default)           | Input channel 1 gain calibration is set to 0 dB      |
| ...                           | ...  |
| 1110 = 14d                    | Input channel 1 gain calibration is set to 0.6 dB    |
| 1111 = 15d                    | Input channel 1 gain calibration is set to 0.7 dB    |

Similarly, the channel gain calibration setting for input channel 2 to channel 4 can be configured using the CH2\_GCAL (P0\_R68) to CH4\_GCAL (P0\_R78) register bits, respectively.

### 6.3.6.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error of the analog microphone. The modulator clock, which is the same clock used for ADC\_MOD\_CLK, is 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz). For the digital microphone interface, the phase calibration clock is dependent on the PDM clock used. For a PDM\_CLK of 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz), the phase calibration clock is the same as PDM\_CLK. For a PDM\_CLK equal to or lower than 3.072 MHz (the output data sample rate is multiples or submultiples of 48 kHz), the phase calibration clock used is 3.072 MHz. Similarly, for a PDM\_CLK of 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (the output data sample rate is multiples or submultiples of 44.1 kHz), and the phase calibration clock used is 2.8224 MHz. This feature is very useful for applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. 表 6-16 shows the available programmable options for channel phase calibration for the analog or digital microphone with a PDM\_CLK of 6.144 MHz or 5.6448 MHz.

**表 6-16. Channel Phase Calibration Programmable Settings**

| P0_R64_D[7:0] : CH1_PCAL[7:0] | CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1                               |
|-------------------------------|---|
| 0000 0000 = 0d (default)      | Input channel 1 phase calibration with no delay                                     |
| 0000 0001 = 1d                | Input channel 1 phase calibration delay is set to one cycle of the modulator clock  |
| 0000 0010 = 2d                | Input channel 1 phase calibration delay is set to two cycles of the modulator clock |
| ...                           | ...   |
| 1111 1110 = 254d              | Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock |
| 1111 1111 = 255d              | Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock |

For a digital microphone interface with a PDM\_CLK frequency below 3.072 MHz, the phase calibration range is from 0 to 127 of the phase calibration clock (3.072 MHz for the output data sample rate is multiples or submultiples of 48 kHz and 2.8224 MHz for the output data sample rate is multiples or submultiples of 44.1 kHz). This range can be configured using CH1\_PCAL[7:1] for channel 1.

Similarly, the channel phase calibration setting for input channel 2 to channel 4 can be configured using the CH2\_PCAL (P0\_R69) to CH4\_PCAL (P0\_R79) register bits, respectively.

The phase calibration feature must not be used when the analog input and PDM input are used together for simultaneous conversion.

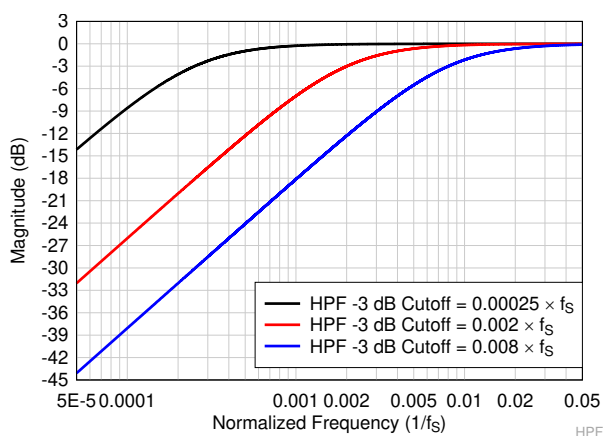
### 6.3.6.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. 表 6-17 shows the predefined –3-dB cutoff frequencies available that can be set by using the HPF\_SEL[1:0] register bits of P0\_R107. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF\_SEL[1:0] register bits are set to 2'b00. 図 6-17 shows a frequency response plot for the HPF filter.

**表 6-17. HPF Programmable Settings**

| P0_R107_D[1:0] : HPF_SEL[1:0] | -3-dB CUTOFF FREQUENCY SETTING    | -3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE | -3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE |
|-------------------------------|-----------------------------------|--|--|
| 00                            | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter            | Programmable 1st-order IIR filter            |
| 01 (default)                  | $0.00025 \times f_s$              | 4 Hz   | 12 Hz  |
| 10                            | $0.002 \times f_s$                | 32 Hz  | 96 Hz  |
| 11                            | $0.008 \times f_s$                | 128 Hz                                       | 384 Hz                                       |





**図 6-17. HPF Filter Frequency Response Plot**

式 1 gives the transfer function for the first-order programmable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (1)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in 表 6-18 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF\_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any ADC channel for recording. 表 6-18 shows the filter coefficients for the first-order IIR filter.

**表 6-18. 1st-Order IIR Filter Coefficients**

| FILTER  | FILTER COEFFICIENT | DEFAULT COEFFICIENT VALUE | COEFFICIENT REGISTER MAPPING |
|---|--------------------|---------------------------|------------------------------|
| Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter) | N <sub>0</sub>     | 0x7FFFFFFF                | P4_R72-R75                   |
|   | N <sub>1</sub>     | 0x00000000                | P4_R76-R79                   |
|   | D <sub>1</sub>     | 0x00000000                | P4_R80-R83                   |



### 6.3.6.5 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters. These highly efficient filters achieve the desired frequency response. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. 式 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1z^{-1} + N_2z^{-2}}{2^{31} - 2D_1z^{-1} - D_2z^{-2}} \quad (2)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in the セクション 7.4.1 and セクション 7.4.2 sections. If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. As described in 表 6-19, these biquad filters can be allocated for each output channel based on the BIQUAD\_CFG[1:0] register setting of P0\_R108. By setting BIQUAD\_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional filtering is required for the system application. See the [TLV320ADCx140 Programmable Biquad Filter Configuration and Applications application report](#) for further details.

**表 6-19. Biquad Filter Allocation to the Record Output Channel**

| PROGRAMMABLE BIQUAD FILTER | RECORD OUTPUT CHANNEL ALLOCATION USING P0_R108_D[6:5] REGISTER SETTING |  |  |
|----------------------------|--|--|--|
|                            | BIQUAD_CFG[1:0] = 2'b01<br>(1 Biquad per Channel)                      | BIQUAD_CFG[1:0] = 2'b10 (Default)<br>(2 Biquads per Channel) | BIQUAD_CFG[1:0] = 2'b11<br>(3 Biquads per Channel) |
| Biquad filter 1            | Allocated to output channel 1  | Allocated to output channel 1                                | Allocated to output channel 1                      |
| Biquad filter 2            | Allocated to output channel 2  | Allocated to output channel 2                                | Allocated to output channel 2                      |
| Biquad filter 3            | Allocated to output channel 3  | Allocated to output channel 3                                | Allocated to output channel 3                      |
| Biquad filter 4            | Allocated to output channel 4  | Allocated to output channel 4                                | Allocated to output channel 4                      |
| Biquad filter 5            | Not used   | Allocated to output channel 1                                | Allocated to output channel 1                      |
| Biquad filter 6            | Not used   | Allocated to output channel 2                                | Allocated to output channel 2                      |
| Biquad filter 7            | Not used   | Allocated to output channel 3                                | Allocated to output channel 3                      |
| Biquad filter 8            | Not used   | Allocated to output channel 4                                | Allocated to output channel 4                      |
| Biquad filter 9            | Not used   | Not used   | Allocated to output channel 1                      |
| Biquad filter 10           | Not used   | Not used   | Allocated to output channel 2                      |
| Biquad filter 11           | Not used   | Not used   | Allocated to output channel 3                      |
| Biquad filter 12           | Not used   | Not used   | Allocated to output channel 4                      |

表 6-20 shows the biquad filter coefficients mapping to the register space.

**表 6-20. Biquad Filter Coefficients Register Mapping**

| PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING | PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING |
|----------------------------|---|----------------------------|---|
| Biquad filter 1            | P2_R8-R27                                   | Biquad filter 7            | P3_R8-R27                                   |
| Biquad filter 2            | P2_R28-R47                                  | Biquad filter 8            | P3_R28-R47                                  |
| Biquad filter 3            | P2_R48-R67                                  | Biquad filter 9            | P3_R48-R67                                  |
| Biquad filter 4            | P2_R68-R87                                  | Biquad filter 10           | P3_R68-R87                                  |
| Biquad filter 5            | P2_R88-R107                                 | Biquad filter 11           | P3_R88-R107                                 |
| Biquad filter 6            | P2_R108-R127                                | Biquad filter 12           | P3_R108-R127                                |

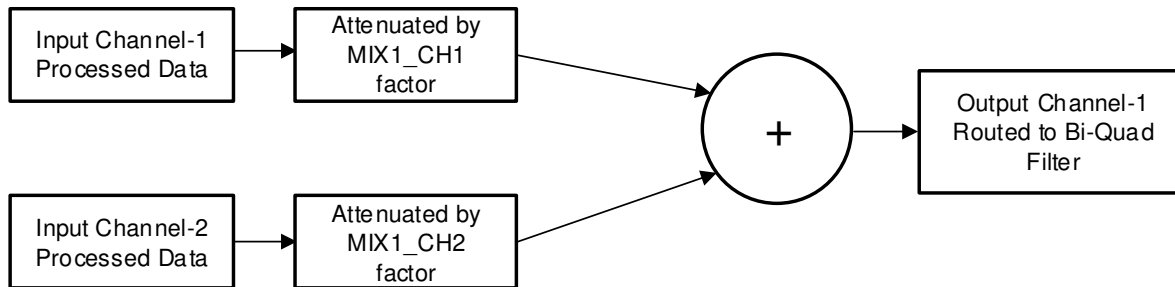
### 6.3.6.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise. 表 6-21 lists the configuration settings available for channel summing mode.

**表 6-21. Channel Summing Mode Programmable Settings**

| P0_R107_D[3:2] : CH_SUM[1:0] | CHANNEL SUMMING MODE FOR INPUT CHANNELS                    | SNR AND DYNAMIC RANGE BOOST                |
|------------------------------|--|--|
| 00 (default)                 | Channel summing mode is disabled                           | Not applicable                             |
| 01                           | Output channel 1 = (input channel 1 + input channel 2) / 2 | Around 3-dB boost in SNR and dynamic range |
|                              | Output channel 2 = (input channel 1 + input channel 2) / 2 |  |
| 10                           | Reserved (do not use this setting)                         | Not applicable                             |
| 11                           | Reserved (do not use this setting)                         | Not applicable                             |

The device additionally supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. The programmable mixer feature is available only if CH\_SUM[1:0] is set to 2'b00. The mixer function is supported for all input channels. 図 6-18 shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the セクション 7.4.3 section.



**図 6-18. Programmable Digital Mixer Block Diagram**

A similar mixer operation is performed by mixer 2 to generate output channel 2.

### 6.3.6.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma ( $\Delta\Sigma$ ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. As illustrated in [Figure 6-16](#), this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the DECI\_FILT (P0\_R107\_D[5:4]) register bits. [Table 6-22](#) shows the configuration register setting for the decimation filter mode selection for the record channel.

**表 6-22. Decimation Filter Mode Selection for the Record Channel**

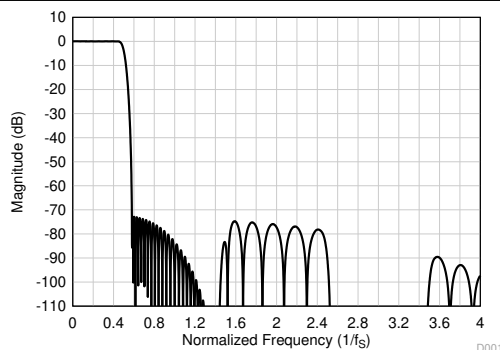
| P0_R107_D[5:4] : DECI_FILT[1:0] | DECIMATION FILTER MODE SELECTION                      |
|---------------------------------|---|
| 00 (default)                    | Linear phase filters are used for the decimation      |
| 01                              | Low latency filters are used for the decimation       |
| 10                              | Ultra-low latency filters are used for the decimation |
| 11                              | Reserved (do not use this setting)                    |

#### 6.3.6.7.1 Linear Phase Filters

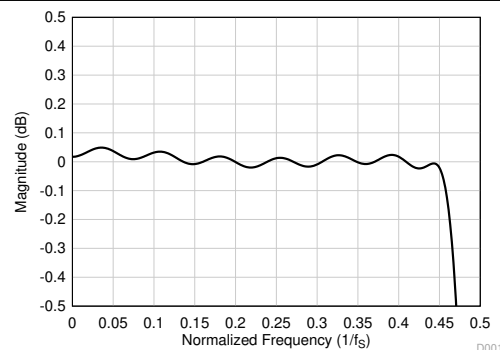
The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

##### 6.3.6.7.1.1 Sampling Rate: 7.35 kHz to 8 kHz

[Figure 6-19](#) and [Figure 6-20](#) respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 7.35 kHz to 8 kHz. [Table 6-23](#) lists the specifications for a decimation filter with a 7.35-kHz to 8-kHz sampling rate.



**図 6-19. Linear Phase Decimation Filter Magnitude Response**



**図 6-20. Linear Phase Decimation Filter Pass-Band Ripple**

**表 6-23. Linear Phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_s$             | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 72.7  |      |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards              | 81.2  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$             |       | 17.1 |      | $1/f_s$ |

### 6.3.6.7.1.2 Sampling Rate: 14.7 kHz to 16 kHz

図 6-21 and 図 6-22 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. 表 6-24 lists the specifications for a decimation filter with a 14.7 kHz to 16-kHz sampling rate.

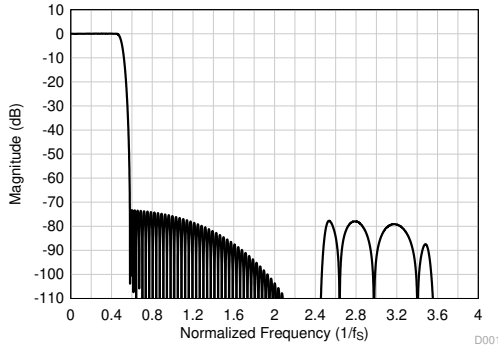


図 6-21. Linear Phase Decimation Filter Magnitude Response

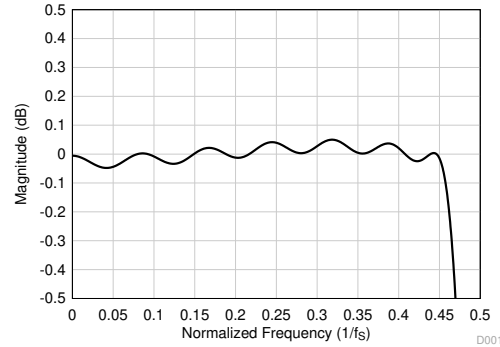


図 6-22. Linear Phase Decimation Filter Pass-Band Ripple

表 6-24. Linear Phase Decimation Filter Specifications

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_s$             | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 73.3  |      |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards              | 95.0  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$             |       | 15.7 |      | $1/f_s$ |

### 6.3.6.7.1.3 Sampling Rate: 22.05 kHz to 24 kHz

図 6-23 and 図 6-24 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. 表 6-25 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

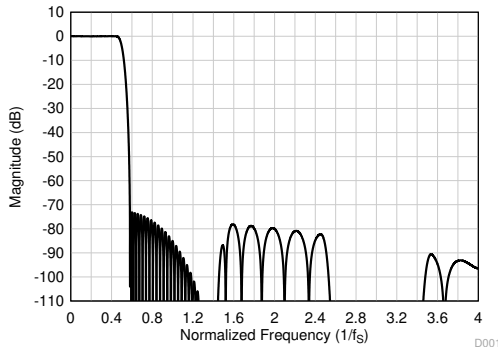


図 6-23. Linear Phase Decimation Filter Magnitude Response

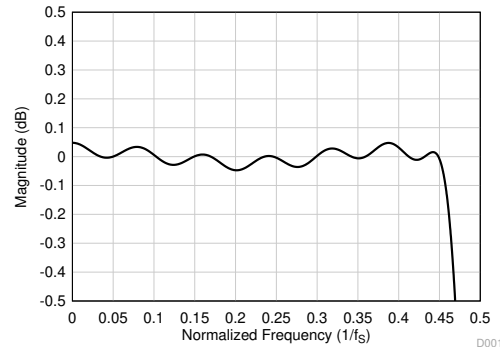


図 6-24. Linear Phase Decimation Filter Pass-Band Ripple

表 6-25. Linear Phase Decimation Filter Specifications

| PARAMETER             | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT |
|-----------------------|--|-------|-----|------|------|
| Pass-band ripple      | Frequency range is 0 to $0.454 \times f_s$             | -0.05 |     | 0.05 | dB   |
| Stop-band attenuation | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 73.0  |     |      | dB   |
|                       | Frequency range is $4 \times f_s$ onwards              | 96.4  |     |      |      |

表 6-25. Linear Phase Decimation Filter Specifications (続き)

| PARAMETER              | TEST CONDITIONS                            | MIN | TYP  | MAX | UNIT    |
|------------------------|--|-----|------|-----|---------|
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$ |     | 16.6 |     | $1/f_s$ |

## 6.3.6.7.1.4 Sampling Rate: 29.4 kHz to 32 kHz

図 6-25 and 図 6-26 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. 表 6-26 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

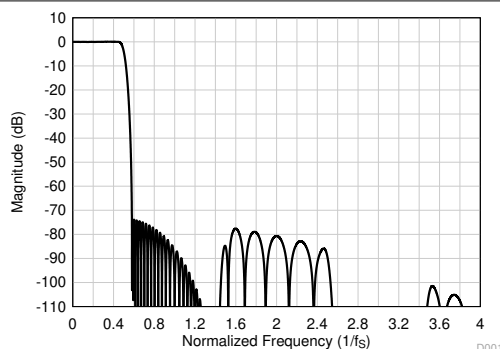


図 6-25. Linear Phase Decimation Filter Magnitude Response

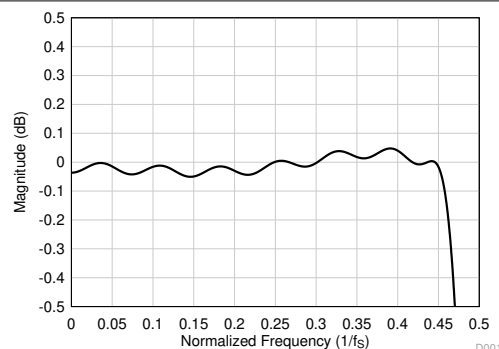


図 6-26. Linear Phase Decimation Filter Pass-Band Ripple

表 6-26. Linear Phase Decimation Filter Specifications

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_s$             | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 73.7  |      |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards              | 107.2 |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$             |       | 16.9 |      | $1/f_s$ |

## 6.3.6.7.1.5 Sampling Rate: 44.1 kHz to 48 kHz

図 6-27 and 図 6-28 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. 表 6-27 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

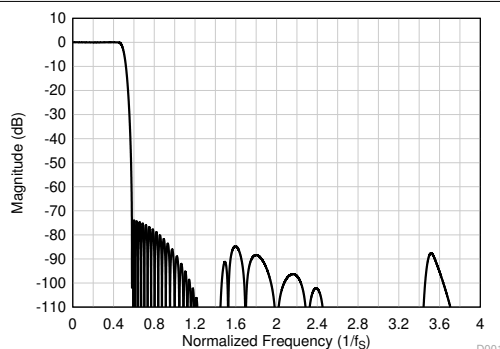


図 6-27. Linear Phase Decimation Filter Magnitude Response

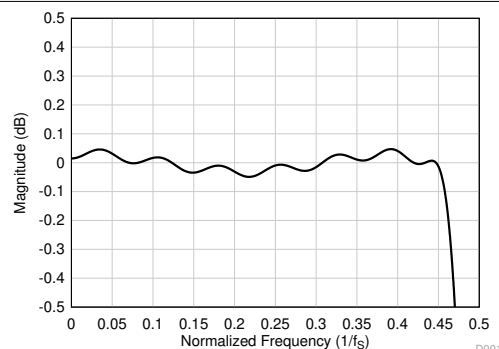


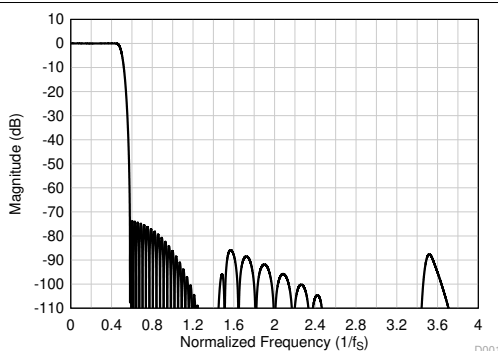
図 6-28. Linear Phase Decimation Filter Pass-Band Ripple

**表 6-27. Linear Phase Decimation Filter Specifications**

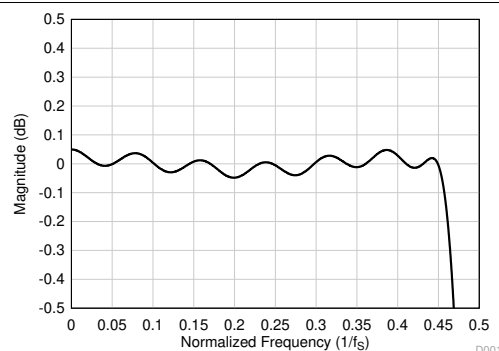
| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_S$             | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 73.8  |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards              | 98.1  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$             |       | 17.1 |      | $1/f_S$ |

#### 6.3.6.7.1.6 Sampling Rate: 88.2 kHz to 96 kHz

図 6-29 and 図 6-30 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. 表 6-28 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.



**図 6-29. Linear Phase Decimation Filter Magnitude Response**



**図 6-30. Linear Phase Decimation Filter Pass-Band Ripple**

**表 6-28. Linear Phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_S$             | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 73.6  |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards              | 97.9  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$             |       | 17.1 |      | $1/f_S$ |

#### 6.3.6.7.1.7 Sampling Rate: 176.4 kHz to 192 kHz

図 6-31 and 図 6-32 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. 表 6-29 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

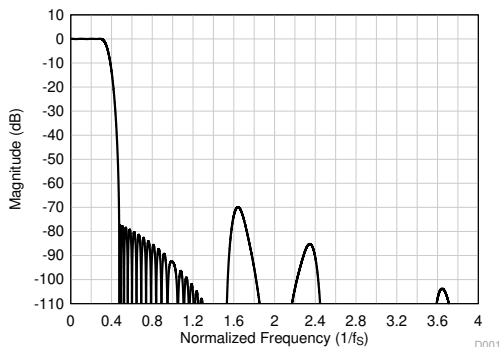


図 6-31. Linear Phase Decimation Filter Magnitude Response

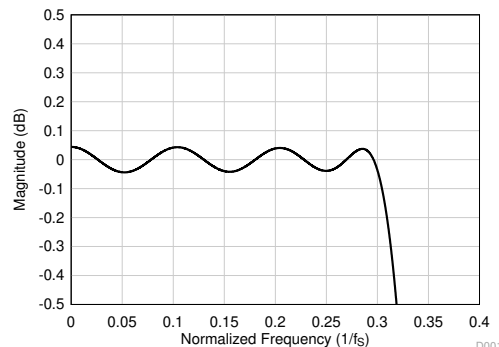


図 6-32. Linear Phase Decimation Filter Pass-Band Ripple

表 6-29. Linear Phase Decimation Filter Specifications

| PARAMETER              | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.3 \times f_s$                | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.473 \times f_s$ to $4 \times f_s$ | 70.0  |      |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards               | 111.0 |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.3 \times f_s$                |       | 11.9 |      | $1/f_s$ |

#### 6.3.6.7.1.8 Sampling Rate: 352.8 kHz to 384 kHz

図 6-33 and 図 6-34 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. 表 6-30 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

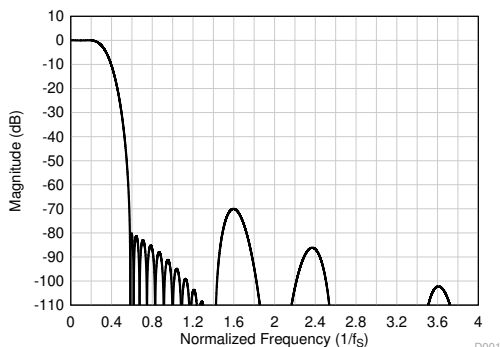


図 6-33. Linear Phase Decimation Filter Magnitude Response

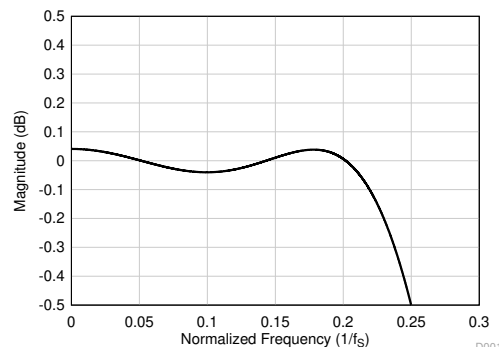


図 6-34. Linear Phase Decimation Filter Pass-Band Ripple

表 6-30. Linear Phase Decimation Filter Specifications

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT    |
|------------------------|--|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.212 \times f_s$             | -0.05 |     | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 70.0  |     |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards              | 108.8 |     |      |         |
| Group delay or latency | Frequency range is 0 to $0.212 \times f_s$             |       | 7.2 |      | $1/f_s$ |



### 6.3.6.7.1.9 Sampling Rate: 705.6 kHz to 768 kHz

図 6-35 and 図 6-36 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 705.6 kHz to 768 kHz. 表 6-31 lists the specifications for a decimation filter with a 705.6-kHz to 768-kHz sampling rate.

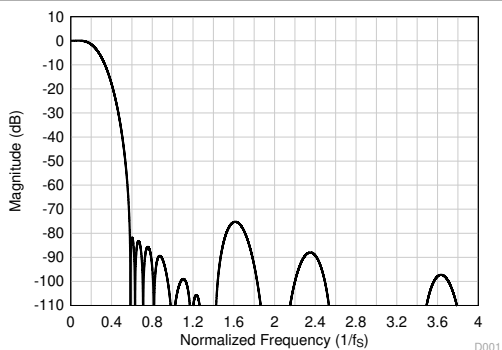


図 6-35. Linear Phase Decimation Filter Magnitude Response

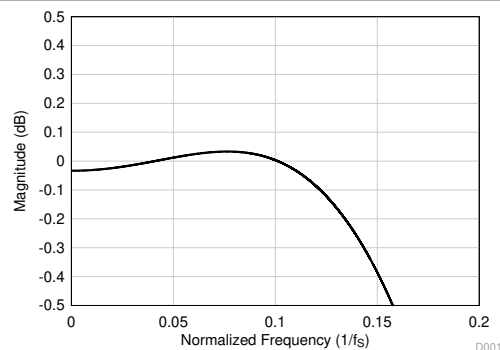


図 6-36. Linear Phase Decimation Filter Pass-Band Ripple

表 6-31. Linear Phase Decimation Filter Specifications

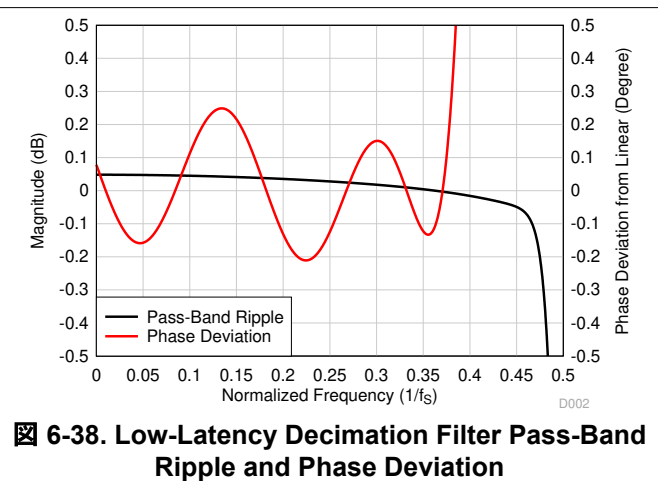
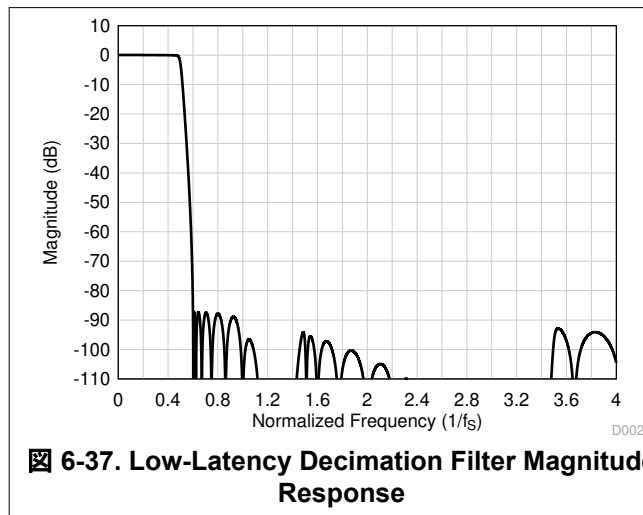
| PARAMETER              | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT    |
|------------------------|--|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.113 \times f_s$             | -0.05 |     | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_s$ to $2 \times f_s$ | 75.0  |     |      | dB      |
|                        | Frequency range is $2 \times f_s$ onwards              | 88.0  |     |      |         |
| Group delay or latency | Frequency range is 0 to $0.113 \times f_s$             |       | 5.9 |      | $1/f_s$ |

### 6.3.6.7.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the TAA3020 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the  $0.365 \times f_s$  frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

#### 6.3.6.7.2.1 Sampling Rate: 14.7 kHz to 16 kHz

図 6-37 shows the magnitude response and 図 6-38 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. 表 6-32 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

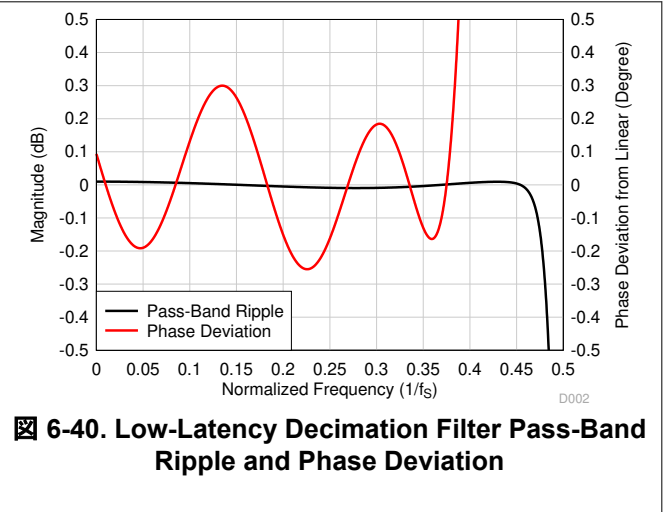
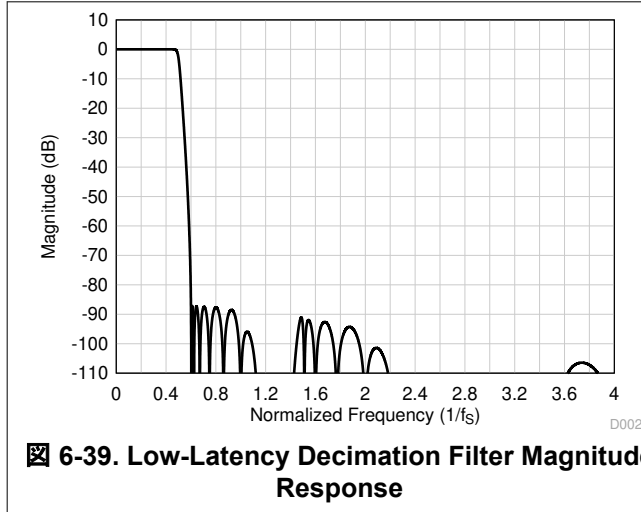


**表 6-32. Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                              | MIN    | TYP | MAX   | UNIT    |
|------------------------|--|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.451 \times f_s$   | -0.05  |     | 0.05  | dB      |
| Stop-band attenuation  | Frequency range is $0.61 \times f_s$ onwards | 87.3   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.363 \times f_s$   |        | 7.6 |       | $1/f_s$ |
| Group delay deviation  | Frequency range is 0 to $0.363 \times f_s$   | -0.022 |     | 0.022 | $1/f_s$ |
| Phase deviation        | Frequency range is 0 to $0.363 \times f_s$   | -0.21  |     | 0.25  | Degrees |

#### 6.3.6.7.2.2 Sampling Rate: 22.05 kHz to 24 kHz

図 6-39 shows the magnitude response and 図 6-40 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. 表 6-33 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

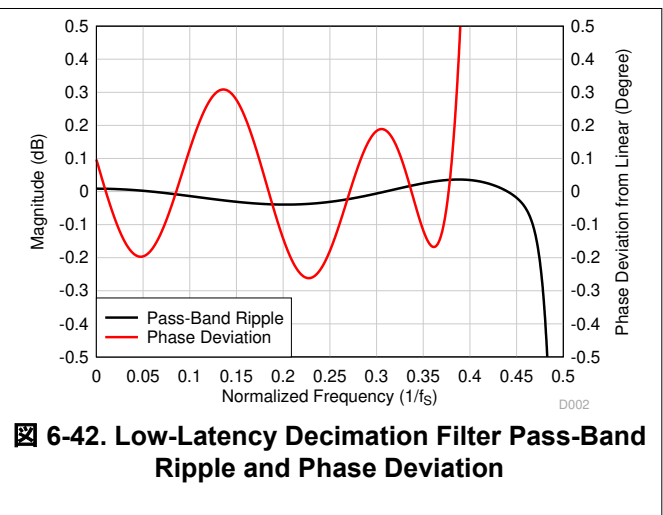
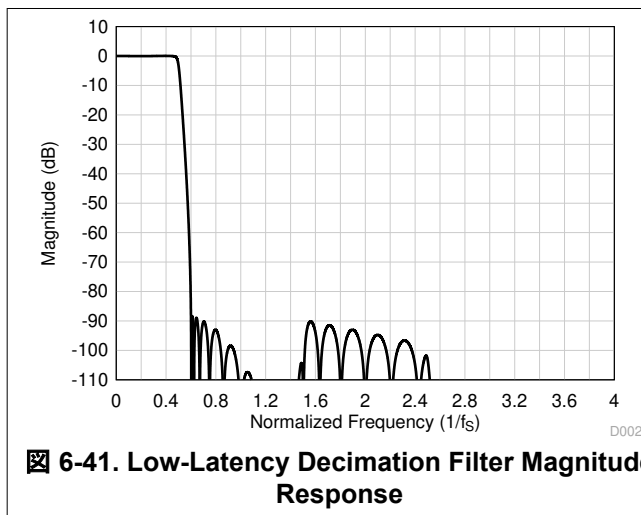


**表 6-33. Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.459 \times f_s$  | -0.01  |     | 0.01  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ onwards | 87.2   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.365 \times f_s$  |        | 7.5 |       | $1/f_s$ |
| Group delay deviation  | Frequency range is 0 to $0.365 \times f_s$  | -0.026 |     | 0.026 | $1/f_s$ |
| Phase deviation        | Frequency range is 0 to $0.365 \times f_s$  | -0.26  |     | 0.30  | Degrees |

#### 6.3.6.7.2.3 Sampling Rate: 29.4 kHz to 32 kHz

図 6-41 shows the magnitude response and 図 6-42 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. 表 6-34 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

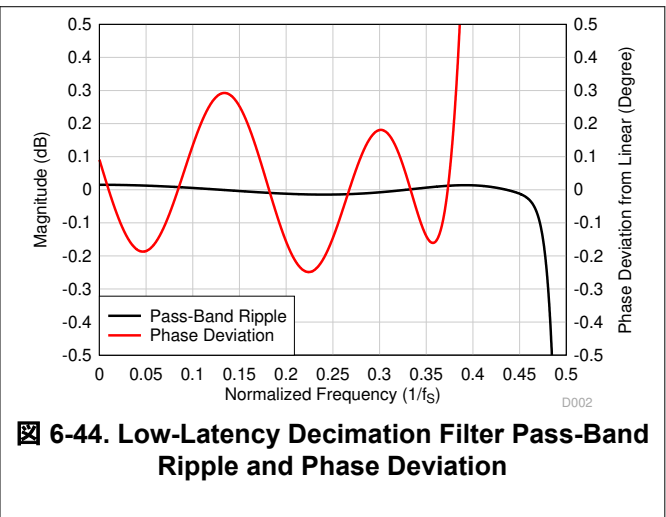
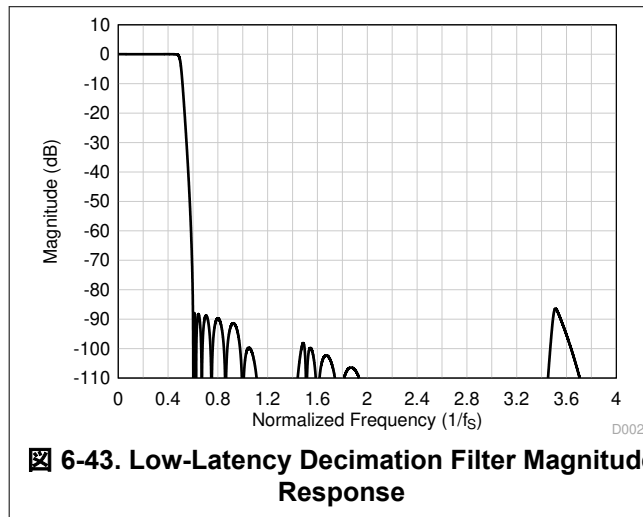


**表 6-34. Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.457 \times f_S$  | −0.04  |     | 0.04  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 88.3   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.368 \times f_S$  |        | 8.7 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.368 \times f_S$  | −0.026 |     | 0.026 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.368 \times f_S$  | −0.26  |     | 0.31  | Degrees |

**6.3.6.7.2.4 Sampling Rate: 44.1 kHz to 48 kHz**

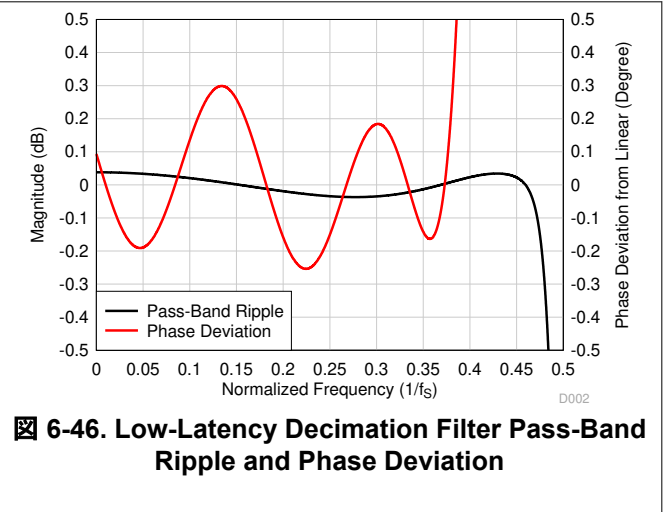
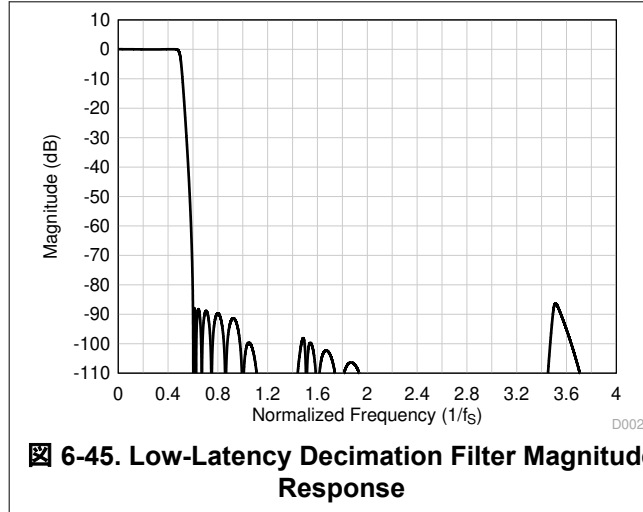
図 6-43 shows the magnitude response and 図 6-44 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. 表 6-35 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

**表 6-35. Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.452 \times f_S$  | −0.015 |     | 0.015 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 86.4   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.365 \times f_S$  |        | 7.7 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.365 \times f_S$  | −0.027 |     | 0.027 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.365 \times f_S$  | −0.25  |     | 0.30  | Degrees |

#### 6.3.6.7.2.5 Sampling Rate: 88.2 kHz to 96 kHz

図 6-45 shows the magnitude response and 図 6-46 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. 表 6-36 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

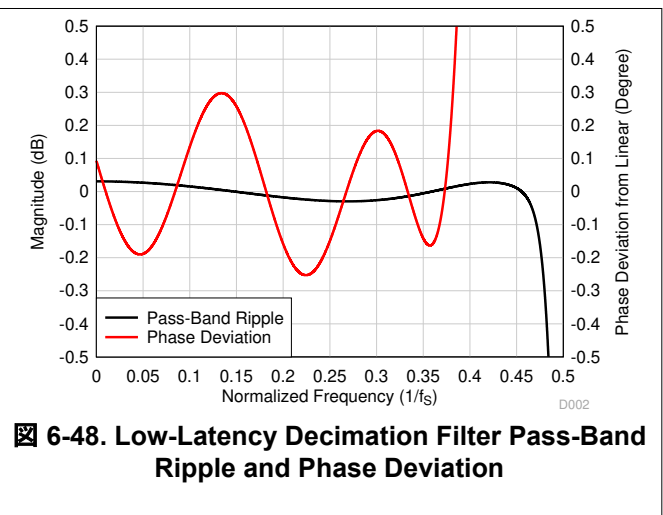
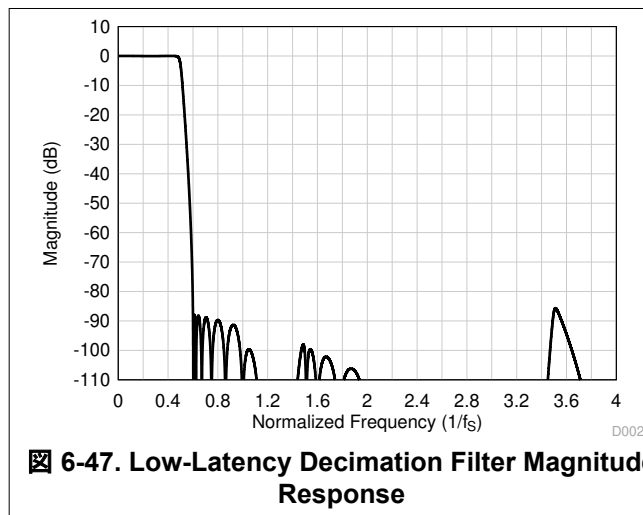


**表 6-36. Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.466 \times f_s$  | -0.04  |     | 0.04  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ onwards | 86.3   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.365 \times f_s$  |        | 7.7 |       | $1/f_s$ |
| Group delay deviation  | Frequency range is 0 to $0.365 \times f_s$  | -0.027 |     | 0.027 | $1/f_s$ |
| Phase deviation        | Frequency range is 0 to $0.365 \times f_s$  | -0.26  |     | 0.30  | Degrees |

#### 6.3.6.7.2.6 Sampling Rate: 176.4 kHz to 192 kHz

図 6-47 shows the magnitude response and 図 6-48 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. 表 6-37 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.



**表 6-37. Low-Latency Decimation Filter Specifications**

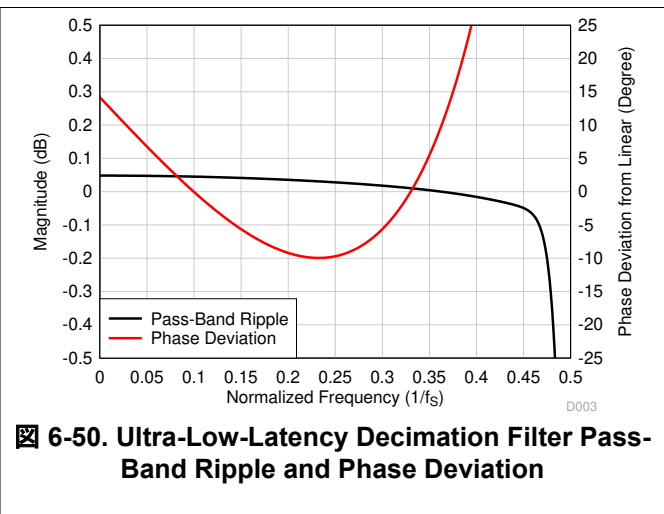
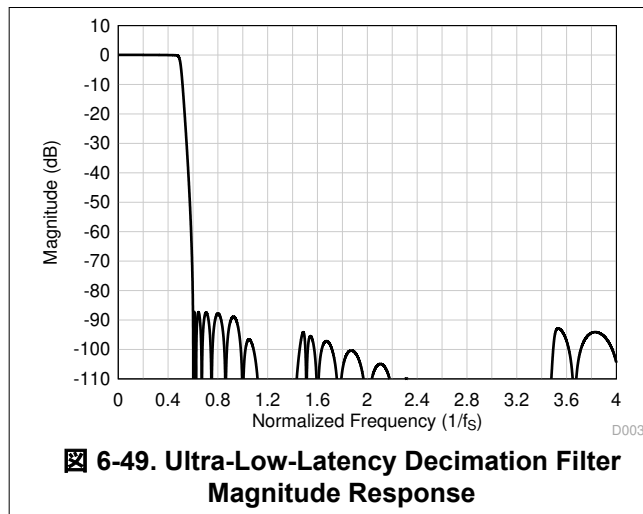
| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $463 \times f_S$    | -0.03  |     | 0.03  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 85.6   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.365 \times f_S$  |        | 7.7 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.365 \times f_S$  | -0.027 |     | 0.027 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.365 \times f_S$  | -0.26  |     | 0.30  | Degrees |

**6.3.6.7.3 Ultra-Low Latency Filters**

For applications where ultra-low latency (within the audio band) is critical, the ultra-low latency decimation filters on the TAA3020 can be used. The device supports these filters with a group delay of approximately four samples with an almost linear phase response within the  $0.325 \times f_S$  frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the ultra-low latency filters.

**6.3.6.7.3.1 Sampling Rate: 14.7 kHz to 16 kHz**

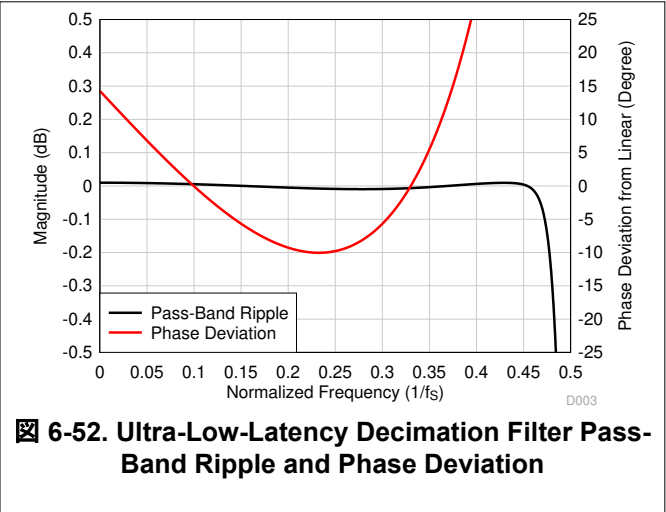
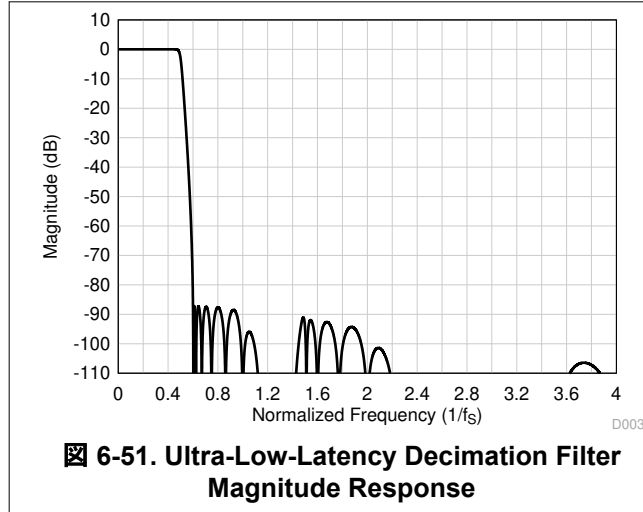
図 6-49 shows the magnitude response and 図 6-50 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. 表 6-38 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

**表 6-38. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.45 \times f_S$   | -0.05  |     | 0.05  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 87.2   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.325 \times f_S$  |        | 4.3 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.325 \times f_S$  | -0.512 |     | 0.512 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.325 \times f_S$  | -10.0  |     | 14.2  | Degrees |

### 6.3.6.7.3.2 Sampling Rate: 22.05 kHz to 24 kHz

図 6-51 shows the magnitude response and 図 6-52 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. 表 6-39 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

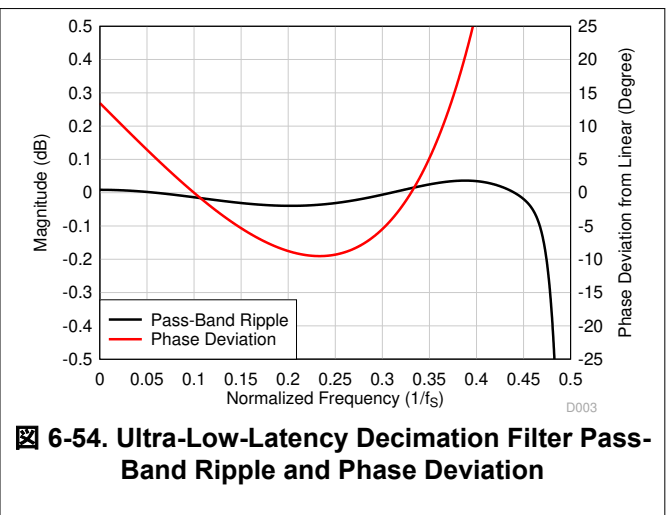
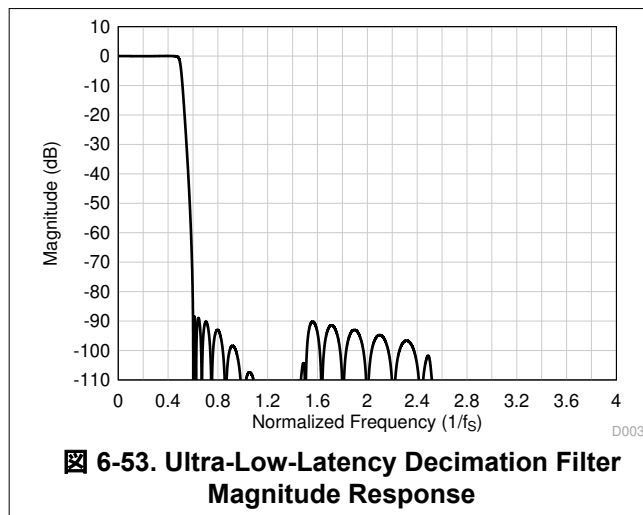


**表 6-39. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.46 \times f_s$   | -0.01  |     | 0.01  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ onwards | 87.1   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.325 \times f_s$  |        | 4.1 |       | $1/f_s$ |
| Group delay deviation  | Frequency range is 0 to $0.325 \times f_s$  | -0.514 |     | 0.514 | $1/f_s$ |
| Phase deviation        | Frequency range is 0 to $0.325 \times f_s$  | -10.0  |     | 14.3  | Degrees |

### 6.3.6.7.3.3 Sampling Rate: 29.4 kHz to 32 kHz

図 6-53 shows the magnitude response and 図 6-54 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. 表 6-40 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

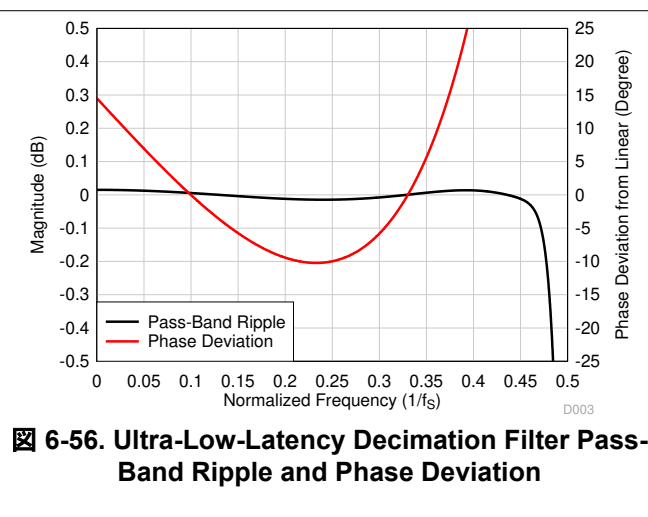
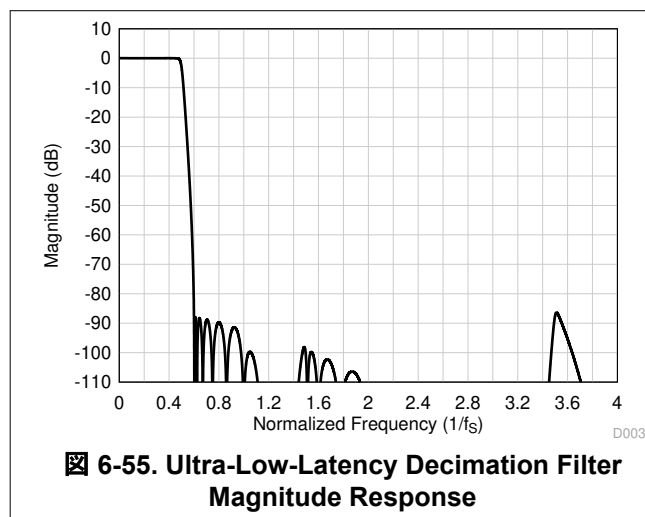


**表 6-40. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.457 \times f_S$  | -0.04  |     | 0.04  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 88.3   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.325 \times f_S$  |        | 5.2 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.325 \times f_S$  | -0.492 |     | 0.492 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.325 \times f_S$  | -9.5   |     | 13.5  | Degrees |

**6.3.6.7.3.4 Sampling Rate: 44.1 kHz to 48 kHz**

図 6-55 shows the magnitude response and 図 6-56 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. 表 6-41 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

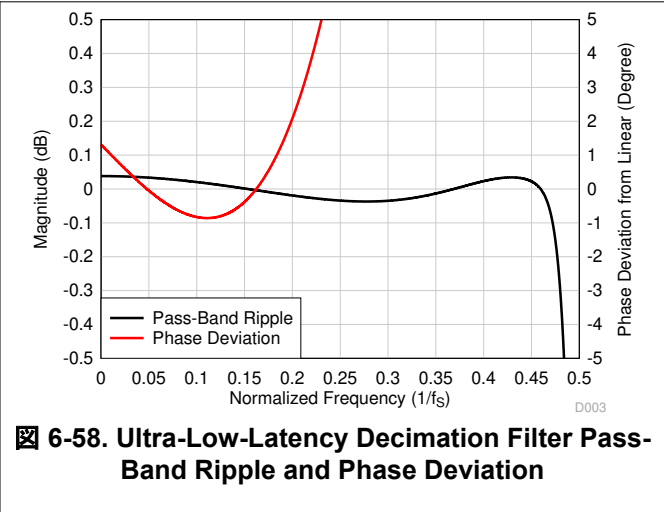
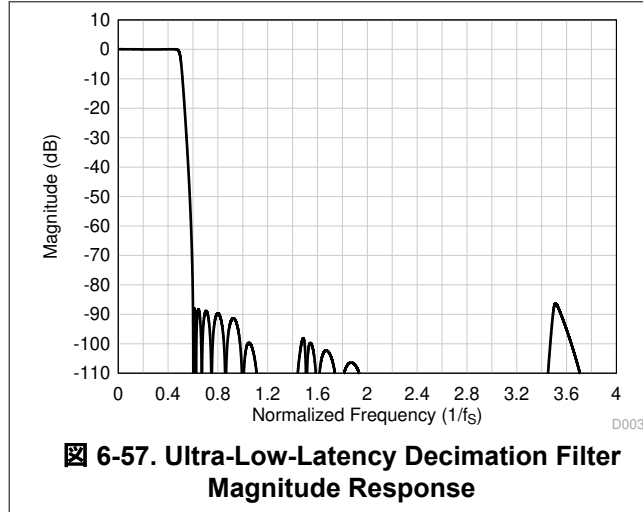
**表 6-41. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.452 \times f_S$  | -0.015 |     | 0.015 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 86.4   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.325 \times f_S$  |        | 4.1 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.325 \times f_S$  | -0.525 |     | 0.525 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.325 \times f_S$  | -10.3  |     | 14.5  | Degrees |



### 6.3.6.7.3.5 Sampling Rate: 88.2 kHz to 96 kHz

図 6-57 shows the magnitude response and 図 6-58 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. 表 6-42 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

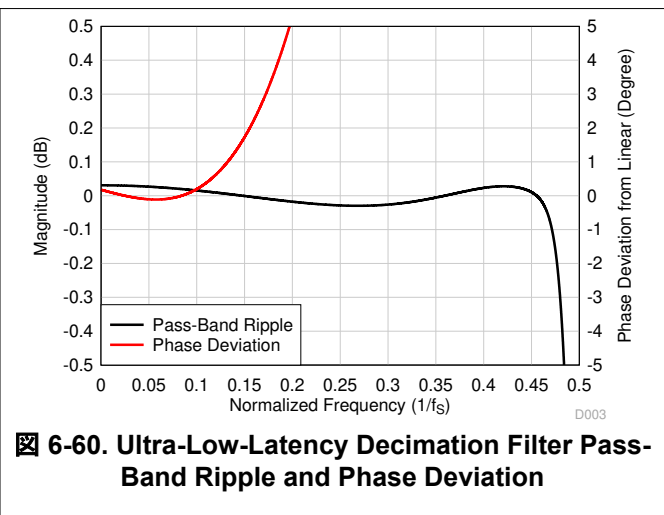
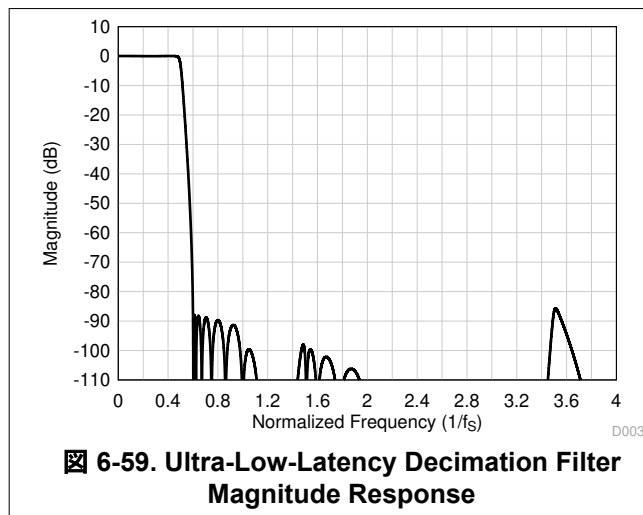


**表 6-42. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.466 \times f_s$  | -0.04  |     | 0.04  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ onwards | 86.3   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.1625 \times f_s$ |        | 3.7 |       | $1/f_s$ |
| Group delay deviation  | Frequency range is 0 to $0.1625 \times f_s$ | -0.091 |     | 0.091 | $1/f_s$ |
| Phase deviation        | Frequency range is 0 to $0.1625 \times f_s$ | -0.86  |     | 1.30  | Degrees |

### 6.3.6.7.3.6 Sampling Rate: 176.4 kHz to 192 kHz

図 6-59 shows the magnitude response and 図 6-60 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. 表 6-43 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

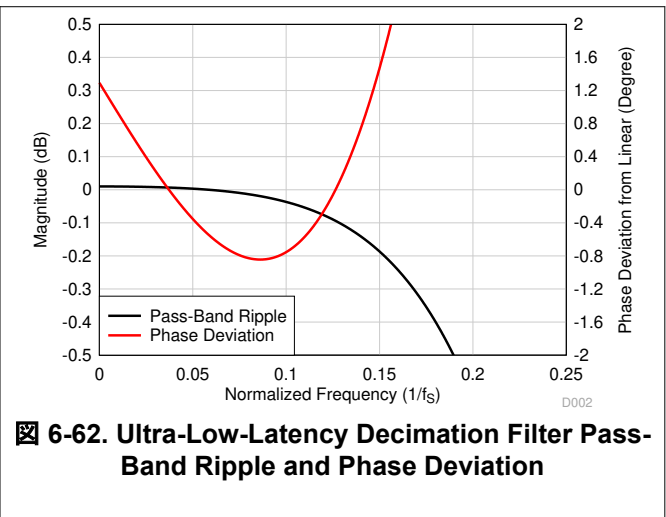
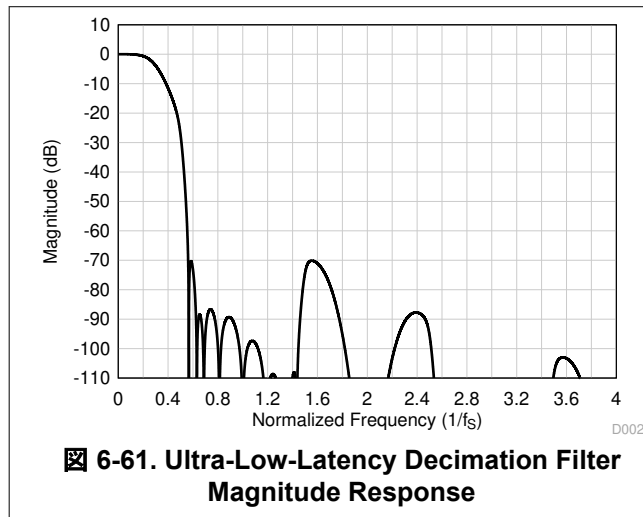


**表 6-43. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                             | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.463 \times f_S$  | -0.03  |     | 0.03  | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ onwards | 85.6   |     |       | dB      |
| Group delay or latency | Frequency range is 0 to $0.085 \times f_S$  |        | 3.7 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.085 \times f_S$  | -0.024 |     | 0.024 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.085 \times f_S$  | -0.12  |     | 0.18  | Degrees |

**6.3.6.7.3.7 Sampling Rate: 352.8 kHz to 384 kHz**

図 6-61 shows the magnitude response and 図 6-62 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. 表 6-44 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

**表 6-44. Ultra-Low-Latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                              | MIN   | TYP | MAX  | UNIT    |
|------------------------|--|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.1 \times f_S$     | -0.04 |     | 0.01 | dB      |
| Stop-band attenuation  | Frequency range is $0.56 \times f_S$ onwards | 70.1  |     |      | dB      |
| Group delay or latency | Frequency range is 0 to $0.157 \times f_S$   |       | 4.1 |      | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.157 \times f_S$   | -0.18 |     | 0.18 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.157 \times f_S$   | -0.85 |     | 2.07 | Degrees |

### 6.3.7 Automatic Gain Controller (AGC)

The device includes an automatic gain controller (AGC) for ADC recording. As shown in 図 6-63, the AGC can be used to maintain a nominally constant output level when recording speech. Instead of manually setting the channel gain in AGC mode, the circuitry automatically adjusts the channel gain when the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters, including target level, maximum gain allowed, attack and release (or decay) time constants, and noise thresholds that allow the algorithm to be fine-tuned for any particular application.

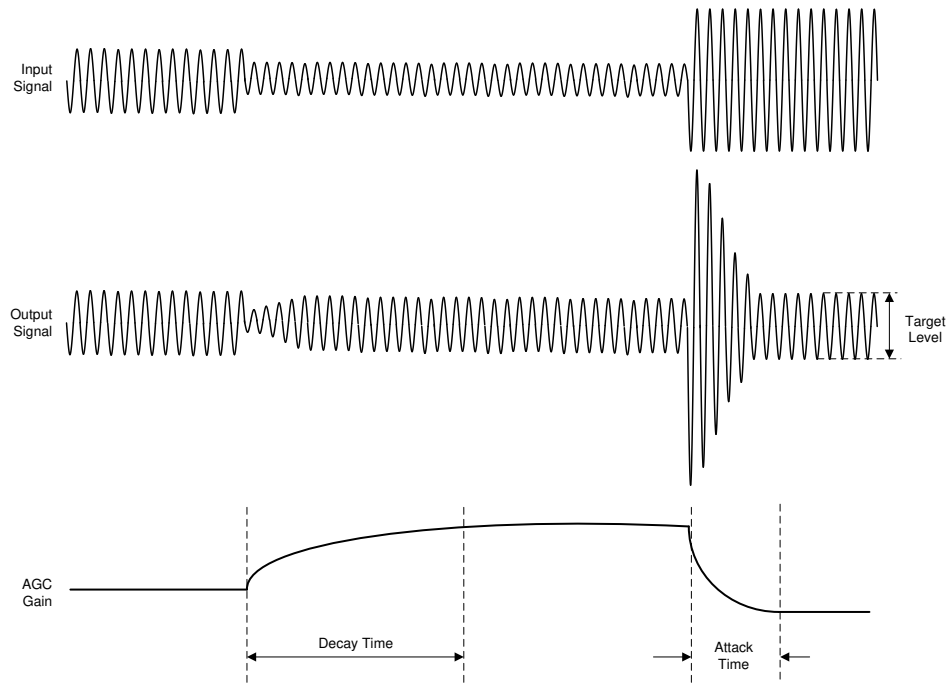


図 6-63. AGC Characteristics

The target level (AGC\_LVL) represents the nominal approximate output level at which the AGC attempts to hold the ADC output signal level. The TAA3020 allows programming of different target levels, which can be programmed from –6 dB to –36 dB relative to a full-scale signal, and the AGC\_LVL default value is set to –34 dB. The target level is recommended to be set with enough margin to prevent clipping when loud sounds occur. 表 6-45 lists the AGC target level configuration settings.

表 6-45. AGC Target Level Programmable Settings

| P0_R112_D[7:4] : AGC_LVL[3:0] | AGC TARGET LEVEL FOR OUTPUT                            |
|-------------------------------|--|
| 0000                          | The AGC target level is the –6-dB output signal level  |
| 0001                          | The AGC target level is the –8-dB output signal level  |
| 0010                          | The AGC target level is the –10-dB output signal level |
| ...                           | ...  |
| 1110 (default)                | The AGC target level is the –34-dB output signal level |
| 1111                          | The AGC target level is the –36-dB output signal level |

The maximum gain allowed (AGC\_MAXGAIN) gives flexibility to the designer to restrict the maximum gain applied by the AGC. This feature limits the channel gain in situations where environmental noise is greater than the programmed noise threshold. The AGC\_MAXGAIN can be programmed from 3 dB to 42 dB with steps of 3 dB and the default value is set to 24 dB. 表 6-46 lists the AGC\_MAXGAIN configuration settings.

**表 6-46. AGC Maximum Gain Programmable Settings**

| P0_R112_D[3:0] :<br>AGC_MAXGAIN[3:0] | AGC MAXIMUM GAIN ALLOWED              |
|--------------------------------------|---------------------------------------|
| 0000                                 | The AGC maximum gain allowed is 3 dB  |
| 0001                                 | The AGC maximum gain allowed is 6 dB  |
| 0010                                 | The AGC maximum gain allowed is 9 dB  |
| ...                                  | ...                                   |
| 0111 (default)                       | The AGC maximum gain allowed is 24 dB |
| ...                                  | ...                                   |
| 1110                                 | The AGC maximum gain allowed is 39 dB |
| 1111                                 | The AGC maximum gain allowed is 42 dB |

For further details on the AGC various configurable parameter and application use, see the [Using the Automatic Gain Controller \(AGC\) in TLV320ADCx120 Family application report](#).

### 6.3.8 Voice Activity Detection (VAD)

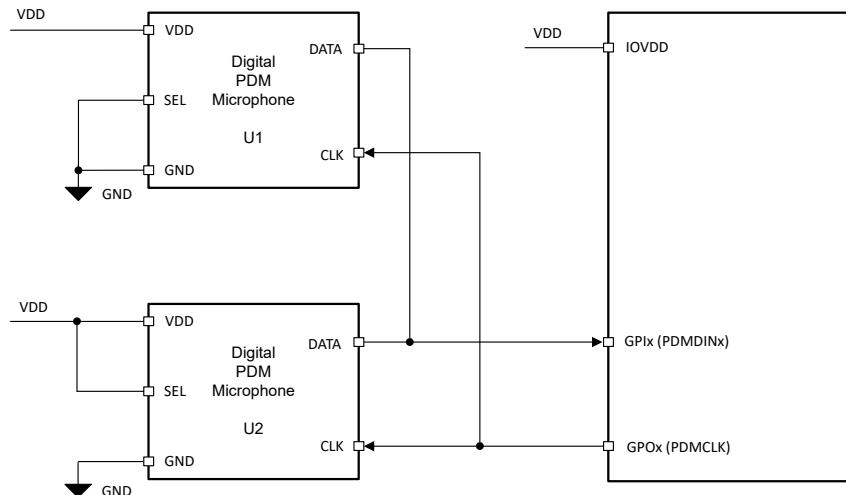
The TAA3020 supports voice activity detection (VAD) mode. In this mode, the TAA3020 continuously monitors one of the input channels for voice detection. The device consumes low quiescent current from the AVDD supply in this mode. This feature can be enabled by setting VAD\_EN (P0\_R117\_D0) to 1'b1. On detecting voice activity, the TAA3020 can alert the host through an interrupt or auto wake up and start recording based on the I<sup>2</sup>C programmed configuration. This alert can be configured through the VAD\_MODE (P1\_R30\_D[7:6]) register bits.

This feature is supported on both the analog and digital microphone interfaces. For lowest power VAD, the digital microphone interface is recommended. The input channel for the VAD can be selected by setting the VAD\_CH\_SEL (P1\_R30\_D[5:4]) register bits to an appropriate value. See the [Using the Voice Activity Detector \(VAD\) in the TLV320ADC5120 and TLV320ADC6120 application report](#) for further details.

### 6.3.9 Digital PDM Microphone Record Channel

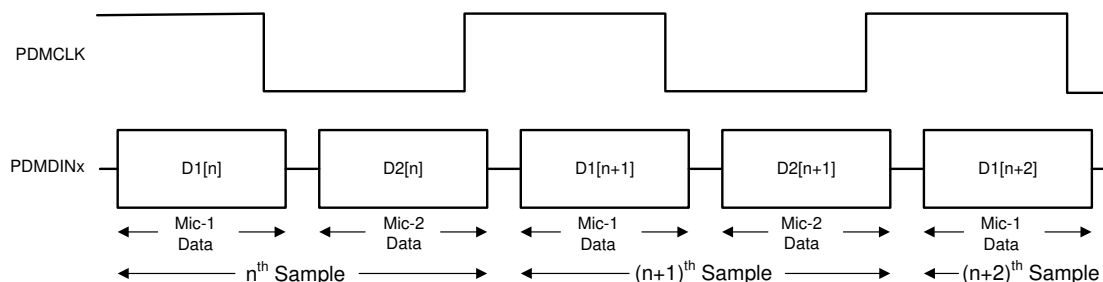
In addition to supporting analog microphones, the device also interfaces to digital pulse-density-modulation (PDM) microphones and uses high-order and high-performance decimation filters to generate pulse code modulation (PCM) output data that can be transmitted on the audio serial interface to the host. The device supports up to four digital microphone recording channels. If the second channel analog microphone is not used in the system, then the analog input pins (IN2P and IN2M) can be repurposed as the GPIO1 and GPO1 pins, respectively, and can be configured for the PDMCLK and PDMCLK clocks for digital PDM microphone recording. GPIO1 or GPIO2 (multiplexed with MICBIAS) can be used as PDMCLK to enable four-channel PDM microphone recording. If two-channel analog input recording is needed, MICBIAS (configured as GPIO2) and GPIO1 can be used as PDMCLK and PDMCLK, respectively, to enable two-channel DMIC recording along with two-channel AIN recording. The device can support a total of four channels at the input (analog and digital).

The device internally generates PDMCLK with a programmable frequency of either 6.144 MHz, 3.072 MHz, 1.536 MHz, or 768 kHz (for output data sample rates in multiples or submultiples of 48 kHz) or 5.6448 MHz, 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (for output data sample rates in multiples or submultiples of 44.1 kHz) using the PDMCLK\_DIV[1:0] (P0\_R31\_D[1:0]) register bits. PDMCLK can be routed on the GPO1 and GPIO1 pins. This clock can be connected to the external digital microphone device. 6-64 shows a connection diagram of the digital PDM microphones.



**6-64. Digital PDM Microphones Connection Diagram for the TAA3020**

The single-bit output of the external digital microphone device can be connected to the GPIx pin. This single data line can be shared by two digital microphones to place their data on the opposite edge of PDMCLK. Internally, the device latches the steady value of the data on either the rising or falling edge of PDMCLK based on the configuration register bits set in P0\_R32\_D[7:4]. 6-65 shows the digital PDM microphone interface timing diagram.



**6-65. Digital PDM Microphone Protocol Timing Diagram**

When the digital microphone is used for recording, the analog blocks of the respective ADC channel are powered down and bypassed for power efficiency. Use the CH1\_INSRC[1:0] (P0\_R60\_D[6:5]) and CH2\_INSRC[1:0] (P0\_R65\_D[6:5]) register bits to select the analog microphone or digital microphone for channel 1 to channel 2. Channel 3 and channel 4 support only the digital microphone interface.

### 6.3.10 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down the record channel as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the record channel. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT\_MASK0[7] (P0\_R51\_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT\_LTCH0 (P0\_R54), which is a read-only register. Reading the latched fault status register, INT\_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIO1 or GPOx pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT\_POL (P0\_R50\_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT\_EVENT[1:0] (P0\_R50\_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV\_STS0 (P0\_R118) and DEV\_STS1 (P0\_R119) register bits.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. Additionally, if the channel is not used for analog input recording, then the analog input pins for that channel (INxP and INxM) can be repurposed as multifunction pins (GPIx and GPOx) by configuring the CHx\_INSRC[1:0] register bits located in the CHx\_CFG0 register. The maximum number of GPO pins supported by the device is four and the maximum number of GPI pins are four. 表 6-47 lists all possible allocations of these multifunctional pins for the various features.

**表 6-47. Multifunction Pin Assignments**

| ROW | PIN FUNCTION <sup>(3)</sup>     | GPIO1            | GPO1        | GPI1              | GPI2        |
|-----|---------------------------------|------------------|-------------|-------------------|-------------|
| —   | —                               | GPIO1_CFG        | GPO1_CFG    | GPI1_CFG          | GPI2_CFG    |
| —   | —                               | P0_R33[7:4]      | P0_R34[7:4] | P0_R43[6:4]       | P0_R43[2:0] |
| A   | Pin disabled                    | S <sup>(1)</sup> | S (default) | S (default)       | S (default) |
| B   | General-purpose output (GPO)    | S                | S           | NS <sup>(2)</sup> | NS          |
| C   | Interrupt output (IRQ)          | S (default)      | S           | NS                | NS          |
| D   | Power down for all ADC channels | S                | NS          | S                 | S           |
| E   | PDM clock output (PDMCLK)       | S                | S           | NS                | NS          |
| F   | MiCBias on/off input (BIASEN)   | S                | NS          | NS                | NS          |
| G   | General-purpose input (GPI)     | S                | NS          | S                 | S           |
| H   | Master clock input (MCLK)       | S                | NS          | S                 | S           |
| I   | ASI daisy-chain input (SDIN)    | S                | NS          | S                 | S           |
| J   | PDM data input 1 (PDM DIN1)     | S                | NS          | S                 | S           |
| K   | PDM data input 2 (PDM DIN2)     | S                | NS          | S                 | S           |

- (1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.  
(2) NS means the feature mentioned in this row is *not supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.  
(3) Only the GPIO1 pin is with reference to the IOVDD supply, the other GPOx and GPIx pins are with reference to the AVDD supply and their primary pin functions are for the PDMCLK or PDM DIN function.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPOx\_DRV[3:0] or GPIO1\_DRV[3:0] register bits. 表 6-48 lists the drive configuration settings.

**表 6-48. GPIO or GPOx Pins Drive Configuration Settings**

| P0_R33_D[3:0] : GPIO1_DRV[3:0] | GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1                           |
|--------------------------------|--|
| 000                            | The GPIO1 pin is set to high impedance (floated)                             |
| 001                            | The GPIO1 pin is set to be driven active low or active high                  |
| 010 (default)                  | The GPIO1 pin is set to be driven active low or weak high (on-chip pullup)   |
| 011                            | The GPIO1 pin is set to be driven active low or Hi-Z (floated)               |
| 100                            | The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high |
| 101                            | The GPIO1 pin is set to be driven Hi-Z (floated) or active high              |
| 110 and 111                    | Reserved (do not use these settings)   |

Similarly, the GPO1 pin can be configured using the GPO1\_DRV(P0\_R34) register bits.

When configured as a general-purpose output (GPO), the GPIO1 or GPOx pin values can be driven by writing the GPIO\_VAL or GPOx\_VAL (P0\_R41) registers. The GPIO\_MON (P0\_R42) register can be used to readback the status of the GPIO1 pin when configured as a general-purpose input (GPI). Similarly, the GPI\_MON (P0\_R47) register can be used to readback the status of the GPIx pins when configured as a general-purpose input (GPI).

## 6.4 Device Functional Modes

### 6.4.1 Sleep Mode or Software Shutdown

In sleep mode or software shutdown mode, the device consumes very low quiescent current from the AVDD supply and, at the same time, allows the I<sup>2</sup>C communication to wake the device for active operation.

The device enters sleep mode when the host device sets the SLEEP\_ENZ (P0\_R2\_D0) bit to 1'b0. If the SLEEP\_ENZ bit is asserted low when the device is in active mode, the device ramps down the volume on the record data, powers down the analog and digital blocks, and enters sleep mode. However, the device still continues to retain the last programmed value of the device configuration registers and programmable coefficients.

In sleep mode, do not perform any I<sup>2</sup>C transactions, except for exiting sleep mode in order to enter active mode. After entering sleep mode, wait at least 10 ms before starting I<sup>2</sup>C transactions to exit sleep mode.

When exiting sleep mode, the host device must configure the TAA3020 to use either an external 1.8-V AREG supply (default setting) or an on-chip-regulator-generated AREG supply. To configure the AREG supply, write to AREG\_SELECT, bit D7 in the same P0\_R2 register.

### 6.4.2 Active Mode

If the host device exits sleep mode by setting the SLEEP\_ENZ bit to 1'b1, the device enters active mode. In active mode, I<sup>2</sup>C transactions can be done to configure and power-up the device for active operation. After entering active mode, wait at least 1 ms before starting any I<sup>2</sup>C transactions in order to allow the device to complete the internal wake-up sequence.

Read and write operations to the programmable coefficient registers in page 2, page 3, and page 4, and to the channel configuration registers (CHx\_CFG[1:4]), and AGC\_CFG0 in page 0 must be done 10 ms after exiting sleep mode.

After configuring all other registers for the target application and system settings, configure the input and output channel enable registers, IN\_CH\_EN (P0\_R115) and ASI\_OUT\_CH\_EN (P0\_R116), respectively. Lastly, configure the device power-up register, PWR\_CFG (P0\_R117). All programmable coefficient values must be written before powering up the respective channel.

In active mode, the power-up and power-down status of various blocks is monitored by reading the read-only device status bits located in the DEV\_STS0 (P0\_R117) and DEV\_STS1 (P0\_R118) registers.

### 6.4.3 Software Reset

A software reset can be done any time by asserting the SW\_RESET (P0\_R1\_D0) register bit, which is a self-clearing bit. This software reset immediately shuts down the device, and restores all device configuration registers and programmable coefficients to their default values.



## 6.5 Programming

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. These registers are called *device control registers* and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3, and page 4. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

### 6.5.1 Control Serial Interfaces

The device control registers can be accessed using I<sup>2</sup>C communication to the device. The device operates with a fixed I<sup>2</sup>C address and can be configured using this address.

#### 6.5.1.1 I<sup>2</sup>C Control Interface

The device supports the I<sup>2</sup>C control protocol as a slave device, and is capable of operating in standard mode, fast mode, and fast mode plus. The I<sup>2</sup>C control protocol requires a 7-bit slave address. The 7-bit slave address is fixed at 1001110 and cannot be changed. If the I2C\_BRDCAST\_EN (P0\_R2\_D2) bit is set to 1'b1, then the I<sup>2</sup>C slave address is fixed to 1001100 in order to allow simultaneous I<sup>2</sup>C broadcast communication to multiple devices in the system, including the TLV320ADCx140, PCMD3140, and PCMD3180 devices. 表 6-49 lists the possible device addresses resulting from this configuration.

**表 6-49. I<sup>2</sup>C Slave Address Settings**

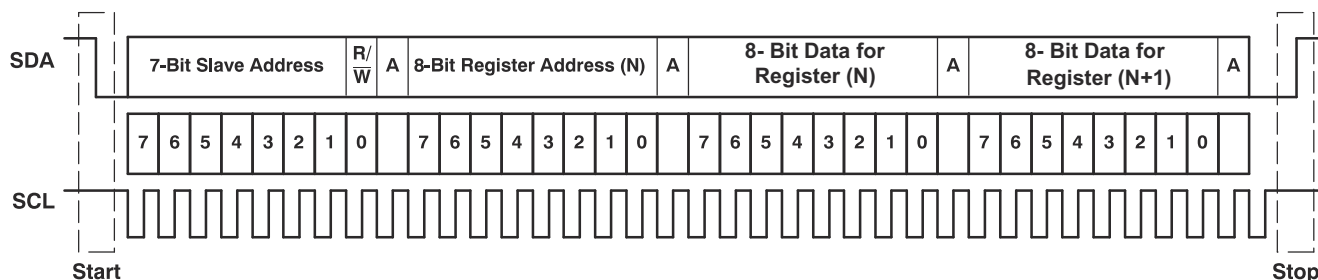
| I2C_BRDCAST_EN (P0_R2_D2) | I <sup>2</sup> C SLAVE ADDRESS |
|---------------------------|--------------------------------|
| 0 (default)               | 1001 110                       |
| 1                         | 1001 100                       |

##### 6.5.1.1.1 General I<sup>2</sup>C Operation

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master device drives a start condition followed by the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The slave device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master device transmits the next byte of the sequence. Each slave device is addressed by a unique 7-bit slave address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master device generates a stop condition to release the bus. [Figure 6-66](#) shows a generic data transfer sequence.



**Figure 6-66. Typical I²C Sequence**

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

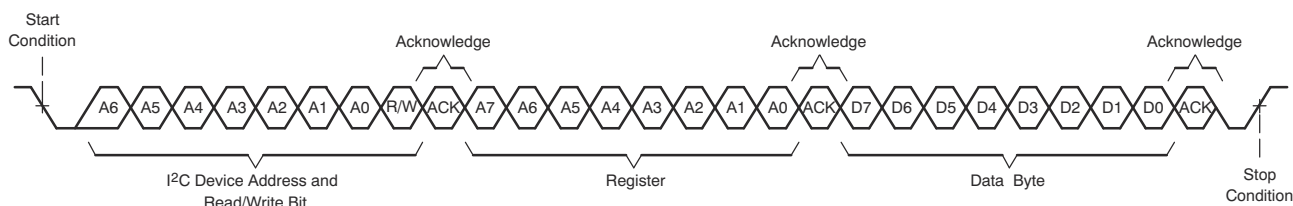
#### 6.5.1.1.1.1 I²C Single-Byte and Multiple-Byte Transfers

The device I²C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The device supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction takes place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

##### 6.5.1.1.1.1.1 I²C Single-Byte Write

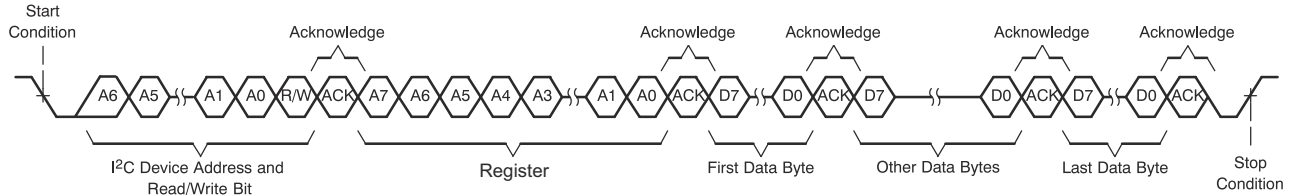
As shown in [Figure 6-67](#), a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C slave address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the master device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the master transmits the byte of data to be written to the specified register. When finished, the slave device responds with an acknowledge bit (ACK). Finally, the master device transmits a stop condition to complete the single-byte data write transfer.



**Figure 6-67. I²C Single-Byte Write Transfer**

#### 6.5.1.1.1.2 I<sup>2</sup>C Multiple-Byte Write

As shown in [Figure 6-68](#), a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the slave device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the master device transmits a stop condition after the last data-byte write transfer.

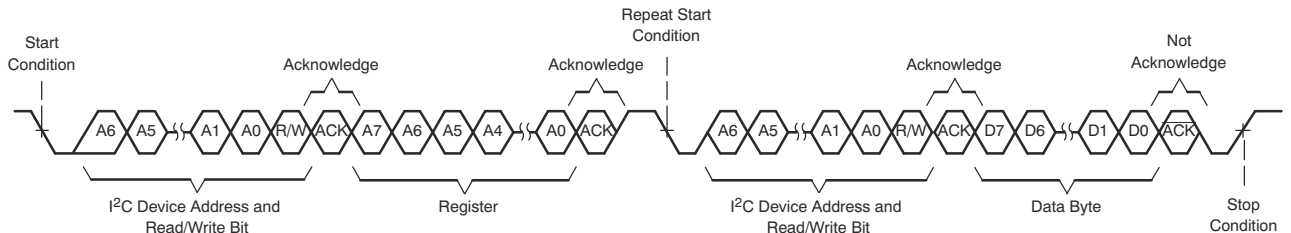


**Figure 6-68. I<sup>2</sup>C Multiple-Byte Write Transfer**

#### 6.5.1.1.1.3 I<sup>2</sup>C Single-Byte Read

As shown in [Figure 6-69](#), a single-byte data read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C slave address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

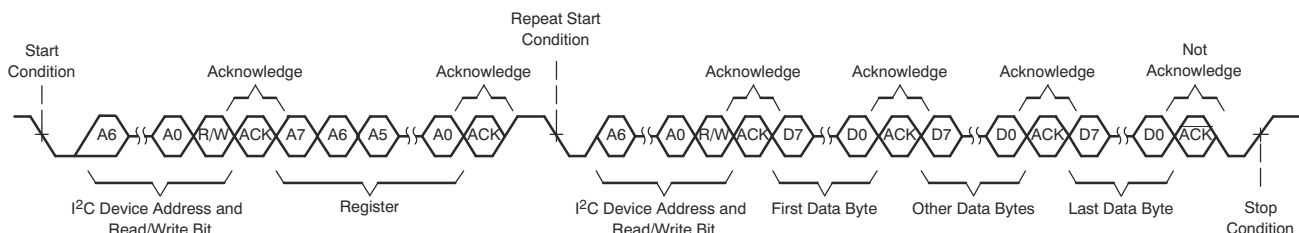
After receiving the slave address and the read/write bit, the device responds with an acknowledge bit (ACK). The master device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The master device transmits another start condition followed by the slave address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the master device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.



**Figure 6-69. I<sup>2</sup>C Single-Byte Read Transfer**

#### 6.5.1.1.1.4 I<sup>2</sup>C Multiple-Byte Read

As shown in [Figure 6-70](#), a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the master device. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the master device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.



**Figure 6-70. I<sup>2</sup>C Multiple-Byte Read Transfer**

## 7 Register Maps

This section describes the control registers for the device in detail. All registers are eight bits in width and are allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using I<sup>2</sup>C communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). All programmable coefficient registers are located in page 2, page 3, and page 4. The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

### 7.1 Device Configuration Registers

This section describes the device configuration registers for page 0 and page 1.

## 7.2 Page\_0 Registers

表 7-1 lists the memory-mapped registers for the Page\_0 registers. All register offset addresses not listed in 表 7-1 should be considered as reserved locations and the register contents should not be modified.

**表 7-1. PAGE\_0 Registers**

| Address | Acronym     | Register Name                               | Reset Value | Section                      |
|---------|-------------|---|-------------|------------------------------|
| 0x0     | PAGE_CFG    | Device page register                        | 0x00        | <a href="#">セクション 7.2.1</a>  |
| 0x1     | SW_RESET    | Software reset register                     | 0x00        | <a href="#">セクション 7.2.2</a>  |
| 0x2     | SLEEP_CFG   | Sleep mode register                         | 0x00        | <a href="#">セクション 7.2.3</a>  |
| 0x5     | SHDN_CFG    | Shutdown configuration register             | 0x05        | <a href="#">セクション 7.2.4</a>  |
| 0x7     | ASI_CFG0    | ASI configuration register 0                | 0x30        | <a href="#">セクション 7.2.5</a>  |
| 0x8     | ASI_CFG1    | ASI configuration register 1                | 0x00        | <a href="#">セクション 7.2.6</a>  |
| 0x9     | ASI_CFG2    | ASI configuration register 2                | 0x00        | <a href="#">セクション 7.2.7</a>  |
| 0xA     | ASI_MIX_CFG | ASI input mixing configuration register     | 0x00        | <a href="#">セクション 7.2.8</a>  |
| 0xB     | ASI_CH1     | Channel 1 ASI slot configuration register   | 0x00        | <a href="#">セクション 7.2.9</a>  |
| 0xC     | ASI_CH2     | Channel 2 ASI slot configuration register   | 0x01        | <a href="#">セクション 7.2.10</a> |
| 0xD     | ASI_CH3     | Channel 3 ASI slot configuration register   | 0x02        | <a href="#">セクション 7.2.11</a> |
| 0xE     | ASI_CH4     | Channel 4 ASI slot configuration register   | 0x03        | <a href="#">セクション 7.2.12</a> |
| 0x13    | MST_CFG0    | ASI master mode configuration register 0    | 0x02        | <a href="#">セクション 7.2.13</a> |
| 0x14    | MST_CFG1    | ASI master mode configuration register 1    | 0x48        | <a href="#">セクション 7.2.14</a> |
| 0x15    | ASI_STS     | ASI bus clock monitor status register       | 0xFF        | <a href="#">セクション 7.2.15</a> |
| 0x16    | CLK_SRC     | Clock source configuration register 0       | 0x10        | <a href="#">セクション 7.2.16</a> |
| 0x1F    | PDMCLK_CFG  | PDM clock generation configuration register | 0x40        | <a href="#">セクション 7.2.17</a> |
| 0x20    | PDMIN_CFG   | PDM DINx sampling edge register             | 0x00        | <a href="#">セクション 7.2.18</a> |
| 0x21    | GPIO_CFG0   | GPIO configuration register 0               | 0x22        | <a href="#">セクション 7.2.19</a> |
| 0x22    | GPO_CFG0    | GPO configuration register 0                | 0x00        | <a href="#">セクション 7.2.20</a> |
| 0x29    | GPO_VAL     | GPIO, GPO output value register             | 0x00        | <a href="#">セクション 7.2.21</a> |
| 0x2A    | GPIO_MON    | GPIO monitor value register                 | 0x00        | <a href="#">セクション 7.2.22</a> |
| 0x2B    | GPI_CFG0    | GPI configuration register 0                | 0x00        | <a href="#">セクション 7.2.23</a> |
| 0x2F    | GPI_MON     | GPI monitor value register                  | 0x00        | <a href="#">セクション 7.2.24</a> |
| 0x32    | INT_CFG     | Interrupt configuration register            | 0x00        | <a href="#">セクション 7.2.25</a> |
| 0x33    | INT_MASK0   | Interrupt mask register 0                   | 0xFF        | <a href="#">セクション 7.2.26</a> |
| 0x36    | INT_LTCH0   | Latched interrupt readback register 0       | 0x00        | <a href="#">セクション 7.2.27</a> |
| 0x3A    | CM_TOL_CFG  | ADC common mode configuration register      | 0x00        | <a href="#">セクション 7.2.28</a> |
| 0x3B    | BIAS_CFG    | Bias and ADC configuration register         | 0x00        | <a href="#">セクション 7.2.29</a> |
| 0x3C    | CH1_CFG0    | Channel 1 configuration register 0          | 0x00        | <a href="#">セクション 7.2.30</a> |
| 0x3D    | CH1_CFG1    | Channel 1 configuration register 1          | 0x00        | <a href="#">セクション 7.2.31</a> |
| 0x3E    | CH1_CFG2    | Channel 1 configuration register 2          | 0xC9        | <a href="#">セクション 7.2.32</a> |
| 0x3F    | CH1_CFG3    | Channel 1 configuration register 3          | 0x80        | <a href="#">セクション 7.2.33</a> |
| 0x40    | CH1_CFG4    | Channel 1 configuration register 4          | 0x00        | <a href="#">セクション 7.2.34</a> |
| 0x41    | CH2_CFG0    | Channel 2 configuration register 0          | 0x00        | <a href="#">セクション 7.2.35</a> |
| 0x42    | CH2_CFG1    | Channel 2 configuration register 1          | 0x00        | <a href="#">セクション 7.2.36</a> |
| 0x43    | CH2_CFG2    | Channel 2 configuration register 2          | 0xC9        | <a href="#">セクション 7.2.37</a> |
| 0x44    | CH2_CFG3    | Channel 2 configuration register 3          | 0x80        | <a href="#">セクション 7.2.38</a> |
| 0x45    | CH2_CFG4    | Channel 2 configuration register 4          | 0x00        | <a href="#">セクション 7.2.39</a> |

表 7-1. PAGE\_0 Registers (続き)

| Address | Acronym       | Register Name                                    | Reset Value | Section                      |
|---------|---------------|--|-------------|------------------------------|
| 0x48    | CH3_CFG2      | Channel 3 configuration register 2               | 0xC9        | <a href="#">セクション 7.2.40</a> |
| 0x49    | CH3_CFG3      | Channel 3 configuration register 3               | 0x80        | <a href="#">セクション 7.2.41</a> |
| 0x4A    | CH3_CFG4      | Channel 3 configuration register 4               | 0x00        | <a href="#">セクション 7.2.42</a> |
| 0x4D    | CH4_CFG2      | Channel 4 configuration register 2               | 0xC9        | <a href="#">セクション 7.2.43</a> |
| 0x4E    | CH4_CFG3      | Channel 4 configuration register 3               | 0x80        | <a href="#">セクション 7.2.44</a> |
| 0x4F    | CH4_CFG4      | Channel 4 configuration register 4               | 0x00        | <a href="#">セクション 7.2.45</a> |
| 0x6B    | DSP_CFG0      | DSP configuration register 0                     | 0x01        | <a href="#">セクション 7.2.46</a> |
| 0x6C    | DSP_CFG1      | DSP configuration register 1                     | 0x40        | <a href="#">セクション 7.2.47</a> |
| 0x70    | AGC_CFG0      | AGC configuration register 0                     | 0xE7        | <a href="#">セクション 7.2.48</a> |
| 0x71    | GAIN_CFG      | Gain change Configuration                        | 0x00        | <a href="#">セクション 7.2.49</a> |
| 0x73    | IN_CH_EN      | Input channel enable configuration register      | 0xC0        | <a href="#">セクション 7.2.50</a> |
| 0x74    | ASI_OUT_CH_EN | ASI output channel enable configuration register | 0x00        | <a href="#">セクション 7.2.51</a> |
| 0x75    | PWR_CFG       | Power up configuration register                  | 0x00        | <a href="#">セクション 7.2.52</a> |
| 0x76    | DEV_STS0      | Device status value register 0                   | 0x00        | <a href="#">セクション 7.2.53</a> |
| 0x77    | DEV_STS1      | Device status value register 1                   | 0x80        | <a href="#">セクション 7.2.54</a> |
| 0x7E    | I2C_CKSUM     | I <sup>2</sup> C checksum register               | 0x00        | <a href="#">セクション 7.2.55</a> |

### 7.2.1 PAGE\_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE\_CFG is shown in [表 7-2](#).

Return to the [Summary Table](#).

The device memory map is divided into pages. This register sets the page.

表 7-2. PAGE\_CFG Register Field Descriptions

| Bit | Field     | Type | Reset     | Description  |
|-----|-----------|------|-----------|--|
| 7-0 | PAGE[7:0] | R/W  | 00000000b | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>2d to 254d = Page 2 to page 254 respectively<br>255d = Page 255 |

### 7.2.2 SW\_RESET Register (Address = 0x1) [Reset = 0x00]

SW\_RESET is shown in [表 7-3](#).

Return to the [Summary Table](#).

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

表 7-3. SW\_RESET Register Field Descriptions

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7-1 | RESERVED | R    | 0b    | Reserved bits; Write only reset value   |
| 0   | SW_RESET | R/W  | 0b    | Software reset. This bit is self clearing.<br>0d = Do not reset<br>1d = Reset all registers to their reset values |

### 7.2.3 SLEEP\_CFG Register (Address = 0x2) [Reset = 0x00]

SLEEP\_CFG is shown in 表 7-4.

Return to the [Summary Table](#).

This register configures the regulator, VREF quick charge, I<sup>2</sup>C broadcast and sleep mode.

**表 7-4. SLEEP\_CFG Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7   | AREG_SELECT    | R/W  | 0b    | The analog supply selection from either the internal regulator supply or the external AREG supply.<br>0d = External 1.8-V AREG supply (use this setting when AVDD is 1.8 V and short AREG with AVDD)<br>1d = Internally generated 1.8-V AREG supply using an on-chip regulator (use this setting when AVDD is 3.3 V)                           |
| 6-5 | RESERVED       | R    | 0b    | Reserved bits; Write only reset values   |
| 4-3 | VREF_QCHG[1:0] | R/W  | 00b   | The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω.<br>0d = VREF quick-charge duration of 3.5 ms (typical)<br>1d = VREF quick-charge duration of 10 ms (typical)<br>2d = VREF quick-charge duration of 50 ms (typical)<br>3d = VREF quick-charge duration of 100 ms (typical) |
| 2   | I2C_BRDCAST_EN | R/W  | 0b    | I <sup>2</sup> C broadcast addressing setting.<br>0d = I <sup>2</sup> C broadcast mode disabled<br>1d = I <sup>2</sup> C broadcast mode enabled; the I <sup>2</sup> C target address is fixed at 1001 100  |
| 1   | RESERVED       | R    | 0b    | Reserved bit; Write only reset value   |
| 0   | SLEEP_ENZ      | R/W  | 0b    | Sleep mode setting.<br>0d = Device is in sleep mode<br>1d = Device is not in sleep mode  |

### 7.2.4 SHDN\_CFG Register (Address = 0x5) [Reset = 0x05]

SHDN\_CFG is shown in 表 7-5.

Return to the [Summary Table](#).

This register configures the device shutdown

**表 7-5. SHDN\_CFG Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7-6 | RESERVED        | R    | 0b    | Reserved bits; Write only reset value  |
| 5-4 | INCAP_QCHG[1:0] | R/W  | 00b   | The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω.<br>0d = INxP, INxM quick-charge duration of 2.5 ms (typical)<br>1d = INxP, INxM quick-charge duration of 12.5 ms (typical)<br>2d = INxP, INxM quick-charge duration of 25 ms (typical)<br>3d = INxP, INxM quick-charge duration of 50 ms (typical) |
| 3-2 | RESERVED        | R    | 0b    | Reserved bits; Write only reset values   |
| 1-0 | RESERVED        | R    | 0b    | Reserved bits; Write only reset values   |

### 7.2.5 ASI\_CFG0 Register (Address = 0x7) [Reset = 0x30]

ASI\_CFG0 is shown in 表 7-6.

Return to the [Summary Table](#).

This register is the ASI configuration register 0.

**表 7-6. ASI\_CFG0 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7-6 | ASI_FORMAT[1:0] | R/W  | 00b   | ASI protocol format.<br>0d = TDM mode<br>1d = I <sup>2</sup> S mode<br>2d = LJ (left-justified) mode<br>3d = Reserved; Don't use  |
| 5-4 | ASI_WLEN[1:0]   | R/W  | 11b   | ASI word or slot length.<br>0d = 16 bits (Recommended this setting to be used with 10-kΩ or 20-kΩ input impedance configuration)<br>1d = 20 bits<br>2d = 24 bits<br>3d = 32 bits  |
| 3   | FSYNC_POL       | R/W  | 0b    | ASI FSYNC polarity.<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol   |
| 2   | BCLK_POL        | R/W  | 0b    | ASI BCLK polarity.<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol  |
| 1   | TX_EDGE         | R/W  | 0b    | ASI data output (on the primary and secondary data pin) transmit edge.<br>0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL)<br>1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 0   | TX_FILL         | R/W  | 0b    | ASI data output (on the primary and secondary data pin) for any unused cycles<br>0d = Always transmit 0 for unused cycles<br>1d = Always use Hi-Z for unused cycles   |

**7.2.6 ASI\_CFG1 Register (Address = 0x8) [Reset = 0x00]**

ASI\_CFG1 is shown in [表 7-7](#).

Return to the [Summary Table](#).

This register is the ASI configuration register 1.

**表 7-7. ASI\_CFG1 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7   | TX_LSB         | R/W  | 0b    | ASI data output (on the primary and secondary data pin) for LSB transmissions.<br>0d = Transmit the LSB for a full cycle<br>1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle  |
| 6-5 | TX_KEEPER[1:0] | R/W  | 00b   | ASI data output (on the primary and secondary data pin) bus keeper.<br>0d = Bus keeper is always disabled<br>1d = Bus keeper is always enabled<br>2d = Bus keeper is enabled during LSB transmissions only for one cycle<br>3d = Bus keeper is enabled during LSB transmissions only for one and half cycles |



**表 7-7. ASI\_CFG1 Register Field Descriptions (続き)**

| Bit | Field          | Type | Reset  | Description  |
|-----|----------------|------|--------|--|
| 4-0 | TX_OFFSET[4:0] | R/W  | 00000b | ASI data MSB slot 0 offset (on the primary and secondary data pin).<br>0d = ASI data MSB location has no offset and is as per standard protocol<br>1d = ASI data MSB location (TDM mode is slot 0 or I <sup>2</sup> S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol<br>2d = ASI data MSB location (TDM mode is slot 0 or I <sup>2</sup> S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol<br>3d to 30d = ASI data MSB location (TDM mode is slot 0 or I <sup>2</sup> S, LJ mode is the left and right slot 0) offset assigned as per configuration<br>31d = ASI data MSB location (TDM mode is slot 0 or I <sup>2</sup> S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

### 7.2.7 ASI\_CFG2 Register (Address = 0x9) [Reset = 0x00]

ASI\_CFG2 is shown in 表 7-8.

Return to the [Summary Table](#).

This register is the ASI configuration register 2.

**表 7-8. ASI\_CFG2 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7   | ASI_DAISSY   | R/W  | 0b    | ASI daisy chain connection.<br>0d = All devices are connected in the common ASI bus<br>1d = All devices are daisy-chained for the ASI bus. This is supported only if ASI input mixing is disabled, refer register 10 for details on ASI input mixing feature. |
| 6   | RESERVED     | R    | 0b    | Reserved bit; Write only reset value  |
| 5   | ASI_ERR      | R/W  | 0b    | ASI bus error detection.<br>0d = Enable bus error detection<br>1d = Disable bus error detection   |
| 4   | ASI_ERR_RCOV | R/W  | 0b    | ASI bus error auto resume.<br>0d = Enable auto resume after bus error recovery<br>1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device  |
| 3   | RESERVED     | R    | 0b    | Reserved bit; Write only reset value  |
| 2-0 | RESERVED     | R    | 0b    | Reserved bits; Write only reset value   |

### 7.2.8 ASI\_MIX\_CFG Register (Address = 0xA) [Reset = 0x00]

ASI\_MIX\_CFG is shown in 表 7-9.

Return to the [Summary Table](#).

This register is the ASI input mixing configuration register.

表 7-9. ASI\_MIX\_CFG Register Field Descriptions

| Bit | Field             | Type | Reset | Description   |
|-----|-------------------|------|-------|---|
| 7-6 | ASI_MIX_SEL[1:0]  | R/W  | 00b   | ASI input (from GPIx or GPIO) mixing selection with channel data.<br>0d = No mixing<br>1d = Channel 1 and channel 2 output data mixed with ASI input data on channel 1 (slot 0)<br>2d = Channel 1 and channel 2 output data mixed with ASI input data on channel 2 (slot 1)<br>3d = Mixed both channel data with ASI input data independently.<br>Mixed asi_in_ch_1 with channel 1 output data and similarly mix asi_in_ch_2 with channel 2 output data |
| 5-4 | ASI_GAIN_SEL[1:0] | R/W  | 00b   | ASI input data gain selection before mixing to channel data.<br>0d = No gain<br>1d = Gain asi input data by -6dB<br>2d = Gain asi input data by -12dB<br>3d = Gain asi input data by -18dB  |
| 3   | ASI_IN_INVERSE    | R/W  | 0b    | Invert ASI input data before mixing to channel data.<br>0d = No inversion done for ASI input data<br>1d = ASI input data inverted before mixing with channel data   |
| 2   | RESERVED          | R    | 0b    | Reserved bit; Write only reset value  |
| 1   | RESERVED          | R    | 0b    | Reserved bit; Write only reset value  |
| 0   | RESERVED          | R    | 0b    | Reserved bit; Write only reset value  |

### 7.2.9 ASI\_CH1 Register (Address = 0xB) [Reset = 0x00]

ASI\_CH1 is shown in 表 7-10.

Return to the [Summary Table](#).

This register is the ASI slot configuration register for channel 1.

表 7-10. ASI\_CH1 Register Field Descriptions

| Bit | Field         | Type | Reset   | Description  |
|-----|---------------|------|---------|--|
| 7-6 | RESERVED      | R    | 0b      | Reserved bits; Write only reset value  |
| 5-0 | CH1_SLOT[5:0] | R/W  | 000000b | Channel 1 slot assignment.<br>0d = TDM is slot 0 or I <sup>2</sup> S, LJ is left slot 0<br>1d = TDM is slot 1 or I <sup>2</sup> S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I <sup>2</sup> S, LJ is left slot 31<br>32d = TDM is slot 32 or I <sup>2</sup> S, LJ is right slot 0<br>33d = TDM is slot 33 or I <sup>2</sup> S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I <sup>2</sup> S, LJ is right slot 31 |

### 7.2.10 ASI\_CH2 Register (Address = 0xC) [Reset = 0x01]

ASI\_CH2 is shown in 表 7-11.

Return to the [Summary Table](#).

This register is the ASI slot configuration register for channel 2.

表 7-11. ASI\_CH2 Register Field Descriptions

| Bit | Field    | Type | Reset | Description                           |
|-----|----------|------|-------|---------------------------------------|
| 7-6 | RESERVED | R    | 0b    | Reserved bits; Write only reset value |

**表 7-11. ASI\_CH2 Register Field Descriptions (続き)**

| Bit | Field         | Type | Reset   | Description  |
|-----|---------------|------|---------|--|
| 5-0 | CH2_SLOT[5:0] | R/W  | 000001b | Channel 2 slot assignment.<br>0d = TDM is slot 0 or I <sup>2</sup> S, LJ is left slot 0<br>1d = TDM is slot 1 or I <sup>2</sup> S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I <sup>2</sup> S, LJ is left slot 31<br>32d = TDM is slot 32 or I <sup>2</sup> S, LJ is right slot 0<br>33d = TDM is slot 33 or I <sup>2</sup> S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I <sup>2</sup> S, LJ is right slot 31 |

### 7.2.11 ASI\_CH3 Register (Address = 0xD) [Reset = 0x02]

ASI\_CH3 is shown in 表 7-12.

Return to the [Summary Table](#).

This register is the ASI slot configuration register for channel 3.

**表 7-12. ASI\_CH3 Register Field Descriptions**

| Bit | Field         | Type | Reset   | Description  |
|-----|---------------|------|---------|--|
| 7-6 | RESERVED      | R    | 0b      | Reserved bits; Write only reset value  |
| 5-0 | CH3_SLOT[5:0] | R/W  | 000010b | Channel 3 slot assignment.<br>0d = TDM is slot 0 or I <sup>2</sup> S, LJ is left slot 0<br>1d = TDM is slot 1 or I <sup>2</sup> S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I <sup>2</sup> S, LJ is left slot 31<br>32d = TDM is slot 32 or I <sup>2</sup> S, LJ is right slot 0<br>33d = TDM is slot 33 or I <sup>2</sup> S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I <sup>2</sup> S, LJ is right slot 31 |

### 7.2.12 ASI\_CH4 Register (Address = 0xE) [Reset = 0x03]

ASI\_CH4 is shown in 表 7-13.

Return to the [Summary Table](#).

This register is the ASI slot configuration register for channel 4.

**表 7-13. ASI\_CH4 Register Field Descriptions**

| Bit | Field         | Type | Reset   | Description  |
|-----|---------------|------|---------|--|
| 7-6 | RESERVED      | R    | 0b      | Reserved bits; Write only reset value  |
| 5-0 | CH4_SLOT[5:0] | R/W  | 000011b | Channel 4 slot assignment.<br>0d = TDM is slot 0 or I <sup>2</sup> S, LJ is left slot 0<br>1d = TDM is slot 1 or I <sup>2</sup> S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I <sup>2</sup> S, LJ is left slot 31<br>32d = TDM is slot 32 or I <sup>2</sup> S, LJ is right slot 0<br>33d = TDM is slot 33 or I <sup>2</sup> S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I <sup>2</sup> S, LJ is right slot 31 |

### 7.2.13 MST\_CFG0 Register (Address = 0x13) [Reset = 0x02]

MST\_CFG0 is shown in 表 7-14.

Return to the [Summary Table](#).

This register is the ASI master mode configuration register 0.

**表 7-14. MST\_CFG0 Register Field Descriptions**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7   | MST_SLV_CFG        | R/W  | 0b    | ASI master or slave configuration register setting.<br>0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device)<br>1d = Device is in master mode (both BCLK and FSYNC are generated from the device)   |
| 6   | AUTO_CLK_CFG       | R/W  | 0b    | Automatic clock configuration setting.<br>0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived)<br>1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings)          |
| 5   | AUTO_MODE_PLL_DIS  | R/W  | 0b    | Automatic mode PLL setting.<br>0d = PLL is enabled in auto clock configuration<br>1d = PLL is disabled in auto clock configuration  |
| 4   | BCLK_FSYNC_GATE    | R/W  | 0b    | BCLK and FSYNC clock gate (valid when the device is in master mode).<br>0d = Do not gate BCLK and FSYNC<br>1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode   |
| 3   | FS_MODE            | R/W  | 0b    | Sample rate setting (valid when the device is in master mode).<br>0d = $f_s$ is a multiple (or submultiple) of 48 kHz<br>1d = $f_s$ is a multiple (or submultiple) of 44.1 kHz  |
| 2-0 | MCLK_FREQ_SEL[2:0] | R/W  | 010b  | These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0).<br>0d = 12 MHz<br>1d = 12.288 MHz<br>2d = 13 MHz<br>3d = 16 MHz<br>4d = 19.2 MHz<br>5d = 19.68 MHz<br>6d = 24 MHz<br>7d = 24.576 MHz |

#### 7.2.14 MST\_CFG1 Register (Address = 0x14) [Reset = 0x48]

MST\_CFG1 is shown in [表 7-15](#).

Return to the [Summary Table](#).

This register is the ASI master mode configuration register 1.

**表 7-15. MST\_CFG1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-4 | FS_RATE[3:0] | R/W  | 0100b | Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration).<br>0d = 7.35 kHz or 8 kHz<br>1d = 14.7 kHz or 16 kHz<br>2d = 22.05 kHz or 24 kHz<br>3d = 29.4 kHz or 32 kHz<br>4d = 44.1 kHz or 48 kHz<br>5d = 88.2 kHz or 96 kHz<br>6d = 176.4 kHz or 192 kHz<br>7d = 352.8 kHz or 384 kHz<br>8d = 705.6 kHz or 768 kHz<br>9d to 15d = Reserved; Don't use |

**表 7-15. MST\_CFG1 Register Field Descriptions (続き)**

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 3-0 | FS_BCLK_RATIO[3:0] | R/W  | 1000b | Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration).<br>0d = Ratio of 16<br>1d = Ratio of 24<br>2d = Ratio of 32<br>3d = Ratio of 48<br>4d = Ratio of 64<br>5d = Ratio of 96<br>6d = Ratio of 128<br>7d = Ratio of 192<br>8d = Ratio of 256<br>9d = Ratio of 384<br>10d = Ratio of 512<br>11d = Ratio of 1024<br>12d = Ratio of 2048<br>13d to 15d = Reserved; Don't use |

### 7.2.15 ASI\_STS Register (Address = 0x15) [Reset = 0xFF]

ASI\_STS is shown in [表 7-16](#).

Return to the [Summary Table](#).

This register is the ASI bus clock monitor status register

**表 7-16. ASI\_STS Register Field Descriptions**

| Bit | Field             | Type | Reset | Description   |
|-----|-------------------|------|-------|---|
| 7-4 | FS_RATE_STS[3:0]  | R    | 1111b | Detected sample rate of the ASI bus.<br>0d = 7.35 kHz or 8 kHz<br>1d = 14.7 kHz or 16 kHz<br>2d = 22.05 kHz or 24 kHz<br>3d = 29.4 kHz or 32 kHz<br>4d = 44.1 kHz or 48 kHz<br>5d = 88.2 kHz or 96 kHz<br>6d = 176.4 kHz or 192 kHz<br>7d = 352.8 kHz or 384 kHz<br>8d = 705.6 kHz or 768 kHz<br>9d to 14d = Reserved status<br>15d = Invalid sample rate                                     |
| 3-0 | FS_RATIO_STS[3:0] | R    | 1111b | Detected BCLK to FSYNC frequency ratio of the ASI bus.<br>0d = Ratio of 16<br>1d = Ratio of 24<br>2d = Ratio of 32<br>3d = Ratio of 48<br>4d = Ratio of 64<br>5d = Ratio of 96<br>6d = Ratio of 128<br>7d = Ratio of 192<br>8d = Ratio of 256<br>9d = Ratio of 384<br>10d = Ratio of 512<br>11d = Ratio of 1024<br>12d = Ratio of 2048<br>13d to 14d = Reserved status<br>15d = Invalid ratio |

### 7.2.16 CLK\_SRC Register (Address = 0x16) [Reset = 0x10]

CLK\_SRC is shown in 表 7-17.

Return to the [Summary Table](#).

This register is the clock source configuration register.

**表 7-17. CLK\_SRC Register Field Descriptions**

| Bit | Field               | Type | Reset | Description   |
|-----|---------------------|------|-------|---|
| 7   | DIS_PLL_SLV_CLK_SRC | R/W  | 0b    | Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1).<br>0d = BCLK is used as the audio root clock source<br>1d = MCLK (GPIO or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting) |
| 6   | MCLK_FREQ_SEL_MODE  | R/W  | 0b    | Master mode MCLK (GPIO or GPIx) frequency selection mode (valid when the device is in auto clock configuration).<br>0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R19) configuration<br>1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R22) configuration  |
| 5-3 | MCLK_RATIO_SEL[2:0] | R/W  | 010b  | These bits select the MCLK (GPIO or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode.<br>0d = Ratio of 64<br>1d = Ratio of 256<br>2d = Ratio of 384<br>3d = Ratio of 512<br>4d = Ratio of 768<br>5d = Ratio of 1024<br>6d = Ratio of 1536<br>7d = Ratio of 2304                         |
| 2   | RESERVED            | R    | 0b    | Reserved bit; Write only reset value  |
| 1   | INV_BCLK_FOR_FSYNC  | R/W  | 0b    | Invert BCLK polarity only for FSYNC generation in master mode configuration.<br>0d = Do not invert BCLK polarity for FSYNC generation<br>1d = Invert BCLK polarity for FSYNC generation   |
| 0   | RESERVED            | R    | 0b    | Reserved bit; Write only reset value  |

### 7.2.17 PDMCLK\_CFG Register (Address = 0x1F) [Reset = 0x40]

PDMCLK\_CFG is shown in 表 7-18.

Return to the [Summary Table](#).

This register is the PDM clock generation configuration register.

**表 7-18. PDMCLK\_CFG Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | RESERVED        | R    | 0b    | Reserved bit; Write only reset value   |
| 6-2 | RESERVED        | R    | 0b    | Reserved bits; Write only reset values   |
| 1-0 | PDMCLK_DIV[1:0] | R/W  | 00b   | PDMCLK divider value.<br>0d = PDMCLK is 2.8224 MHz or 3.072 MHz<br>1d = PDMCLK is 1.4112 MHz or 1.536 MHz<br>2d = PDMCLK is 705.6 kHz or 768 kHz<br>3d = PDMCLK is 5.6448 MHz or 6.144 MHz (applicable only for PDM channel 1 and 2) |

### 7.2.18 PDMIN\_CFG Register (Address = 0x20) [Reset = 0x00]

PDMIN\_CFG is shown in [表 7-19](#).

Return to the [Summary Table](#).

This register is the PDM DINx sampling edge configuration register.

**表 7-19. PDMIN\_CFG Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7   | PDMDIN1_EDGE | R/W  | 0b    | PDMCLK latching edge used for channel 1 and channel 2 data.<br>0d = Channel 1 data are latched on the negative edge, channel 2 data are latched on the positive edge<br>1d = Channel 1 data are latched on the positive edge, channel 2 data are latched on the negative edge |
| 6   | RESERVED     | R    | 0b    | Reserved bit; Write only reset value  |
| 5-0 | RESERVED     | R    | 0b    | Reserved bits; Write only reset value   |

### 7.2.19 GPIO\_CFG0 Register (Address = 0x21) [Reset = 0x22]

GPIO\_CFG0 is shown in [表 7-20](#).

Return to the [Summary Table](#).

This register is the GPIO configuration register 0.

**表 7-20. GPIO\_CFG0 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7-4 | GPIO1_CFG[3:0] | R/W  | 0010b | GPIO1 configuration.<br>0d = GPIO1 is disabled<br>1d = GPIO1 is configured as a general-purpose output (GPO)<br>2d = GPIO1 is configured as a device interrupt output (IRQ)<br>3d = Reserved; Don't use<br>4d = GPIO1 is configured as a PDM clock output (PDMCLK)<br>5d = Reserved; Don't use<br>6d = Reserved; Don't use<br>7d = PD all ADC channels<br>8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPIO1 is configured as a general-purpose input (GPI)<br>10d = GPIO1 is configured as a master clock input (MCLK)<br>11d = GPIO1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN)<br>12d = GPIO1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1)<br>13d = GPIO1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2)<br>14d to 15d = Reserved; Don't use |
| 3   | RESERVED       | R    | 0b    | Reserved bit; Write only reset value   |
| 2-0 | GPIO1_DRV[2:0] | R/W  | 010b  | GPIO1 output drive configuration.<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use  |

### 7.2.20 GPO\_CFG0 Register (Address = 0x22) [Reset = 0x00]

GPO\_CFG0 is shown in [表 7-21](#).

Return to the [Summary Table](#).

This register is the GPO configuration register 0.

**表 7-21. GPO\_CFG0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-4 | GPO1_CFG[3:0] | R/W  | 0000b | IN2M_GPO1 (GPO1) configuration.<br>0d = GPO1 is disabled<br>1d = GPO1 is configured as a general-purpose output (GPO)<br>2d = GPO1 is configured as a device interrupt output (IRQ)<br>3d = Reserved; Don't use<br>4d = GPO1 is configured as a PDM clock output (PDMCLK)<br>5d to 15d = Reserved; Don't use |
| 3   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 2-0 | GPO1_DRV[2:0] | R/W  | 000b  | IN2M_GPO1 (GPO1) output drive configuration.<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Reserved; Don't use<br>3d = Drive active low and Hi-Z<br>4d = Reserved; Don't use<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use                                     |

#### 7.2.21 GPO\_VAL Register (Address = 0x29) [Reset = 0x00]

GPO\_VAL is shown in [表 7-22](#).

Return to the [Summary Table](#).

This register is the GPIO and GPO output value register.

**表 7-22. GPO\_VAL Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7   | GPIO1_VAL | R/W  | 0b    | GPIO1 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 |
| 6   | GPO1_VAL  | R/W  | 0b    | GPO1 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1  |
| 5-0 | RESERVED  | R    | 0b    | Reserved bits; Write only reset value  |

#### 7.2.22 GPIO\_MON Register (Address = 0x2A) [Reset = 0x00]

GPIO\_MON is shown in [表 7-23](#).

Return to the [Summary Table](#).

This register is the GPIO monitor value register.

**表 7-23. GPIO\_MON Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7   | GPIO1_MON | R    | 0b    | GPIO1 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 |
| 6-0 | RESERVED  | R    | 0b    | Reserved bits; Write only reset value   |



### 7.2.23 GPI\_CFG0 Register (Address = 0x2B) [Reset = 0x00]

GPI\_CFG0 is shown in 表 7-24.

Return to the [Summary Table](#).

This register is the GPI configuration register 0.

**表 7-24. GPI\_CFG0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 6-4 | GPI1_CFG[2:0] | R/W  | 000b  | IN2P_GPI1 (GPI1) configuration.<br>0d = GPI1 is disabled<br>1d = GPI1 is configured as a general-purpose input (GPI)<br>2d = GPI1 is configured as a master clock input (MCLK)<br>3d = GPI1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN)<br>4d = GPI1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1)<br>5d = GPI1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2)<br>6d = Reserved; Don't use<br>7d = PD all ADC channels |
| 3   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 2-0 | GPI2_CFG[2:0] | R/W  | 000b  | MICBIAS as GPI2 configuration.<br>0d = GPI2 is disabled<br>1d = GPI2 is configured as a general-purpose input (GPI)<br>2d = GPI2 is configured as a master clock input (MCLK)<br>3d = GPI2 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN)<br>4d = GPI2 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1)<br>5d = GPI2 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2)<br>6d = Reserved; Don't use<br>7d = PD all ADC channels  |

### 7.2.24 GPI\_MON Register (Address = 0x2F) [Reset = 0x00]

GPI\_MON is shown in 表 7-25.

Return to the [Summary Table](#).

This register is the GPI monitor value register.

**表 7-25. GPI\_MON Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7   | GPI1_MON | R    | 0b    | GPI1 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1            |
| 6   | GPI2_MON | R    | 0b    | GPI2 monitor value when MICBIAS is configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 |
| 5-0 | RESERVED | R    | 0b    | Reserved bits; Write only reset value   |

### 7.2.25 INT\_CFG Register (Address = 0x32) [Reset = 0x00]

INT\_CFG is shown in 表 7-26.

Return to the [Summary Table](#).

This register is the interrupt configuration register.

**表 7-26. INT\_CFG Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7   | INT_POL        | R/W  | 0b    | Interrupt polarity.<br>0d = Active low (IRQZ)<br>1d = Active high (IRQ)  |
| 6-5 | INT_EVENT[1:0] | R/W  | 00b   | Interrupt event configuration.<br>0d = INT asserts on any unmasked latched interrupts event<br>Don't use<br>2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event<br>3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event |
| 4-3 | RESERVED       | R    | 0b    | Reserved bits; Write only reset value  |
| 2   | LTCH_READ_CFG  | R/W  | 0b    | Interrupt latch registers readback configuration.<br>0d = All interrupts can be read through the LTCH registers<br>1d = Only unmasked interrupts can be read through the LTCH registers  |
| 1-0 | RESERVED       | R    | 0b    | Reserved bits; Write only reset value  |

### 7.2.26 INT\_MASK0 Register (Address = 0x33) [Reset = 0xFF]

INT\_MASK0 is shown in [表 7-27](#).

Return to the [Summary Table](#).

This register is the interrupt masks register 0.

**表 7-27. INT\_MASK0 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7   | INT_MASK0 | R/W  | 1b    | ASI clock error mask.<br>0d = Do not mask<br>1d = Mask                   |
| 6   | INT_MASK0 | R/W  | 1b    | PLL Lock interrupt mask.<br>0d = Do not mask<br>1d = Mask                |
| 5   | INT_MASK0 | R/W  | 1b    | ASI input mixing saturation alert mask.<br>0d = Do not mask<br>1d = Mask |
| 4   | INT_MASK0 | R/W  | 1b    | VAD Power up detect interrupt mask.<br>0d = Do not mask<br>1d = Mask     |
| 3   | INT_MASK0 | R/W  | 1b    | VAD Power down detect interrupt mask.<br>0d = Do not mask<br>1d = Mask   |
| 2   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value                                     |
| 1   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value                                     |
| 0   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value                                     |

### 7.2.27 INT\_LTCH0 Register (Address = 0x36) [Reset = 0x00]

INT\_LTCH0 is shown in [表 7-28](#).

Return to the [Summary Table](#).

This register is the latched Interrupt readback register 0.

**表 7-28. INT\_LTCH0 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7   | INT_LTCH0 | R    | 0b    | Interrupt caused by an ASI bus clock error (self-clearing bit).<br>0d = No interrupt<br>1d = Interrupt                    |
| 6   | INT_LTCH0 | R    | 0b    | Interrupt caused by PLL LOCK (self-clearing bit).<br>0d = No interrupt<br>1d = Interrupt                                  |
| 5   | INT_LTCH0 | R    | 0b    | Interrupt caused by ASI input mixing channel saturation alert (self clearing bit).<br>0d = No interrupt<br>1d = Interrupt |
| 4   | INT_LTCH0 | R    | 0b    | Interrupt caused by VAD power up detect (self clearing bit).<br>0d = No interrupt<br>1d = Interrupt                       |
| 3   | INT_LTCH0 | R    | 0b    | Interrupt caused by VAD power down detect (self clearing bit).<br>0d = No interrupt<br>1d = Interrupt                     |
| 2   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value  |
| 1   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value  |
| 0   | RESERVED  | R    | 0b    | Reserved bit; Write only reset value  |

## 7.2.28 CM\_TOL\_CFG Register (Address = 0x3A) [Reset = 0x00]

CM\_TOL\_CFG is shown in 表 7-29.

Return to the [Summary Table](#).

This register is the ADC common mode configuration register

**表 7-29. CM\_TOL\_CFG Register Field Descriptions**

| Bit | Field                   | Type | Reset | Description  |
|-----|-------------------------|------|-------|--|
| 7-6 | CH1_INP_CM_TOL_CFG[1:0] | R/W  | 00b   | Channel 1 input common mode variance tolerance configuration.<br>0d = Common mode variance tolerance for AC coupled = 100 mVpp and DC coupled = 2.82 Vpp<br>1d = Common Mode Tolerance of: AC/DC Coupled Input=1V peak to peak<br>2d = Common Mode Tolerance of: AC/DC Coupled Input=0-AVDD(Supported only with Input Impedance of 10 kΩ/20 kΩ). For input impedance of 2.5 kΩ, input common mode tolerance= 0.4V to 2.6V.<br>3d = Reserved; Don't use |
| 5-4 | CH2_INP_CM_TOL_CFG[1:0] | R/W  | 00b   | Channel 2 input common mode variance tolerance configuration.<br>0d = Common mode variance tolerance for AC coupled = 100 mVpp and DC coupled = 2.82 Vpp<br>1d = Common Mode Tolerance of: AC/DC Coupled Input=1V peak to peak<br>2d = Common Mode Tolerance of: AC/DC Coupled Input=0-AVDD(Supported only with Input Impedance of 10 kΩ/20 kΩ). For input impedance of 2.5 kΩ, input common mode tolerance= 0.4V to 2.6V.<br>3d = Reserved; Don't use |
| 3-0 | RESERVED                | R    | 0b    | Reserved bits; Write only reset value  |

## 7.2.29 BIAS\_CFG Register (Address = 0x3B) [Reset = 0x00]

BIAS\_CFG is shown in 表 7-30.

Return to the [Summary Table](#).

This register is the bias and ADC configuration register

**表 7-30. BIAS\_CFG Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | RESERVED        | R    | 0b    | Reserved bit; Write only reset value   |
| 6-4 | MBIAS_VAL[2:0]  | R/W  | 000b  | MICBIAS value.<br>0d = Microphone bias is set to VREF (2.750 V, 2.500 V, or 1.375 V)<br>1d = Microphone bias is set to VREF x 1.096 (3.014 V, 2.740 V, or 1.507 V)<br>2d = Microphone bias is set to VCM = IN1M, for ADC single-ended configuration<br>3d = Microphone bias is set to VCM = IN2M, for ADC single-ended configuration<br>4d = Microphone bias is set to VCM = average of IN1M and IN2M, for ADC single-ended configuration<br>5d = Microphone bias is set to VCM = internal crude common mode<br>6d = Microphone bias is set to AVDD<br>7d = MICBIAS configured as GPI2 |
| 3-2 | RESERVED        | R    | 0b    | Reserved bits; Write only reset value  |
| 1-0 | ADC_FSCALE[1:0] | R/W  | 00b   | ADC full-scale setting (configure this setting based on the AVDD supply minimum voltage used).<br>0d = VREF is set to 2.75 V to support 2 V <sub>RMS</sub> for the differential input or 1 V <sub>RMS</sub> for the single-ended input<br>1d = VREF is set to 2.5 V to support 1.818 V <sub>RMS</sub> for the differential input or 0.909 V <sub>RMS</sub> for the single-ended input<br>2d = VREF is set to 1.375 V to support 1 V <sub>RMS</sub> for the differential input or 0.5 V <sub>RMS</sub> for the single-ended input<br>3d = Reserved; Don't use                           |

### 7.2.30 CH1\_CFG0 Register (Address = 0x3C) [Reset = 0x00]

CH1\_CFG0 is shown in [表 7-31](#).

Return to the [Summary Table](#).

This register is configuration register 0 for channel 1.

**表 7-31. CH1\_CFG0 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7   | CH1_INTYP      | R/W  | 0b    | Channel 1 input type.<br>0d = Microphone input<br>1d = Line input   |
| 6-5 | CH1_INSRC[1:0] | R/W  | 00b   | Channel 1 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK)<br>3d = Reserved; Don't use |
| 4   | CH1_DC         | R/W  | 0b    | Channel 1 input coupling (applicable for the analog input).<br>0d = AC-coupled input<br>1d = DC-coupled input   |
| 3-2 | CH1_IMP[1:0]   | R/W  | 00b   | Channel 1 input impedance (applicable for the analog input).<br>0d = Typical 2.5-kΩ input impedance<br>1d = Typical 10-kΩ input impedance<br>2d = Typical 20-kΩ input impedance<br>3d = Reserved; Don't use                             |
| 1   | RESERVED       | R    | 0b    | Reserved bit; Write only reset value  |

**表 7-31. CH1\_CFG0 Register Field Descriptions (続き)**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 0   | CH1_AGCEN | R/W  | 0b    | Channel 1 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108) |

### 7.2.31 CH1\_CFG1 Register (Address = 0x3D) [Reset = 0x00]

CH1\_CFG1 is shown in [表 7-32](#).

Return to the [Summary Table](#).

This register is configuration register 1 for channel 1.

**表 7-32. CH1\_CFG1 Register Field Descriptions**

| Bit | Field             | Type | Reset    | Description  |
|-----|-------------------|------|----------|--|
| 7-1 | CH1_GAIN[6:0]     | R/W  | 0000000b | Channel 1 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 0.5 dB<br>2d = Channel gain is set to 1 dB<br>3d to 83d = Channel gain is set as per configuration<br>84d = Channel gain is set to 42 dB<br>85d to 127d = Reserved; Don't use |
| 0   | CH1_GAIN_SIGN_BIT | R/W  | 0b       | Channel-1 gain sign configuration.<br>0d = Positive channel gain<br>1d = Negative channel gain (minimum channel gain supported till -11 dB; supported only for channel input impedance of 10-kΩ and 20-kΩ)   |

### 7.2.32 CH1\_CFG2 Register (Address = 0x3E) [Reset = 0xC9]

CH1\_CFG2 is shown in [表 7-33](#).

Return to the [Summary Table](#).

This register is configuration register 2 for channel 1.

**表 7-33. CH1\_CFG2 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description  |
|-----|---------------|------|-----------|--|
| 7-0 | CH1_DVOL[7:0] | R/W  | 11001001b | Channel 1 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB |

### 7.2.33 CH1\_CFG3 Register (Address = 0x3F) [Reset = 0x80]

CH1\_CFG3 is shown in [表 7-34](#).

Return to the [Summary Table](#).

This register is configuration register 3 for channel 1.

**表 7-34. CH1\_CFG3 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-4 | CH1_GCAL[3:0] | R/W  | 1000b | Channel 1 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB |
| 3-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset value  |

**7.2.34 CH1\_CFG4 Register (Address = 0x40) [Reset = 0x00]**

CH1\_CFG4 is shown in [表 7-35](#).

Return to the [Summary Table](#).

This register is configuration register 4 for channel 1.

**表 7-35. CH1\_CFG4 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description   |
|-----|---------------|------|-----------|---|
| 7-0 | CH1_PCAL[7:0] | R/W  | 00000000b | Channel 1 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock |

**7.2.35 CH2\_CFG0 Register (Address = 0x41) [Reset = 0x00]**

CH2\_CFG0 is shown in [表 7-36](#).

Return to the [Summary Table](#).

This register is configuration register 0 for channel 2.

**表 7-36. CH2\_CFG0 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7   | CH2_INTYP      | R/W  | 0b    | Channel 2 input type.<br>0d = Microphone input<br>1d = Line input   |
| 6-5 | CH2_INSRC[1:0] | R/W  | 00b   | Channel 2 input configuration.<br>0d = Analog differential input (the GPI1 and GPO1 pin functions must be disabled)<br>1d = Analog single-ended input (the GPI1 and GPO1 pin functions must be disabled)<br>2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK)<br>3d = Reserved; Don't use |
| 4   | CH2_DC         | R/W  | 0b    | Channel 2 input coupling (applicable for the analog input).<br>0d = AC-coupled input<br>1d = DC-coupled input   |

**表 7-36. CH2\_CFG0 Register Field Descriptions (続き)**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 3-2 | CH2_IMP[1:0] | R/W  | 00b   | Channel 2 input impedance (applicable for the analog input).<br>0d = Typical 2.5-kΩ input impedance<br>1d = Typical 10-kΩ input impedance<br>2d = Typical 20-kΩ input impedance<br>3d = Reserved; Don't use |
| 1   | RESERVED     | R    | 0b    | Reserved bit; Write only reset value  |
| 0   | CH2_AGCEN    | R/W  | 0b    | Channel 2 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108)   |

### 7.2.36 CH2\_CFG1 Register (Address = 0x42) [Reset = 0x00]

CH2\_CFG1 is shown in [表 7-37](#).

Return to the [Summary Table](#).

This register is configuration register 1 for channel 2.

**表 7-37. CH2\_CFG1 Register Field Descriptions**

| Bit | Field             | Type | Reset    | Description  |
|-----|-------------------|------|----------|--|
| 7-1 | CH2_GAIN[6:0]     | R/W  | 0000000b | Channel 2 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 0.5 dB<br>2d = Channel gain is set to 1 dB<br>3d to 83d = Channel gain is set as per configuration<br>84d = Channel gain is set to 42 dB<br>85d to 127d = Reserved; Don't use |
| 0   | CH2_GAIN_SIGN_BIT | R/W  | 0b       | Channel-2 gain sign configuration.<br>0d = Positive channel gain<br>1d = Negative channel gain (minimum channel gain supported till -11 dB; supported only for channel input impedance of 10-kΩ and 20-kΩ)   |

### 7.2.37 CH2\_CFG2 Register (Address = 0x43) [Reset = 0xC9]

CH2\_CFG2 is shown in [表 7-38](#).

Return to the [Summary Table](#).

This register is configuration register 2 for channel 2.

**表 7-38. CH2\_CFG2 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description  |
|-----|---------------|------|-----------|--|
| 7-0 | CH2_DVOL[7:0] | R/W  | 11001001b | Channel 2 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB |

### 7.2.38 CH2\_CFG3 Register (Address = 0x44) [Reset = 0x80]

CH2\_CFG3 is shown in [表 7-39](#).

Return to the [Summary Table](#).

This register is configuration register 3 for channel 2.

**表 7-39. CH2\_CFG3 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-4 | CH2_GCAL[3:0] | R/W  | 1000b | Channel 2 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB |
| 3-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset value  |

### 7.2.39 CH2\_CFG4 Register (Address = 0x45) [Reset = 0x00]

CH2\_CFG4 is shown in [表 7-40](#).

Return to the [Summary Table](#).

This register is configuration register 4 for channel 2.

**表 7-40. CH2\_CFG4 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description   |
|-----|---------------|------|-----------|---|
| 7-0 | CH2_PCAL[7:0] | R/W  | 00000000b | Channel 2 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock |

### 7.2.40 CH3\_CFG2 Register (Address = 0x48) [Reset = 0xC9]

CH3\_CFG2 is shown in [表 7-41](#).

Return to the [Summary Table](#).

This register is configuration register 2 for channel 3.



**表 7-41. CH3\_CFG2 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description  |
|-----|---------------|------|-----------|--|
| 7-0 | CH3_DVOL[7:0] | R/W  | 11001001b | Channel 3 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB |

#### 7.2.41 CH3\_CFG3 Register (Address = 0x49) [Reset = 0x80]

CH3\_CFG3 is shown in [表 7-42](#).

Return to the [Summary Table](#).

This register is configuration register 3 for channel 3.

**表 7-42. CH3\_CFG3 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-4 | CH3_GCAL[3:0] | R/W  | 1000b | Channel 3 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB |
| 3-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset value  |

#### 7.2.42 CH3\_CFG4 Register (Address = 0x4A) [Reset = 0x00]

CH3\_CFG4 is shown in [表 7-43](#).

Return to the [Summary Table](#).

This register is configuration register 4 for channel 3.

**表 7-43. CH3\_CFG4 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description   |
|-----|---------------|------|-----------|---|
| 7-0 | CH3_PCAL[7:0] | R/W  | 00000000b | Channel 3 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock |

#### 7.2.43 CH4\_CFG2 Register (Address = 0x4D) [Reset = 0xC9]

CH4\_CFG2 is shown in [表 7-44](#).

Return to the [Summary Table](#).

This register is configuration register 2 for channel 4.

**表 7-44. CH4\_CFG2 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description  |
|-----|---------------|------|-----------|--|
| 7-0 | CH4_DVOL[7:0] | R/W  | 11001001b | Channel 4 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB |

#### 7.2.44 CH4\_CFG3 Register (Address = 0x4E) [Reset = 0x80]

CH4\_CFG3 is shown in [表 7-45](#).

Return to the [Summary Table](#).

This register is configuration register 3 for channel 4.

**表 7-45. CH4\_CFG3 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-4 | CH4_GCAL[3:0] | R/W  | 1000b | Channel 4 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB |
| 3-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset value  |

#### 7.2.45 CH4\_CFG4 Register (Address = 0x4F) [Reset = 0x00]

CH4\_CFG4 is shown in [表 7-46](#).

Return to the [Summary Table](#).

This register is configuration register 4 for channel 4.

**表 7-46. CH4\_CFG4 Register Field Descriptions**

| Bit | Field         | Type | Reset     | Description   |
|-----|---------------|------|-----------|---|
| 7-0 | CH4_PCAL[7:0] | R/W  | 00000000b | Channel 4 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock |

## 7.2.46 DSP\_CFG0 Register (Address = 0x6B) [Reset = 0x01]

DSP\_CFG0 is shown in 表 7-47.

Return to the [Summary Table](#).

This register is the digital signal processor (DSP) configuration register 0.

**表 7-47. DSP\_CFG0 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7   | DIS_DVOL_OTF_CHG | R/W  | 0b    | Disable run-time changes to DVOL settings.<br>0d = Digital volume control changes supported while ADC is powered-on<br>1d = Digital volume control changes not supported while ADC is powered-on. This is useful for 384 kHz and higher sample rate if more than one channel processing is required.   |
| 6   | RESERVED         | R    | 0b    | Reserved bit; Write only reset value   |
| 5-4 | DECI_FILT[1:0]   | R/W  | 00b   | Decimation filter response.<br>0d = Linear phase<br>1d = Low latency<br>2d = Ultra-low latency<br>3d = Reserved; Don't use   |
| 3-2 | CH_SUM[1:0]      | R/W  | 00b   | Channel summation mode for higher SNR<br>0d = Channel summation mode is disabled<br>1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 output<br>2d = Reserved; Don't use<br>3d = Reserved; Don't use  |
| 1-0 | HPF_SEL[1:0]     | R/W  | 01b   | High-pass filter (HPF) selection.<br>0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter<br>1d = HPF with a cutoff of $0.00025 \times f_S$ (12 Hz at $f_S = 48$ kHz) is selected<br>2d = HPF with a cutoff of $0.002 \times f_S$ (96 Hz at $f_S = 48$ kHz) is selected<br>3d = HPF with a cutoff of $0.008 \times f_S$ (384 Hz at $f_S = 48$ kHz) is selected |

## 7.2.47 DSP\_CFG1 Register (Address = 0x6C) [Reset = 0x40]

DSP\_CFG1 is shown in 表 7-48.

Return to the [Summary Table](#).

This register is the digital signal processor (DSP) configuration register 1.

**表 7-48. DSP\_CFG1 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | DVOL_GANG         | R/W  | 0b    | DVOL control ganged across channels.<br>0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits<br>1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not |
| 6-5 | BIQUAD_CFG[1:0]   | R/W  | 10b   | Number of biquads per channel configuration.<br>0d = No biquads per channel; biquads are all disabled<br>1d = 1 biquad per channel<br>2d = 2 biquads per channel<br>3d = 3 biquads per channel   |
| 4   | DISABLE_SOFT_STEP | R/W  | 0b    | Soft-stepping disable during DVOL change, mute, and unmute.<br>0d = Soft-stepping enabled<br>1d = Soft-stepping disabled   |

表 7-48. DSP\_CFG1 Register Field Descriptions (続き)

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 3   | AGC_SEL       | R/W  | 0b    | AGC Selection when is enabled for any channel<br>0d = AGC is not selected<br>1d = AGC is selected  |
| 2   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 1   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 0   | EN_AVOID_CLIP | R/W  | 0b    | Anti clipper when channel gain > 0 dB and AGC mode enabled.<br>0d = Channel gain is maintained as per user programmed value<br>1d = Signal level is compressed to avoid clipping when channel gain > 0 dB and signal level crosses programmed threshold setting set in page-4. |

**7.2.48 AGC\_CFG0 Register (Address = 0x70) [Reset = 0xE7]**

AGC\_CFG0 is shown in 表 7-49.

Return to the [Summary Table](#).

This register is the automatic gain controller (AGC) configuration register 0.

表 7-49. AGC\_CFG0 Register Field Descriptions

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7-4 | AGC_LVL[3:0]     | R/W  | 1110b | AGC output signal target level.<br>0d = Output signal target level is -6 dB<br>1d = Output signal target level is -8 dB<br>2d = Output signal target level is -10 dB<br>3d to 13d = Output signal target level is as per configuration<br>14d = Output signal target level is -34 dB<br>15d = Output signal target level is -36 dB |
| 3-0 | AGC_MAXGAIN[3:0] | R/W  | 0111b | AGC maximum gain allowed.<br>0d = Maximum gain allowed is 3 dB<br>1d = Maximum gain allowed is 6 dB<br>2d = Maximum gain allowed is 9 dB<br>3d to 11d = Maximum gain allowed is as per configuration<br>12d = Maximum gain allowed is 39 dB<br>13d = Maximum gain allowed is 42 dB<br>14d to 15d = Reserved; Don't use             |

**7.2.49 GAIN\_CFG Register (Address = 0x71) [Reset = 0x00]**

GAIN\_CFG is shown in 表 7-50.

Return to the [Summary Table](#).

This register is the channel gain change configuration register.

表 7-50. GAIN\_CFG Register Field Descriptions

| Bit | Field                    | Type | Reset | Description   |
|-----|--------------------------|------|-------|---|
| 7-6 | OTF_GAIN_CHANGE_CFG[1:0] | R/W  | 00b   | On the fly channel gain change configuration<br>0d = On-the-fly gain change with some artifacts due to applying gain change immediately<br>1d = On-the-fly gain change enabled with reduced artifacts but without soft-stepping<br>2d = On-the-fly gain change enabled with soft-stepping of 0.5 dB per ~20 $\mu$ s, supported channel gain up to 30 dB for 10-k $\Omega$ input impedance mode and 24 dB for 20-k $\Omega$ input impedance mode<br>3d = On-the-fly gain change enabled with soft-stepping of 0.5 dB per ~40 $\mu$ s, supported channel gain up to 30 dB for 10-k $\Omega$ input impedance mode and 24 dB for 20-k $\Omega$ input impedance mode |

**表 7-50. GAIN\_CFG Register Field Descriptions (続き)**

| Bit | Field    | Type | Reset | Description                           |
|-----|----------|------|-------|---------------------------------------|
| 5   | RESERVED | R    | 0b    | Reserved bit; Write only reset value  |
| 4-0 | RESERVED | R    | 0b    | Reserved bits; Write only reset value |

### 7.2.50 IN\_CH\_EN Register (Address = 0x73) [Reset = 0xC0]

IN\_CH\_EN is shown in [表 7-51](#).

Return to the [Summary Table](#).

This register is the input channel enable configuration register.

**表 7-51. IN\_CH\_EN Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7   | IN_CH1_EN | R/W  | 1b    | Input channel 1 enable setting.<br>0d = Channel 1 is disabled<br>1d = Channel 1 is enabled            |
| 6   | IN_CH2_EN | R/W  | 1b    | Input channel 2 enable setting.<br>0d = Channel 2 is disabled<br>1d = Channel 2 is enabled            |
| 5   | IN_CH3_EN | R/W  | 0b    | Input channel 3 (PDM only) enable setting.<br>0d = Channel 3 is disabled<br>1d = Channel 3 is enabled |
| 4   | IN_CH4_EN | R/W  | 0b    | Input channel 4 (PDM only) enable setting.<br>0d = Channel 4 is disabled<br>1d = Channel 4 is enabled |
| 3-0 | RESERVED  | R    | 0b    | Reserved bits; Write only reset value   |

### 7.2.51 ASI\_OUT\_CH\_EN Register (Address = 0x74) [Reset = 0x00]

ASI\_OUT\_CH\_EN is shown in [表 7-52](#).

Return to the [Summary Table](#).

This register is the ASI output channel enable configuration register.

**表 7-52. ASI\_OUT\_CH\_EN Register Field Descriptions**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7   | ASI_OUT_CH1_EN | R/W  | 0b    | ASI output channel 1 enable setting.<br>0d = Channel 1 output slot is in a tri-state condition<br>1d = Channel 1 output slot is enabled |
| 6   | ASI_OUT_CH2_EN | R/W  | 0b    | ASI output channel 2 enable setting.<br>0d = Channel 2 output slot is in a tri-state condition<br>1d = Channel 2 output slot is enabled |
| 5   | ASI_OUT_CH3_EN | R/W  | 0b    | ASI output channel 3 enable setting.<br>0d = Channel 3 output slot is in a tri-state condition<br>1d = Channel 3 output slot is enabled |
| 4   | ASI_OUT_CH4_EN | R/W  | 0b    | ASI output channel 4 enable setting.<br>0d = Channel 4 output slot is in a tri-state condition<br>1d = Channel 4 output slot is enabled |
| 3-0 | RESERVED       | R    | 0b    | Reserved bits; Write only reset value   |

### 7.2.52 PWR\_CFG Register (Address = 0x75) [Reset = 0x00]

PWR\_CFG is shown in 表 7-53.

Return to the [Summary Table](#).

This register is the power-up configuration register.

**表 7-53. PWR\_CFG Register Field Descriptions**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7   | MICBIAS_PDZ        | R/W  | 0b    | Power control for MICBIAS.<br>0d = Power down MICBIAS<br>1d = Power up MICBIAS  |
| 6   | ADC_PDZ            | R/W  | 0b    | Power control for ADC and PDM channels.<br>0d = Power down all ADC and PDM channels<br>1d = Power up all enabled ADC and PDM channels   |
| 5   | PLL_PDZ            | R/W  | 0b    | Power control for the PLL.<br>0d = Power down the PLL<br>1d = Power up the PLL  |
| 4   | DYN_CH_PUPD_EN     | R/W  | 0b    | Dynamic channel power-up, power-down enable.<br>0d = Channel power-up, power-down is not supported if any channel recording is on<br>1d = Channel can be powered up or down individually, even if channel recording is on   |
| 3-2 | DYN_MAXCH_SEL[1:0] | R/W  | 00b   | Dynamic mode maximum channel select configuration.<br>0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled<br>1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled<br>2d = Reserved; Don't use<br>3d = Reserved; Don't use |
| 1   | RESERVED           | R    | 0b    | Reserved bit; Write only reset value  |
| 0   | VAD_EN             | R/W  | 0b    | Enable voice activity detection (VAD) algorithm.<br>0d = VAD is disabled<br>1d = VAD is enabled   |

### 7.2.53 DEV\_STS0 Register (Address = 0x76) [Reset = 0x00]

DEV\_STS0 is shown in 表 7-54.

Return to the [Summary Table](#).

This register is the device status value register 0.

**表 7-54. DEV\_STS0 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7   | CH1_STATUS | R    | 0b    | ADC or PDM channel 1 power status.<br>0d = ADC or PDM channel is powered down<br>1d = ADC or PDM channel is powered up |
| 6   | CH2_STATUS | R    | 0b    | ADC or PDM channel 2 power status.<br>0d = ADC or PDM channel is powered down<br>1d = ADC or PDM channel is powered up |
| 5-0 | RESERVED   | R    | 0b    | Reserved bits; Write only reset value  |

### 7.2.54 DEV\_STS1 Register (Address = 0x77) [Reset = 0x80]

DEV\_STS1 is shown in 表 7-55.

Return to the [Summary Table](#).

This register is the device status value register 1.

**表 7-55. DEV\_STS1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-5 | MODE_STS[2:0] | R    | 100b  | Device mode status.<br>4d = Device is in sleep mode or software shutdown mode<br>6d = Device is in active mode with all ADC or PDM channels turned off<br>7d = Device is in active mode with at least one ADC or PDM channel turned on |
| 4-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset value  |

### 7.2.55 I2C\_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C\_CKSUM is shown in 表 7-56.

Return to the [Summary Table](#).

This register returns the I<sup>2</sup>C transactions checksum value.

**表 7-56. I2C\_CKSUM Register Field Descriptions**

| Bit | Field          | Type | Reset     | Description  |
|-----|----------------|------|-----------|--|
| 7-0 | I2C_CKSUM[7:0] | R/W  | 00000000b | These bits return the I <sup>2</sup> C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages. |

## 7.3 Page\_1 Registers

表 7-57 lists the memory-mapped registers for the Page\_1 registers. All register offset addresses not listed in 表 7-57 should be considered as reserved locations and the register contents should not be modified.

**表 7-57. PAGE\_1 Registers**

| Address | Acronym  | Register Name                                     | Reset Value | Section                     |
|---------|----------|---|-------------|-----------------------------|
| 0x0     | PAGE_CFG | Device page register                              | 0x00        | <a href="#">セクション 7.3.1</a> |
| 0x1E    | VAD_CFG1 | Voice activity detection configuration register 1 | 0x20        | <a href="#">セクション 7.3.2</a> |
| 0x1F    | VAD_CFG2 | Voice activity detection configuration register 2 | 0x08        | <a href="#">セクション 7.3.3</a> |

### 7.3.1 PAGE\_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE\_CFG is shown in 表 7-58.

Return to the [Summary Table](#).

The device memory map is divided into pages. This register sets the page.

**表 7-58. PAGE\_CFG Register Field Descriptions**

| Bit | Field     | Type | Reset     | Description  |
|-----|-----------|------|-----------|--|
| 7-0 | PAGE[7:0] | R/W  | 00000000b | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>2d to 254d = Page 2 to page 254 respectively<br>255d = Page 255 |

### 7.3.2 VAD\_CFG1 Register (Address = 0x1E) [Reset = 0x20]

VAD\_CFG1 is shown in 表 7-59.

Return to the [Summary Table](#).

This register is configuration register 1 for voice activity detection.

**表 7-59. VAD\_CFG1 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7-6 | VAD_MODE[1:0]    | R/W  | 00b   | Auto ADC power up / power down configuration selection.<br>0d = User initiated ADC power-up and ADC power-down<br>1d = VAD interrupt based ADC power up and ADC power down<br>2d = VAD interrupt based ADC power up but user initiated ADC power down<br>3d = User initiated ADC power-up but VAD interrupt based ADC power down |
| 5-4 | VAD_CH_SEL[1:0]  | R/W  | 10b   | VAD channel select.<br>0d = Channel 1 is monitored for VAD activity<br>1d = Channel 2 is monitored for VAD activity<br>2d = Channel 3 is monitored for VAD activity<br>3d = Channel 4 is monitored for VAD activity  |
| 3-2 | VAD_CLK_CFG[1:0] | R/W  | 00b   | Clock select for VAD<br>0d = VAD processing using internal oscillator clock<br>1d = VAD processing using external clock on BCLK input<br>2d = VAD processing using external clock on MCLK input<br>3d = Custom clock configuration based on MST_CFG, CLK_SRC and CLKGEN_CFG registers in page 0                                  |



**表 7-59. VAD\_CFG1 Register Field Descriptions (続き)**

| Bit | Field                | Type | Reset | Description   |
|-----|----------------------|------|-------|---|
| 1-0 | VAD_EXT_CLK_CFG[1:0] | R/W  | 00b   | Clock configuration using external clock for VAD.<br>0d = External clock is 3.072 MHz<br>1d = External clock is 6.144 MHz<br>2d = External clock is 12.288 MHz<br>3d = External clock is 18.432 MHz |

### 7.3.3 VAD\_CFG2 Register (Address = 0x1F) [Reset = 0x08]

VAD\_CFG2 is shown in [表 7-60](#).

Return to the [Summary Table](#).

This register is configuration register 2 for voice activity detection.

**表 7-60. VAD\_CFG2 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 6   | SDOUT_INT_CFG | R/W  | 0b    | SDOUT interrupt configuration.<br>0d = SDOUT pin is not enabled for interrupt function<br>1d = SDOUT pin is enabled to support interrupt output when channel data is not being recorded                      |
| 5   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 4   | RESERVED      | R    | 0b    | Reserved bit; Write only reset value   |
| 3   | VAD_PD_DET_EN | R/W  | 1b    | Enable ASI output data during VAD activity.<br>0d = VAD processing is not enabled during ADC recording<br>1d = VAD processing is enabled during ADC recording and VAD interrupts are generated as configured |
| 2-0 | RESERVED      | R    | 0b    | Reserved bits; Write only reset values   |

## 7.4 Programmable Coefficient Registers

### 7.4.1 Programmable Coefficient Registers: Page 2

This register page (shown in 表 7-61) consists of the programmable coefficients for the biquad 1 to biquad 6 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I<sup>2</sup>C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

**表 7-61. Page 2 Programmable Coefficient Registers**

| ADDRESS | ACRONYM          | REGISTER NAME                                     | RESET VALUE |
|---------|------------------|---|-------------|
| 0x00    | PAGE[7:0]        | Device page register                              | 0x00        |
| 0x08    | BQ1_N0_BYT1[7:0] | Programmable biquad 1, N0 coefficient byte[31:24] | 0x7F        |
| 0x09    | BQ1_N0_BYT2[7:0] | Programmable biquad 1, N0 coefficient byte[23:16] | 0xFF        |
| 0x0A    | BQ1_N0_BYT3[7:0] | Programmable biquad 1, N0 coefficient byte[15:8]  | 0xFF        |
| 0x0B    | BQ1_N0_BYT4[7:0] | Programmable biquad 1, N0 coefficient byte[7:0]   | 0xFF        |
| 0x0C    | BQ1_N1_BYT1[7:0] | Programmable biquad 1, N1 coefficient byte[31:24] | 0x00        |
| 0x0D    | BQ1_N1_BYT2[7:0] | Programmable biquad 1, N1 coefficient byte[23:16] | 0x00        |
| 0x0E    | BQ1_N1_BYT3[7:0] | Programmable biquad 1, N1 coefficient byte[15:8]  | 0x00        |
| 0x0F    | BQ1_N1_BYT4[7:0] | Programmable biquad 1, N1 coefficient byte[7:0]   | 0x00        |
| 0x10    | BQ1_N2_BYT1[7:0] | Programmable biquad 1, N2 coefficient byte[31:24] | 0x00        |
| 0x11    | BQ1_N2_BYT2[7:0] | Programmable biquad 1, N2 coefficient byte[23:16] | 0x00        |
| 0x12    | BQ1_N2_BYT3[7:0] | Programmable biquad 1, N2 coefficient byte[15:8]  | 0x00        |
| 0x13    | BQ1_N2_BYT4[7:0] | Programmable biquad 1, N2 coefficient byte[7:0]   | 0x00        |
| 0x14    | BQ1_D1_BYT1[7:0] | Programmable biquad 1, D1 coefficient byte[31:24] | 0x00        |
| 0x15    | BQ1_D1_BYT2[7:0] | Programmable biquad 1, D1 coefficient byte[23:16] | 0x00        |
| 0x16    | BQ1_D1_BYT3[7:0] | Programmable biquad 1, D1 coefficient byte[15:8]  | 0x00        |
| 0x17    | BQ1_D1_BYT4[7:0] | Programmable biquad 1, D1 coefficient byte[7:0]   | 0x00        |
| 0x18    | BQ1_D2_BYT1[7:0] | Programmable biquad 1, D2 coefficient byte[31:24] | 0x00        |
| 0x19    | BQ1_D2_BYT2[7:0] | Programmable biquad 1, D2 coefficient byte[23:16] | 0x00        |
| 0x1A    | BQ1_D2_BYT3[7:0] | Programmable biquad 1, D2 coefficient byte[15:8]  | 0x00        |
| 0x1B    | BQ1_D2_BYT4[7:0] | Programmable biquad 1, D2 coefficient byte[7:0]   | 0x00        |
| 0x1C    | BQ2_N0_BYT1[7:0] | Programmable biquad 2, N0 coefficient byte[31:24] | 0x7F        |
| 0x1D    | BQ2_N0_BYT2[7:0] | Programmable biquad 2, N0 coefficient byte[23:16] | 0xFF        |
| 0x1E    | BQ2_N0_BYT3[7:0] | Programmable biquad 2, N0 coefficient byte[15:8]  | 0xFF        |
| 0x1F    | BQ2_N0_BYT4[7:0] | Programmable biquad 2, N0 coefficient byte[7:0]   | 0xFF        |
| 0x20    | BQ2_N1_BYT1[7:0] | Programmable biquad 2, N1 coefficient byte[31:24] | 0x00        |
| 0x21    | BQ2_N1_BYT2[7:0] | Programmable biquad 2, N1 coefficient byte[23:16] | 0x00        |
| 0x22    | BQ2_N1_BYT3[7:0] | Programmable biquad 2, N1 coefficient byte[15:8]  | 0x00        |
| 0x23    | BQ2_N1_BYT4[7:0] | Programmable biquad 2, N1 coefficient byte[7:0]   | 0x00        |
| 0x24    | BQ2_N2_BYT1[7:0] | Programmable biquad 2, N2 coefficient byte[31:24] | 0x00        |
| 0x25    | BQ2_N2_BYT2[7:0] | Programmable biquad 2, N2 coefficient byte[23:16] | 0x00        |
| 0x26    | BQ2_N2_BYT3[7:0] | Programmable biquad 2, N2 coefficient byte[15:8]  | 0x00        |
| 0x27    | BQ2_N2_BYT4[7:0] | Programmable biquad 2, N2 coefficient byte[7:0]   | 0x00        |
| 0x28    | BQ2_D1_BYT1[7:0] | Programmable biquad 2, D1 coefficient byte[31:24] | 0x00        |
| 0x29    | BQ2_D1_BYT2[7:0] | Programmable biquad 2, D1 coefficient byte[23:16] | 0x00        |
| 0x2A    | BQ2_D1_BYT3[7:0] | Programmable biquad 2, D1 coefficient byte[15:8]  | 0x00        |
| 0x2B    | BQ2_D1_BYT4[7:0] | Programmable biquad 2, D1 coefficient byte[7:0]   | 0x00        |
| 0x2C    | BQ2_D2_BYT1[7:0] | Programmable biquad 2, D2 coefficient byte[31:24] | 0x00        |
| 0x2D    | BQ2_D2_BYT2[7:0] | Programmable biquad 2, D2 coefficient byte[23:16] | 0x00        |
| 0x2E    | BQ2_D2_BYT3[7:0] | Programmable biquad 2, D2 coefficient byte[15:8]  | 0x00        |
| 0x2F    | BQ2_D2_BYT4[7:0] | Programmable biquad 2, D2 coefficient byte[7:0]   | 0x00        |
| 0x30    | BQ3_N0_BYT1[7:0] | Programmable biquad 3, N0 coefficient byte[31:24] | 0x7F        |

**表 7-61. Page 2 Programmable Coefficient Registers (続き)**

| ADDRESS | ACRONYM          | REGISTER NAME                                     | RESET VALUE |
|---------|------------------|---|-------------|
| 0x31    | BQ3_N0_BYT2[7:0] | Programmable biquad 3, N0 coefficient byte[23:16] | 0xFF        |
| 0x32    | BQ3_N0_BYT3[7:0] | Programmable biquad 3, N0 coefficient byte[15:8]  | 0xFF        |
| 0x33    | BQ3_N0_BYT4[7:0] | Programmable biquad 3, N0 coefficient byte[7:0]   | 0xFF        |
| 0x34    | BQ3_N1_BYT1[7:0] | Programmable biquad 3, N1 coefficient byte[31:24] | 0x00        |
| 0x35    | BQ3_N1_BYT2[7:0] | Programmable biquad 3, N1 coefficient byte[23:16] | 0x00        |
| 0x36    | BQ3_N1_BYT3[7:0] | Programmable biquad 3, N1 coefficient byte[15:8]  | 0x00        |
| 0x37    | BQ3_N1_BYT4[7:0] | Programmable biquad 3, N1 coefficient byte[7:0]   | 0x00        |
| 0x38    | BQ3_N2_BYT1[7:0] | Programmable biquad 3, N2 coefficient byte[31:24] | 0x00        |
| 0x39    | BQ3_N2_BYT2[7:0] | Programmable biquad 3, N2 coefficient byte[23:16] | 0x00        |
| 0x3A    | BQ3_N2_BYT3[7:0] | Programmable biquad 3, N2 coefficient byte[15:8]  | 0x00        |
| 0x3B    | BQ3_N2_BYT4[7:0] | Programmable biquad 3, N2 coefficient byte[7:0]   | 0x00        |
| 0x3C    | BQ3_D1_BYT1[7:0] | Programmable biquad 3, D1 coefficient byte[31:24] | 0x00        |
| 0x3D    | BQ3_D1_BYT2[7:0] | Programmable biquad 3, D1 coefficient byte[23:16] | 0x00        |
| 0x3E    | BQ3_D1_BYT3[7:0] | Programmable biquad 3, D1 coefficient byte[15:8]  | 0x00        |
| 0x3F    | BQ3_D1_BYT4[7:0] | Programmable biquad 3, D1 coefficient byte[7:0]   | 0x00        |
| 0x40    | BQ3_D2_BYT1[7:0] | Programmable biquad 3, D2 coefficient byte[31:24] | 0x00        |
| 0x41    | BQ3_D2_BYT2[7:0] | Programmable biquad 3, D2 coefficient byte[23:16] | 0x00        |
| 0x42    | BQ3_D2_BYT3[7:0] | Programmable biquad 3, D2 coefficient byte[15:8]  | 0x00        |
| 0x43    | BQ3_D2_BYT4[7:0] | Programmable biquad 3, D2 coefficient byte[7:0]   | 0x00        |
| 0x44    | BQ4_N0_BYT1[7:0] | Programmable biquad 4, N0 coefficient byte[31:24] | 0x7F        |
| 0x45    | BQ4_N0_BYT2[7:0] | Programmable biquad 4, N0 coefficient byte[23:16] | 0xFF        |
| 0x46    | BQ4_N0_BYT3[7:0] | Programmable biquad 4, N0 coefficient byte[15:8]  | 0xFF        |
| 0x47    | BQ4_N0_BYT4[7:0] | Programmable biquad 4, N0 coefficient byte[7:0]   | 0xFF        |
| 0x48    | BQ4_N1_BYT1[7:0] | Programmable biquad 4, N1 coefficient byte[31:24] | 0x00        |
| 0x49    | BQ4_N1_BYT2[7:0] | Programmable biquad 4, N1 coefficient byte[23:16] | 0x00        |
| 0x4A    | BQ4_N1_BYT3[7:0] | Programmable biquad 4, N1 coefficient byte[15:8]  | 0x00        |
| 0x4B    | BQ4_N1_BYT4[7:0] | Programmable biquad 4, N1 coefficient byte[7:0]   | 0x00        |
| 0x4C    | BQ4_N2_BYT1[7:0] | Programmable biquad 4, N2 coefficient byte[31:24] | 0x00        |
| 0x4D    | BQ4_N2_BYT2[7:0] | Programmable biquad 4, N2 coefficient byte[23:16] | 0x00        |
| 0x4E    | BQ4_N2_BYT3[7:0] | Programmable biquad 4, N2 coefficient byte[15:8]  | 0x00        |
| 0x4F    | BQ4_N2_BYT4[7:0] | Programmable biquad 4, N2 coefficient byte[7:0]   | 0x00        |
| 0x50    | BQ4_D1_BYT1[7:0] | Programmable biquad 4, D1 coefficient byte[31:24] | 0x00        |
| 0x51    | BQ4_D1_BYT2[7:0] | Programmable biquad 4, D1 coefficient byte[23:16] | 0x00        |
| 0x52    | BQ4_D1_BYT3[7:0] | Programmable biquad 4, D1 coefficient byte[15:8]  | 0x00        |
| 0x53    | BQ4_D1_BYT4[7:0] | Programmable biquad 4, D1 coefficient byte[7:0]   | 0x00        |
| 0x54    | BQ4_D2_BYT1[7:0] | Programmable biquad 4, D2 coefficient byte[31:24] | 0x00        |
| 0x55    | BQ4_D2_BYT2[7:0] | Programmable biquad 4, D2 coefficient byte[23:16] | 0x00        |
| 0x56    | BQ4_D2_BYT3[7:0] | Programmable biquad 4, D2 coefficient byte[15:8]  | 0x00        |
| 0x57    | BQ4_D2_BYT4[7:0] | Programmable biquad 4, D2 coefficient byte[7:0]   | 0x00        |
| 0x58    | BQ5_N0_BYT1[7:0] | Programmable biquad 5, N0 coefficient byte[31:24] | 0x7F        |
| 0x59    | BQ5_N0_BYT2[7:0] | Programmable biquad 5, N0 coefficient byte[23:16] | 0xFF        |
| 0x5A    | BQ5_N0_BYT3[7:0] | Programmable biquad 5, N0 coefficient byte[15:8]  | 0xFF        |
| 0x5B    | BQ5_N0_BYT4[7:0] | Programmable biquad 5, N0 coefficient byte[7:0]   | 0xFF        |
| 0x5C    | BQ5_N1_BYT1[7:0] | Programmable biquad 5, N1 coefficient byte[31:24] | 0x00        |
| 0x5D    | BQ5_N1_BYT2[7:0] | Programmable biquad 5, N1 coefficient byte[23:16] | 0x00        |
| 0x5E    | BQ5_N1_BYT3[7:0] | Programmable biquad 5, N1 coefficient byte[15:8]  | 0x00        |
| 0x5F    | BQ5_N1_BYT4[7:0] | Programmable biquad 5, N1 coefficient byte[7:0]   | 0x00        |
| 0x60    | BQ5_N2_BYT1[7:0] | Programmable biquad 5, N2 coefficient byte[31:24] | 0x00        |
| 0x61    | BQ5_N2_BYT2[7:0] | Programmable biquad 5, N2 coefficient byte[23:16] | 0x00        |

表 7-61. Page 2 Programmable Coefficient Registers (続き)

| ADDRESS | ACRONYM          | REGISTER NAME                                     | RESET VALUE |
|---------|------------------|---|-------------|
| 0x62    | BQ5_N2_BYT3[7:0] | Programmable biquad 5, N2 coefficient byte[15:8]  | 0x00        |
| 0x63    | BQ5_N2_BYT4[7:0] | Programmable biquad 5, N2 coefficient byte[7:0]   | 0x00        |
| 0x64    | BQ5_D1_BYT1[7:0] | Programmable biquad 5, D1 coefficient byte[31:24] | 0x00        |
| 0x65    | BQ5_D1_BYT2[7:0] | Programmable biquad 5, D1 coefficient byte[23:16] | 0x00        |
| 0x66    | BQ5_D1_BYT3[7:0] | Programmable biquad 5, D1 coefficient byte[15:8]  | 0x00        |
| 0x67    | BQ5_D1_BYT4[7:0] | Programmable biquad 5, D1 coefficient byte[7:0]   | 0x00        |
| 0x68    | BQ5_D2_BYT1[7:0] | Programmable biquad 5, D2 coefficient byte[31:24] | 0x00        |
| 0x69    | BQ5_D2_BYT2[7:0] | Programmable biquad 5, D2 coefficient byte[23:16] | 0x00        |
| 0x6A    | BQ5_D2_BYT3[7:0] | Programmable biquad 5, D2 coefficient byte[15:8]  | 0x00        |
| 0x6B    | BQ5_D2_BYT4[7:0] | Programmable biquad 5, D2 coefficient byte[7:0]   | 0x00        |
| 0x6C    | BQ6_N0_BYT1[7:0] | Programmable biquad 6, N0 coefficient byte[31:24] | 0x7F        |
| 0x6D    | BQ6_N0_BYT2[7:0] | Programmable biquad 6, N0 coefficient byte[23:16] | 0xFF        |
| 0x6E    | BQ6_N0_BYT3[7:0] | Programmable biquad 6, N0 coefficient byte[15:8]  | 0xFF        |
| 0x6F    | BQ6_N0_BYT4[7:0] | Programmable biquad 6, N0 coefficient byte[7:0]   | 0xFF        |
| 0x70    | BQ6_N1_BYT1[7:0] | Programmable biquad 6, N1 coefficient byte[31:24] | 0x00        |
| 0x71    | BQ6_N1_BYT2[7:0] | Programmable biquad 6, N1 coefficient byte[23:16] | 0x00        |
| 0x72    | BQ6_N1_BYT3[7:0] | Programmable biquad 6, N1 coefficient byte[15:8]  | 0x00        |
| 0x73    | BQ6_N1_BYT4[7:0] | Programmable biquad 6, N1 coefficient byte[7:0]   | 0x00        |
| 0x74    | BQ6_N2_BYT1[7:0] | Programmable biquad 6, N2 coefficient byte[31:24] | 0x00        |
| 0x75    | BQ6_N2_BYT2[7:0] | Programmable biquad 6, N2 coefficient byte[23:16] | 0x00        |
| 0x76    | BQ6_N2_BYT3[7:0] | Programmable biquad 6, N2 coefficient byte[15:8]  | 0x00        |
| 0x77    | BQ6_N2_BYT4[7:0] | Programmable biquad 6, N2 coefficient byte[7:0]   | 0x00        |
| 0x78    | BQ6_D1_BYT1[7:0] | Programmable biquad 6, D1 coefficient byte[31:24] | 0x00        |
| 0x79    | BQ6_D1_BYT2[7:0] | Programmable biquad 6, D1 coefficient byte[23:16] | 0x00        |
| 0x7A    | BQ6_D1_BYT3[7:0] | Programmable biquad 6, D1 coefficient byte[15:8]  | 0x00        |
| 0x7B    | BQ6_D1_BYT4[7:0] | Programmable biquad 6, D1 coefficient byte[7:0]   | 0x00        |
| 0x7C    | BQ6_D2_BYT1[7:0] | Programmable biquad 6, D2 coefficient byte[31:24] | 0x00        |
| 0x7D    | BQ6_D2_BYT2[7:0] | Programmable biquad 6, D2 coefficient byte[23:16] | 0x00        |
| 0x7E    | BQ6_D2_BYT3[7:0] | Programmable biquad 6, D2 coefficient byte[15:8]  | 0x00        |
| 0x7F    | BQ6_D2_BYT4[7:0] | Programmable biquad 6, D2 coefficient byte[7:0]   | 0x00        |

## 7.4.2 Programmable Coefficient Registers: Page 3

This register page (shown in 表 7-62) consists of the programmable coefficients for the biquad 7 to biquad 12 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I<sup>2</sup>C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

**表 7-62. Page 3 Programmable Coefficient Registers**

| ADDRESS | ACRONYM          | REGISTER NAME                                     | RESET VALUE |
|---------|------------------|---|-------------|
| 0x00    | PAGE[7:0]        | Device page register                              | 0x00        |
| 0x08    | BQ7_N0_BYT1[7:0] | Programmable biquad 7, N0 coefficient byte[31:24] | 0x7F        |
| 0x09    | BQ7_N0_BYT2[7:0] | Programmable biquad 7, N0 coefficient byte[23:16] | 0xFF        |
| 0x0A    | BQ7_N0_BYT3[7:0] | Programmable biquad 7, N0 coefficient byte[15:8]  | 0xFF        |
| 0x0B    | BQ7_N0_BYT4[7:0] | Programmable biquad 7, N0 coefficient byte[7:0]   | 0xFF        |
| 0x0C    | BQ7_N1_BYT1[7:0] | Programmable biquad 7, N1 coefficient byte[31:24] | 0x00        |
| 0x0D    | BQ7_N1_BYT2[7:0] | Programmable biquad 7, N1 coefficient byte[23:16] | 0x00        |
| 0x0E    | BQ7_N1_BYT3[7:0] | Programmable biquad 7, N1 coefficient byte[15:8]  | 0x00        |
| 0x0F    | BQ7_N1_BYT4[7:0] | Programmable biquad 7, N1 coefficient byte[7:0]   | 0x00        |
| 0x10    | BQ7_N2_BYT1[7:0] | Programmable biquad 7, N2 coefficient byte[31:24] | 0x00        |
| 0x11    | BQ7_N2_BYT2[7:0] | Programmable biquad 7, N2 coefficient byte[23:16] | 0x00        |
| 0x12    | BQ7_N2_BYT3[7:0] | Programmable biquad 7, N2 coefficient byte[15:8]  | 0x00        |
| 0x13    | BQ7_N2_BYT4[7:0] | Programmable biquad 7, N2 coefficient byte[7:0]   | 0x00        |
| 0x14    | BQ7_D1_BYT1[7:0] | Programmable biquad 7, D1 coefficient byte[31:24] | 0x00        |
| 0x15    | BQ7_D1_BYT2[7:0] | Programmable biquad 7, D1 coefficient byte[23:16] | 0x00        |
| 0x16    | BQ7_D1_BYT3[7:0] | Programmable biquad 7, D1 coefficient byte[15:8]  | 0x00        |
| 0x17    | BQ7_D1_BYT4[7:0] | Programmable biquad 7, D1 coefficient byte[7:0]   | 0x00        |
| 0x18    | BQ7_D2_BYT1[7:0] | Programmable biquad 7, D2 coefficient byte[31:24] | 0x00        |
| 0x19    | BQ7_D2_BYT2[7:0] | Programmable biquad 7, D2 coefficient byte[23:16] | 0x00        |
| 0x1A    | BQ7_D2_BYT3[7:0] | Programmable biquad 7, D2 coefficient byte[15:8]  | 0x00        |
| 0x1B    | BQ7_D2_BYT4[7:0] | Programmable biquad 7, D2 coefficient byte[7:0]   | 0x00        |
| 0x1C    | BQ8_N0_BYT1[7:0] | Programmable biquad 8, N0 coefficient byte[31:24] | 0x7F        |
| 0x1D    | BQ8_N0_BYT2[7:0] | Programmable biquad 8, N0 coefficient byte[23:16] | 0xFF        |
| 0x1E    | BQ8_N0_BYT3[7:0] | Programmable biquad 8, N0 coefficient byte[15:8]  | 0xFF        |
| 0x1F    | BQ8_N0_BYT4[7:0] | Programmable biquad 8, N0 coefficient byte[7:0]   | 0xFF        |
| 0x20    | BQ8_N1_BYT1[7:0] | Programmable biquad 8, N1 coefficient byte[31:24] | 0x00        |
| 0x21    | BQ8_N1_BYT2[7:0] | Programmable biquad 8, N1 coefficient byte[23:16] | 0x00        |
| 0x22    | BQ8_N1_BYT3[7:0] | Programmable biquad 8, N1 coefficient byte[15:8]  | 0x00        |
| 0x23    | BQ8_N1_BYT4[7:0] | Programmable biquad 8, N1 coefficient byte[7:0]   | 0x00        |
| 0x24    | BQ8_N2_BYT1[7:0] | Programmable biquad 8, N2 coefficient byte[31:24] | 0x00        |
| 0x25    | BQ8_N2_BYT2[7:0] | Programmable biquad 8, N2 coefficient byte[23:16] | 0x00        |
| 0x26    | BQ8_N2_BYT3[7:0] | Programmable biquad 8, N2 coefficient byte[15:8]  | 0x00        |
| 0x27    | BQ8_N2_BYT4[7:0] | Programmable biquad 8, N2 coefficient byte[7:0]   | 0x00        |
| 0x28    | BQ8_D1_BYT1[7:0] | Programmable biquad 8, D1 coefficient byte[31:24] | 0x00        |
| 0x29    | BQ8_D1_BYT2[7:0] | Programmable biquad 8, D1 coefficient byte[23:16] | 0x00        |
| 0x2A    | BQ8_D1_BYT3[7:0] | Programmable biquad 8, D1 coefficient byte[15:8]  | 0x00        |
| 0x2B    | BQ8_D1_BYT4[7:0] | Programmable biquad 8, D1 coefficient byte[7:0]   | 0x00        |
| 0x2C    | BQ8_D2_BYT1[7:0] | Programmable biquad 8, D2 coefficient byte[31:24] | 0x00        |
| 0x2D    | BQ8_D2_BYT2[7:0] | Programmable biquad 8, D2 coefficient byte[23:16] | 0x00        |
| 0x2E    | BQ8_D2_BYT3[7:0] | Programmable biquad 8, D2 coefficient byte[15:8]  | 0x00        |
| 0x2F    | BQ8_D2_BYT4[7:0] | Programmable biquad 8, D2 coefficient byte[7:0]   | 0x00        |
| 0x30    | BQ9_N0_BYT1[7:0] | Programmable biquad 9, N0 coefficient byte[31:24] | 0x7F        |
| 0x31    | BQ9_N0_BYT2[7:0] | Programmable biquad 9, N0 coefficient byte[23:16] | 0xFF        |

表 7-62. Page 3 Programmable Coefficient Registers (続き)

| ADDRESS | ACRONYM           | REGISTER NAME                                      | RESET VALUE |
|---------|-------------------|--|-------------|
| 0x32    | BQ9_N0_BYT3[7:0]  | Programmable biquad 9, N0 coefficient byte[15:8]   | 0xFF        |
| 0x33    | BQ9_N0_BYT4[7:0]  | Programmable biquad 9, N0 coefficient byte[7:0]    | 0xFF        |
| 0x34    | BQ9_N1_BYT1[7:0]  | Programmable biquad 9, N1 coefficient byte[31:24]  | 0x00        |
| 0x35    | BQ9_N1_BYT2[7:0]  | Programmable biquad 9, N1 coefficient byte[23:16]  | 0x00        |
| 0x36    | BQ9_N1_BYT3[7:0]  | Programmable biquad 9, N1 coefficient byte[15:8]   | 0x00        |
| 0x37    | BQ9_N1_BYT4[7:0]  | Programmable biquad 9, N1 coefficient byte[7:0]    | 0x00        |
| 0x38    | BQ9_N2_BYT1[7:0]  | Programmable biquad 9, N2 coefficient byte[31:24]  | 0x00        |
| 0x39    | BQ9_N2_BYT2[7:0]  | Programmable biquad 9, N2 coefficient byte[23:16]  | 0x00        |
| 0x3A    | BQ9_N2_BYT3[7:0]  | Programmable biquad 9, N2 coefficient byte[15:8]   | 0x00        |
| 0x3B    | BQ9_N2_BYT4[7:0]  | Programmable biquad 9, N2 coefficient byte[7:0]    | 0x00        |
| 0x3C    | BQ9_D1_BYT1[7:0]  | Programmable biquad 9, D1 coefficient byte[31:24]  | 0x00        |
| 0x3D    | BQ9_D1_BYT2[7:0]  | Programmable biquad 9, D1 coefficient byte[23:16]  | 0x00        |
| 0x3E    | BQ9_D1_BYT3[7:0]  | Programmable biquad 9, D1 coefficient byte[15:8]   | 0x00        |
| 0x3F    | BQ9_D1_BYT4[7:0]  | Programmable biquad 9, D1 coefficient byte[7:0]    | 0x00        |
| 0x40    | BQ9_D2_BYT1[7:0]  | Programmable biquad 9, D2 coefficient byte[31:24]  | 0x00        |
| 0x41    | BQ9_D2_BYT2[7:0]  | Programmable biquad 9, D2 coefficient byte[23:16]  | 0x00        |
| 0x42    | BQ9_D2_BYT3[7:0]  | Programmable biquad 9, D2 coefficient byte[15:8]   | 0x00        |
| 0x43    | BQ9_D2_BYT4[7:0]  | Programmable biquad 9, D2 coefficient byte[7:0]    | 0x00        |
| 0x44    | BQ10_N0_BYT1[7:0] | Programmable biquad 10, N0 coefficient byte[31:24] | 0x7F        |
| 0x45    | BQ10_N0_BYT2[7:0] | Programmable biquad 10, N0 coefficient byte[23:16] | 0xFF        |
| 0x46    | BQ10_N0_BYT3[7:0] | Programmable biquad 10, N0 coefficient byte[15:8]  | 0xFF        |
| 0x47    | BQ10_N0_BYT4[7:0] | Programmable biquad 10, N0 coefficient byte[7:0]   | 0xFF        |
| 0x48    | BQ10_N1_BYT1[7:0] | Programmable biquad 10, N1 coefficient byte[31:24] | 0x00        |
| 0x49    | BQ10_N1_BYT2[7:0] | Programmable biquad 10, N1 coefficient byte[23:16] | 0x00        |
| 0x4A    | BQ10_N1_BYT3[7:0] | Programmable biquad 10, N1 coefficient byte[15:8]  | 0x00        |
| 0x4B    | BQ10_N1_BYT4[7:0] | Programmable biquad 10, N1 coefficient byte[7:0]   | 0x00        |
| 0x4C    | BQ10_N2_BYT1[7:0] | Programmable biquad 10, N2 coefficient byte[31:24] | 0x00        |
| 0x4D    | BQ10_N2_BYT2[7:0] | Programmable biquad 10, N2 coefficient byte[23:16] | 0x00        |
| 0x4E    | BQ10_N2_BYT3[7:0] | Programmable biquad 10, N2 coefficient byte[15:8]  | 0x00        |
| 0x4F    | BQ10_N2_BYT4[7:0] | Programmable biquad 10, N2 coefficient byte[7:0]   | 0x00        |
| 0x50    | BQ10_D1_BYT1[7:0] | Programmable biquad 10, D1 coefficient byte[31:24] | 0x00        |
| 0x51    | BQ10_D1_BYT2[7:0] | Programmable biquad 10, D1 coefficient byte[23:16] | 0x00        |
| 0x52    | BQ10_D1_BYT3[7:0] | Programmable biquad 10, D1 coefficient byte[15:8]  | 0x00        |
| 0x53    | BQ10_D1_BYT4[7:0] | Programmable biquad 10, D1 coefficient byte[7:0]   | 0x00        |
| 0x54    | BQ10_D2_BYT1[7:0] | Programmable biquad 10, D2 coefficient byte[31:24] | 0x00        |
| 0x55    | BQ10_D2_BYT2[7:0] | Programmable biquad 10, D2 coefficient byte[23:16] | 0x00        |
| 0x56    | BQ10_D2_BYT3[7:0] | Programmable biquad 10, D2 coefficient byte[15:8]  | 0x00        |
| 0x57    | BQ10_D2_BYT4[7:0] | Programmable biquad 10, D2 coefficient byte[7:0]   | 0x00        |
| 0x58    | BQ11_N0_BYT1[7:0] | Programmable biquad 11, N0 coefficient byte[31:24] | 0x7F        |
| 0x59    | BQ11_N0_BYT2[7:0] | Programmable biquad 11, N0 coefficient byte[23:16] | 0xFF        |
| 0x5A    | BQ11_N0_BYT3[7:0] | Programmable biquad 11, N0 coefficient byte[15:8]  | 0xFF        |
| 0x5B    | BQ11_N0_BYT4[7:0] | Programmable biquad 11, N0 coefficient byte[7:0]   | 0xFF        |
| 0x5C    | BQ11_N1_BYT1[7:0] | Programmable biquad 11, N1 coefficient byte[31:24] | 0x00        |
| 0x5D    | BQ11_N1_BYT2[7:0] | Programmable biquad 11, N1 coefficient byte[23:16] | 0x00        |
| 0x5E    | BQ11_N1_BYT3[7:0] | Programmable biquad 11, N1 coefficient byte[15:8]  | 0x00        |
| 0x5F    | BQ11_N1_BYT4[7:0] | Programmable biquad 11, N1 coefficient byte[7:0]   | 0x00        |
| 0x60    | BQ11_N2_BYT1[7:0] | Programmable biquad 11, N2 coefficient byte[31:24] | 0x00        |
| 0x61    | BQ11_N2_BYT2[7:0] | Programmable biquad 11, N2 coefficient byte[23:16] | 0x00        |
| 0x62    | BQ11_N2_BYT3[7:0] | Programmable biquad 11, N2 coefficient byte[15:8]  | 0x00        |

**表 7-62. Page 3 Programmable Coefficient Registers (続き)**

| ADDRESS | ACRONYM           | REGISTER NAME                                      | RESET VALUE |
|---------|-------------------|--|-------------|
| 0x63    | BQ11_N2_BYT4[7:0] | Programmable biquad 11, N2 coefficient byte[7:0]   | 0x00        |
| 0x64    | BQ11_D1_BYT1[7:0] | Programmable biquad 11, D1 coefficient byte[31:24] | 0x00        |
| 0x65    | BQ11_D1_BYT2[7:0] | Programmable biquad 11, D1 coefficient byte[23:16] | 0x00        |
| 0x66    | BQ11_D1_BYT3[7:0] | Programmable biquad 11, D1 coefficient byte[15:8]  | 0x00        |
| 0x67    | BQ11_D1_BYT4[7:0] | Programmable biquad 11, D1 coefficient byte[7:0]   | 0x00        |
| 0x68    | BQ11_D2_BYT1[7:0] | Programmable biquad 11, D2 coefficient byte[31:24] | 0x00        |
| 0x69    | BQ11_D2_BYT2[7:0] | Programmable biquad 11, D2 coefficient byte[23:16] | 0x00        |
| 0x6A    | BQ11_D2_BYT3[7:0] | Programmable biquad 11, D2 coefficient byte[15:8]  | 0x00        |
| 0x6B    | BQ11_D2_BYT4[7:0] | Programmable biquad 11, D2 coefficient byte[7:0]   | 0x00        |
| 0x6C    | BQ12_N0_BYT1[7:0] | Programmable biquad 12, N0 coefficient byte[31:24] | 0x7F        |
| 0x6D    | BQ12_N0_BYT2[7:0] | Programmable biquad 12, N0 coefficient byte[23:16] | 0xFF        |
| 0x6E    | BQ12_N0_BYT3[7:0] | Programmable biquad 12, N0 coefficient byte[15:8]  | 0xFF        |
| 0x6F    | BQ12_N0_BYT4[7:0] | Programmable biquad 12, N0 coefficient byte[7:0]   | 0xFF        |
| 0x70    | BQ12_N1_BYT1[7:0] | Programmable biquad 12, N1 coefficient byte[31:24] | 0x00        |
| 0x71    | BQ12_N1_BYT2[7:0] | Programmable biquad 12, N1 coefficient byte[23:16] | 0x00        |
| 0x72    | BQ12_N1_BYT3[7:0] | Programmable biquad 12, N1 coefficient byte[15:8]  | 0x00        |
| 0x73    | BQ12_N1_BYT4[7:0] | Programmable biquad 12, N1 coefficient byte[7:0]   | 0x00        |
| 0x74    | BQ12_N2_BYT1[7:0] | Programmable biquad 12, N2 coefficient byte[31:24] | 0x00        |
| 0x75    | BQ12_N2_BYT2[7:0] | Programmable biquad 12, N2 coefficient byte[23:16] | 0x00        |
| 0x76    | BQ12_N2_BYT3[7:0] | Programmable biquad 12, N2 coefficient byte[15:8]  | 0x00        |
| 0x77    | BQ12_N2_BYT4[7:0] | Programmable biquad 12, N2 coefficient byte[7:0]   | 0x00        |
| 0x78    | BQ12_D1_BYT1[7:0] | Programmable biquad 12, D1 coefficient byte[31:24] | 0x00        |
| 0x79    | BQ12_D1_BYT2[7:0] | Programmable biquad 12, D1 coefficient byte[23:16] | 0x00        |
| 0x7A    | BQ12_D1_BYT3[7:0] | Programmable biquad 12, D1 coefficient byte[15:8]  | 0x00        |
| 0x7B    | BQ12_D1_BYT4[7:0] | Programmable biquad 12, D1 coefficient byte[7:0]   | 0x00        |
| 0x7C    | BQ12_D2_BYT1[7:0] | Programmable biquad 12, D2 coefficient byte[31:24] | 0x00        |
| 0x7D    | BQ12_D2_BYT2[7:0] | Programmable biquad 12, D2 coefficient byte[23:16] | 0x00        |
| 0x7E    | BQ12_D2_BYT3[7:0] | Programmable biquad 12, D2 coefficient byte[15:8]  | 0x00        |
| 0x7F    | BQ12_D2_BYT4[7:0] | Programmable biquad 12, D2 coefficient byte[7:0]   | 0x00        |



### 7.4.3 Programmable Coefficient Registers: Page 4

This register page (shown in 表 7-63) consists of the programmable coefficients for mixer 1 to mixer 4 and the first-order IIR filter.

**表 7-63. Page 4 Programmable Coefficient Registers**

| ADDRESS | ACRONYM            | REGISTER NAME                                      | RESET VALUE |
|---------|--------------------|--|-------------|
| 0x00    | PAGE[7:0]          | Device page register                               | 0x00        |
| 0x08    | MIX1_CH1_BYT1[7:0] | Digital mixer 1, channel 1 coefficient byte[31:24] | 0x7F        |
| 0x09    | MIX1_CH1_BYT2[7:0] | Digital mixer 1, channel 1 coefficient byte[23:16] | 0xFF        |
| 0x0A    | MIX1_CH1_BYT3[7:0] | Digital mixer 1, channel 1 coefficient byte[15:8]  | 0xFF        |
| 0x0B    | MIX1_CH1_BYT4[7:0] | Digital mixer 1, channel 1 coefficient byte[7:0]   | 0xFF        |
| 0x0C    | MIX1_CH2_BYT1[7:0] | Digital mixer 1, channel 2 coefficient byte[31:24] | 0x00        |
| 0x0D    | MIX1_CH2_BYT2[7:0] | Digital mixer 1, channel 2 coefficient byte[23:16] | 0x00        |
| 0x0E    | MIX1_CH2_BYT3[7:0] | Digital mixer 1, channel 2 coefficient byte[15:8]  | 0x00        |
| 0x0F    | MIX1_CH2_BYT4[7:0] | Digital mixer 1, channel 2 coefficient byte[7:0]   | 0x00        |
| 0x10    | MIX1_CH3_BYT1[7:0] | Digital mixer 1, channel 3 coefficient byte[31:24] | 0x00        |
| 0x11    | MIX1_CH3_BYT2[7:0] | Digital mixer 1, channel 3 coefficient byte[23:16] | 0x00        |
| 0x12    | MIX1_CH3_BYT3[7:0] | Digital mixer 1, channel 3 coefficient byte[15:8]  | 0x00        |
| 0x13    | MIX1_CH3_BYT4[7:0] | Digital mixer 1, channel 3 coefficient byte[7:0]   | 0x00        |
| 0x14    | MIX1_CH4_BYT1[7:0] | Digital mixer 1, channel 4 coefficient byte[31:24] | 0x00        |
| 0x15    | MIX1_CH4_BYT2[7:0] | Digital mixer 1, channel 4 coefficient byte[23:16] | 0x00        |
| 0x16    | MIX1_CH4_BYT3[7:0] | Digital mixer 1, channel 4 coefficient byte[15:8]  | 0x00        |
| 0x17    | MIX1_CH4_BYT4[7:0] | Digital mixer 1, channel 4 coefficient byte[7:0]   | 0x00        |
| 0x18    | MIX2_CH1_BYT1[7:0] | Digital mixer 2, channel 1 coefficient byte[31:24] | 0x00        |
| 0x19    | MIX2_CH1_BYT2[7:0] | Digital mixer 2, channel 1 coefficient byte[23:16] | 0x00        |
| 0x1A    | MIX2_CH1_BYT3[7:0] | Digital mixer 2, channel 1 coefficient byte[15:8]  | 0x00        |
| 0x1B    | MIX2_CH1_BYT4[7:0] | Digital mixer 2, channel 1 coefficient byte[7:0]   | 0x00        |
| 0x1C    | MIX2_CH2_BYT1[7:0] | Digital mixer 2, channel 2 coefficient byte[31:24] | 0x7F        |
| 0x1D    | MIX2_CH2_BYT2[7:0] | Digital mixer 2, channel 2 coefficient byte[23:16] | 0xFF        |
| 0x1E    | MIX2_CH2_BYT3[7:0] | Digital mixer 2, channel 2 coefficient byte[15:8]  | 0xFF        |
| 0x1F    | MIX2_CH2_BYT4[7:0] | Digital mixer 2, channel 2 coefficient byte[7:0]   | 0xFF        |
| 0x20    | MIX2_CH3_BYT1[7:0] | Digital mixer 2, channel 3 coefficient byte[31:24] | 0x00        |
| 0x21    | MIX2_CH3_BYT2[7:0] | Digital mixer 2, channel 3 coefficient byte[23:16] | 0x00        |
| 0x22    | MIX2_CH3_BYT3[7:0] | Digital mixer 2, channel 3 coefficient byte[15:8]  | 0x00        |
| 0x23    | MIX2_CH3_BYT4[7:0] | Digital mixer 2, channel 3 coefficient byte[7:0]   | 0x00        |
| 0x24    | MIX2_CH4_BYT1[7:0] | Digital mixer 2, channel 4 coefficient byte[31:24] | 0x00        |
| 0x25    | MIX2_CH4_BYT2[7:0] | Digital mixer 2, channel 4 coefficient byte[23:16] | 0x00        |
| 0x26    | MIX2_CH4_BYT3[7:0] | Digital mixer 2, channel 4 coefficient byte[15:8]  | 0x00        |
| 0x27    | MIX2_CH4_BYT4[7:0] | Digital mixer 2, channel 4 coefficient byte[7:0]   | 0x00        |
| 0x28    | MIX3_CH1_BYT1[7:0] | Digital mixer 3, channel 1 coefficient byte[31:24] | 0x00        |
| 0x29    | MIX3_CH1_BYT2[7:0] | Digital mixer 3, channel 1 coefficient byte[23:16] | 0x00        |
| 0x2A    | MIX3_CH1_BYT3[7:0] | Digital mixer 3, channel 1 coefficient byte[15:8]  | 0x00        |
| 0x2B    | MIX3_CH1_BYT4[7:0] | Digital mixer 3, channel 1 coefficient byte[7:0]   | 0x00        |
| 0x2C    | MIX3_CH2_BYT1[7:0] | Digital mixer 3, channel 2 coefficient byte[31:24] | 0x00        |
| 0x2D    | MIX3_CH2_BYT2[7:0] | Digital mixer 3, channel 2 coefficient byte[23:16] | 0x00        |
| 0x2E    | MIX3_CH2_BYT3[7:0] | Digital mixer 3, channel 2 coefficient byte[15:8]  | 0x00        |
| 0x2F    | MIX3_CH2_BYT4[7:0] | Digital mixer 3, channel 2 coefficient byte[7:0]   | 0x00        |
| 0x30    | MIX3_CH3_BYT1[7:0] | Digital mixer 3, channel 3 coefficient byte[31:24] | 0x7F        |
| 0x31    | MIX3_CH3_BYT2[7:0] | Digital mixer 3, channel 3 coefficient byte[23:16] | 0xFF        |
| 0x32    | MIX3_CH3_BYT3[7:0] | Digital mixer 3, channel 3 coefficient byte[15:8]  | 0xFF        |
| 0x33    | MIX3_CH3_BYT4[7:0] | Digital mixer 3, channel 3 coefficient byte[7:0]   | 0xFF        |



**表 7-63. Page 4 Programmable Coefficient Registers (続き)**

| ADDRESS | ACRONYM            | REGISTER NAME  | RESET VALUE |
|---------|--------------------|--|-------------|
| 0x34    | MIX3_CH4_BYT1[7:0] | Digital mixer 3, channel 4 coefficient byte[31:24]       | 0x00        |
| 0x35    | MIX3_CH4_BYT2[7:0] | Digital mixer 3, channel 4 coefficient byte[23:16]       | 0x00        |
| 0x36    | MIX3_CH4_BYT3[7:0] | Digital mixer 3, channel 4 coefficient byte[15:8]        | 0x00        |
| 0x37    | MIX3_CH4_BYT4[7:0] | Digital mixer 3, channel 4 coefficient byte[7:0]         | 0x00        |
| 0x38    | MIX4_CH1_BYT1[7:0] | Digital mixer 4, channel 1 coefficient byte[31:24]       | 0x00        |
| 0x39    | MIX4_CH1_BYT2[7:0] | Digital mixer 4, channel 1 coefficient byte[23:16]       | 0x00        |
| 0x3A    | MIX4_CH1_BYT3[7:0] | Digital mixer 4, channel 1 coefficient byte[15:8]        | 0x00        |
| 0x3B    | MIX4_CH1_BYT4[7:0] | Digital mixer 4, channel 1 coefficient byte[7:0]         | 0x00        |
| 0x3C    | MIX4_CH2_BYT1[7:0] | Digital mixer 4, channel 2 coefficient byte[31:24]       | 0x00        |
| 0x3D    | MIX4_CH2_BYT2[7:0] | Digital mixer 4, channel 2 coefficient byte[23:16]       | 0x00        |
| 0x3E    | MIX4_CH2_BYT3[7:0] | Digital mixer 4, channel 2 coefficient byte[15:8]        | 0x00        |
| 0x3F    | MIX4_CH2_BYT4[7:0] | Digital mixer 4, channel 2 coefficient byte[7:0]         | 0x00        |
| 0x40    | MIX4_CH3_BYT1[7:0] | Digital mixer 4, channel 3 coefficient byte[31:24]       | 0x00        |
| 0x41    | MIX4_CH3_BYT2[7:0] | Digital mixer 4, channel 3 coefficient byte[23:16]       | 0x00        |
| 0x42    | MIX4_CH3_BYT3[7:0] | Digital mixer 4, channel 3 coefficient byte[15:8]        | 0x00        |
| 0x43    | MIX4_CH3_BYT4[7:0] | Digital mixer 4, channel 3 coefficient byte[7:0]         | 0x00        |
| 0x44    | MIX4_CH4_BYT1[7:0] | Digital mixer 4, channel 4 coefficient byte[31:24]       | 0x7F        |
| 0x45    | MIX4_CH4_BYT2[7:0] | Digital mixer 4, channel 4 coefficient byte[23:16]       | 0xFF        |
| 0x46    | MIX4_CH4_BYT3[7:0] | Digital mixer 4, channel 4 coefficient byte[15:8]        | 0xFF        |
| 0x47    | MIX4_CH4_BYT4[7:0] | Digital mixer 4, channel 4 coefficient byte[7:0]         | 0xFF        |
| 0x48    | IIR_N0_BYT1[7:0]   | Programmable first-order IIR, N0 coefficient byte[31:24] | 0x7F        |
| 0x49    | IIR_N0_BYT2[7:0]   | Programmable first-order IIR, N0 coefficient byte[23:16] | 0xFF        |
| 0x4A    | IIR_N0_BYT3[7:0]   | Programmable first-order IIR, N0 coefficient byte[15:8]  | 0xFF        |
| 0x4B    | IIR_N0_BYT4[7:0]   | Programmable first-order IIR, N0 coefficient byte[7:0]   | 0xFF        |
| 0x4C    | IIR_N1_BYT1[7:0]   | Programmable first-order IIR, N1 coefficient byte[31:24] | 0x00        |
| 0x4D    | IIR_N1_BYT2[7:0]   | Programmable first-order IIR, N1 coefficient byte[23:16] | 0x00        |
| 0x4E    | IIR_N1_BYT3[7:0]   | Programmable first-order IIR, N1 coefficient byte[15:8]  | 0x00        |
| 0x4F    | IIR_N1_BYT4[7:0]   | Programmable first-order IIR, N1 coefficient byte[7:0]   | 0x00        |
| 0x50    | IIR_D1_BYT1[7:0]   | Programmable first-order IIR, D1 coefficient byte[31:24] | 0x00        |
| 0x51    | IIR_D1_BYT2[7:0]   | Programmable first-order IIR, D1 coefficient byte[23:16] | 0x00        |
| 0x52    | IIR_D1_BYT3[7:0]   | Programmable first-order IIR, D1 coefficient byte[15:8]  | 0x00        |
| 0x53    | IIR_D1_BYT4[7:0]   | Programmable first-order IIR, D1 coefficient byte[7:0]   | 0x00        |

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The TAA3020 is a multichannel, high-performance audio analog-to-digital converter (ADC) that supports output sample rates of up to 768 kHz. The device supports either up to two analog microphones or up to four digital pulse density modulation (PDM) microphones for simultaneous recording applications.

Communication to the TAA3020 for configuration of the control registers is supported using an I<sup>2</sup>C interface. The device supports a highly flexible, audio serial interface (TDM, I<sup>2</sup>S, and LJ) to transmit audio data seamlessly in the system across devices.

### 8.2 Typical Applications

#### 8.2.1 Two-Channel Analog Microphone Recording

図 8-1 shows a typical configuration of the TAA3020 for an application using two analog microelectrical-mechanical system (MEMS) microphones for simultaneous recording operation with an I<sup>2</sup>C control interface and a time-division multiplexing (TDM) audio data slave interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

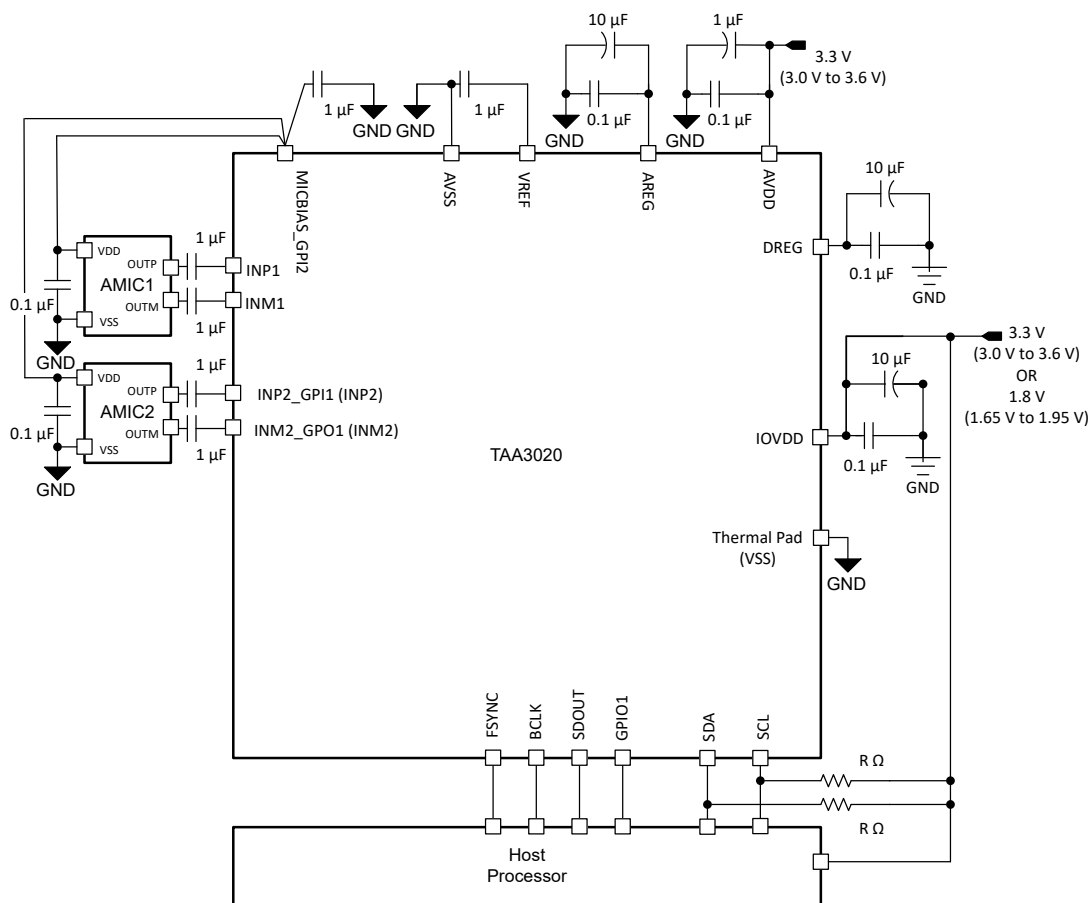


図 8-1. Two-Channel Analog Microphone Recording Diagram

### 8.2.1.1 Design Requirements

表 8-1 lists the design parameters for this application.

**表 8-1. Design Parameters**

| KEY PARAMETER                   | SPECIFICATION  |
|---------------------------------|--|
| AVDD                            | 3.3 V  |
| AVDD supply current consumption | >14 mA (PLL on, two-channel recording, $f_s = 48$ kHz) |
| IOVDD                           | 1.8 V or 3.3 V   |
| Maximum MICBIAS current         | 5 mA (MICBIAS voltage is the same as AVDD)             |

### 8.2.1.2 Detailed Design Procedure

This section describes the necessary steps to configure the TAA3020 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
  - a. Power-up the IOVDD and AVDD power supplies
  - b. Wait for at least 1 ms to allow the device to initialize the internal registers initialization
  - c. The device now goes into sleep mode (low-power mode < 10  $\mu$ A)
2. Transition from sleep mode to active mode whenever required for the recording operation:
  - a. Wake up the device by writing to P0\_R2 to disable sleep mode
  - b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
  - c. Override default configuration registers or programmable coefficients value as required (this step is optional)
  - d. Enable all desired input channels by writing to P0\_R115
  - e. Enable all desired audio serial interface output channels by writing to P0\_R116
  - f. Power-up the ADC, MICBIAS, and PLL by writing to P0\_R117
  - g. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio  
 This specific step can be done at any point in the sequence after step a.  
 See the [Phase-Locked Loop \(PLL\) and Clock Generation](#) section for supported sample rates and the BCLK to FSYNC ratio.
  - h. The device recording data are now sent to the host processor via the TDM audio serial data bus
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
  - a. Enter sleep mode by writing to P0\_R2 to enable sleep mode
  - b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
  - c. Read P0\_R119 to check the device shutdown and sleep mode status
  - d. If the device P0\_R119\_D7 status bit is 1'b1 then stop FSYNC and BCLK in the system
  - e. The device now goes into sleep mode (low-power mode < 10  $\mu$ A) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
  - a. Wake up the device by writing to P0\_R2 to disable sleep mode
  - b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
  - c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
  - d. The device recording data are now sent to the host processor via the TDM audio serial data bus
5. Repeat step 2 to step 4 as required for configuration changes or step 3 to step 4 for mode transitions

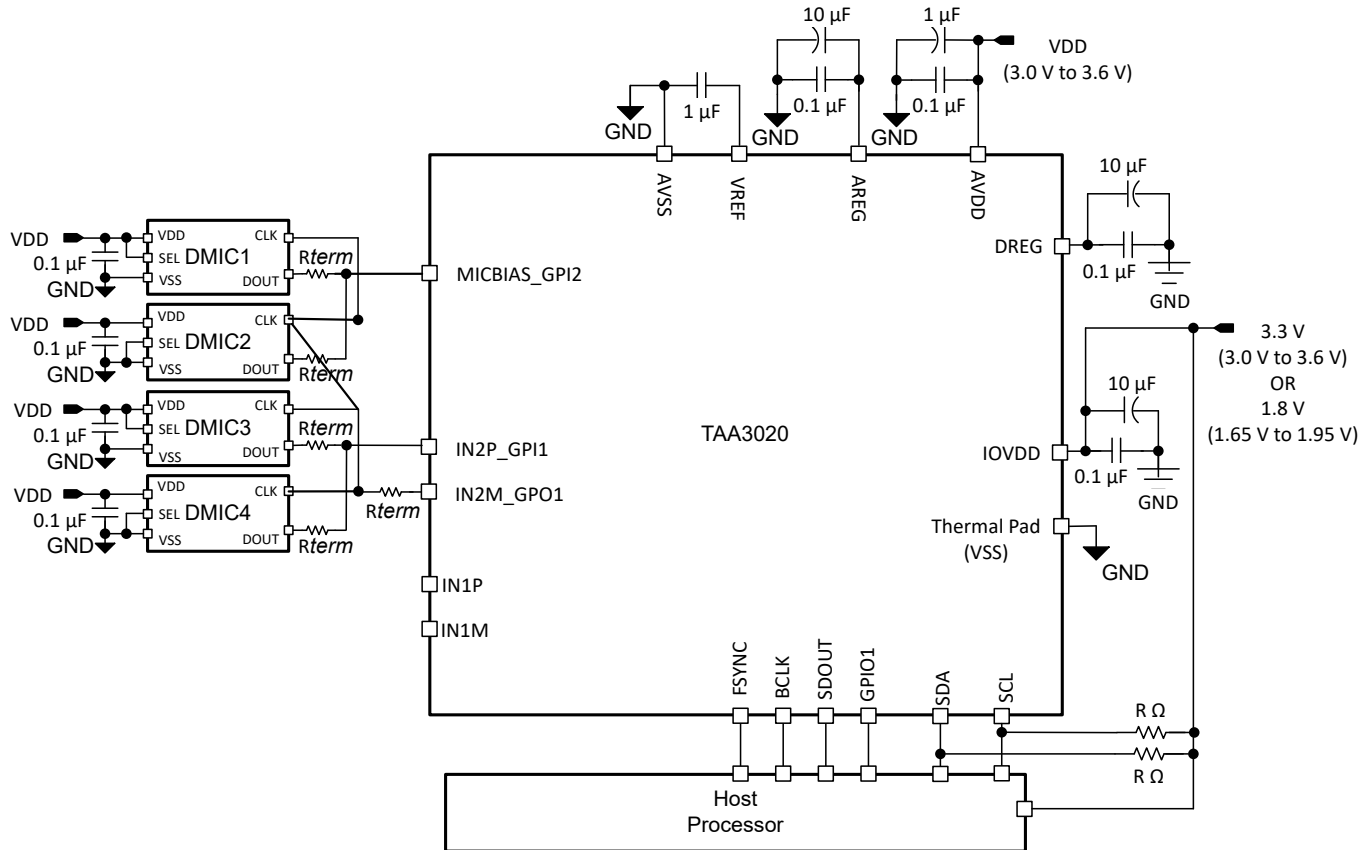
### 8.2.1.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I<sup>2</sup>C register control script that shows how to set up the TAA3020 in a two-channel analog microphone recording mode with differential inputs.

```
# Key: w 9C XX YY ==> write to I2C address 0x9C, to register 0xXX, data 0xYY
#           # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. There are
# other valid sequences depending on which features are used.
#
# See the TAA3020EVM user guide for jumper settings and audio connections.
#
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 44.1 kHz (output data sample rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#####
#
# Power-up the IOVDD and AVDD power supplies
# Wait for the IOVDD and AVDD power supplies to settle to a steady-state operating voltage range.
# Wait for 1 ms.
#
# Wake-up the device with an I2C write into P0_R2 using an internal AREG
w 9C 02 81
#
# Enable input Ch-1 and Ch-2 by an I2C write into P0_R115
w 9C 73 C0
#
# Enable ASI output Ch-1 and Ch-2 slots by an I2C write into P0_R116
w 9C 74 C0
#
# Power-up the ADC, MICBIAS, and PLL by an I2C write into P0_R117
w 9C 75 E0
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data via the host on the ASI bus with a TDM protocol 32-bits channel wordlength
```

## 8.2.2 Four-Channel Digital PDM Microphone Recording

Figure 8-2 shows a typical configuration of the TAA3020 for an application using four digital PDM MEMS microphones with simultaneous recording operation using an I<sup>2</sup>C control interface and the TDM audio data slave interface. If the MICBIAS output is not used in the system then the 1  $\mu$ F capacitor for the MICBIAS pin is not must.



**Figure 8-2. Four-Channel Digital PDM Microphone Recording Diagram**

### 8.2.2.1 Design Requirements

Table 8-2 lists the design parameters for this application.

**Table 8-2. Design Parameters**

| KEY PARAMETER                   | SPECIFICATION  |
|---------------------------------|--|
| AVDD                            | 3.3 V  |
| AVDD supply current consumption | >8 mA (PLL on, four-channel recording, $f_s = 48$ kHz) |
| IOVDD                           | 1.8 V or 3.3 V   |

### 8.2.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the TAA3020 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
  - a. Power up the IOVDD and AVDD power supplies
  - b. Wait for at least 1 ms to allow the device to initialize the internal registers initialization
  - c. The device now goes into sleep mode (low-power mode < 10  $\mu$ A)
2. Transition from sleep mode to active mode whenever required for the recording operation:
  - a. Wake up the device by writing to P0\_R2 to disable sleep mode
  - b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
  - c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
  - d. Configure channel 1 to channel 2 (CHx\_INSRC) for the digital microphone as the input source for recording
  - e. Configure GPO1 (GPO1\_CFG) and GPIO1 (GPIO1\_CFG) as the PDMCLK output
  - f. Configure GPIx (GPI1x\_CFG) as PDMDINx
  - g. Enable all desired input channels by writing to P0\_R115
  - h. Enable all desired audio serial interface output channels by writing to P0\_R116
  - i. Power-up the ADC and PLL by writing to P0\_R117
  - j. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

This specific step can be done at any point in the sequence after step a.

See the [Phase-Locked Loop \(PLL\) and Clock Generation](#) section for supported sample rates and the BCLK to FSYNC ratio.

- k. The device recording data is now sent to the host processor using the TDM audio serial data bus
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
  - a. Enter sleep mode by writing to P0\_R2 to enable sleep mode
  - b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
  - c. Read P0\_R119 to check the device shutdown and sleep mode status
  - d. If the device P0\_R119\_D7 status bit is 1'b1 then stop FSYNC and BCLK in the system
  - e. The device now goes into sleep mode (low-power mode < 10  $\mu$ A) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
  - a. Wake up the device by writing to P0\_R2 to disable sleep mode
  - b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
  - c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
  - d. The device recording data are now sent to the host processor using the TDM audio serial data bus
5. Repeat step 3 and step 4 as required for mode transitions and step 2 to step 4 for configuration changes

### 8.2.2.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I<sup>2</sup>C register control script that shows how to set up the TAA3020 in a four-channel digital PDM microphone recording mode.

```
# Key: w 9C XX YY ==> write to I2C address 0x9C, to register 0xXX, data 0xYY
#           # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. There are
# other valid sequences depending on which features are used.
#
# See the TAA3020EVM user guide for jumper settings and audio connections.
#
# PDM 4-channel : PDMDIN1 - Ch1 and Ch2, PDMDIN2 - Ch3 and Ch4
#
# FSYNC = 44.1 kHz (output data sample rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#####
#
# Power-up the IOVDD and AVDD power supplies
# Wait for the IOVDD and AVDD power supplies to settle to a steady state operating voltage range.
# Wait for 1 ms.
#
# Wake-up the device by an I2C write into P0_R2 using an internal AREG
w 9C 02 81
#
# Configure CH2_INSRC as a digital PDM input by an I2C write into P0_R65
w 9C 41 40
#
# Configure MICBIAS_GPI2 as a digital PDM input by an I2C write into P0_R59
w 9C 3B 70
#
# Configure GP01 as PDMCLK by an I2C write into P0_R34
w 9C 22 41
#
# Configure GPI1 and GPI2 as PDMDIN1 and PDMDIN2 by an I2C write into P0_R43
w 9C 2B 45
#
# Enable input Ch-1 to Ch-4 by an I2C write into P0_R115
w 9C 73 F0
#
# Enable ASI output Ch-1 to Ch-4 slots by an I2C write into P0_R116
w 9C 74 F0
#
# Power-up the ADC and PLL by an I2C write into P0_R117
w 9C 75 60
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data via the host on the ASI bus with a TDM protocol 32-bits channel wordlength
```

### 8.3 What to Do and What Not to Do

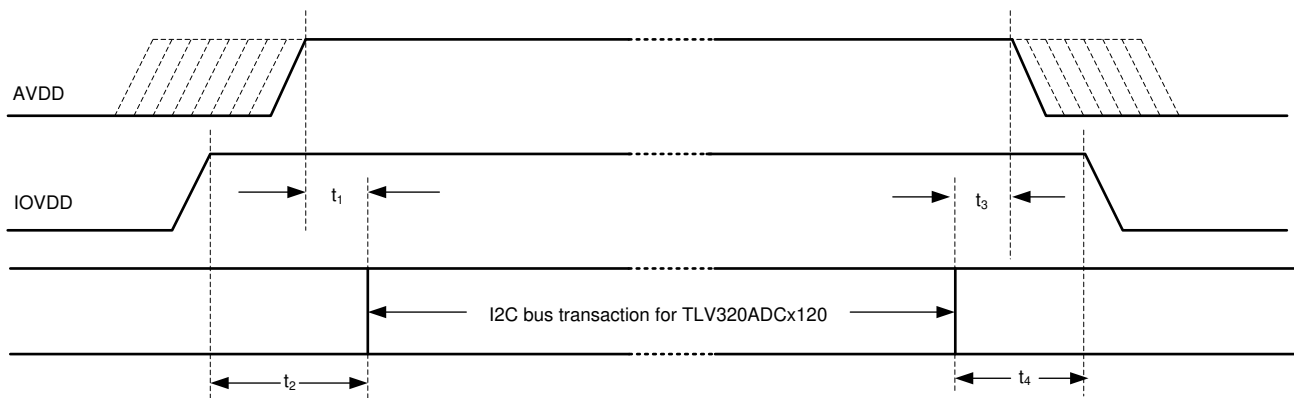
In the VAD mode of operation, there are some limitations on interrupt generation when auto wake up is enabled. For details about these limitations, see the [Using the Voice Activity Detector \(VAD\) in the TLV320ADC5120 and TLV320ADC6120 application report](#).

The automatic gain controller (AGC) feature has some limitation when using sampling rates lower than 44.1 kHz. For further details about this limitation, see the [Using the Automatic Gain Controller \(AGC\) in TLV320ADCx120 Family application report](#).

### 8.4 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all supplies are stable, then only initiate the I<sup>2</sup>C transactions to initialize the device.

For the supply power-up requirement,  $t_1$  and  $t_2$  must be at least 2 ms to allow the device to initialize the internal registers. See the [セクション 6.4](#) section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement,  $t_3$  and  $t_4$  must be at least 10 ms. This timing (as shown in [図 8-3](#)) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.



**図 8-3. Power-Supply Sequencing Requirement Timing Diagram**

Make sure that the supply ramp rate is slower than 1 V/ $\mu$ s and that the wait time between a power-down and a power-up event is at least 100 ms. For supply ramp rate slower than 0.1 V/ms, host device must apply a software reset as first transaction before doing any device configuration. Make sure all digital input pins are at valid input levels and not toggling during supply sequencing.

The TAA3020 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG. However, if the AVDD voltage is less than 1.98 V in the system, then short the AREG and AVDD pins onboard and do not enable the internal AREG by keeping the AREG\_SELECT bit to 1b'0 (default value) of P0\_R2. If the AVDD supply used in the system is higher than 2.7 V, then the host device can set AREG\_SELECT to 1'b1 while exiting sleep mode to allow the device internal regulator to generate the AREG supply.

### 8.5 Layout

#### 8.5.1 Layout Guidelines

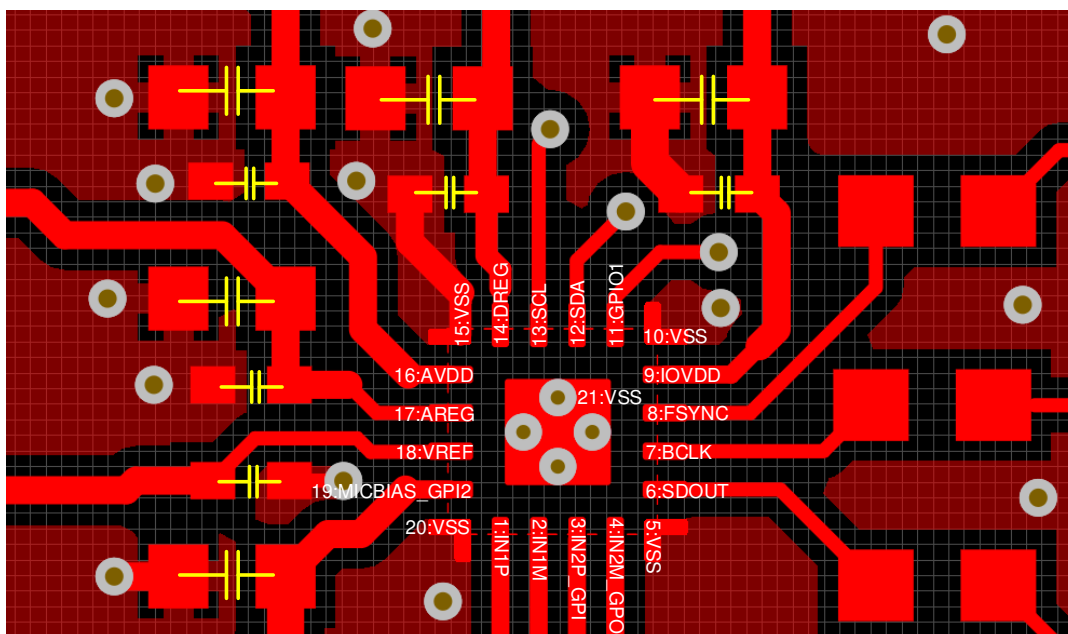
Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.



- The decoupling capacitors for the power supplies must be placed close to the device pins.
- The supply decoupling capacitors must be used ceramic type with low ESR.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

### 8.5.2 Layout Example



8-4. Layout Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 9.4 Trademarks

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### 9.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| November 2024 | *        | Initial Release |

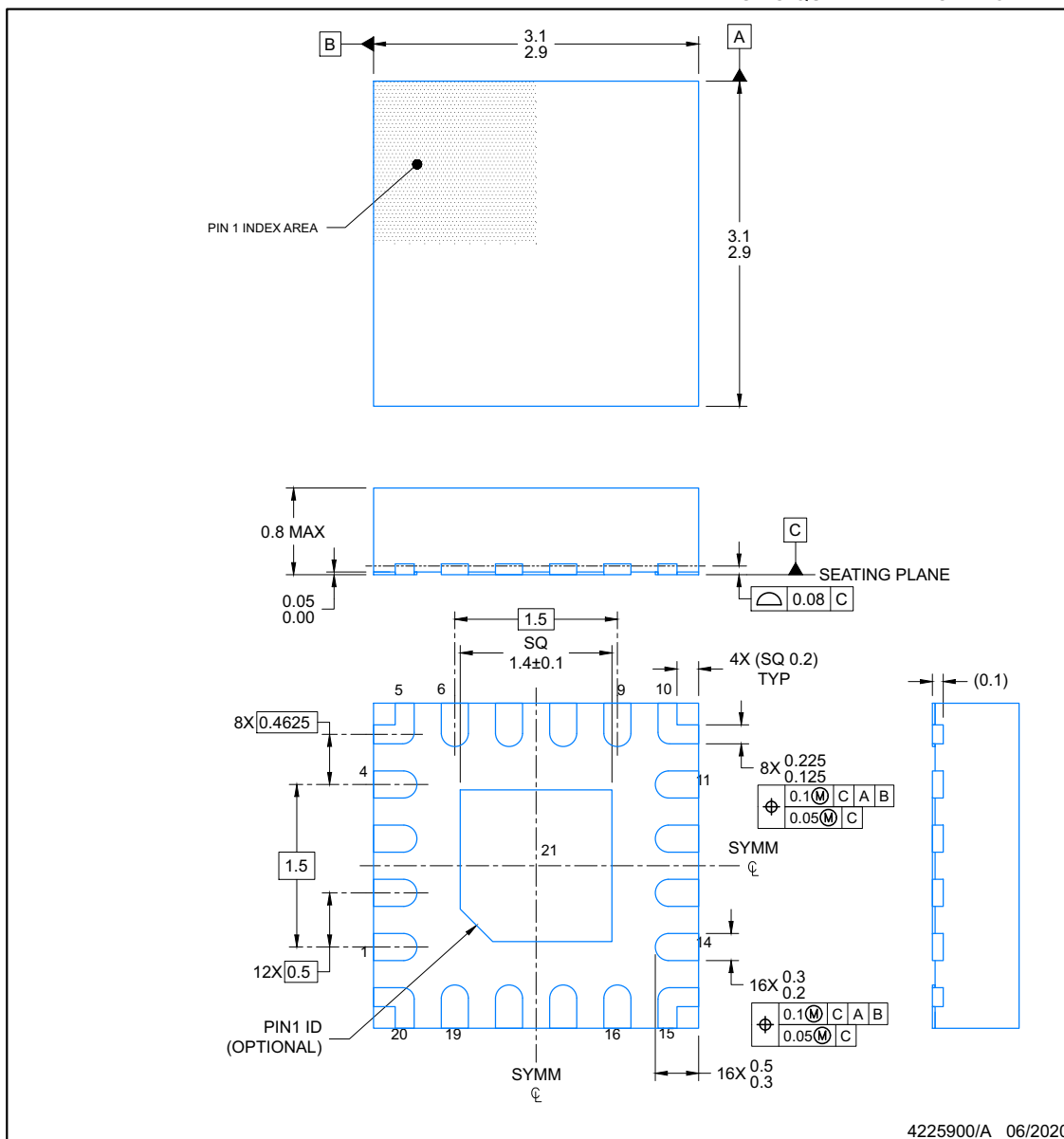
## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## RTE0020A

## PACKAGE OUTLINE WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

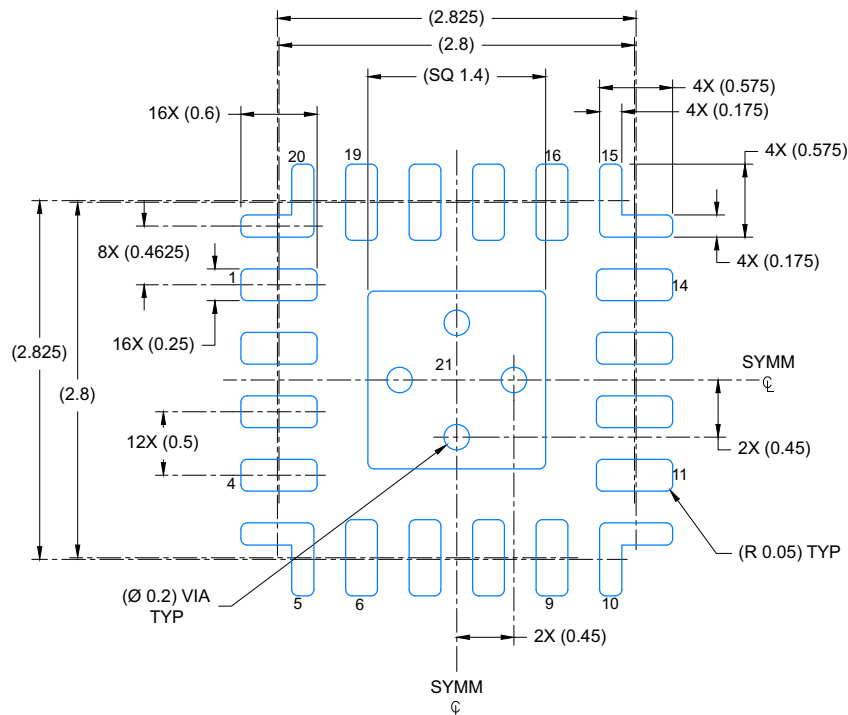


### NOTES:

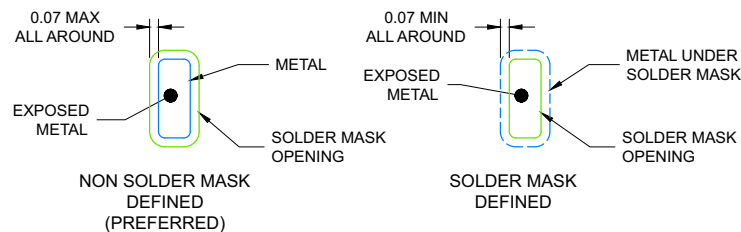
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT****WQFN - 0.8 mm max height****RTE0020A**

PLASTIC QUAD FLATPACK- NO LEAD



**LAND PATTERN EXAMPLE**  
 EXPOSED METAL SHOWN  
 SCALE: 20X

**SOLDER MASK DETAILS**

4225900/A 06/2020

NOTES: (continued)

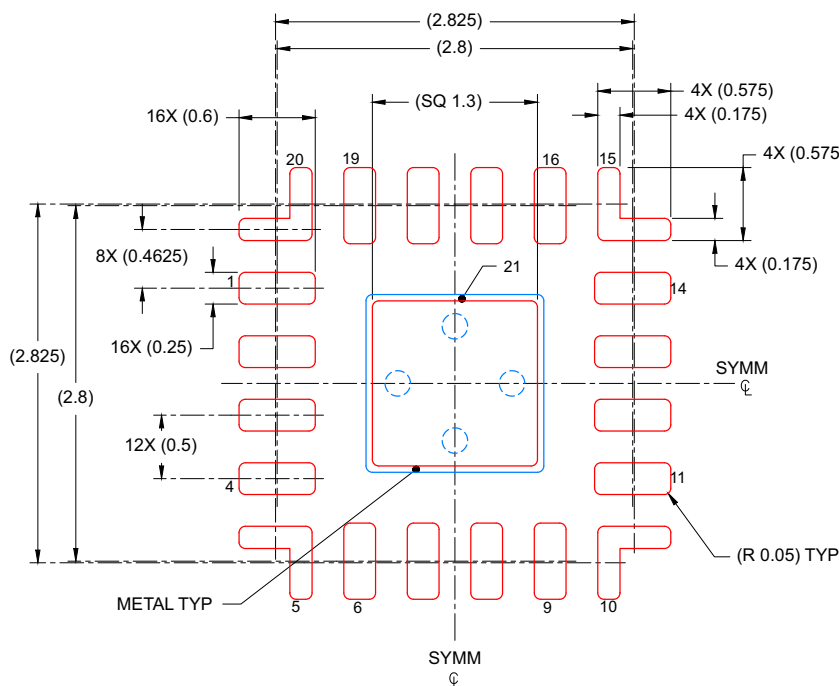
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**WQFN - 0.8 mm max height**

**RTE0020A**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
86% PRINTED COVERAGE BY AREA  
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 11.1 Package Option Addendum

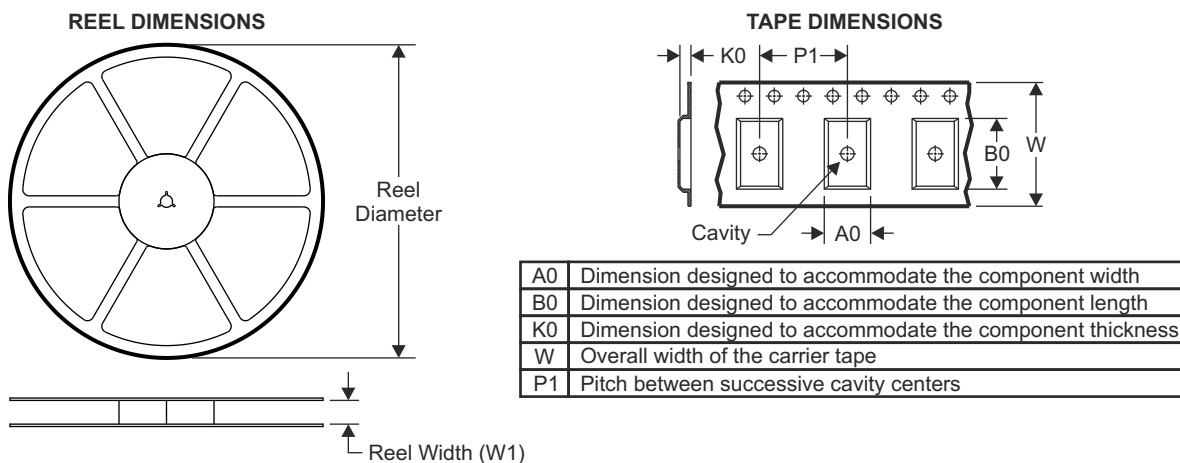
### Packaging Information

| Orderable Device | Status | Package Type | Package Drawing | Pins | Package Qty | Eco Plan     | Lead/Ball Finish | MSL Peak Temp           | Op Temp (°C) | Device Marking |
|------------------|--------|--------------|-----------------|------|-------------|--------------|------------------|-------------------------|--------------|----------------|
| TAA3020RTER      | ACTIVE | WQFN         | RTE             | 20   | 3000        | RoHS & Green | NIPDAU           | Level-2-260C<br>-1 YEAR | -40 to 125   | AD3120         |

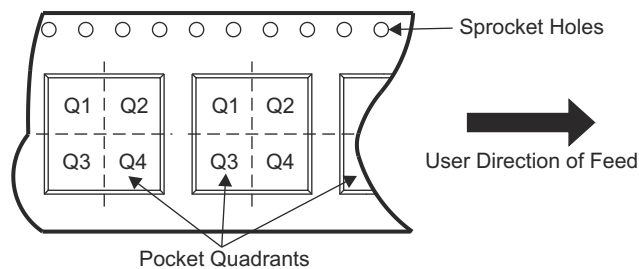
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## 11.2 Tape and Reel Information

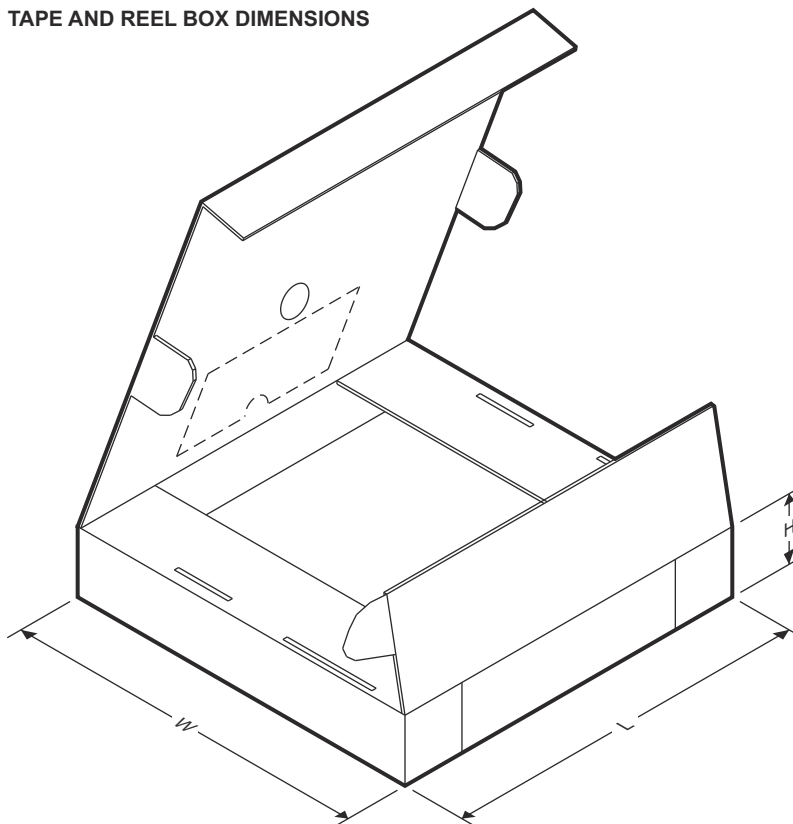


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAA3020RTER | WQFN         | RTE             | 20   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAA3020RTER | WQFN         | RTE             | 20   | 3000 | 367.0       | 367.0      | 35.0        |



PACKAGING INFORMATION

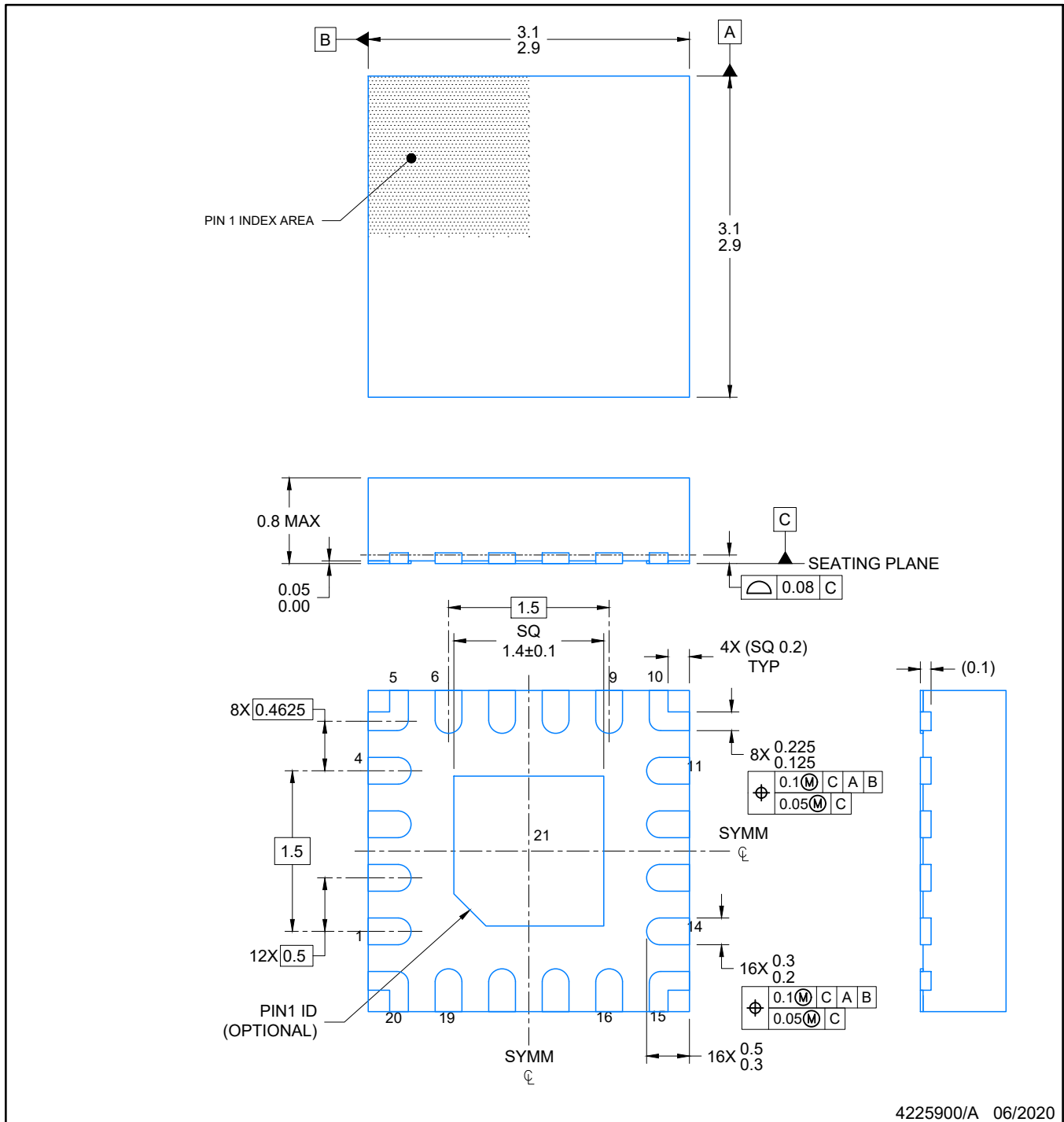
| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TAA3020IRTER          | Active        | Production           | WQFN (RTE)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | AD3120              |

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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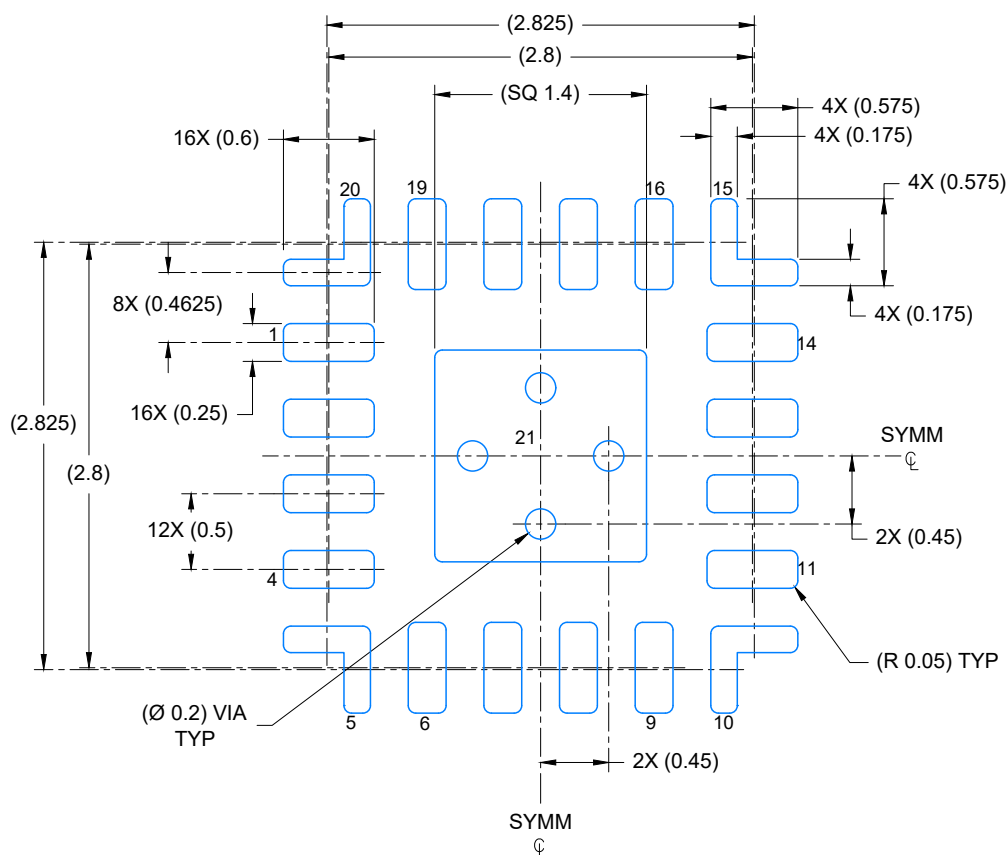
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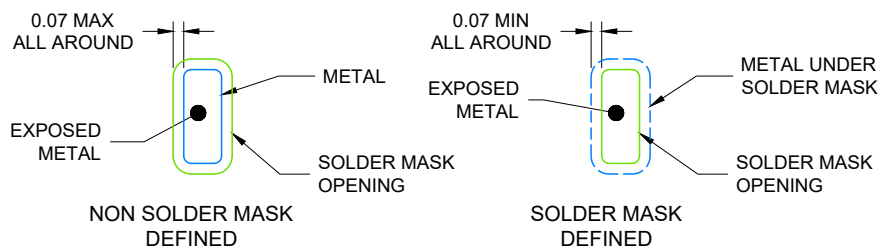
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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



## SOLDER MASK DETAILS

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NOTES: (continued)

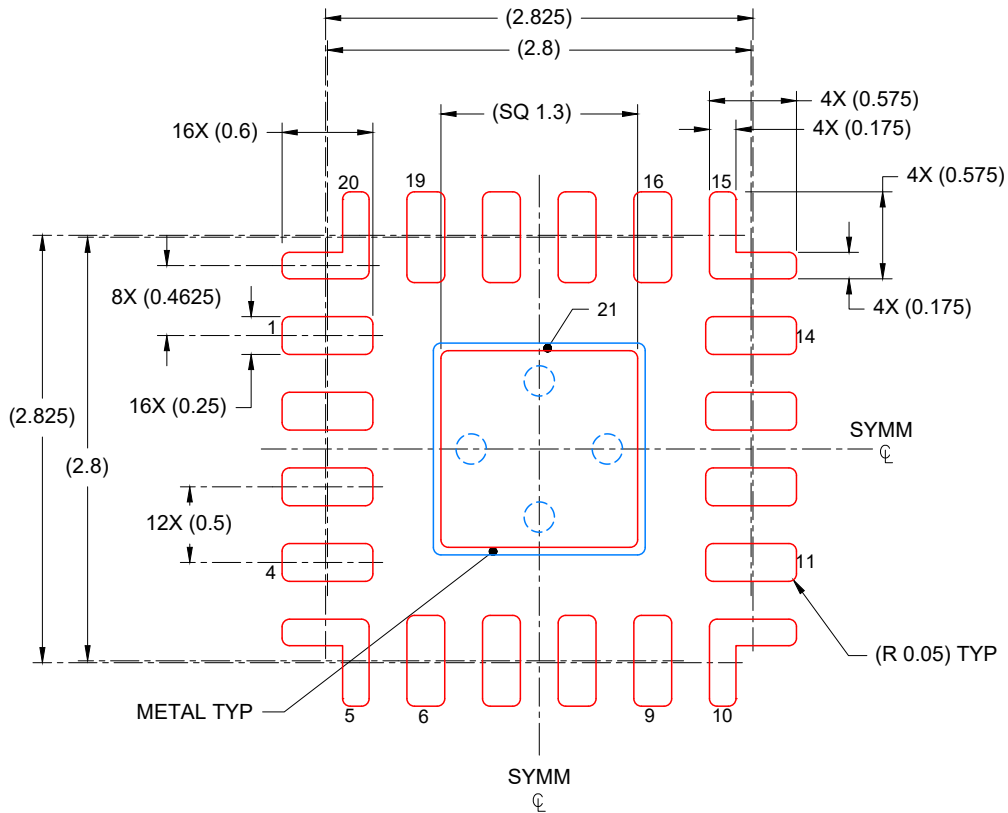
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
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RTE0020A

WQFN - 0.8 mm max height

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4225900/A 06/2020

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最終更新日：2025 年 10 月