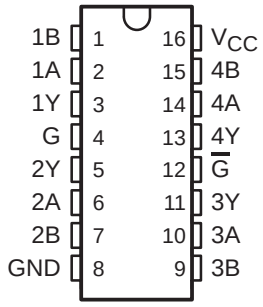
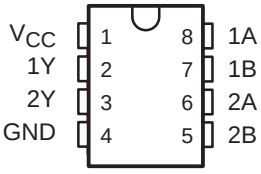
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Operates With a Single 3.3-V Supply**
- **Designed for Signaling Rate of up to 155 Mbps**
- **Differential Input Thresholds ±100 mV Max**
- **Low-Voltage TTL (LVTTL) Logic Output Levels**
- **Open-Circuit Fail Safe**
- **Characterized For Operation From 0°C to 70°C**

SN75LVDS32D (Marked as **75LVDS32**)
SN75LVDS32PW (Marked as **DS32**)
(TOP VIEW)



SN75LVDS9637D (Marked as **DF637** or **7L9637**)
SN75LVDS9637DGK (Marked as **AXI**)
(TOP VIEW)



description

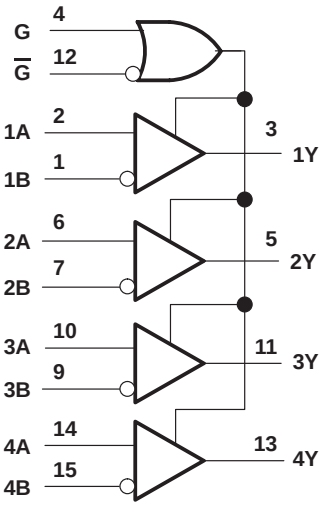
The SN75LVDS32 and SN75LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ±100 mV allow operation with a differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

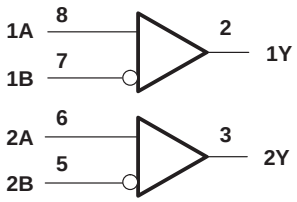
The SN75LVDS32 and SN75LVDS9637 are characterized for operation from 0°C to 70°C.

logic diagram

'LVDS32 logic diagram (positive logic)



'LVDS9637D logic diagram (positive logic)



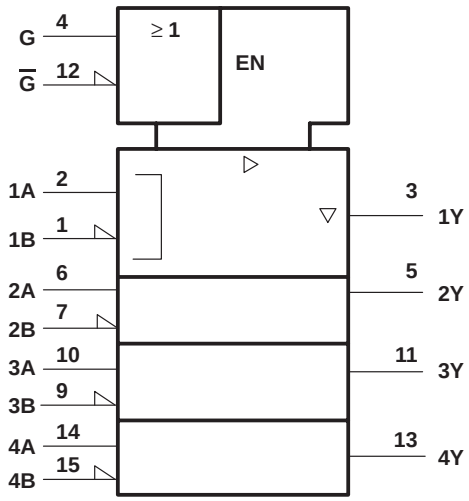
Function Tables

SN75LVDS32			
DIFFERENTIAL INPUT	**ENABLES**		**OUTPUT**
A, B	**G**	**$\overline{G}$**	**Y**
$V_{ID} \geq 100$ mV	H X	X L	H H
-100 mV $< V_{ID} < 100$ mV	H X	X L	? ?
$V_{ID} \leq -100$ mV	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

logic symbol†

SN75LVDS32



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Table

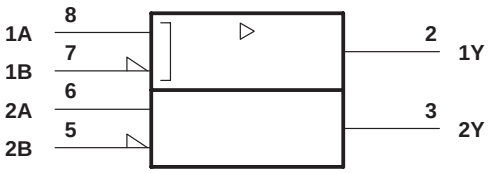
SN75LVDS9637

DIFFERENTIAL INPUT	OUTPUT
A, B	Y
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

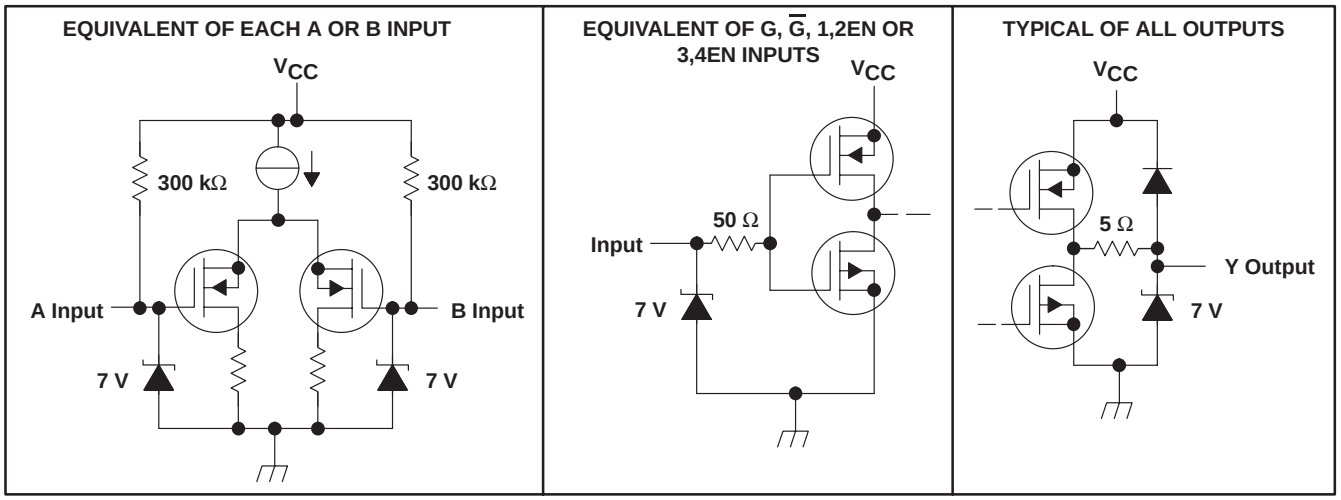
logic symbol†

SN75LVDS9637



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (A or B) . . . . . –0.5 V to 4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW
D (16)	950 mW	7.6 mW/°C	608 mW
PW	774 mW	6.2 mW/°C	496 mW
DGK	425 mW	3.4 mW/°C	272 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$		0.1		0.6	V
Common-mode input voltage, V_{IC} (see Figure 1)		$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
				$V_{CC} - 0.8$	V
Operating free-air temperature, T_A		0		70	°C

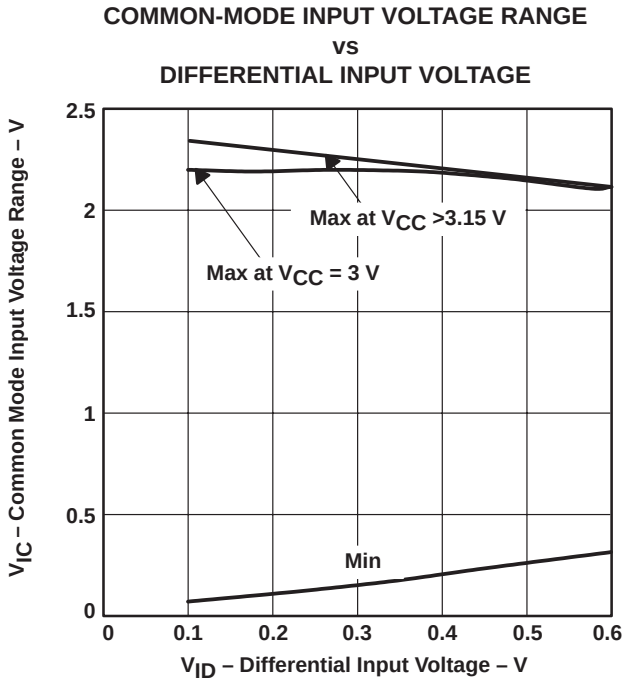


Figure 1. V_{IC} Versus V_{ID} and V_{CC}

SN75LVDSxxxx electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN75LVDS32, SN75LVDS9637			UNIT
				MIN	TYP†	MAX	
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 2 and Table 1			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold‡		See Figure 2 and Table 1	–100			mV
V_{OH}	High-level output voltage		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	V
I_{CC}	Supply current	SN75LVDS32	Enabled, No load		10	18	mA
		SN75LVDS32	Disabled		0.25	0.5	mA
		SN75LVDS9637	No load		5.5	10	mA
I_I	Input current (A or B inputs)		V_I = 0	–2	–10	–20	µA
			V_I = 2.4 V	–1.2	–3		µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)		V_{CC} = 0, V_I = 3.6 V		6	20	µA
I_{IH}	High-level input current (G, or $\overline{G}$ inputs)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (G, or $\overline{G}$ inputs)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current		V_O = 0 or V_{CC}			±10	µA

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

SN75LVDSxxxx switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN75LVDS32, SN75LVDS9637			UNIT
			MIN	TYP†	MAX	
t_{pLH}	Propagation delay time, low-to-high-level output	C_L = 100 pF, See Figure 3		2.1	6	ns
t_{pHL}	Propagation delay time, high-to-low-level output	C_L = 100 pF, See Figure 3		2.1	6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	C_L = 100 pF, See Figure 3		0.6	1.5	ns
$t_{sk(o)}$	Channel-to-channel output skew†	C_L = 100 pF, See Figure 3		0.7	1.5	ns
$t_{sk(pp)}$	Part-to-part skew‡	C_L = 100 pF, See Figure 3			0.6	ns
t_r	Output signal rise time, 20% to 80%	C_L = 100 pF, See Figure 3			0.6	ns
t_f	Output signal fall time, 80% to 20%	C_L = 100 pF, See Figure 3			1	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4			25	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 4			25	ns
t_{pZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4			25	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 4			25	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output
§ $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.
¶ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

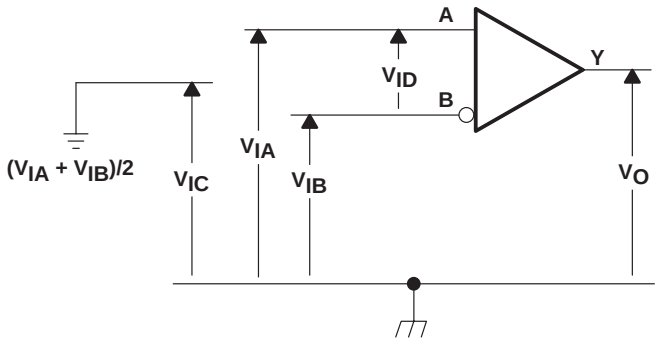
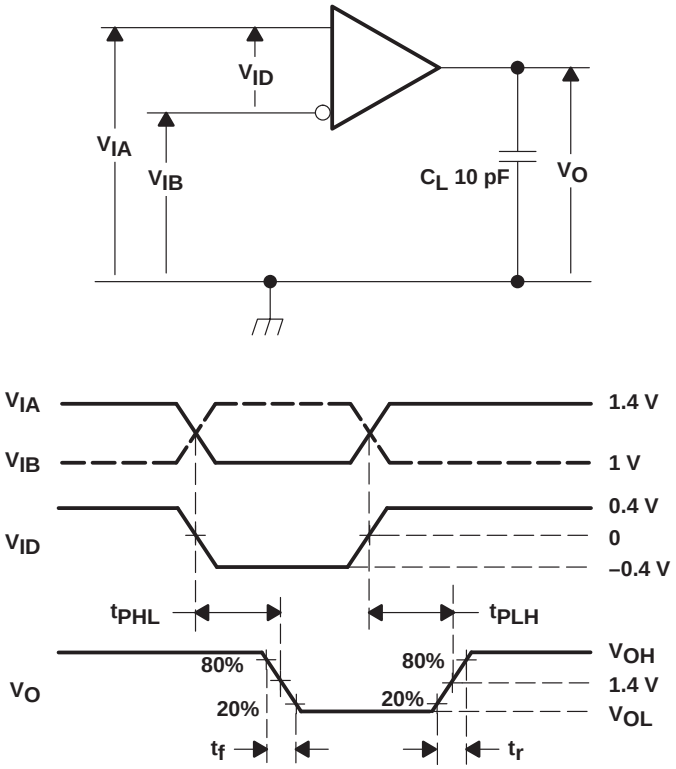


Figure 2. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

PARAMETER MEASUREMENT INFORMATION

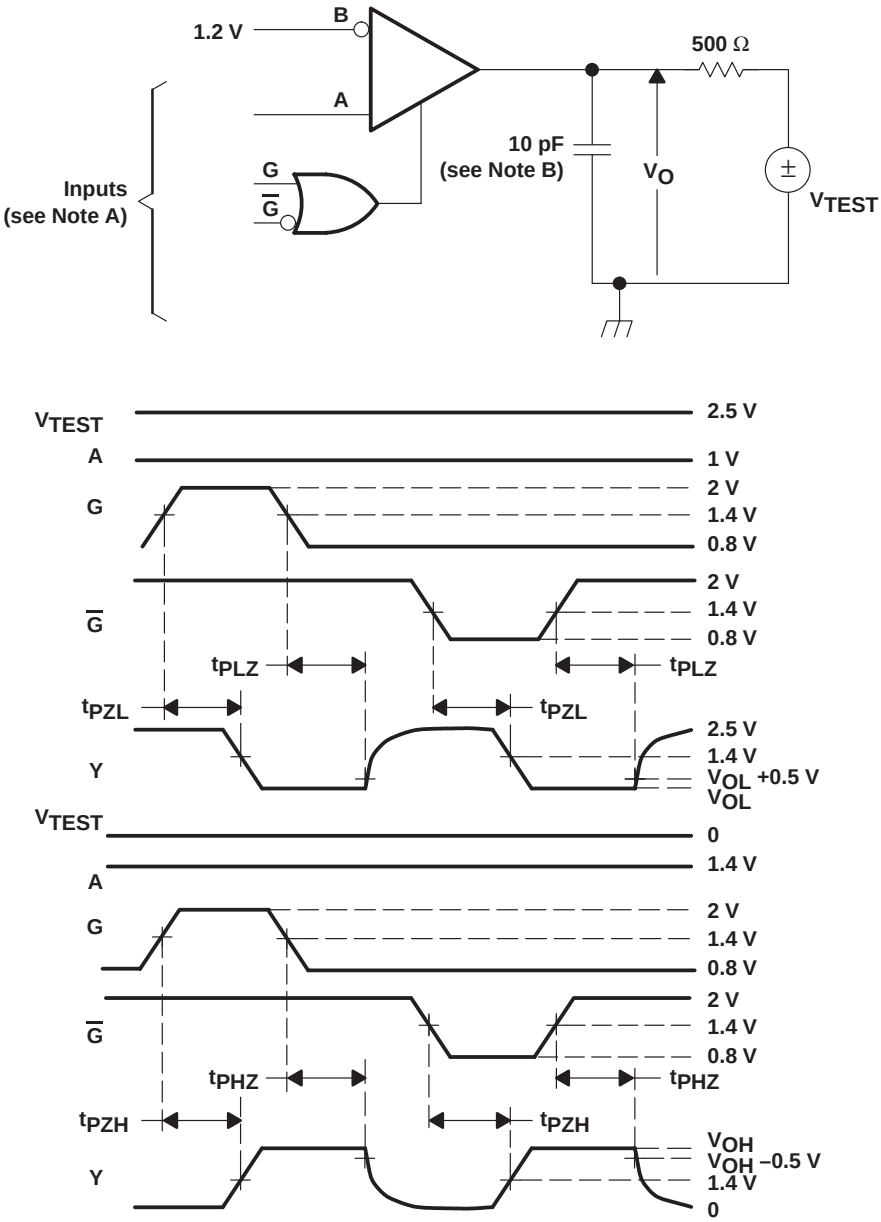


NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 3. Timing Test Circuit and Wave Forms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable/Disable Time Test Circuit and Wave Forms

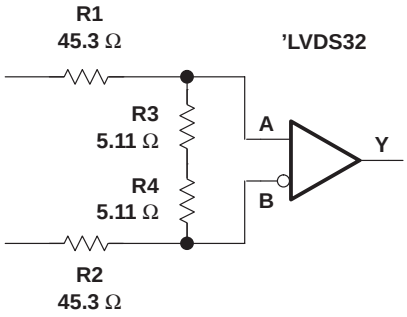
APPLICATION INFORMATION

using an LVDS receiver with RS-422 data

Receipt of data from a TIA/EIA-422 line driver may be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a very high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than ±1 V), the answer can be as simple as shown below in Figure 5. The use of a resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of 100 Ω to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal or 6 V is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a better than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.



NOTE A: The components used were standard values.
R1, R2 = NRC12F45R3TR, NIC Components, 45.3 Ohm, 1/8W, 1%, 1206 Package
R3, R4 = NRC12F5R11TR, NIC Components, 5.11 Ohm, 1/8W, 1%, 1206 Package

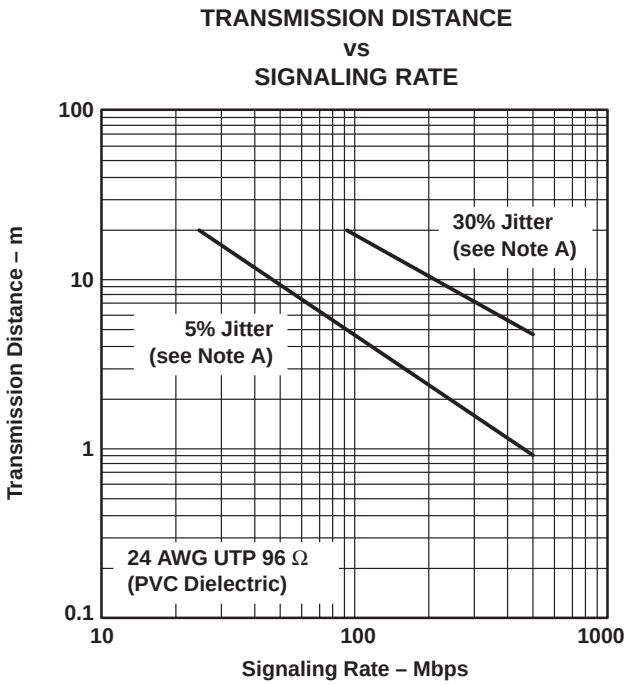
The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than 100 Ω in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

Figure 5. RS-422 Data Input to an LVDS Receiver Under Low Ground Noise Conditions

If ground noise between the RS-422 driver and LVDS receiver is a concern, then the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from ±1 V to greater than ±4.5 V.

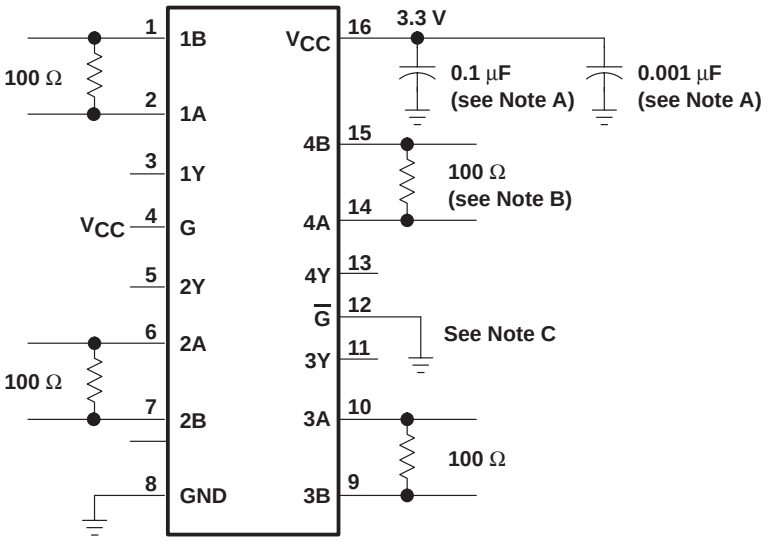
APPLICATIONS INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

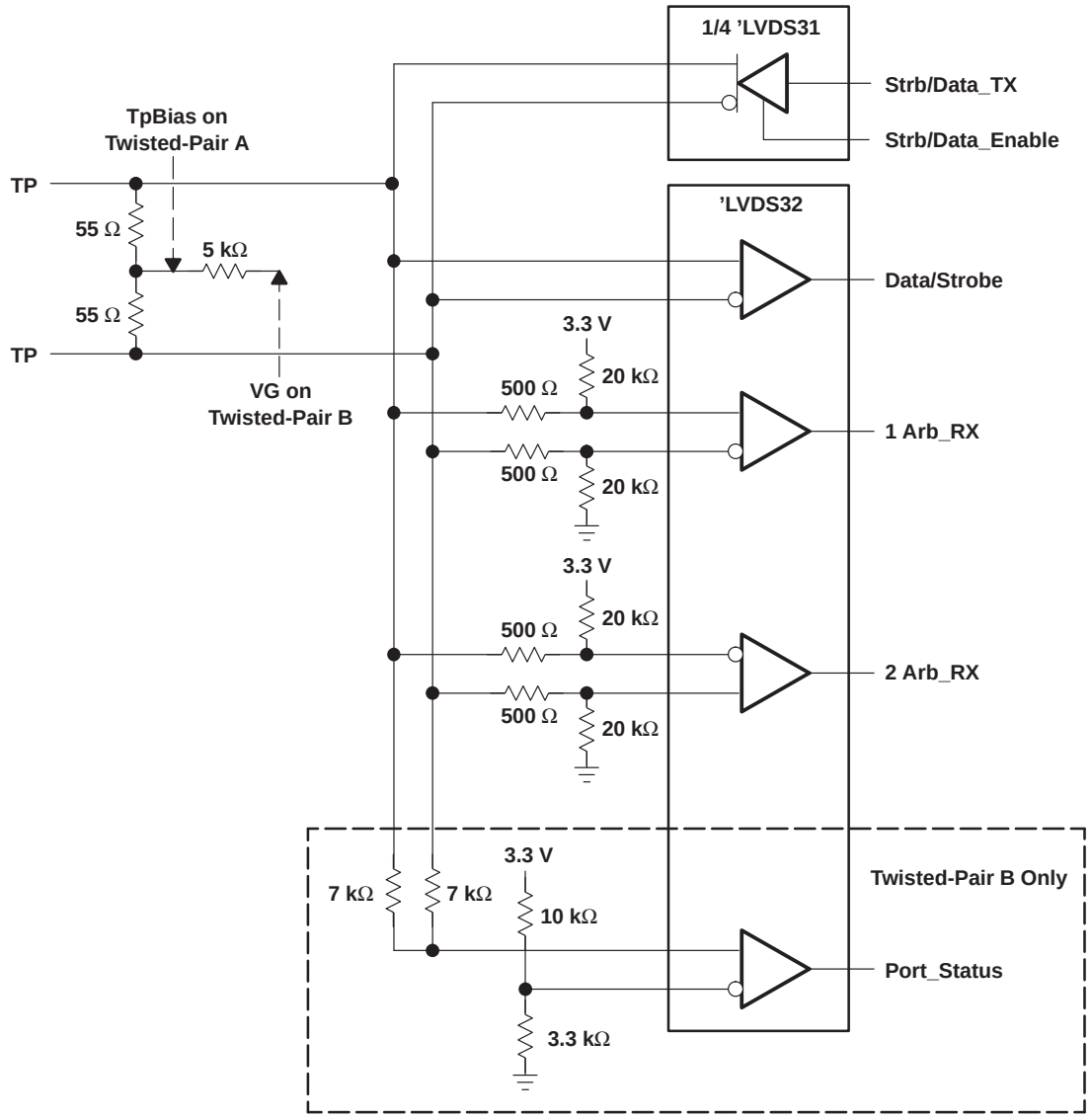
Figure 6. Typical Transmission Distance vs Signaling Rate



NOTES: A. Place a 0.1 μF and a 0.001 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 7. Typical Application Circuit Schematic

APPLICATION INFORMATION



NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.
B. Decoupling capacitance is not shown but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that allowed by IEEE1394.

Figure 8. 100-Mbps IEEE 1394 Transceiver

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV if it is within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 9. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level, regardless of the differential input voltage.

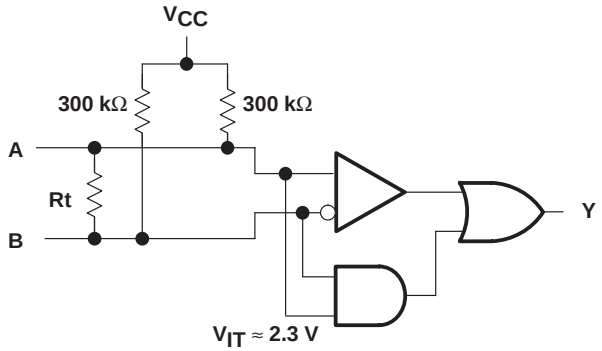
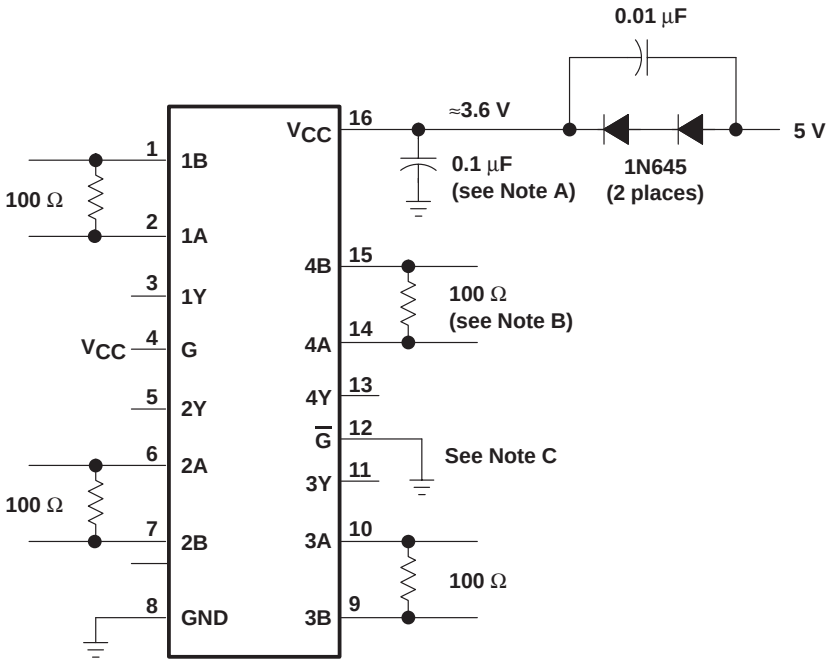


Figure 9. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

APPLICATION INFORMATION



NOTES: A. Place a 0.1 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 10. Operation With 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (TI literature SLLA038)
- *Reducing EMI with LVDS* (TI literature SLLA030)
- *Slew Rate Control of LVDS Circuits* (TI literature SLLA034)
- *Using an LVDS Receiver with RS-422 Data* (TI literature SLLA031)
- *Evaluating the LVDS EVM* (TI literature SLLA033)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVDS32D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32
SN75LVDS32D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32
SN75LVDS32DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32
SN75LVDS32DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS32
SN75LVDS9637D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DF637
SN75LVDS9637D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	DF637

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN75LVDS32 :

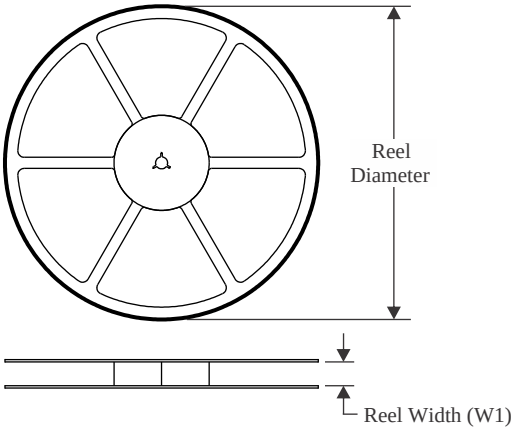
- Military : SN55LVDS32

NOTE: Qualified Version Definitions:

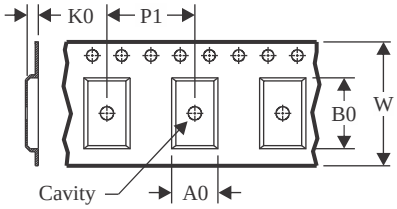
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

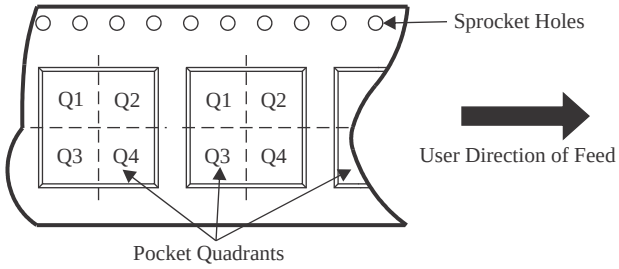


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

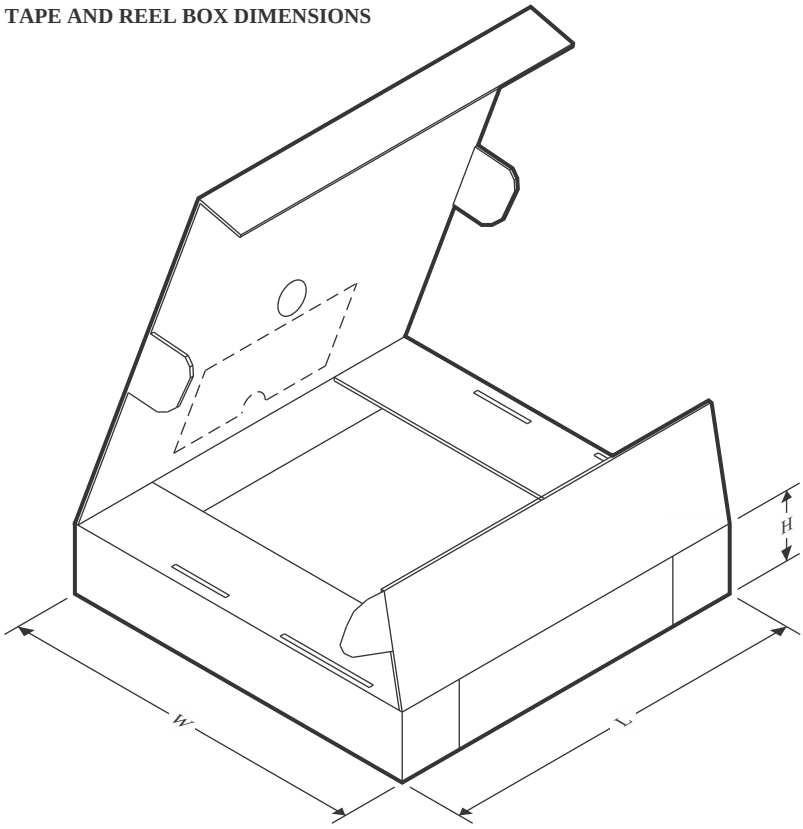
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS32DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

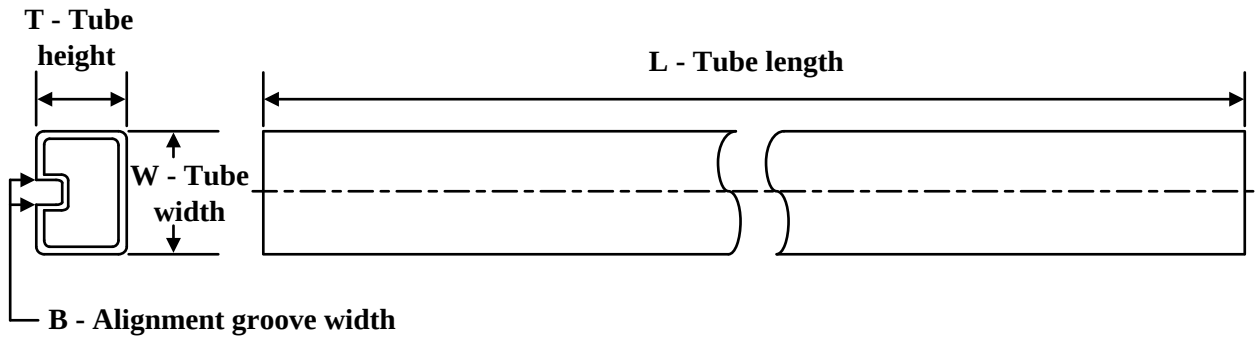
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS32DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LVDS32D	D	SOIC	16	40	507	8	3940	4.32
SN75LVDS32D.B	D	SOIC	16	40	507	8	3940	4.32
SN75LVDS9637D	D	SOIC	8	75	505.46	6.76	3810	4
SN75LVDS9637D	D	SOIC	8	75	507	8	3940	4.32
SN75LVDS9637D.B	D	SOIC	8	75	507	8	3940	4.32
SN75LVDS9637D.B	D	SOIC	8	75	505.46	6.76	3810	4

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