

# SN74LVTH574-EP

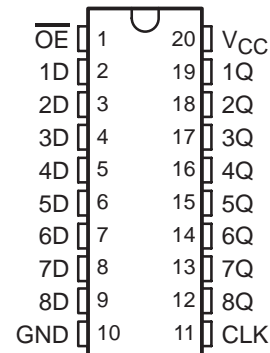
## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Supports Unregulated Battery Operation Down To 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE  
(TOP VIEW)



### description/ordering information

This octal flip-flop is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the SN74LVTH574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	TSSOP – PW	Tape and reel	SN74LVTH574IPWREP	LH574EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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description/ordering information (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

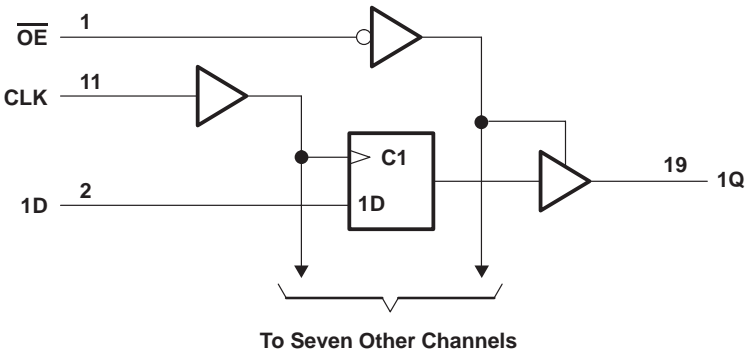
This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	128 mA
Current into any output in the high state, $I_O$ (see Note 2)	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	83°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  - The package thermal impedance is calculated in accordance with JESD 51-7.

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## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		5.5	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10 ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		$\mu$ s/V
$T_A$	Operating free-air temperature	-40	85	$^{\circ}$ C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 2.7$ V,	$I_I = -18$ mA			-1.2	V
$V_{OH}$		$V_{CC} = 2.7$ V to 3.6 V,	$I_{OH} = -100$ $\mu$ A	$V_{CC}-0.2$			V
		$V_{CC} = 2.7$ V,	$I_{OH} = -8$ mA	2.4			
		$V_{CC} = 3$ V,	$I_{OH} = -32$ mA	2			
$V_{OL}$		$V_{CC} = 2.7$ V	$I_{OL} = 100$ $\mu$ A			0.2	V
			$I_{OL} = 24$ mA			0.5	
		$V_{CC} = 3$ V	$I_{OL} = 16$ mA			0.4	
			$I_{OL} = 32$ mA			0.5	
			$I_{OL} = 64$ mA			0.55	
$I_I$	Control inputs	$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V			10	$\mu$ A
		$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND			$\pm 1$	
	Data inputs	$V_{CC} = 3.6$ V	$V_I = V_{CC}$			1	
			$V_I = 0$			-5	
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5 V			$\pm 100$	$\mu$ A
$I_{I(hold)}$	Data inputs	$V_{CC} = 3$ V	$V_I = 0.8$ V		75		$\mu$ A
			$V_I = 2$ V		-75		
		$V_{CC} = 3.6$ V‡,	$V_I = 0$ to 3.6 V			$\pm 500$	
$I_{OZH}$		$V_{CC} = 3.6$ V,	$V_O = 3$ V			5	$\mu$ A
$I_{OZL}$		$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			-5	$\mu$ A
$I_{OZPU}$		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE} =$ don't care				$\pm 100$	$\mu$ A
$I_{OZPD}$		$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE} =$ don't care				$\pm 100$	$\mu$ A
$I_{CC}$		$V_{CC} = 3.6$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high			0.19	mA
			Outputs low			5	
			Outputs disabled			0.19	
$\Delta I_{CC}^{\S}$		$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND				0.2	mA
$C_i$		$V_I = 3$ V or 0				3	pF
$C_o$		$V_O = 3$ V or 0				7	pF

† All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}$ C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.



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## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

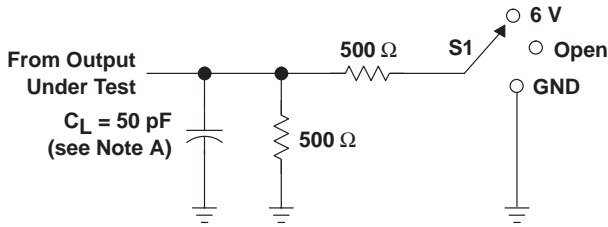
		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		150		150	MHz
$t_w$	Pulse duration, CLK high or low	3.3		3.3		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	2		2.4		ns
$t_h$	Hold time, data after CLK $\uparrow$	0.3		0		ns

switching characteristics over recommended free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

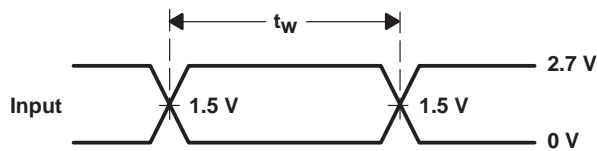
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP $\dagger$	MAX	MIN	MAX	
$f_{\text{max}}$			150			150		MHz
$t_{\text{PLH}}$	CLK	Q	1.8	3	4.5	5.3		ns
$t_{\text{PHL}}$			1.8	3	4.5	5.3		
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1.5	3.2	4.8	5.9		ns
$t_{\text{PZL}}$			1.5	3.5	4.8	5.9		
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2	3.5	4.8	5.1		ns
$t_{\text{PLZ}}$			2	3.2	4.4	4.4		

$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

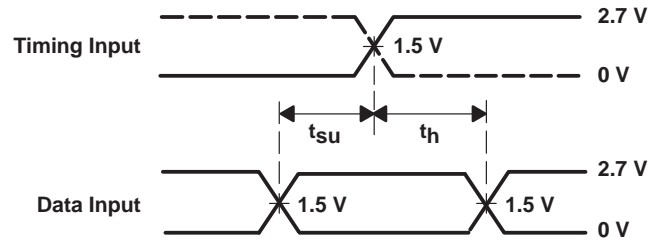
## PARAMETER MEASUREMENT INFORMATION



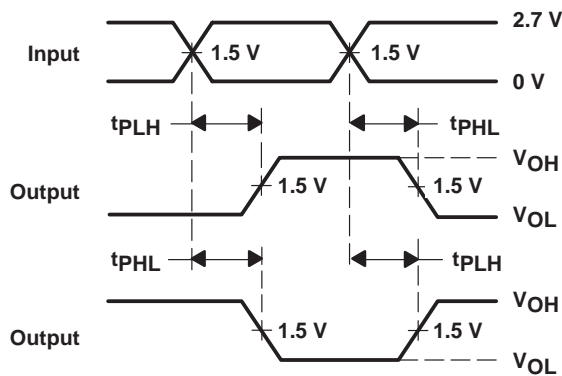
LOAD CIRCUIT



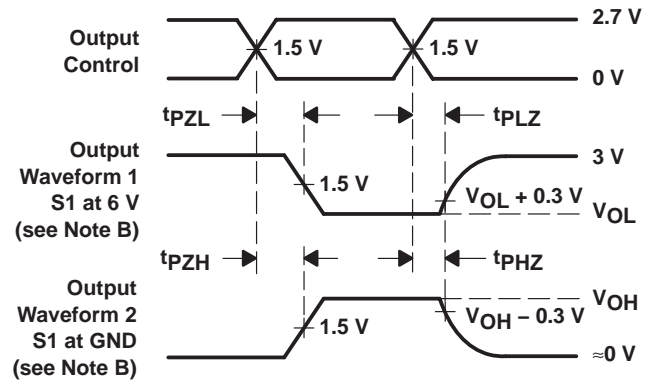
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVTH574IPWREP	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH574EP

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN74LVTH574-EP :

● Catalog : [SN74LVTH574](#)

● Military : [SN54LVTH574](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH574IPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH574IPWREP	TSSOP	PW	20	2000	353.0	353.0	32.0

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