![Texas Instruments logo] TEXAS INSTRUMENTS
www.ti.com

SN54LVTH162373, SN74LVTH162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS261M−JULY 1993−REVISED DECEMBER 2006

FEATURES

- **Members of the Texas Instruments Widebus™ Family**

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH162373 . . . WD PACKAGE
SN74LVTH162373 . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2$\overline{OE}$	24	25	2LE

DESCRIPTION/ORDERING INFORMATION

The 'LVTH162373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube of 25	SN74LVTH162373DL	LVTH162373
			74LVTH162373DLG4	
		Reel of 1000	SN74LVTH162373DLR	
			74LVTH162373DLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH162373DGGR	LVTH162373
			74LVTH162373DGGRE4	
	VFBGA – GQL	Reel of 1000	SN74LVTH162373KR	LL2373
	VFBGA – ZQL (Pb-free)		74LVTH162373ZQLR	
−55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162373WD	SNJ54LVTH162373WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

![warning triangle icon] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

GQL OR ZQL PACKAGE
**(TOP VIEW)**
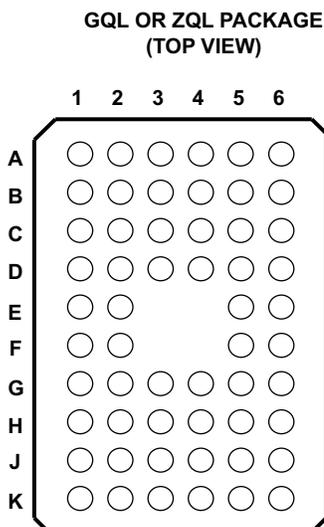
TERMINAL ASSIGNMENTS[1]

	1	2	3	4	5	6
A	1$\overline{OE}$	NC	NC	NC	NC	1LE
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2$\overline{OE}$	NC	NC	NC	NC	2LE

(1)   NC - No internal connection

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)
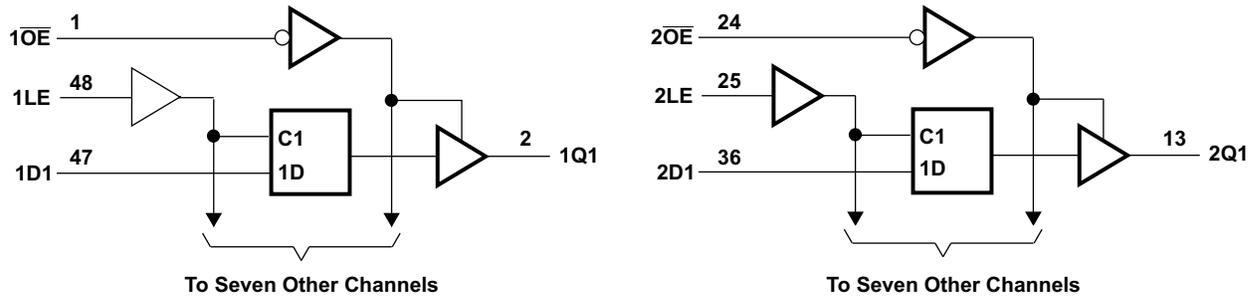
Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings[1]

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high state[2]		−0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state			30	mA
I_O	Current into any output in the high state[3]			30	mA
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and V_O > V_{CC}.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			SN54LVTH162373		SN74LVTH162373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage range		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**TEXAS
INSTRUMENTS**
www.ti.com

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162373			SN74LVTH162373			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 3 V,	I_{OH} = −12 mA	2			2			V
V_{OL}		V_{CC} = 3 V,	I_{OL} = 12 mA			0.8			0.8	V
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V[2],	V_I = 0 to 3.6 V						500 −750	
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			−5			−5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[3]			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[3]			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}[4]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			3			3		pF
C_o		V_O = 3 V or 0			9			9		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

|		SN54LVTH162373				SN74LVTH162373				UNIT
		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		3		3		3		ns
t_{su}	Setup time, data before LE↓	1.3		0.6		1		0.6		ns
t_h	Hold time, data after LE↓	1		1.1		1		1.1		ns

Submit Documentation Feedback

SN54LVTH162373, SN74LVTH162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS
SCBS261M−JULY 1993−REVISED DECEMBER 2006

www.ti.com

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162373				SN74LVTH162373					UNIT
			V_{CC} = 3.3 V $\pm$0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}	D	Q	1.8	5		5.7	1.9	3.1	4.6		5.1	ns
t_{PHL}			1.8	4.4		4.8	1.9	2.8	4		4.3	
t_{PLH}	LE	Q	2.1	5.4		6.2	2.2	3.4	5.1		5.8	ns
t_{PHL}			2.1	4.9		4.7	2.2	3.2	4.6		4.3	
t_{PZH}	$\overline{OE}$	Q	1.7	5.6		7	1.8	3.2	5.4		6.6	ns
t_{PZL}			1.7	5.3		5.9	1.8	3.2	4.9		5.5	
t_{PHZ}	$\overline{OE}$	Q	2.3	6.3		6.6	2.4	3.8	5.4		5.7	ns
t_{PLZ}			1	7.4		6.4	2.2	3.5	5.1		5	
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TEXAS
INSTRUMENTS
www.ti.com

PARAMETER MEASUREMENT INFORMATION

From Output
Under Test

C_L = 50 pF
(see Note A)

500 Ω

500 Ω

S1

6 V

Open

GND
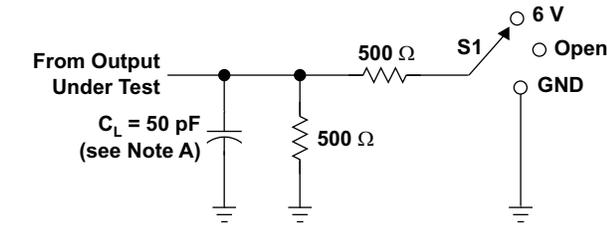
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

Timing Input

2.7 V

1.5 V

0 V

t_w

Input

1.5 V

1.5 V

2.7 V

0 V
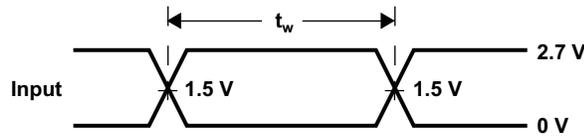
**VOLTAGE WAVEFORMS
PULSE DURATION**

t_{su} t_h

Data Input

1.5 V

1.5 V

2.7 V

0 V
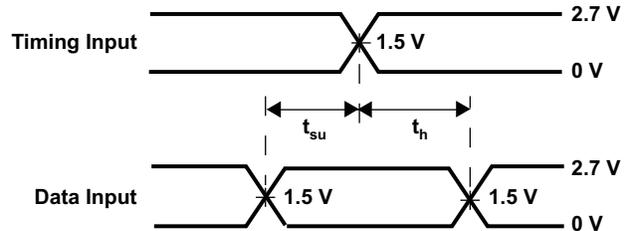
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Input

1.5 V

1.5 V

2.7 V

0 V

t_{PLH} t_{PHL}

Output

1.5 V

1.5 V

V_{OH}

V_{OL}

t_{PHL} t_{PLH}

Output

1.5 V

1.5 V

V_{OH}

V_{OL}
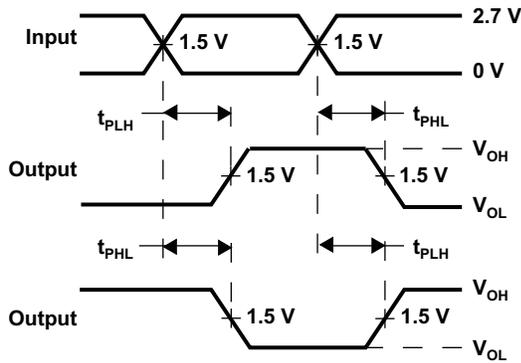
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

Output
Control

1.5 V

1.5 V

2.7 V

0 V

t_{PZL} t_{PLZ}

Output
Waveform 1
S1 at 6 V
(see Note B)

1.5 V

V_{OL} + 0.3 V

3 V

V_{OL}

t_{PZH} t_{PHZ}

Output
Waveform 2
S1 at GND
(see Note B)

1.5 V

V_{OH} − 0.3 V

V_{OH}

≈0 V
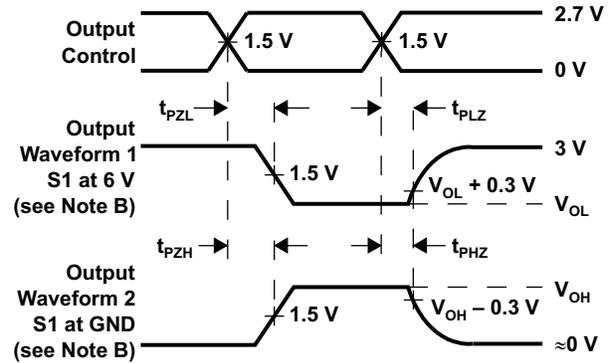
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

Submit Documentation Feedback

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9763801VXA	Active	Production	CFP (WD) | 48	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9763801VXA SNV54LVTH162373WD
74LVTH162373DGGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
74LVTH162373DGGRG4.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
74LVTH162373DLRG4	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
74LVTH162373DLRG4.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DGGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DL.B	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373
SN74LVTH162373DLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVTH162373 :

- Enhanced Product : SN74LVTH162373-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
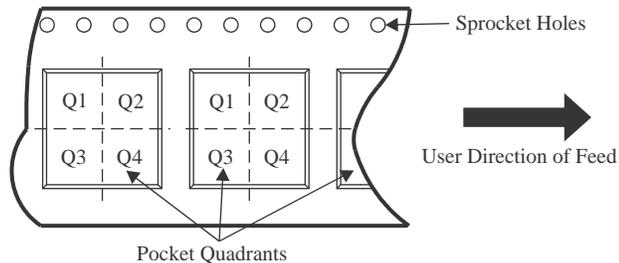
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH162373DGGRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74LVTH162373DLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH162373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH162373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH162373DGGRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
74LVTH162373DLRG4	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVTH162373DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH162373DLR	SSOP	DL	48	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH162373DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH162373DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

8.3
7.9 TYP

PIN 1 ID
AREA

A

1

46X 0.5

48

12.6
12.4
NOTE 3

2X

11.5

24

25

6.2
6.0

B

48X 0.27
0.17

⊕ | 0.08Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

1.2
1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

48

SYMM

24

25

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
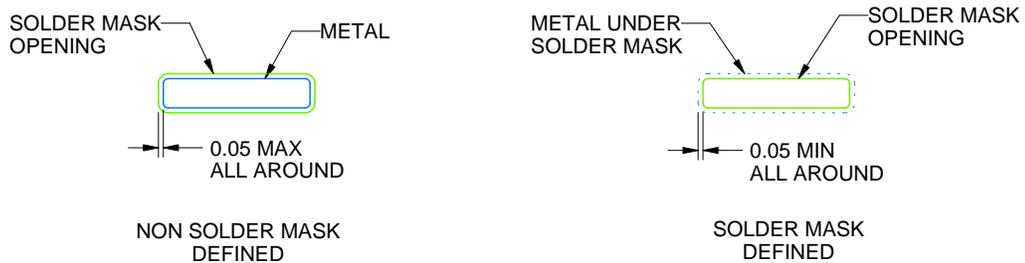
SOLDER MASK DETAILS

4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

SYMM

48

24

25

(7.5)
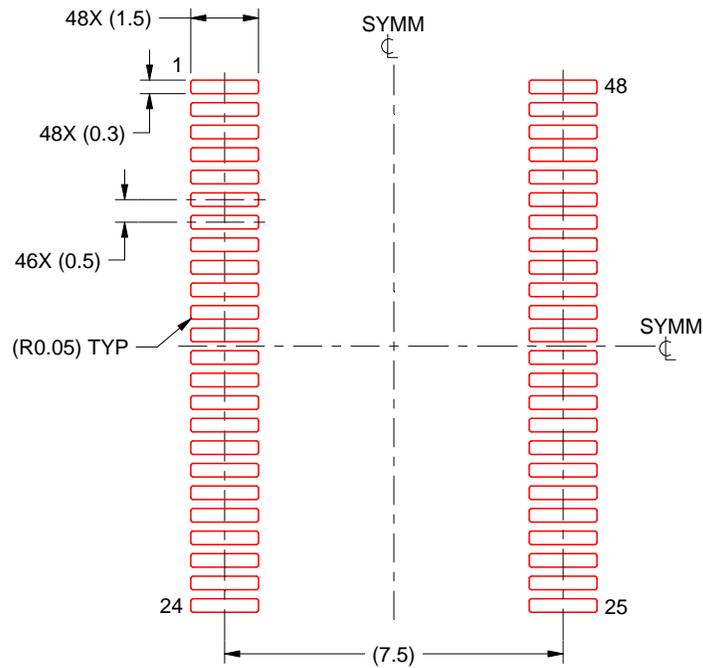
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0,50

0,27 / 0,17   ⊕ 0,08 Ⓜ

48   25

6,20 / 6,00   8,30 / 7,90

0,15 NOM

Gage Plane

0°–8°

0,25

0,75 / 0,50

1   24

A

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10

DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
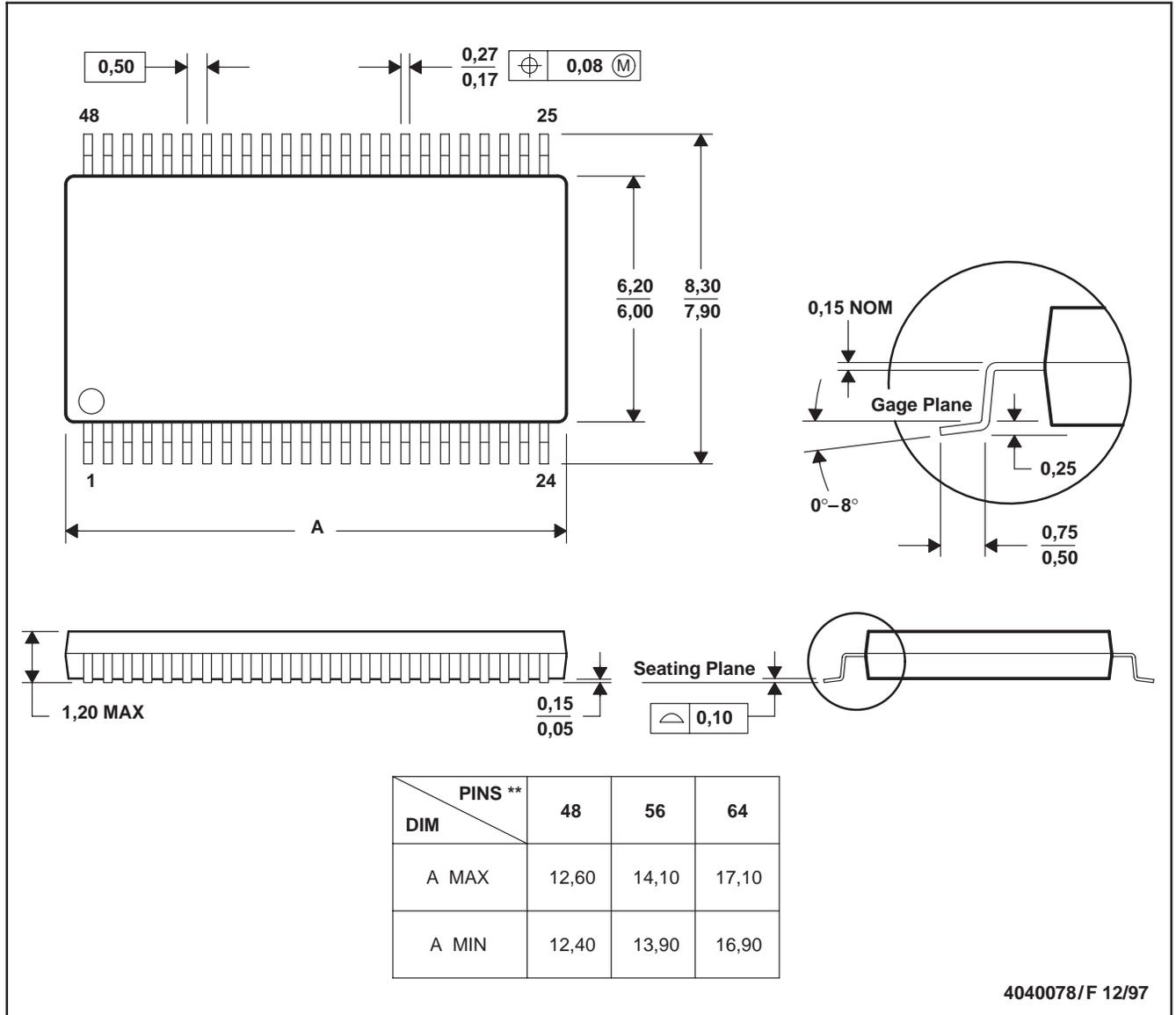
NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold protrusion not to exceed 0,15.
       D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

WD (R-GDFP-F**)   **CERAMIC DUAL FLATPACK**

48 LEADS SHOWN
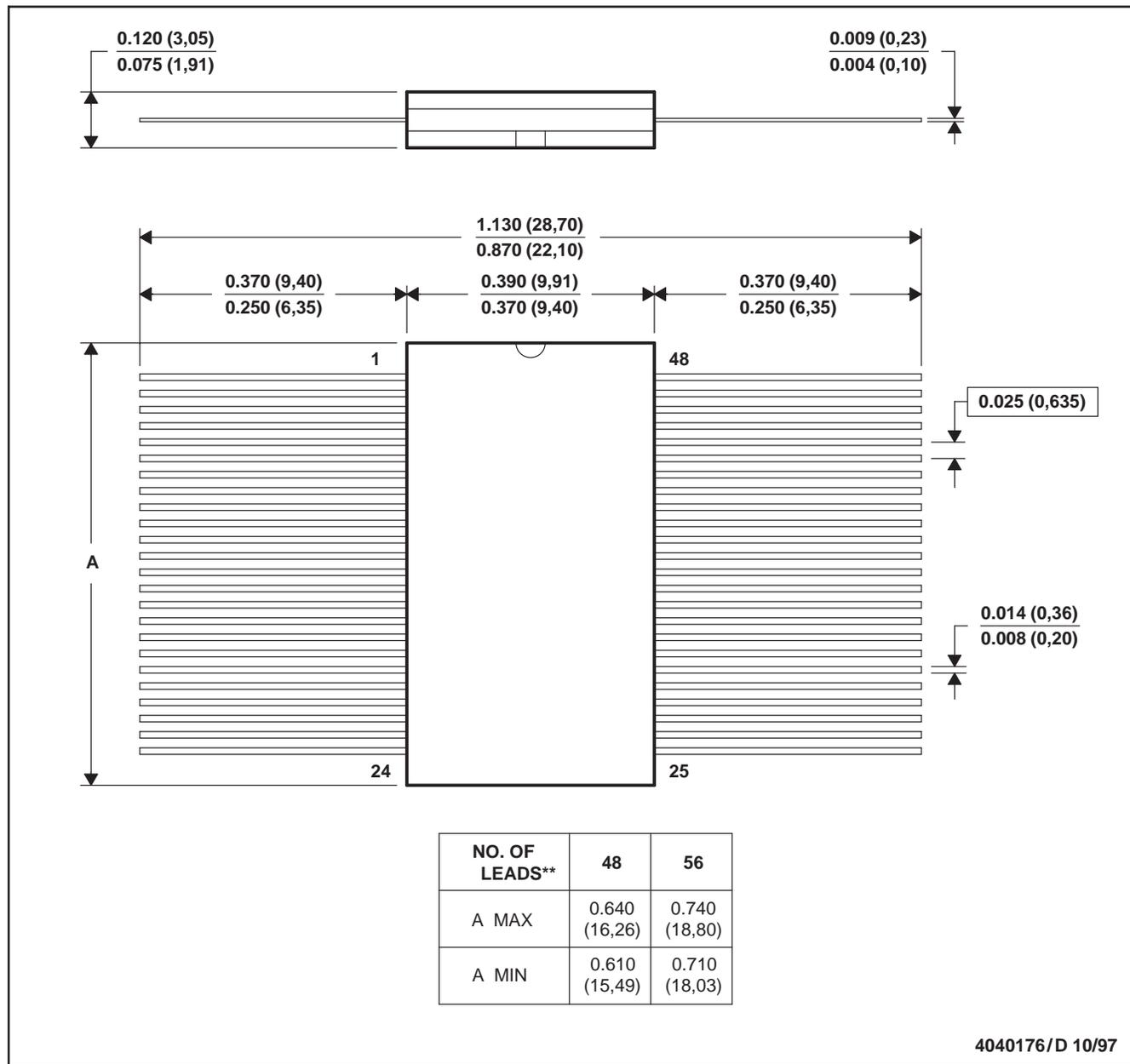
0.120 (3,05) / 0.075 (1,91)

0.009 (0,23) / 0.004 (0,10)

1.130 (28,70) / 0.870 (22,10)

0.370 (9,40) / 0.250 (6,35)

0.390 (9,91) / 0.370 (9,40)

0.370 (9,40) / 0.250 (6,35)

1   48

0.025 (0,635)

A

0.014 (0,36) / 0.008 (0,20)

24   25

NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only
         E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
                              GDFP1-F56 and JEDEC MO-146AB

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE
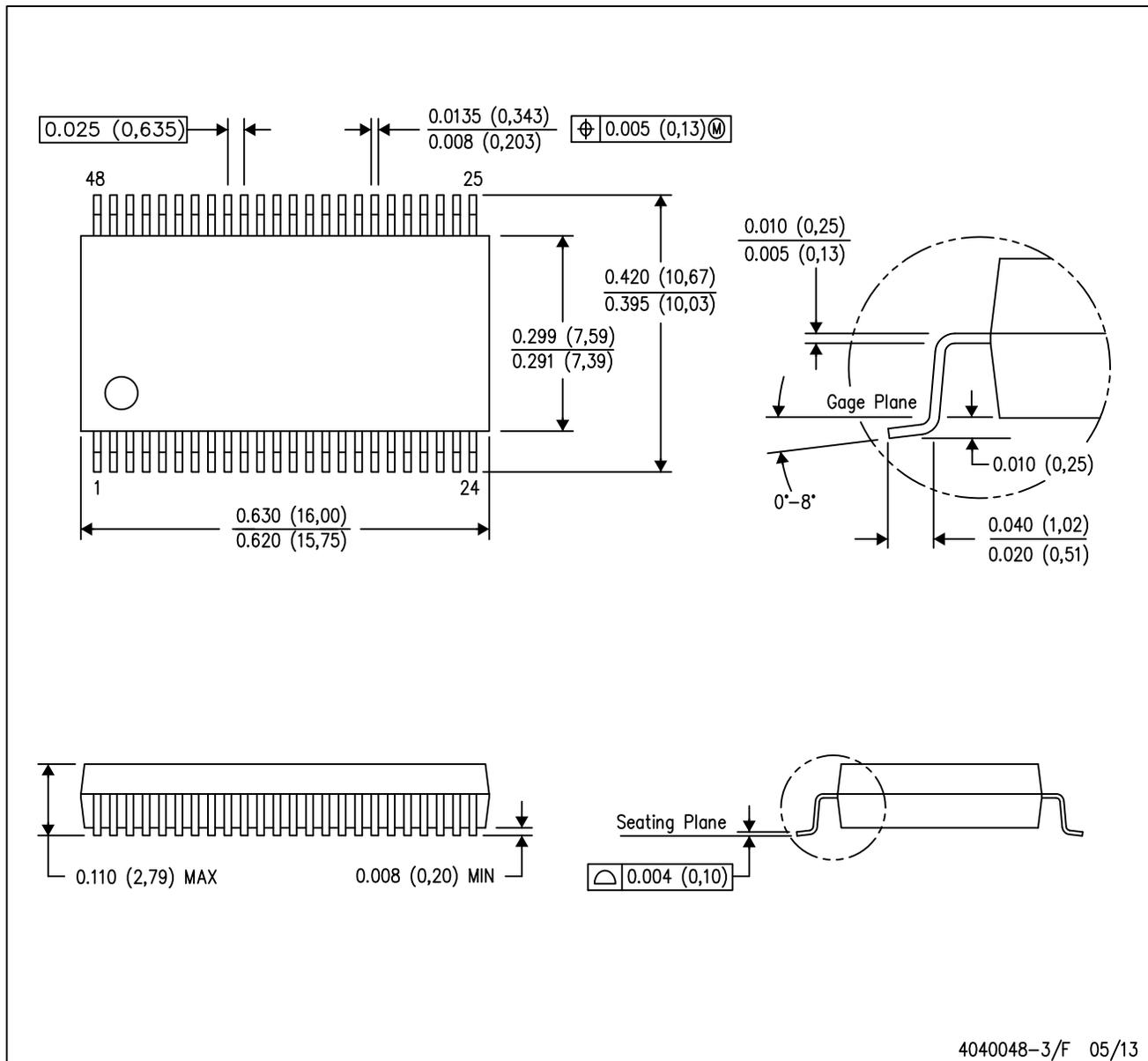
0.025 (0,635)

$\dfrac{0.0135\ (0,343)}{0.008\ (0,203)}$ ⊕ 0.005 (0,13) Ⓜ

48   25

$\dfrac{0.420\ (10,67)}{0.395\ (10,03)}$

$\dfrac{0.299\ (7,59)}{0.291\ (7,39)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

0.010 (0,25)

0°−8°

$\dfrac{0.040\ (1,02)}{0.020\ (0,51)}$

1   24

$\dfrac{0.630\ (16,00)}{0.620\ (15,75)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE AND DISCLAIMER