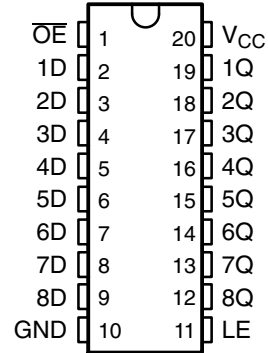


# SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

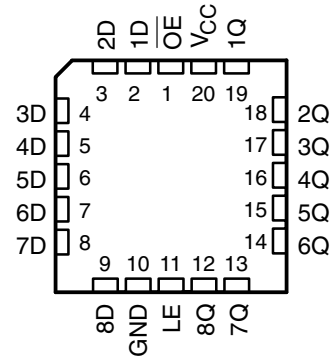
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT573 . . . J OR W PACKAGE  
SN74LVT573 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LVT573 . . . FK PACKAGE  
(TOP VIEW)



## description

These octal latches are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT573 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVT573 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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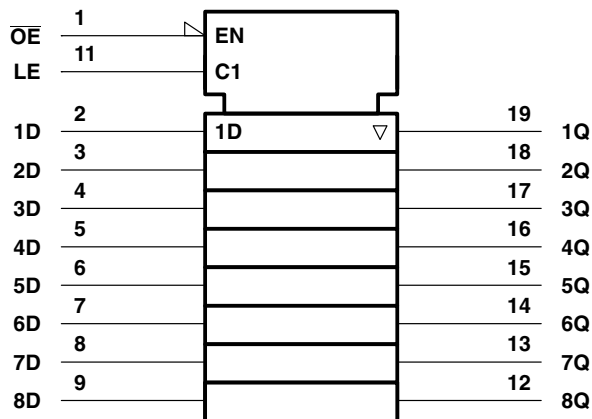
# SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS138D – MAY 1992 – REVISED JULY 1995

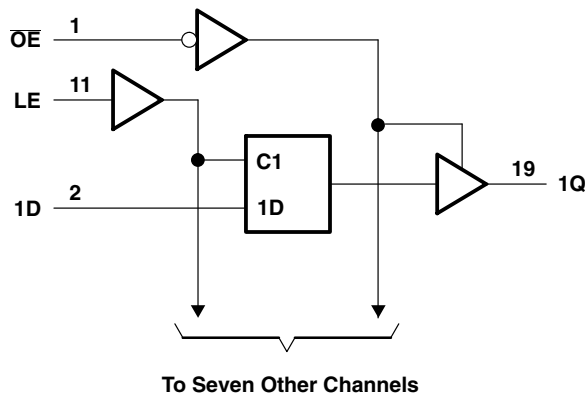
FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT573	96 mA
SN74LVT573	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT573	48 mA
SN74LVT573	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

**SN54LVT573, SN74LVT573**  
**3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 4)**

		SN54LVT573		SN74LVT573		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

# SN54LVT573, SN74LVT573

## 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT573		SN74LVT573		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		V		
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$			$V_{CC} - 0.2$		$V_{CC} - 0.2$		V		
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$			2.4		2.4				
	$V_{CC} = 3\text{ V}$			2		2				
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V		
		$I_{OL} = 24\text{ mA}$		0.5		0.5				
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4		0.4				
		$I_{OL} = 32\text{ mA}$		0.5		0.5				
		$I_{OL} = 48\text{ mA}$		0.55		0.55				
		$I_{OL} = 64\text{ mA}$				0.55				
$I_I$	$V_{CC} = 0\text{ or MAX}^\ddagger$ , $V_I = 5.5\text{ V}$			50		10		$\mu\text{A}$		
	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}\text{ or GND}$		$\pm 1$		$\pm 1$				
		$V_I = V_{CC}$		1		1				
		$V_I = 0$		-5		-5				
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					$\pm 100$		$\mu\text{A}$		
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75		75		$\mu\text{A}$		
		$V_I = 2\text{ V}$		-75		-75				
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$			1		1		$\mu\text{A}$		
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$			-1		-1		$\mu\text{A}$		
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$ , $I_O = 0$			Outputs high		0.13 0.39		0.13 0.19		mA
				Outputs low		8.6 14		8.6 12		
				Outputs disabled		0.13 0.39		0.13 0.19		
$\Delta I_{CC}^\S$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.3		0.2		mA		
$C_i$	$V_I = 3\text{ V or }0$			4		4		pF		
$C_o$	$V_O = 3\text{ V or }0$			8		8		pF		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	SN54LVT573				SN74LVT573				UNIT
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high								
	3.3		3.3		3.3		3.3		ns
$t_{su}$	Setup time, data before LE↓								
	1		0.9		0.7		0.6		ns
$t_h$	Hold time, data after LE↓								
	1.8		2		1.6		1.8		ns



**SN54LVT573, SN74LVT573**  
**3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

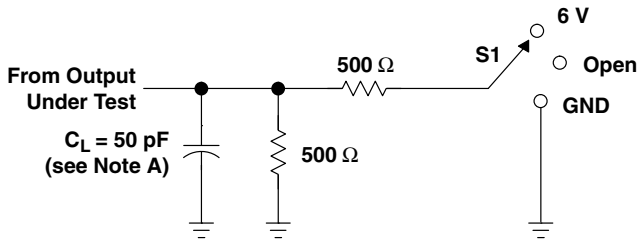
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT573				SN74LVT573				UNIT	
			$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$t_{PLH}$	D	Q	0.5	4.7	4.9		1	2.5	4.2	4.7		ns
$t_{PHL}$			0.5	4.9	5.4		1	2.7	4.3	5.2		
$t_{PLH}$	LE	Q	1	6	6.9		1.6	3.5	5.6	6.3		ns
$t_{PHL}$			1.4	6.9	7.6		2.5	4.3	6.5	7.2		
$t_{PZH}$	$\bar{O}E$	Q	0.5	5.3	6.4		1	2.8	5.1	6.2		ns
$t_{PZL}$			0.7	5.7	7.2		1.3	3.3	5.5	6.6		
$t_{PHZ}$	$\bar{O}E$	Q	1.2	5.9	6.9		2	3.7	5.7	6.7		ns
$t_{PLZ}$			1	5.4	5.5		1.5	3	4.6	5.1		

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

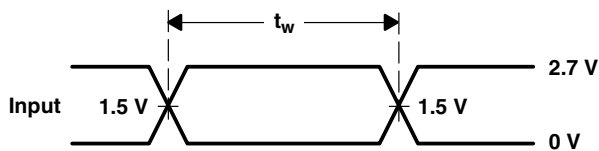
SCBS138D – MAY 1992 – REVISED JULY 1995

## PARAMETER MEASUREMENT INFORMATION

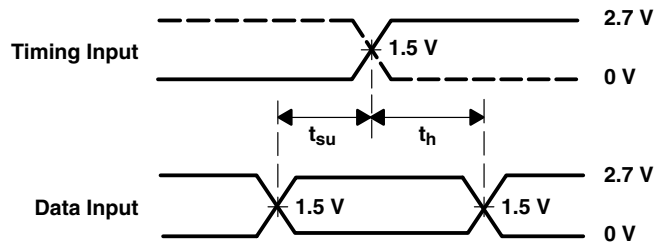


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

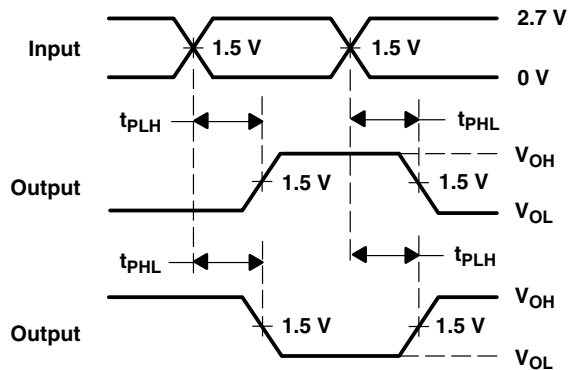
LOAD CIRCUIT FOR OUTPUTS



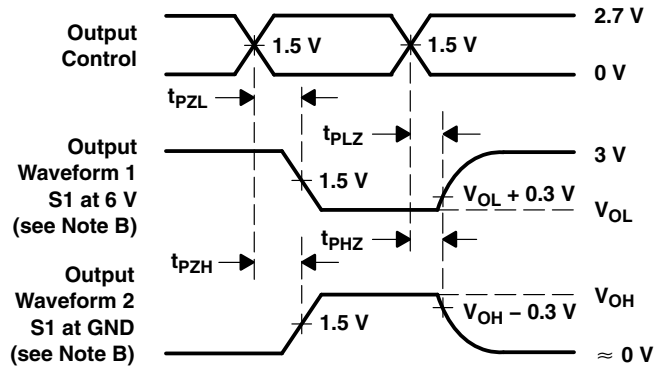
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVT573DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT573
SN74LVT573DW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT573
<a href="#">SN74LVT573PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX573
SN74LVT573PWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX573

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVT573DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVT573DW.B	DW	SOIC	20	25	507	12.83	5080	6.6

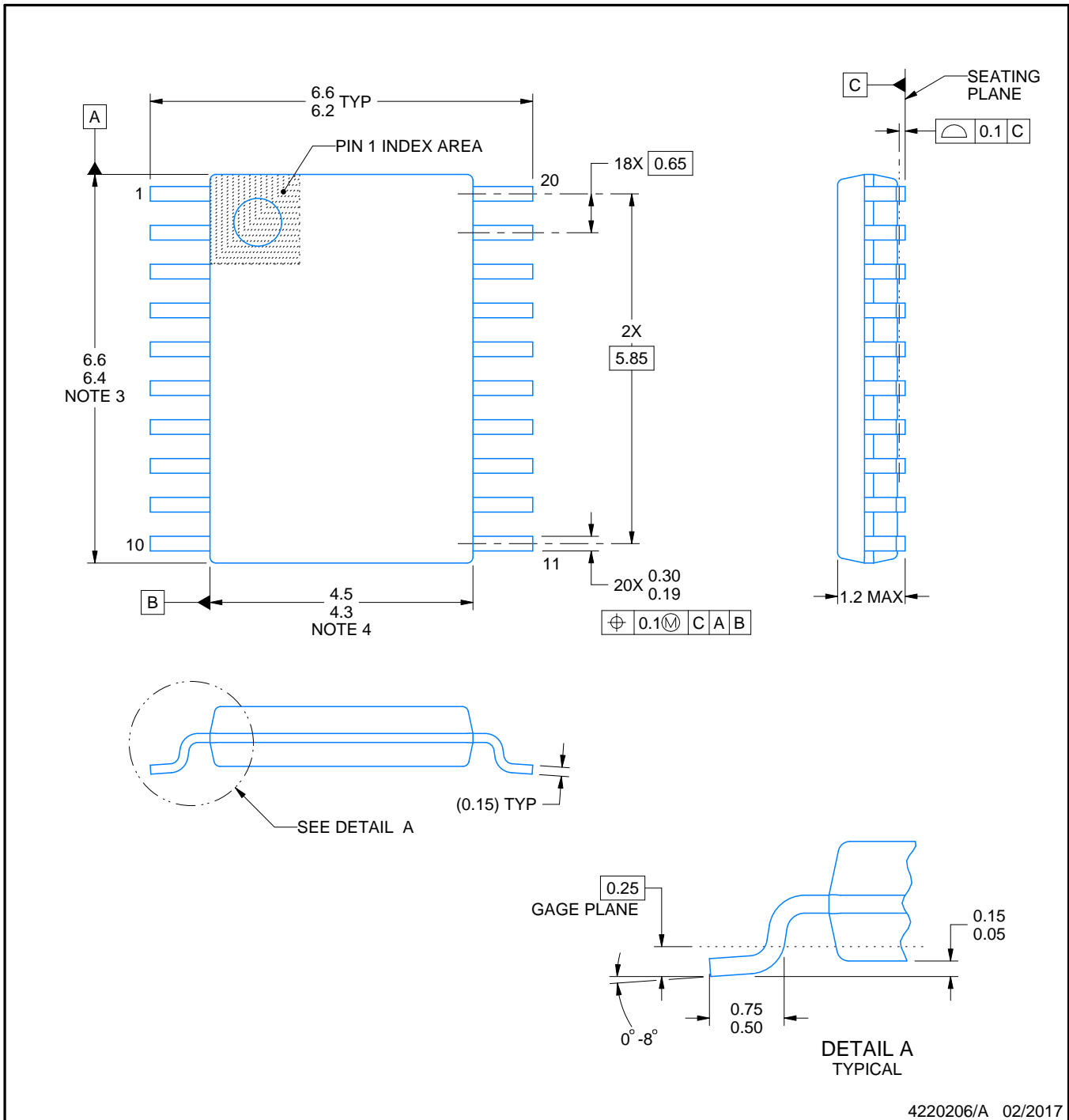
PW0020A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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