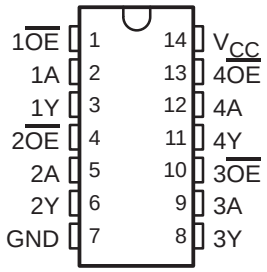
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**D, DB, NS, OR PW PACKAGE**
**(TOP VIEW)**




## description/ordering information

This bus buffer is designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

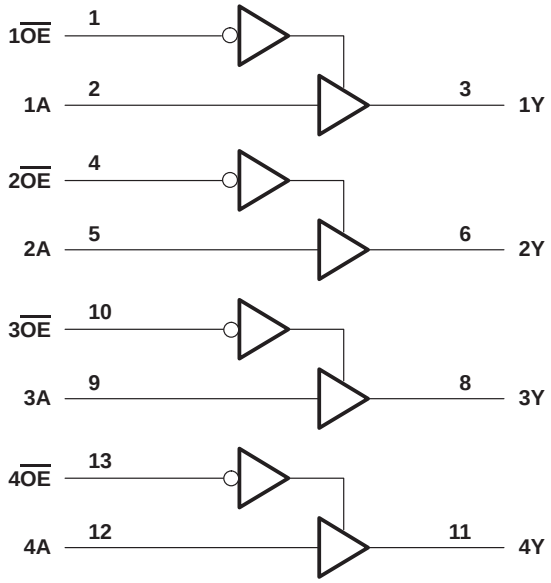
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC − D | Tube | SN74LVT125D | LVT125 |
| | | Tape and reel | SN74LVT125DR | |
| | SOP − NS | Tape and reel | SN74LVT125NSR | LVT125 |
| | SSOP − DB | Tape and reel | SN74LVT125DBR | LX125 |
| | TSSOP − PW | Tube | SN74LVT125PW | LX125 |
| | | Tape and reel | SN74LVT125PWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) . . . . −0.5 V to 7 V
Current into any output in the low state, $I_O$ . . . . . 128 mA
Current into any output in the high state, $I_O$ (see Note 2) . . . . . 64 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = −100 μA | | $V_{CC}$−0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −8 mA | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −32 mA | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 μA | | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | |
| | | $I_{OL}$ = 64 mA | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | μA |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ or GND | Control inputs | | | ±1 | |
| | | $V_I$ = $V_{CC}$ | Data inputs | | | 1 | |
| | | $V_I$ = 0 | | | | −5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | ±100 | μA |
| $I_{I(hold)}$ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | Data inputs | 75 | | | μA |
| | | $V_I$ = 2 V | | −75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | | 5 | μA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | | −5 | μA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $V_I$ = $V_{CC}$ or GND | $I_O$ = 0, | Outputs high | | 0.12 | 0.19 | mA |
| | | | Outputs low | | 4.5 | 7 | |
| | | | Outputs disabled | | 0.12 | 0.19 | |
| $\Delta I_{CC}$§ | $V_{CC}$ = 3 V to 3.6 V, | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | | | 0.2 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | pF |

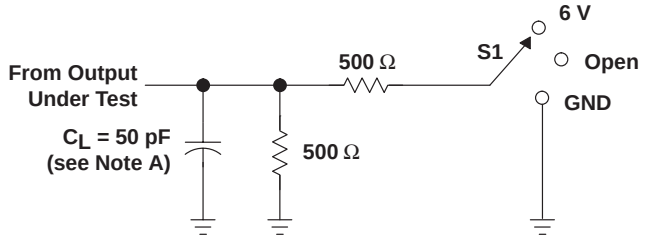
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1 | 2.7 | 4 | | 4.5 | ns |
| $t_{PHL}$ | | | 1 | 2.9 | 3.9 | | 4.9 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1 | 3.4 | 4.7 | | 6 | ns |
| $t_{PZL}$ | | | 1.1 | 3.4 | 4.7 | | 6.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.8 | 3.7 | 5.1 | | 5.7 | ns |
| $t_{PLZ}$ | | | 1.3 | 2.6 | 4.5 | | 4 | |

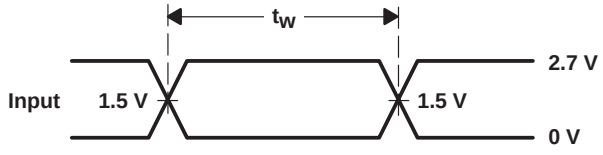
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION

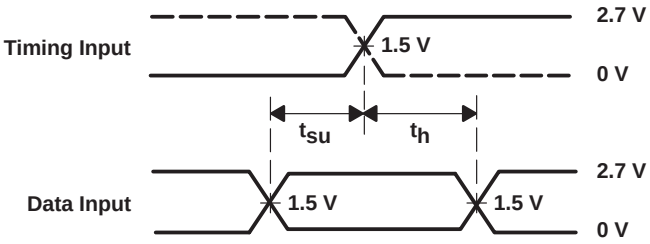



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

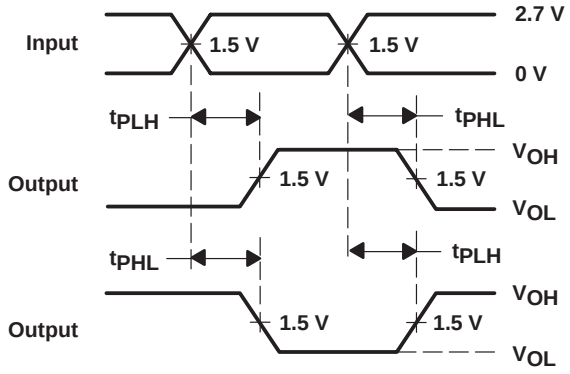
LOAD CIRCUIT FOR OUTPUTS



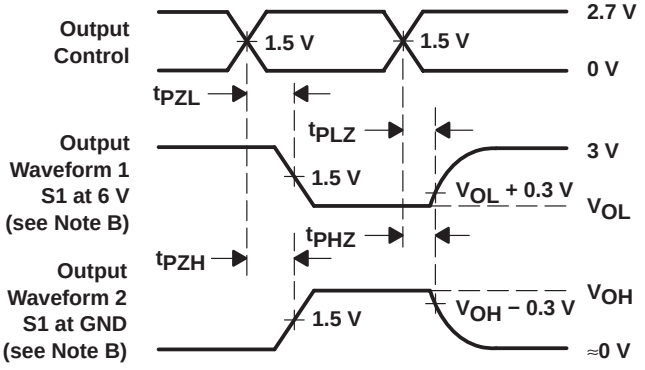

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVT125D | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125D.B | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125D1G4 | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125D1G4.B | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125DBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125DBR.B | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125DBR1G4 | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125DBR1G4.B | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125DR.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125DRG4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125NSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125NSR.B | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVT125 |
| SN74LVT125PW | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125PW.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125PWR.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |
| SN74LVT125PWRG4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LX125 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVT125 :**

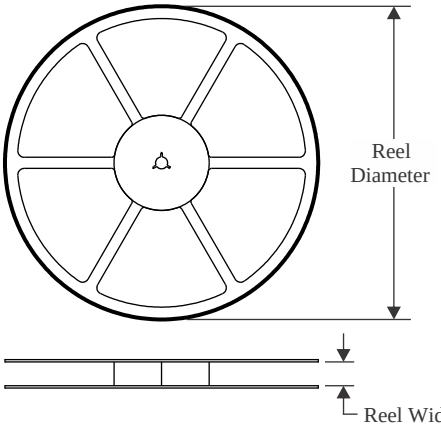
- Automotive : SN74LVT125-Q1
- Enhanced Product : SN74LVT125-EP

NOTE: Qualified Version Definitions:

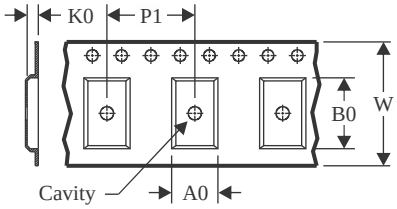
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

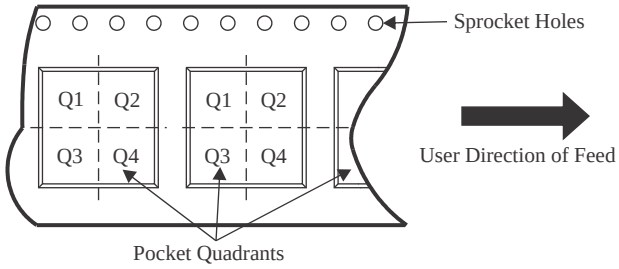



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

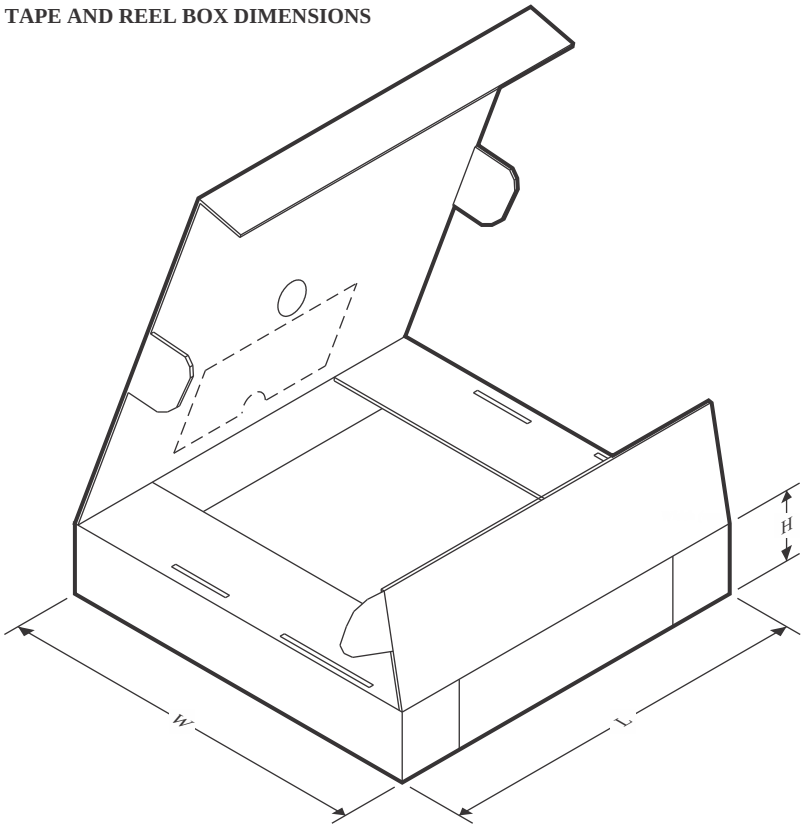
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVT125DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVT125DBR1G4 | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVT125NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVT125PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

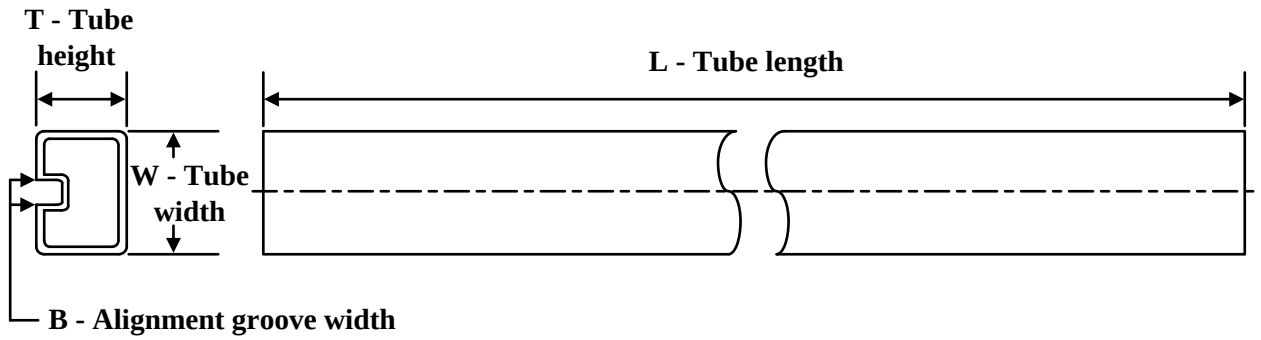
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVT125DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVT125DBR1G4 | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LVT125NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVT125PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

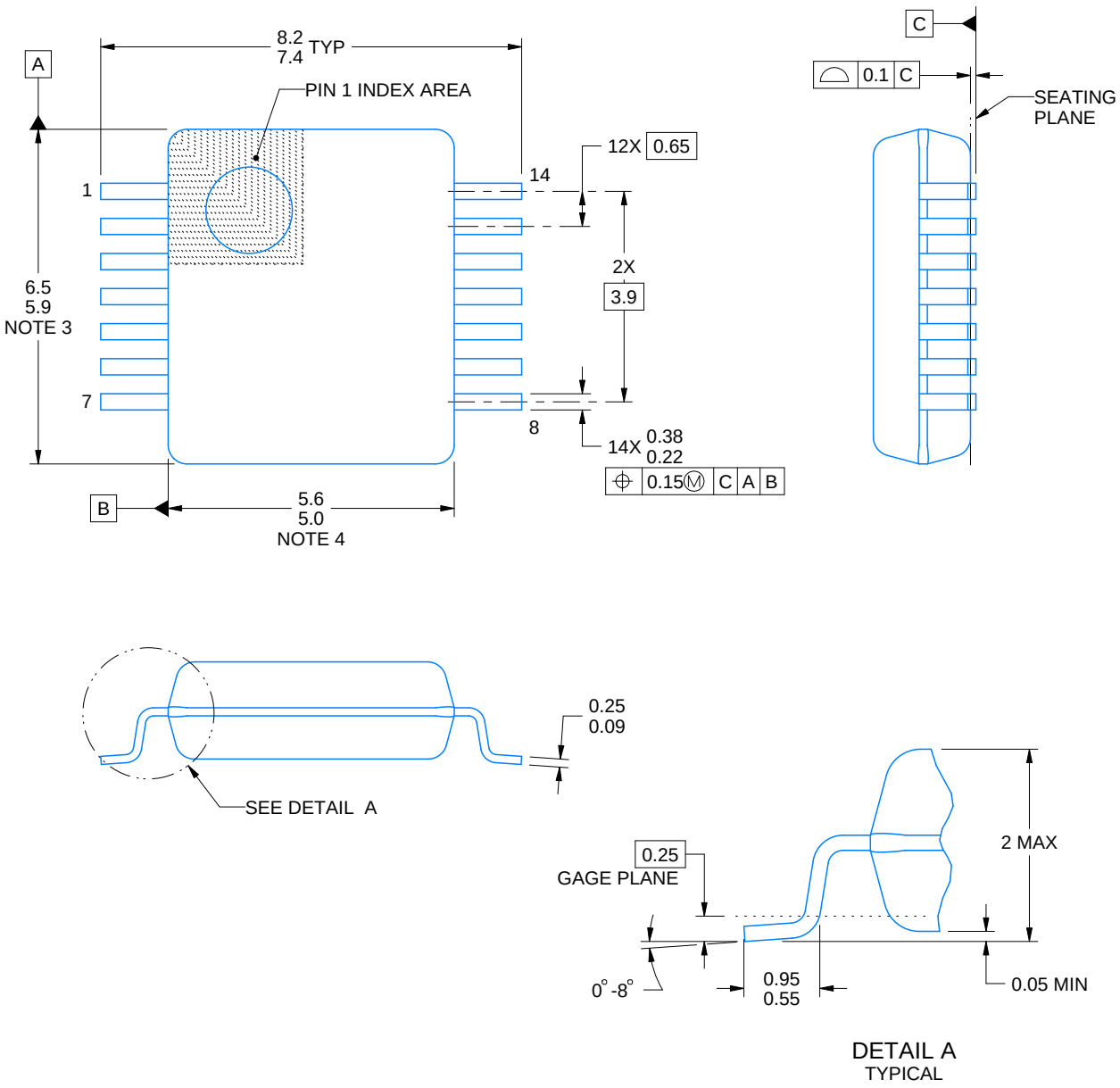
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LVT125D | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN74LVT125D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVT125D.B | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN74LVT125D.B | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVT125D1G4 | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN74LVT125D1G4.B | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN74LVT125PW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVT125PW.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

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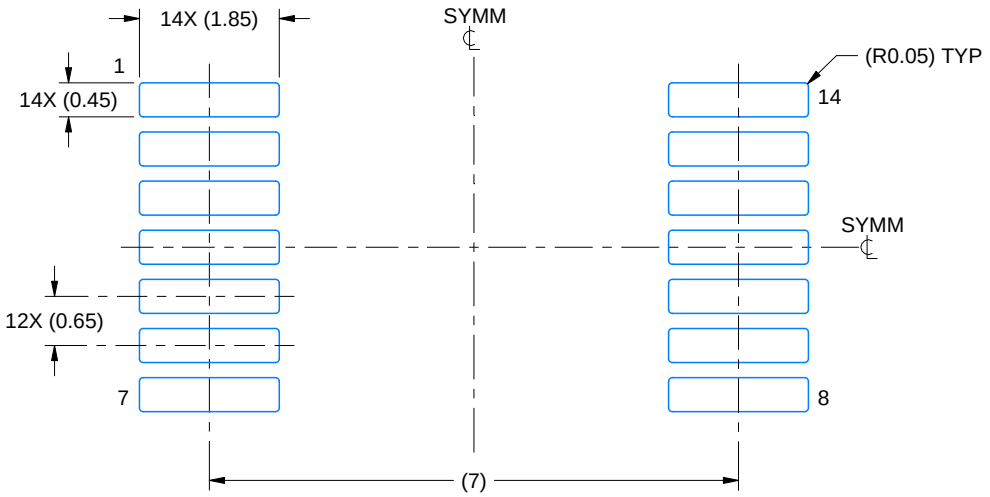
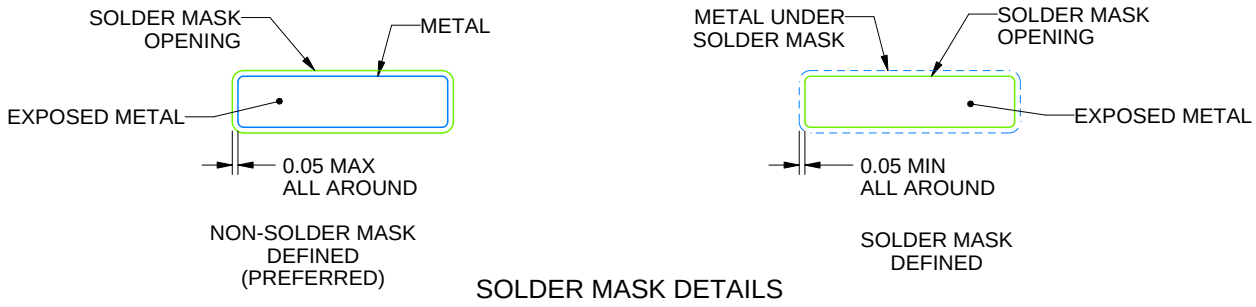
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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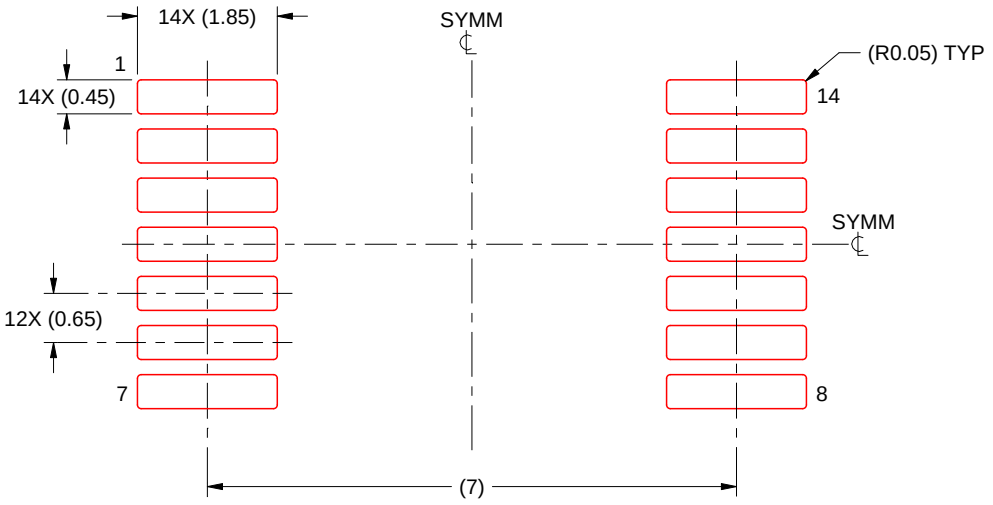
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

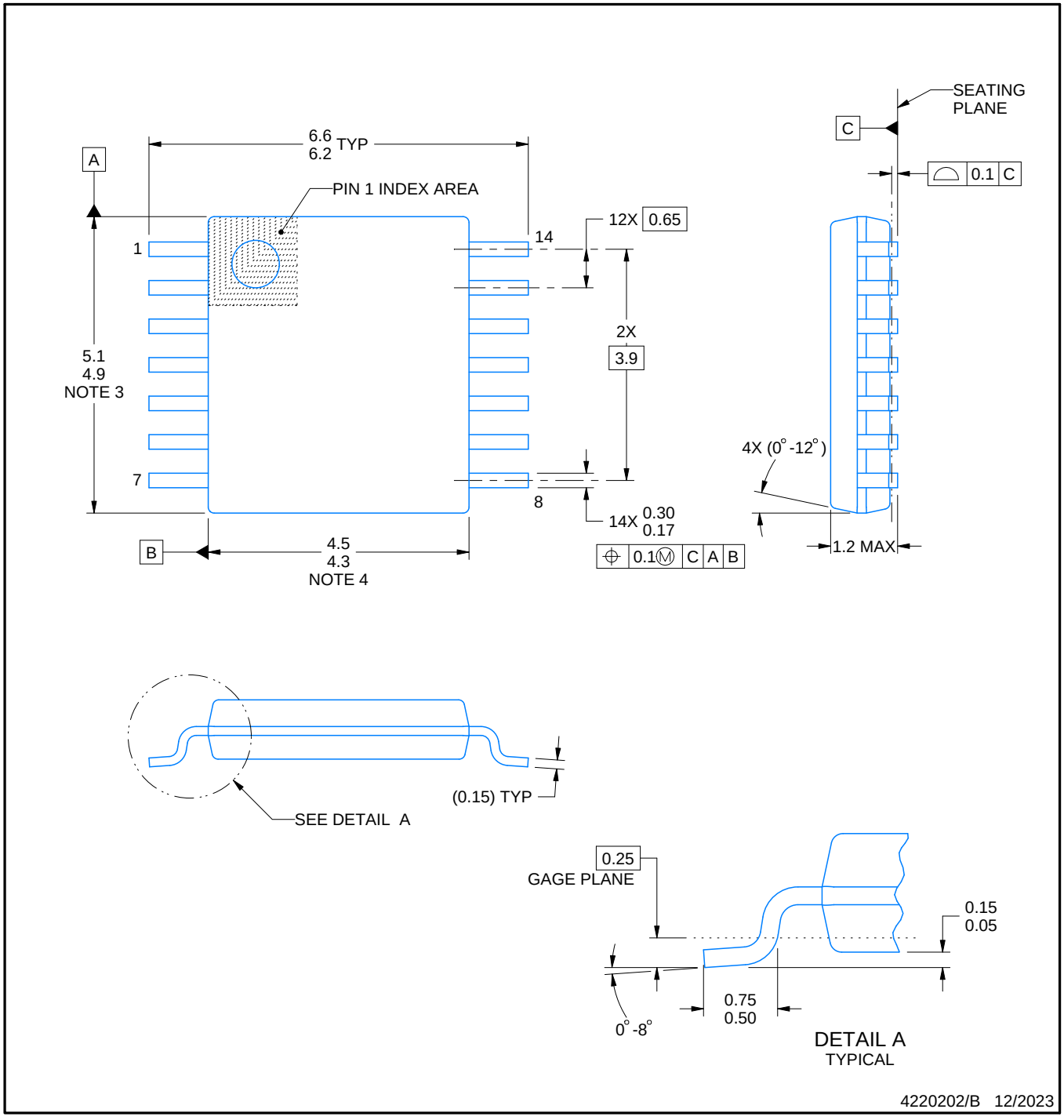
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

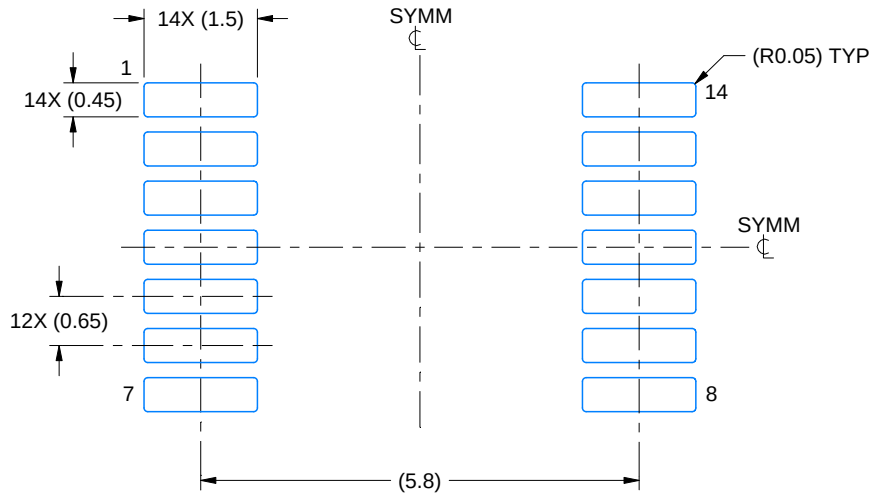
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

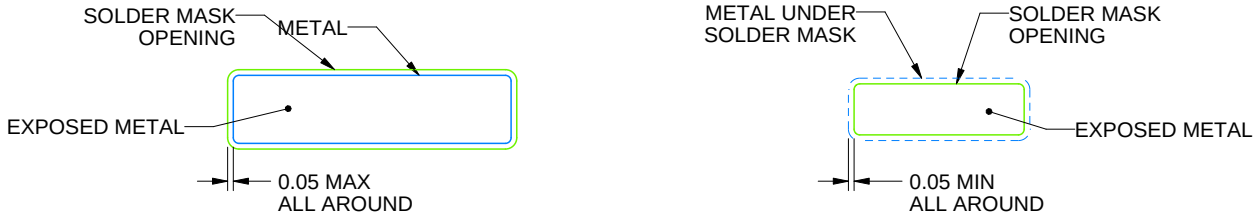



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

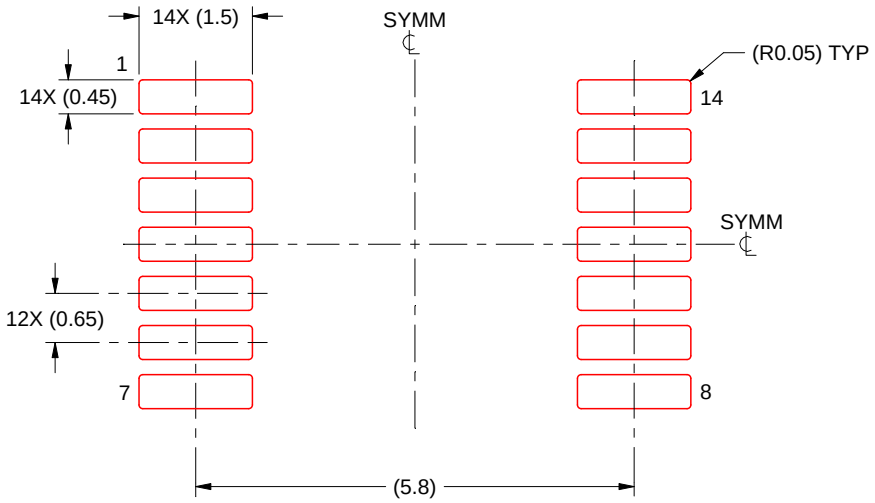



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

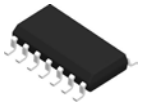



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

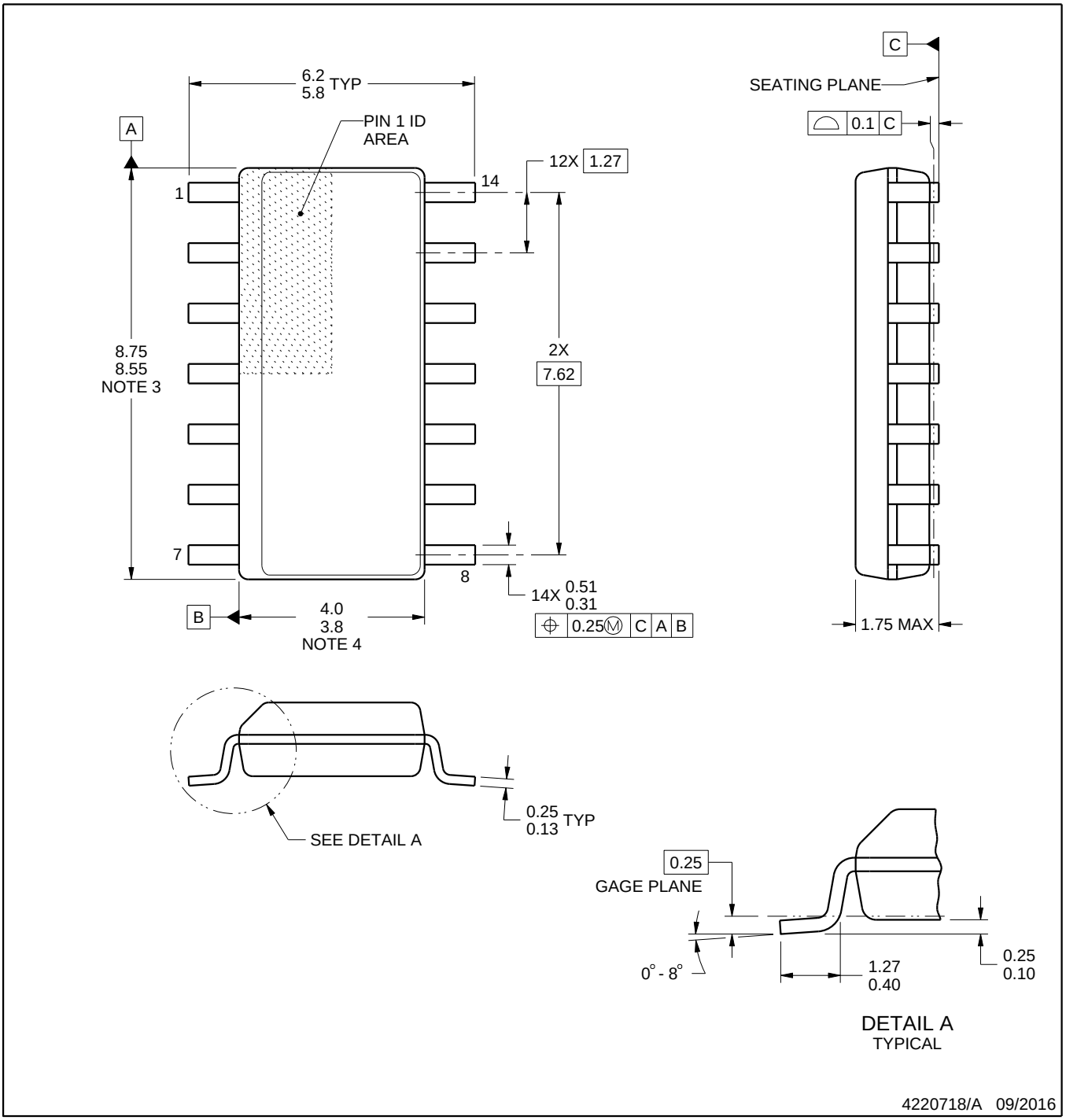


# PACKAGE OUTLINE

## D0014A

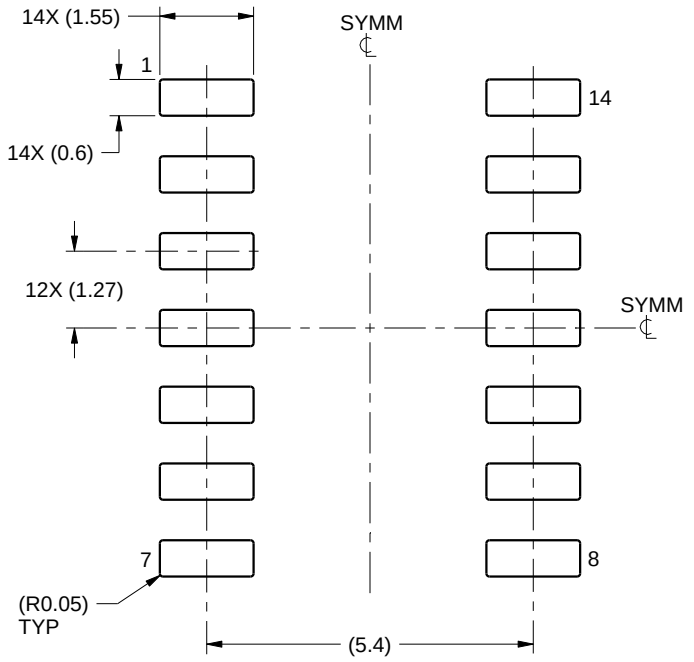
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

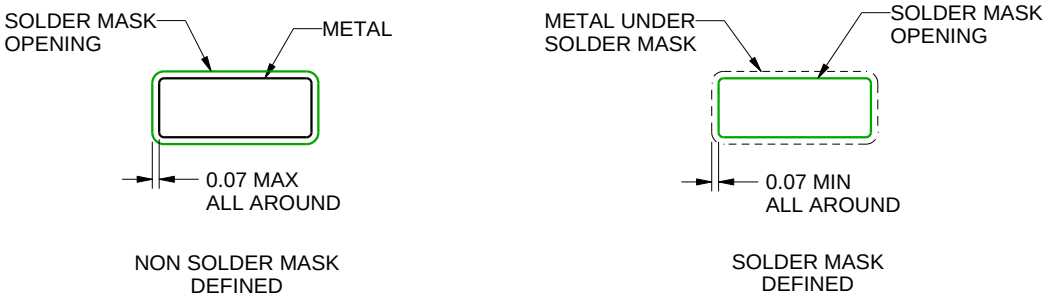



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

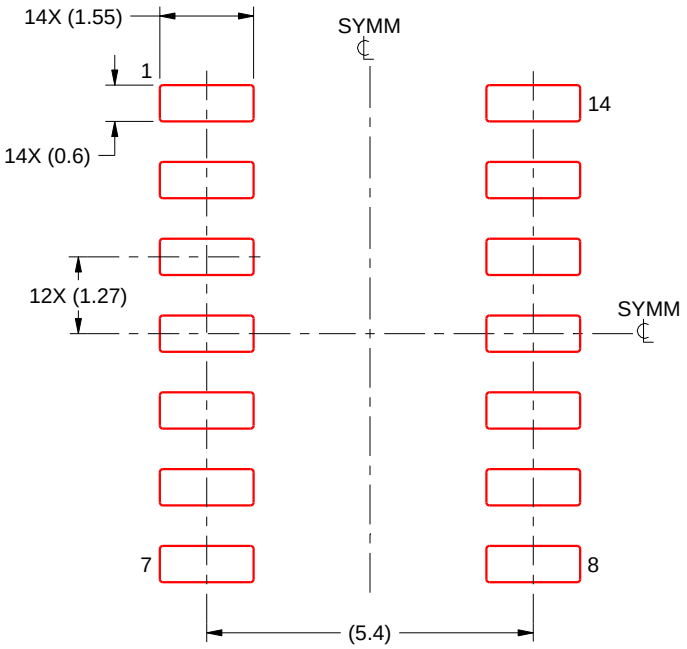
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

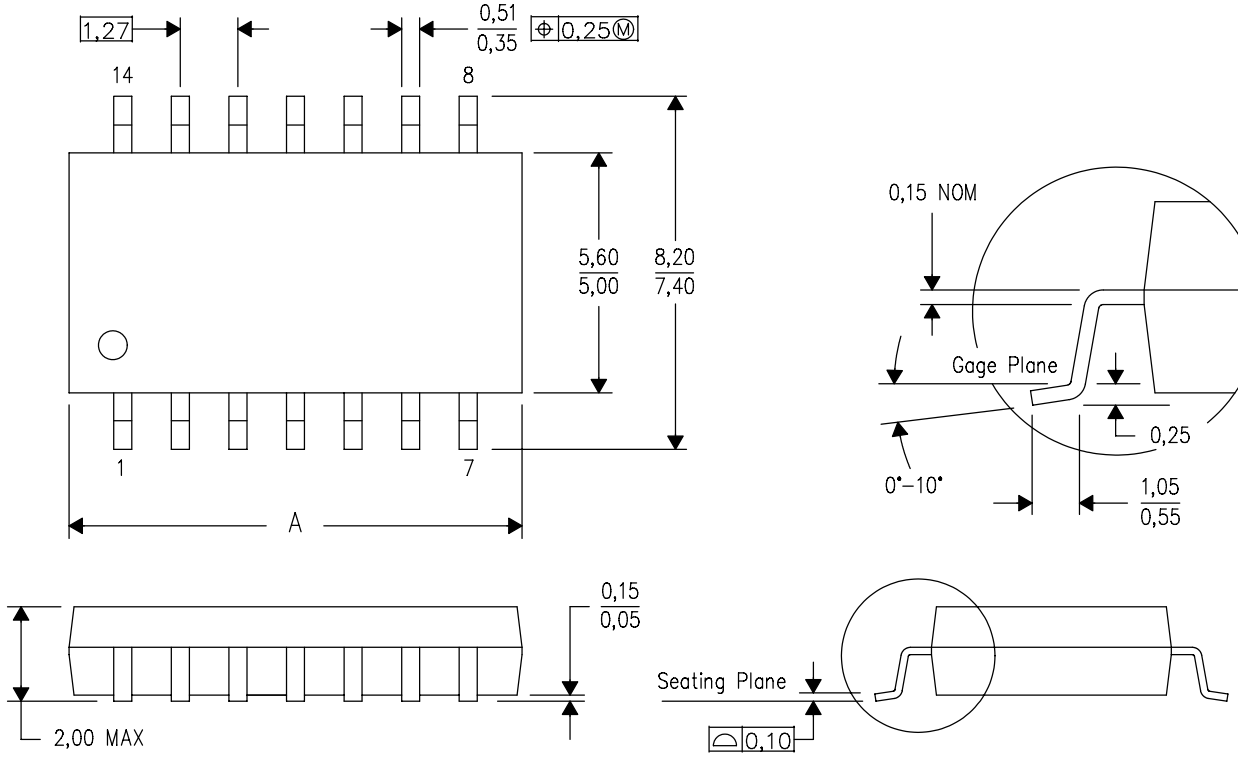
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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