SN74LVCC3245A 可変出力電圧、3 ステート出力、オクタル・バス・トランシーバ

1 特長

- 双方向電圧変換
- 2.3V～3.6V (A ポート)、3V～5.5V (B ポート)
- V_{CCA} 電圧基準の制御入力 V_{IH}/V_{IL} レベル
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、荷電デバイス・モデル (C101)

2 アプリケーション

- レベル変換
- USB
- インターフェイス
- アナログおよびデジタル・アプリケーション

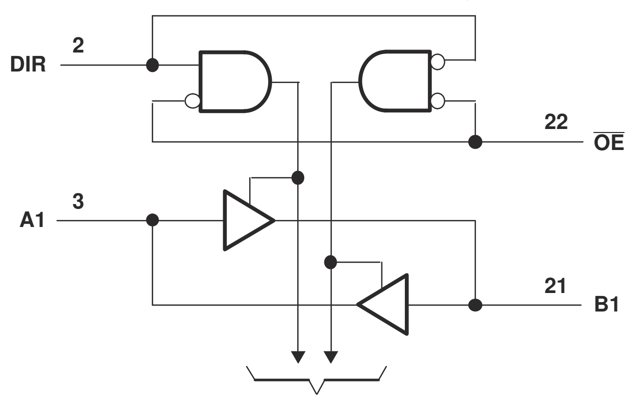
3 概要

SN74LVCC3245A デバイスは、8 ビット (オクタル) 非反転バス・トランシーバで、2 つの独立した電源レールを搭載しています。B ポートは、V_{CCB} をトラッキングするように設計されており、3V～5.5V に対応できます。A ポートは、V_{CCA} をトラッキングするように設計されており、2.3V～3.6V で動作します。これにより、3.3V から 5V のシステム環境への変換とその逆変換、
2.5V から 3.3V のシステム環境への変換とその逆変換が可能です。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74LVCC3245A	DB (SSOP) (24)	8.65mm × 3.90mm
	DW (SOIC、24)	15.40mm × 7.50mm
	DBQ (SSOP、24)	8.20mm × 5.30mm
	NS (SO、24)	15.00mm × 5.30mm
	PW (TSSOP、24)	7.80mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

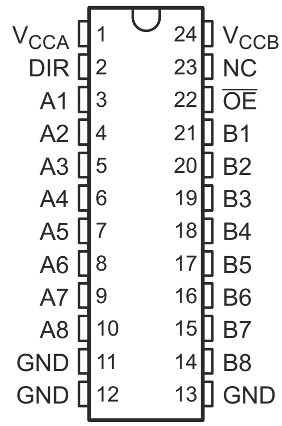
Changes from Revision P (December 2015) to Revision Q (December 2022) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新........ 1
- Added thermal information for DB and PW package........ 6
- Added inclusive terminology........ 15

Changes from Revision O (March 2005) to Revision P (December 2015) **Page**

- 「アプリケーション」セクション、「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加........ 1
- 「注文情報」表を削除........ 1

5 Pin Configuration and Functions



NC – No internal connection

See *セクション 12* for dimensions.

図 5-1. DB, DBQ, DW, NS, or PW Package, 24-Pin SSOP, SOIC, SO, or TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
B1	21	I/O	B1 port
B2	20	I/O	B2 port
B3	19	I/O	B3 port
B4	18	I/O	B4 port
B5	17	I/O	B5 port
B6	16	I/O	B6 port
B7	15	I/O	B7 port
B8	14	I/O	B8 port
DIR	2	I	Dir input
GND	11	—	Ground
	12		
	13		
NC	23	—	Unconnected
$\overline{OE}$	22	I	Output Enable active low
V_{CCA}	1	—	A port power
V_{CCB}	24	—	B port power

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	6	V
V_I	Input voltage	All A ports(2)	–0.5	V_{CCA} + 0.5	V
		All B ports(3)	–0.5	V_{CCB} + 0.5	
		Except I/O ports(2)	–0.5	V_{CCA} + 0.5	
V_O	Output voltage(3)	All A ports	–0.5	V_{CCA} + 0.5	V
		All B ports	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW		46	°C/W
		NS		65	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.
(3) This value is limited to 6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			2.3	3.3	3.6	V
V_{CCB}	Supply voltage			3	5	5.5	V
V_{IHA}	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			

6.3 Recommended Operating Conditions (continued)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{ILA}	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control terminals) (referenced to V_{CCA})	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IL}	Low-level input voltage (control terminals) (referenced to V_{CCA})	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{IA}	Input voltage			0		V_{CCA}	V
V_{IB}	Input voltage			0		V_{CCB}	V
V_{OA}	Output voltage			0		V_{CCA}	V
V_{OB}	Output voltage			0		V_{CCB}	V
I_{OHA}	High-level output current	2.3 V	3 V			–8	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OHB}	High-level output current	2.3 V	3 V			–12	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
I_{OLB}	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
T_A	Operating free-air temperature			–40		85	°C

6.4 Thermal Information

THERMAL METRIC[(1)] [(4)]		SN74LVCC3245A DB (SSOP) 24 PINS	SN74LVCC3245A DBQ (SSOP) 24 PINS	SN74LVCC3245A PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	61	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	44.8	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	34.5	55.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.8	9.5	6.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.3	37.2	55.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –8 mA	2.3 V	3 V	2			
		I_{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	3.6 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I_{OZ} [(1)]	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}	3.6 V	3.6 V		±0.5	±5	µA
I_{CCA}	B to A	A port = V_{CCA} or GND, $I_O = 0$	3.6 V	Open		5	50	µA
		B port = V_{CCB} or GND, $I_O = 0$	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, $I_O = 0$	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
ΔI_{CCA} (2)	A port	$V_I = V_{CCA} - 0.6$ V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	$V_I = V_{CCA} - 0.6$ V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	$V_I = V_{CCA} - 0.6$ V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB} (2)	B port	$V_I = V_{CCB} - 2.1$ V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open	Open		4		pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 through 図 7-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}, V_{CCB}	MIN	MAX	UNIT
t_{PHL}	A	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.4	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	6	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.1	
t_{PLH}	A	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.1	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	5.3	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.2	
t_{PHL}	B	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	11.2	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	5.8	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.4	
t_{PLH}	B	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.6	
t_{PZL}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	14.5	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	9.2	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.7	

6.6 Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 through 図 7-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}, V_{CCB}	MIN	MAX	UNIT
t_{PZH}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	12.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	9.5	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.5	
t_{PZL}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	13	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	8.1	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.2	
t_{PZH}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	12.8	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	8.4	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.9	
t_{PLZ}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.1	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.6	
t_{PHZ}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.3	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7.8	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.9	
t_{PLZ}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	8.8	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7.3	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.5	
t_{PHZ}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	8.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.9	

6.7 Operating Characteristics

V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50, f = 10 MHz	38	pF
		Outputs disabled		4.5	

6.8 Typical Characteristics

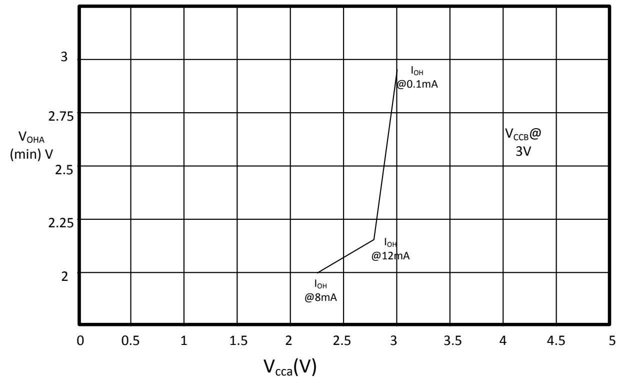
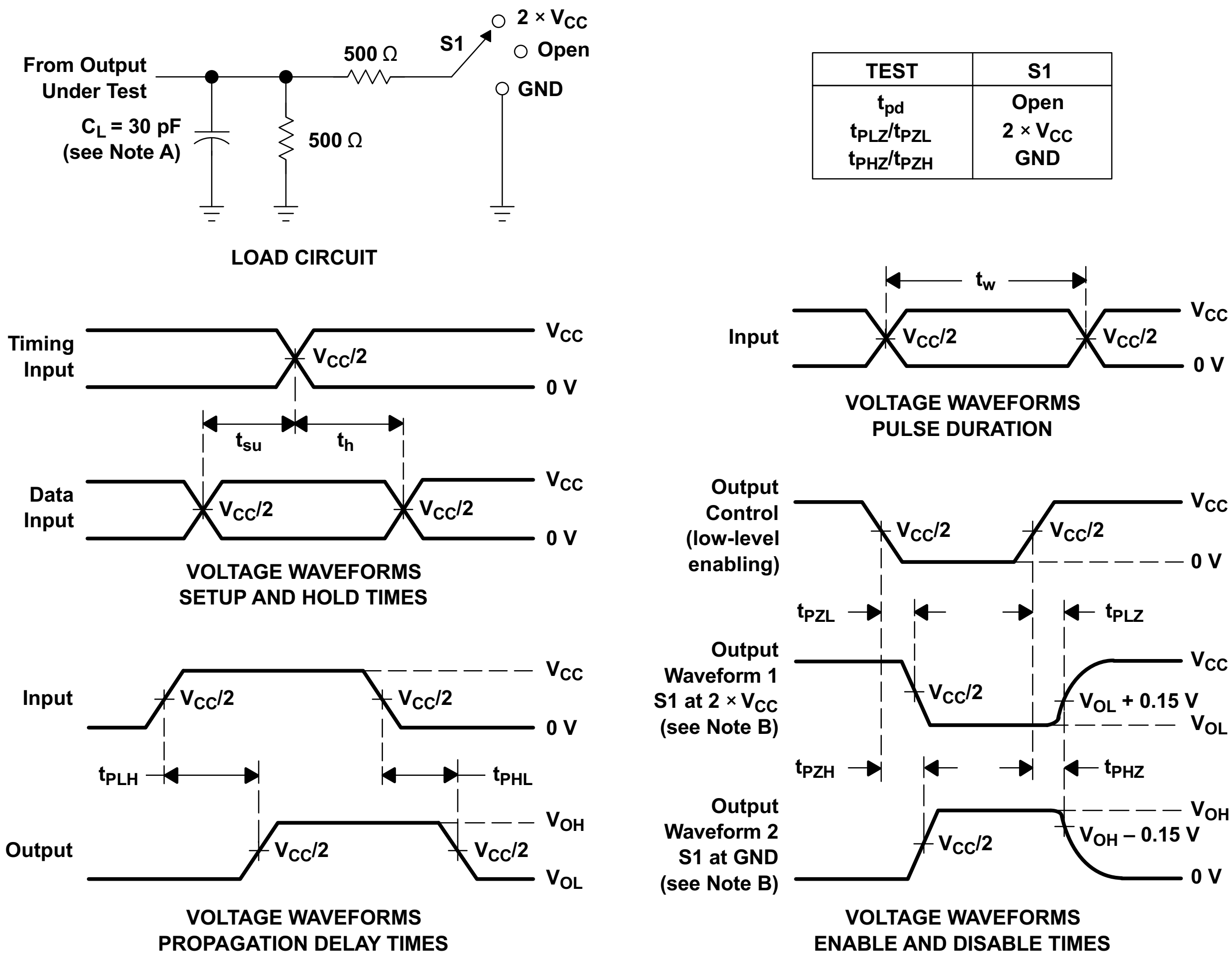


図 6-1. $V_{OHA(min)}$ VS V_{CCA}

7 Parameter Measurement Information

7.1 A Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)

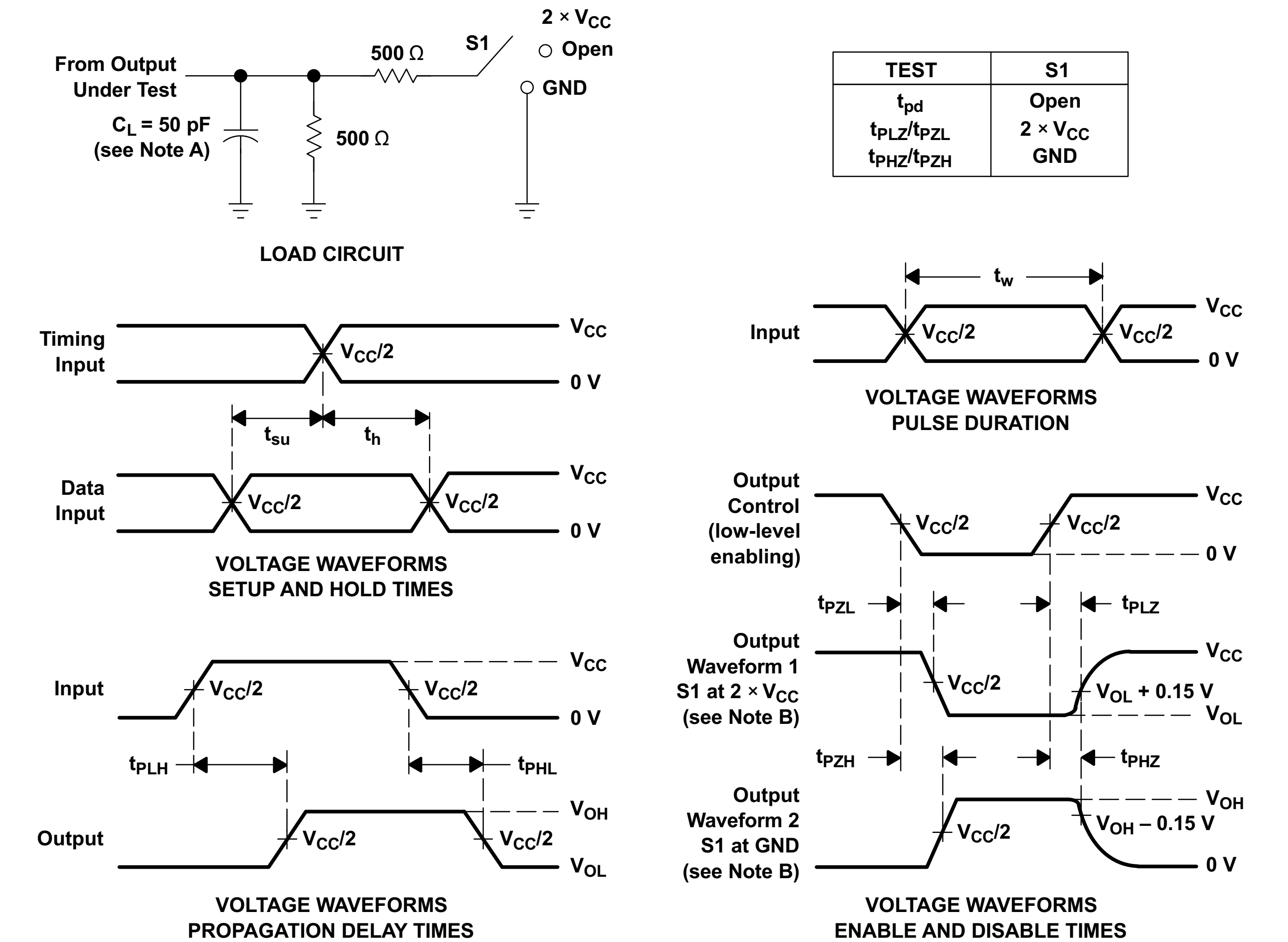


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and $t_{PZH}$are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

7.2 B Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

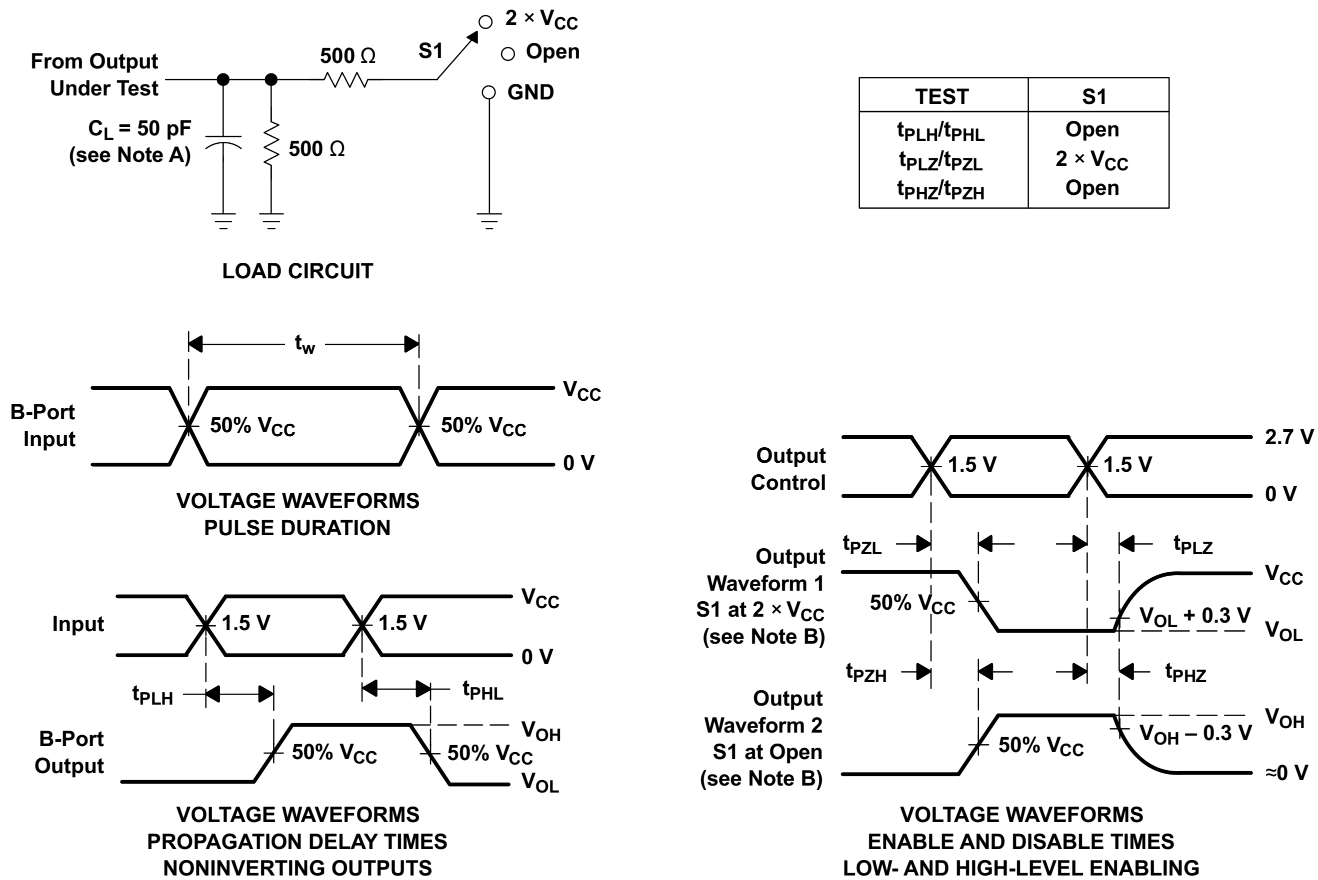
F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

図 7-2. Load Circuit and Voltage Waveforms

7.3 B Port (V_{CCA} = 3.6 V and V_{CCB} = 5.5 V)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

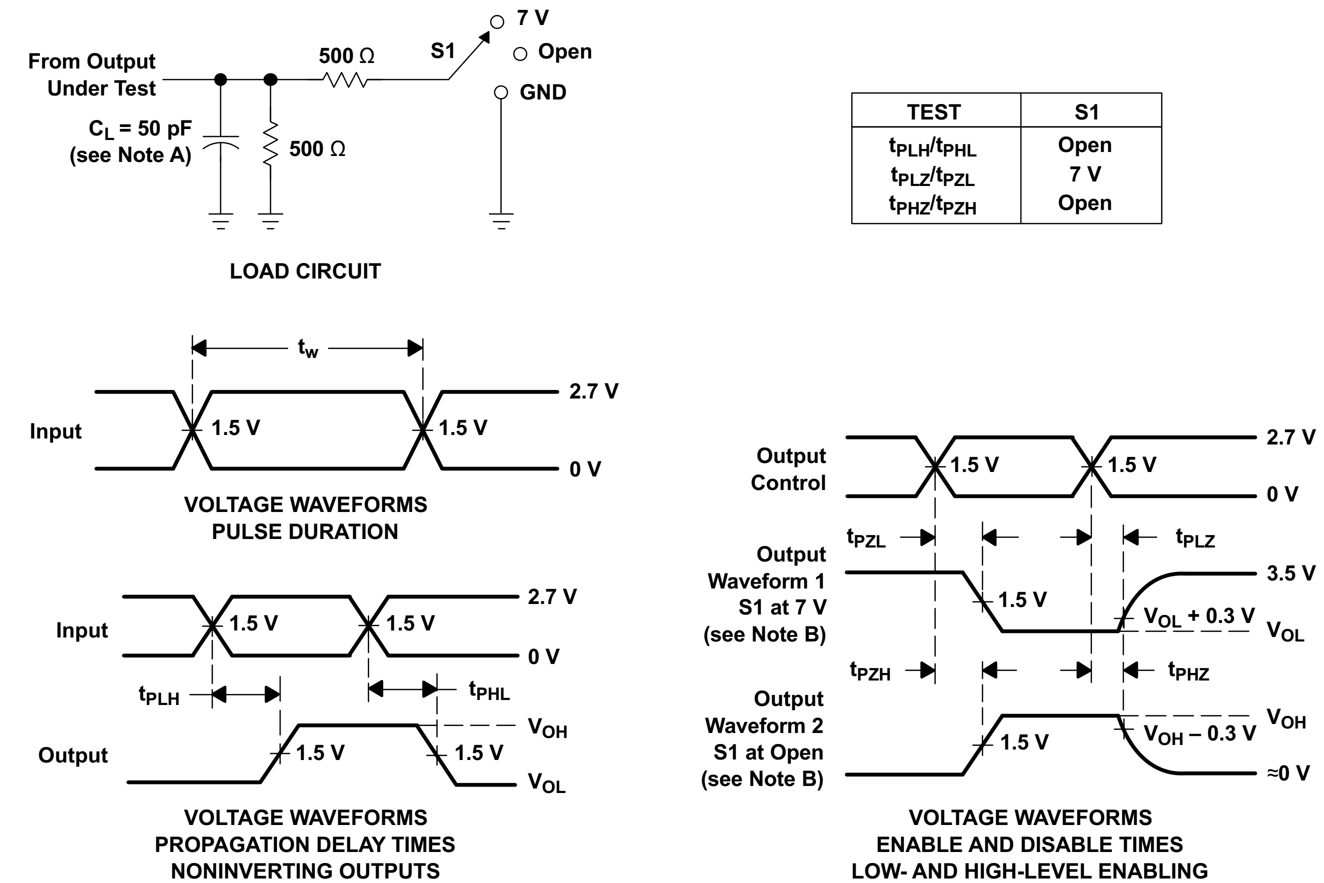
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

図 7-3. Load Circuit and Voltage Waveforms

7.4 A and B Port (V_{CCA} and V_{CCB} = 3.6 V)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

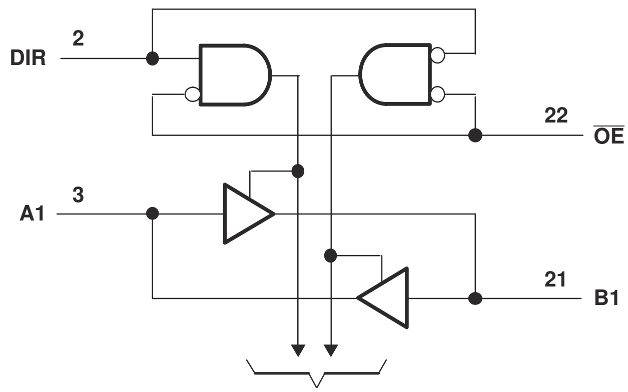
図 7-4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

8.2 Functional Block Diagram



8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to V_{CCA} Voltage.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LVCC3245A.

表 8-1. Function Table (Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

9.2 Typical Application

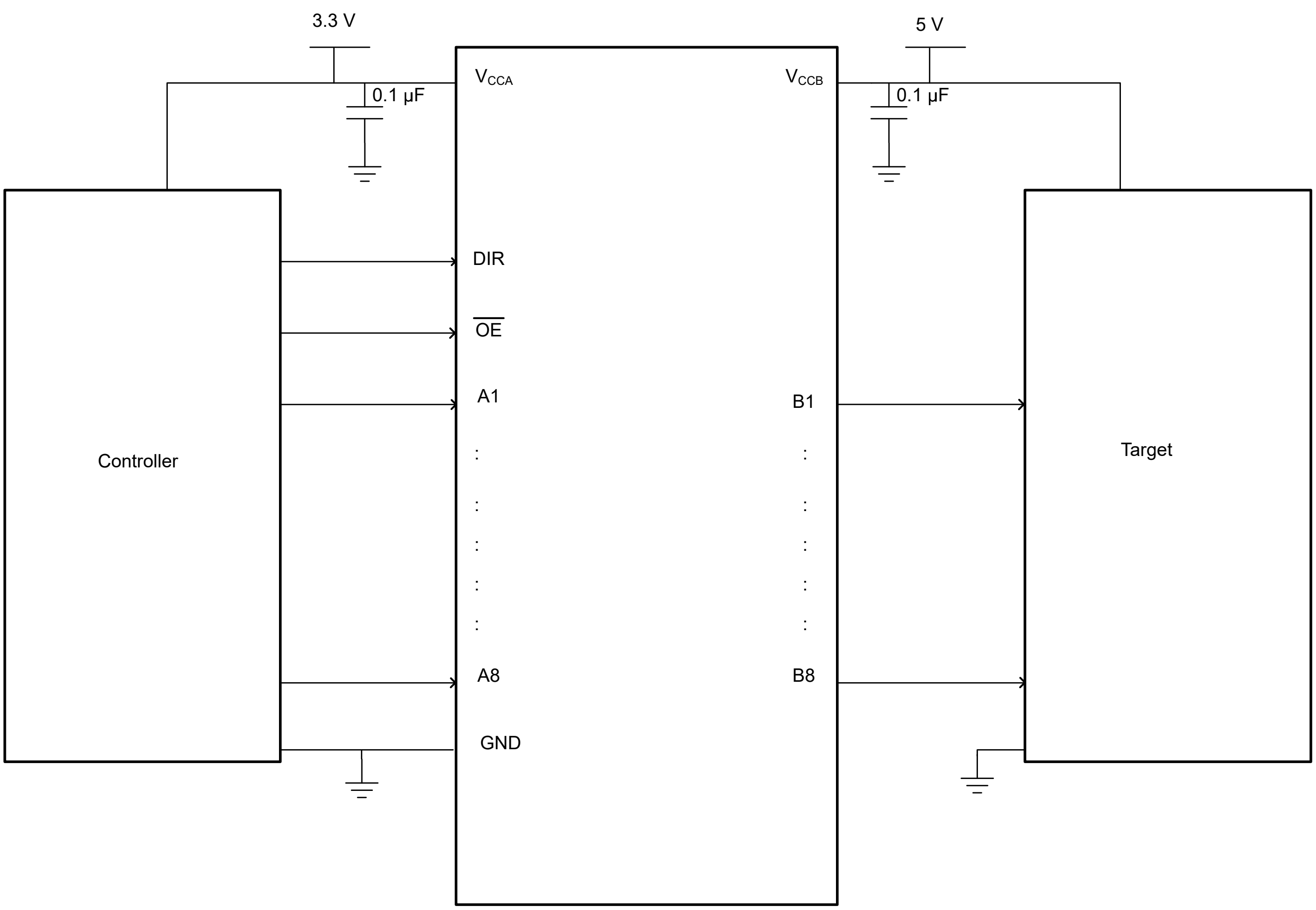


図 9-1. Typical Application

9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of controller with signals at 3.3 V to target operating at 5 V. The $\overline{OE}$ pin is low and DIR pin is 3.3-V high.

9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Absolute Maximum Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - All the voltages on A and B ports should not exceed above V_{CCA} or V_{CCB} to prevent the biasing of Electrostatic discharge (ESD) diodes.

9.2.3 Application Curve

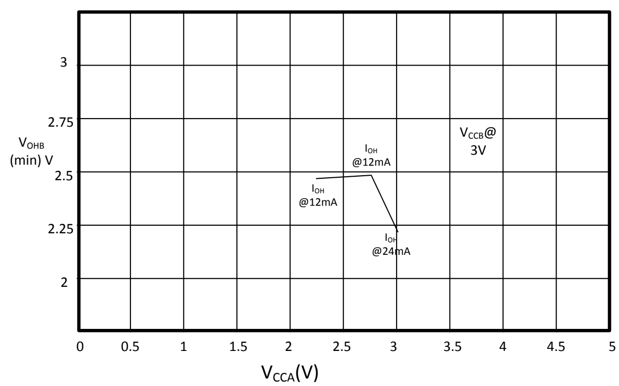


図 9-2. $V_{OHB(min)}$ vs V_{CCA}

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

10.2 Layout Example

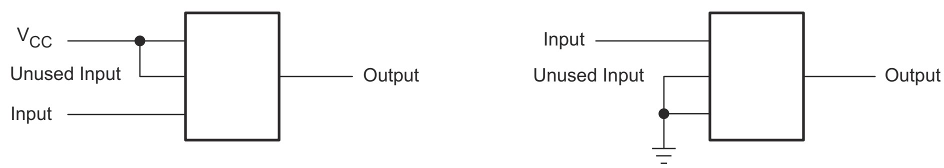


図 10-1. Layout Example

10.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

For more information, refer to *Voltage-Level-Translation Devices* application note.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Voltage-Level-Translation Devices*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.4 Trademarks

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11.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVCC3245ADBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A
SN74LVCC3245ADBQR.B	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A
SN74LVCC3245ADBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245ADBR.A	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245ADBR.B	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245ADBRE4	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245ADBRG4	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245ADW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADW.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWE4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWG4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWRG4	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ADWRG4.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ANSR	Active	Production	SOP (NS) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245ANSR.B	Active	Production	SOP (NS) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A
SN74LVCC3245APW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWRE4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWT	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWT.B	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A
SN74LVCC3245APWTG4	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

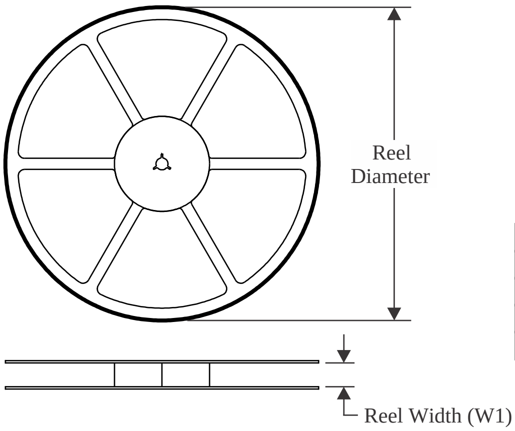
- Enhanced Product : SN74LVCC3245A-EP

NOTE: Qualified Version Definitions:

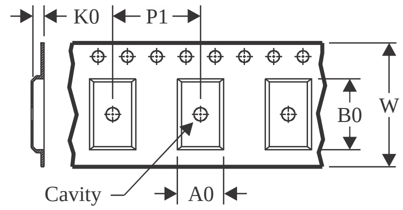
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

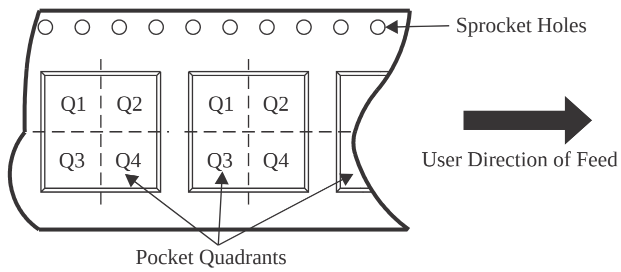


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

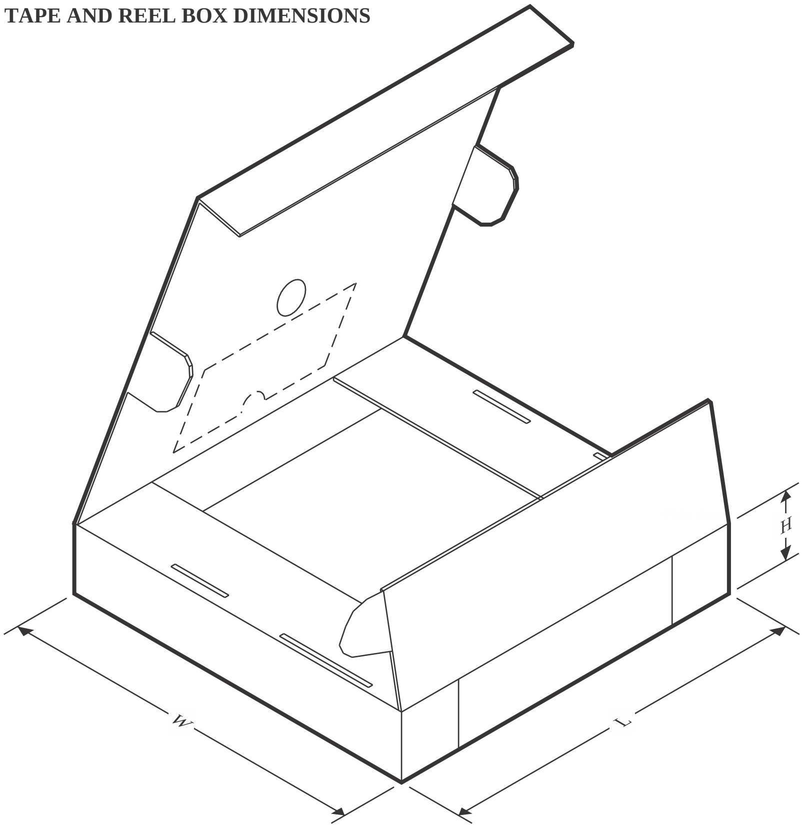
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SOP	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

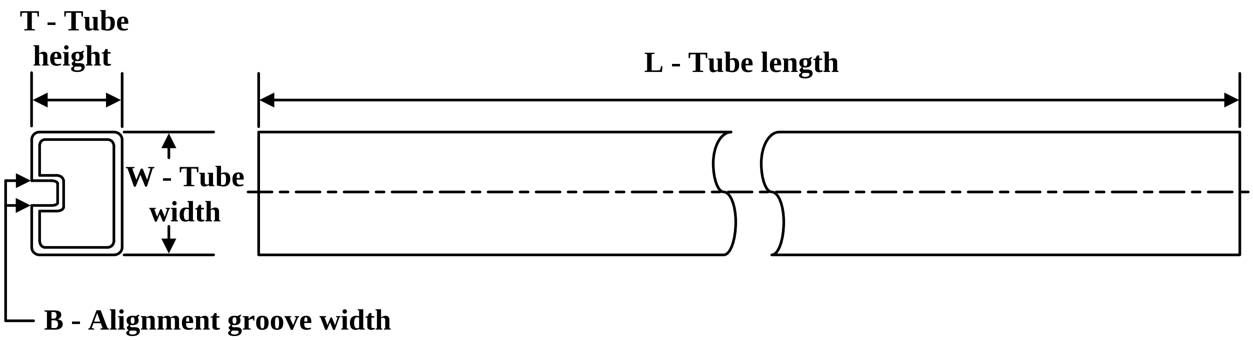
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ANSR	SOP	NS	24	2000	356.0	356.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74LVCC3245APWT	TSSOP	PW	24	250	353.0	353.0	32.0

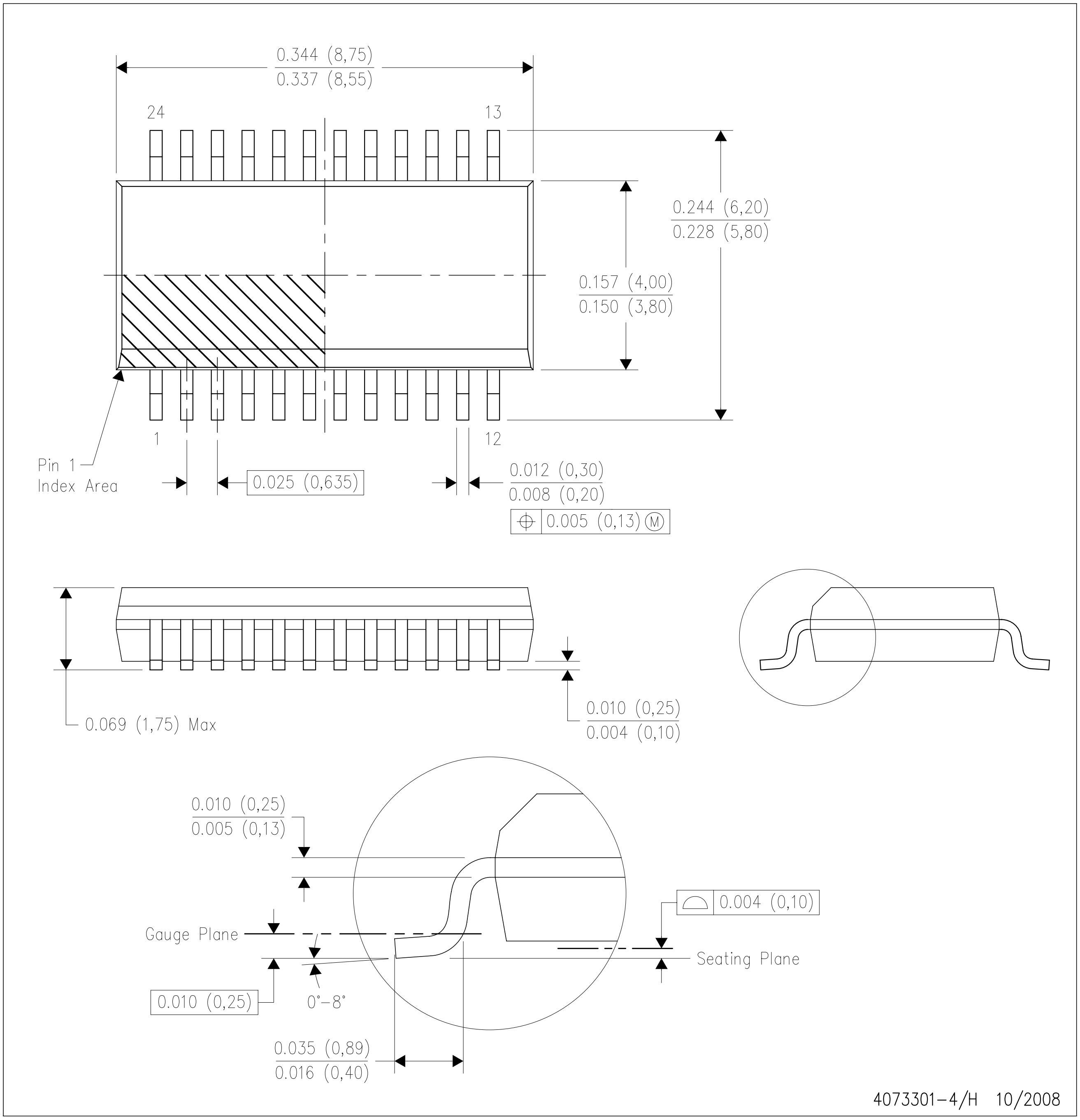
TUBE



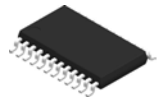
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVCC3245ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245ADWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245ADWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVCC3245APW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



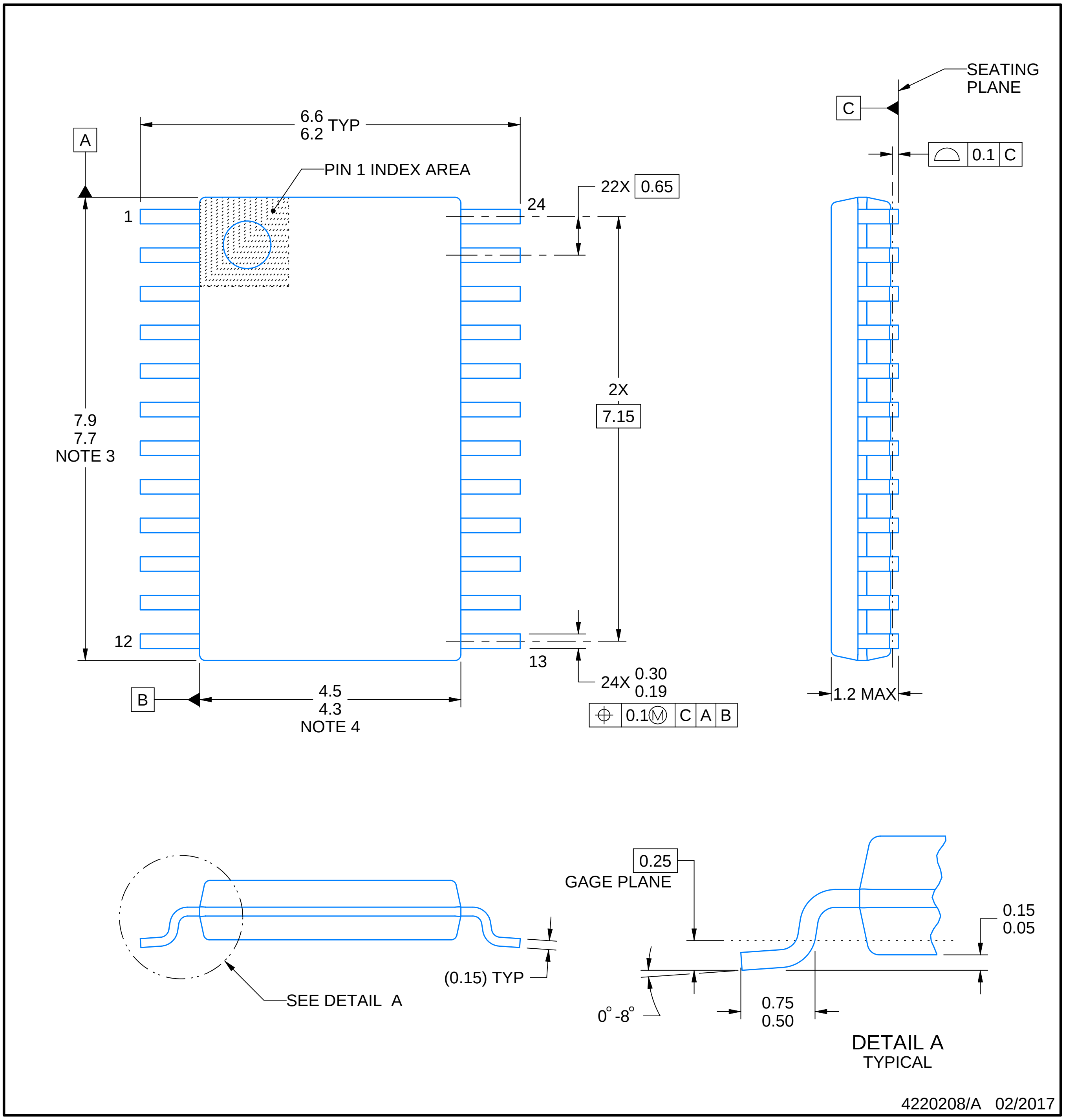
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.



PACKAGE OUTLINE

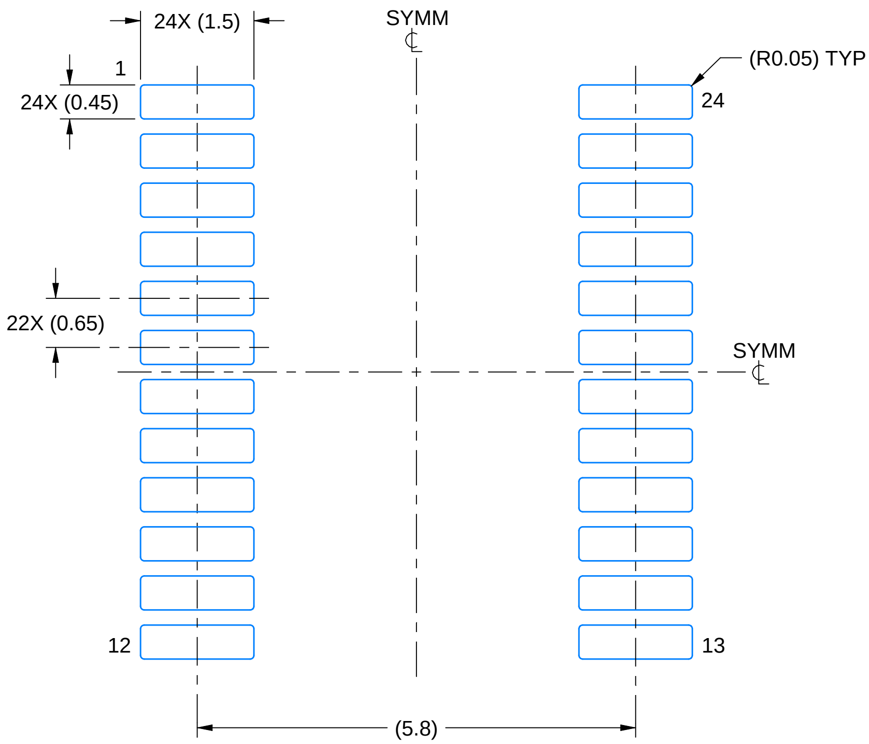
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

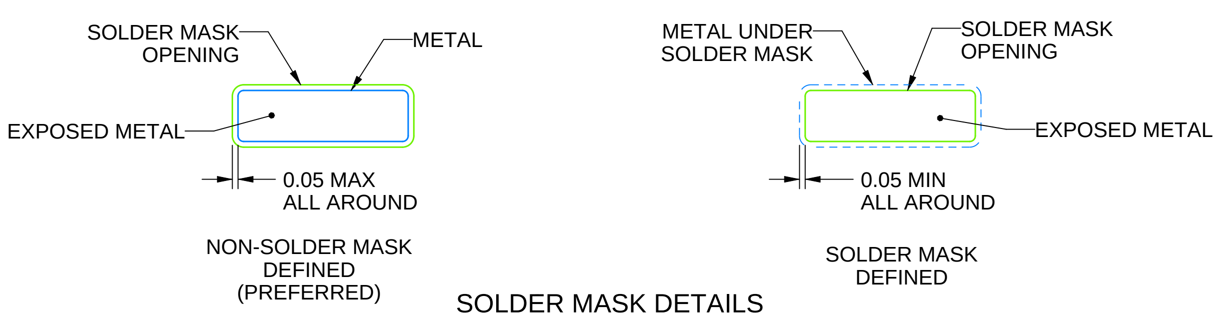


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

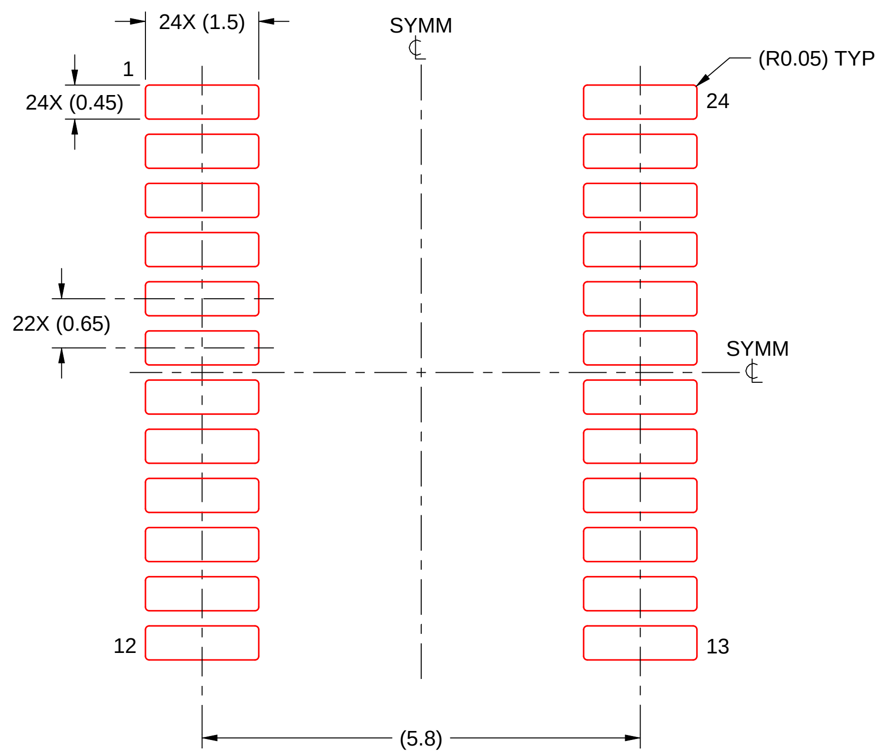


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

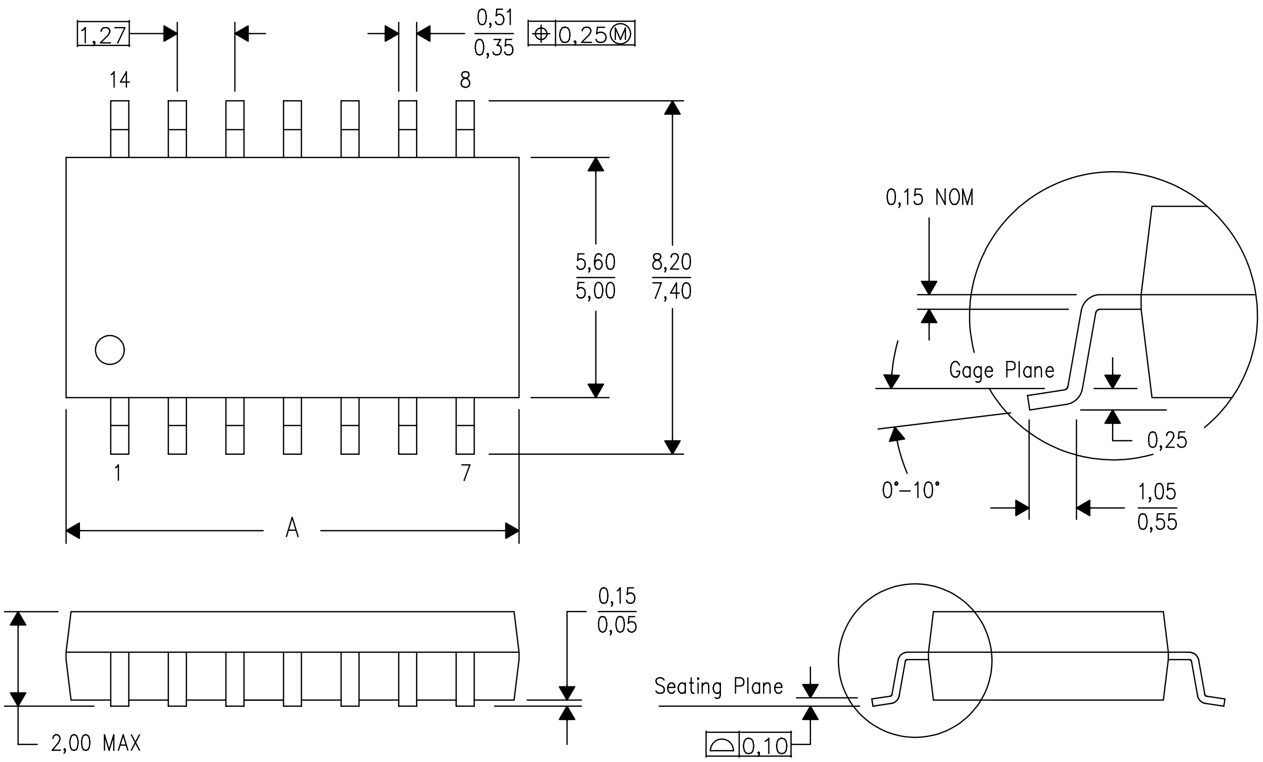
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

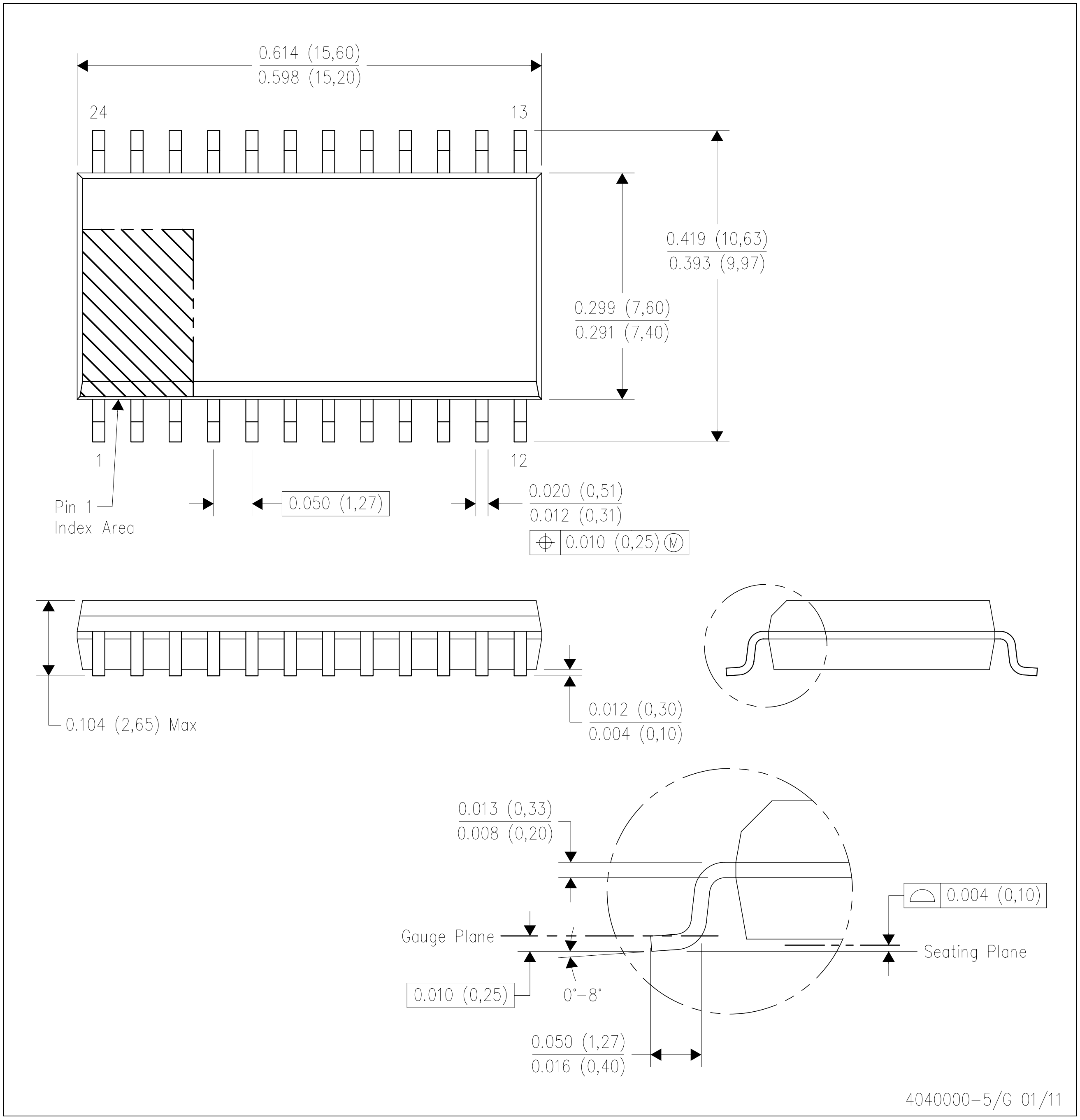


PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

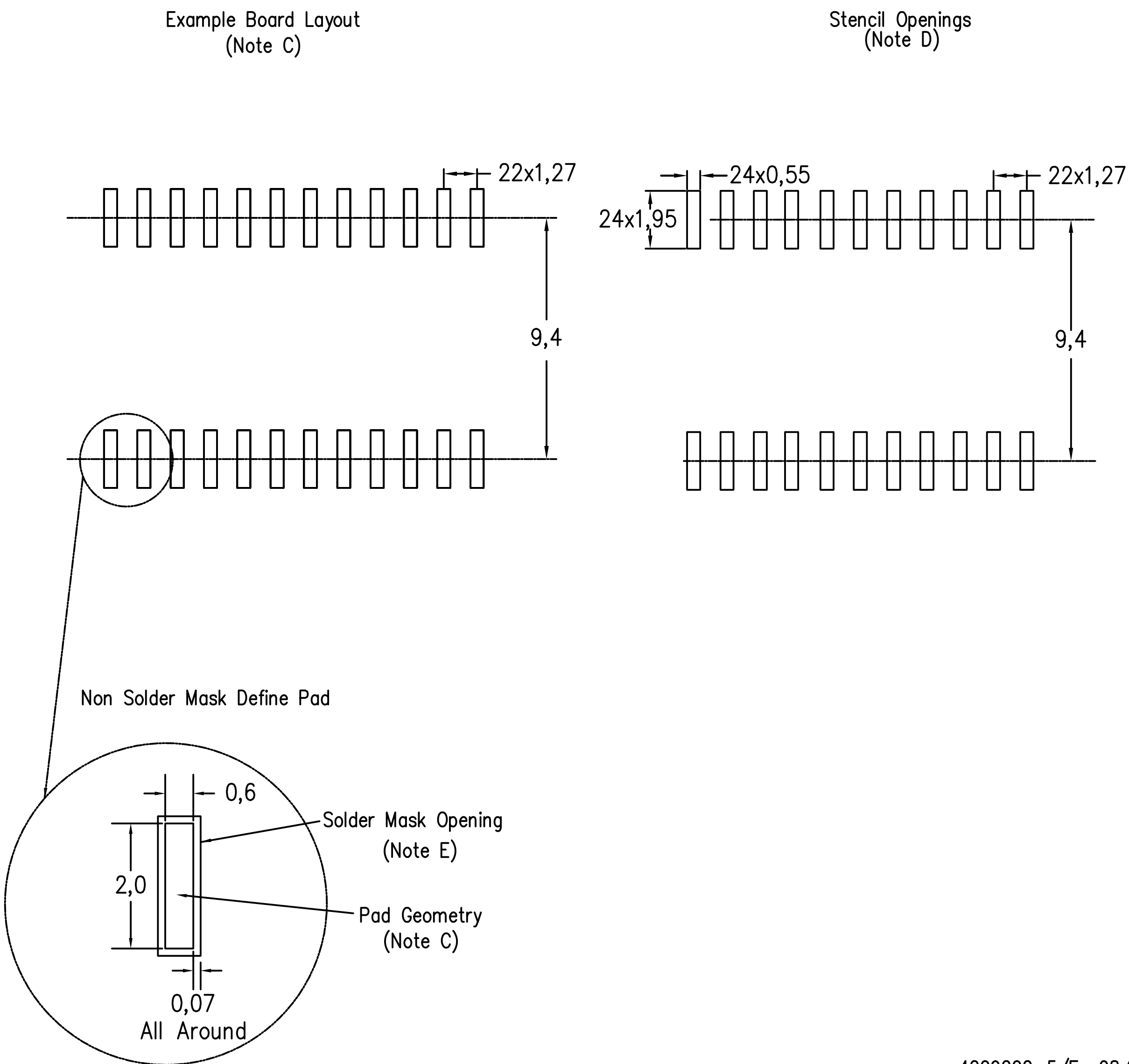
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

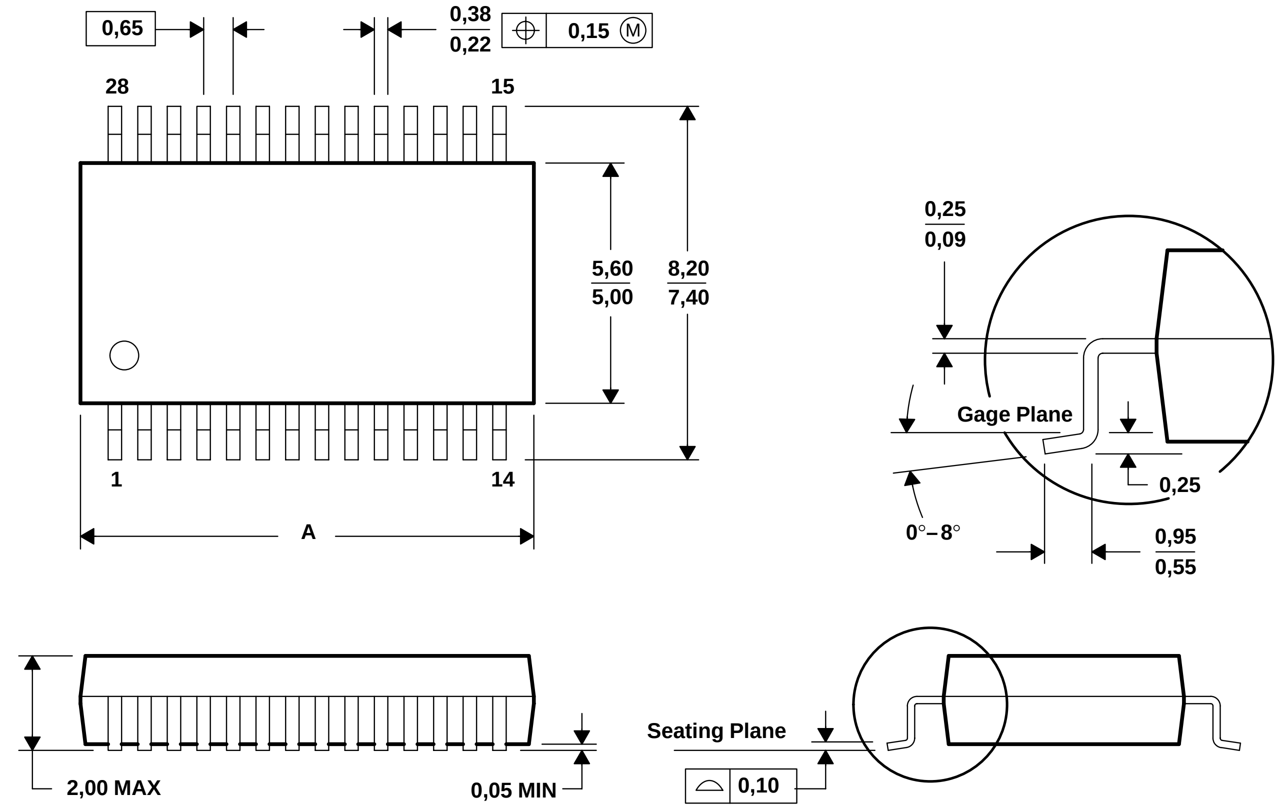


4209202–5/F 08/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

重要なお知らせと免責事項