SN74LVC2G02 デュアル 2 入力の正論理 NOR ゲート

1 特長

- テキサス・インスツルメンツの NanoFree™パッケージで供給
- 5V V_{CC} 動作をサポート
- 5.5V までの入力電圧に対応
- 最大 t_{pd}：4.9ns (3.3V 時)
- 低消費電力、最大 I_{CC}：10µA
- 3.3V において±24mA の出力駆動能力
- 標準 V_{OLP} (出力グランド・バウンス) < 0.8V (V_{CC} = 3.3V、T_A = 25°C)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2V (V_{CC} = 3.3V、T_A = 25°C)
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- AV レシーバ
- オーディオ・ドック：ポータブル
- ブルーレイ・プレーヤおよびホーム・シアター
- 組み込み PC
- MP3 プレーヤおよびレコーダ (携帯用オーディオ)
- パーソナル・デジタル・アシスタント (PDA)
- 電源：テレコム/サーバーの AC/DC 電源：シングル・コントローラ：アナログおよびデジタル
- ソリッド・ステート・ドライブ (SSD)：クライアントおよびエンタープライズ
- テレビ：LCD、デジタル、高解像度 (HD)
- タブレット：エンタープライズ
- ビデオ・アナリティクス：サーバー
- ワイヤレス・ヘッドセット、キーボード、マウス

3 概要

このデュアル 2 入力の正論理 NOR ゲートは、1.65V～5.5V の V_{CC} で動作するよう設計されています。

SN74LVC2G02 デバイスは、ブール関数 $Y = \overline{A + B}$ または $Y = \overline{A} \times \overline{B}$ を正論理で実行します。

ダイをパッケージとして使用する NanoFree™ パッケージ技術は、IC パッケージの概念を大きく覆すものです。

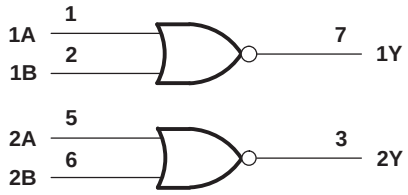
このデバイスは、I_{off}を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN74LVC2G02DCT	SSOP (8)	2.95mm × 2.8mm
SN74LVC2G02DCU	VSSOP (8)	2.3mm × 2.0mm
SN74LVC2G02YZP	DSBGA (8)	1.91mm × 0.91mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 6
6.7 Switching Characteristics ... 6
6.8 Operating Characteristics ... 6
6.9 Typical Characteristics ... 7
7 **Parameter Measurement Information** ... 8
8 **Detailed Description** ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 9
9 **Application and Implementation** ... 10
9.1 Application Information ... 10
9.2 Typical Application ... 10
10 **Power Supply Recommendations** ... 11
11 **Layout** ... 11
11.1 Layout Guidelines ... 11
11.2 Layout Example ... 11
12 デバイスおよびドキュメントのサポート ... 12
12.1 コミュニティ・リソース ... 12
12.2 商標 ... 12
12.3 静電気放電に関する注意事項 ... 12
12.4 Glossary ... 12
13 メカニカル、パッケージ、および注文情報 ... 12

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision M (November 2013) から Revision N に変更 **Page**

- ドキュメントを新しい TI データシートのフォーマットに更新 ... 1
- 「製品情報」表 追加 ... 1
- Added T_J(Max) spec to Abs Max Ratings table ... 4
- Moved T_{stg} spec to Abs Max Ratings table. ... 4

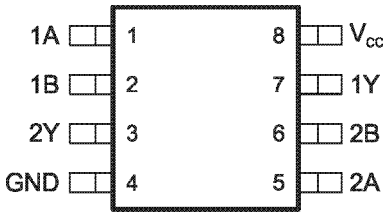
Revision L (April 1999) から Revision M に変更 **Page**

- 「注文情報」表を削除 ... 1
- Updated operating temperature range. ... 5

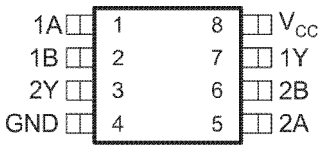
Copyright © 1999–2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

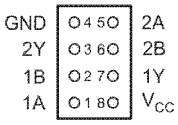
DCT Package
8-Pin SSOP
Top View



DCU Package
8-Pin VSSOP
Top View



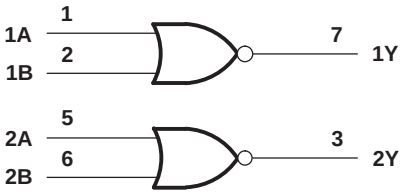
YZP Package
8-Pin DSBGA
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1 input A
1B	2	Input	Channel 1 input B
2Y	3	Output	Channel 2 output Y
GND	4	–	Ground
2A	5	Input	Channel 2 input A
2B	6	Input	Channel 2 input B
1Y	7	Output	Channel 1 output Y
VCC	8	–	Positive supply

Logic Diagram (Positive Logic)



6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 1999–2019, Texas Instruments Incorporated

6.3 Recommended Operating Conditions[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[(1)]		SN74LVC2G02			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.8	201.8	99.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.8	93.3	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.9	124.0	27.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.7	32.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	96.6	123.6	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

Copyright © 1999–2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{OH}		I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –4 mA	1.65 V	1.2			1.2			
		I_{OH} = –8 mA	2.3 V	1.9			1.9			
		I_{OH} = –16 mA	3 V	2.4			2.4			
		I_{OH} = –24 mA		2.3			2.3			
		I_{OH} = –32 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45			0.45	
		I_{OL} = 8 mA	2.3 V			0.3			0.3	
		I_{OL} = 16 mA	3 V			0.4			0.4	
		I_{OL} = 24 mA				0.55			0.75	
		I_{OL} = 32 mA	4.5 V			0.55			0.75	
I_I	A or B inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i		V_I = V_{CC} or GND	3.3 V		5			5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	3.2	8.9	1	5.4	1	4.9	1	4.4	ns

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	3.2	10.9	1	6.4	1	5.9	1	5.4	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	18	18	19	22	pF

Copyright © 1999–2019, Texas Instruments Incorporated

6.9 Typical Characteristics

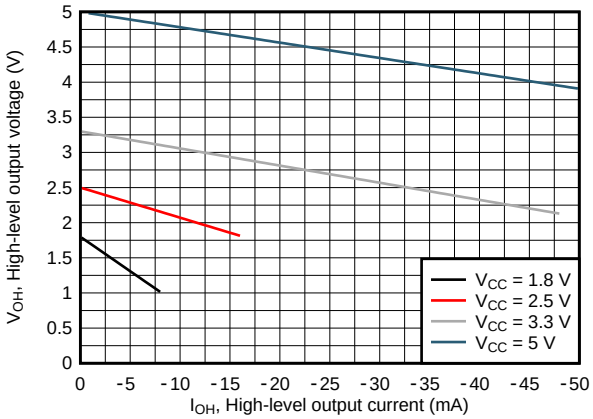


Figure 1. Simulated typical high-level output voltage (V_{OH}) across high-level output current (I_{OH}) at common supply values

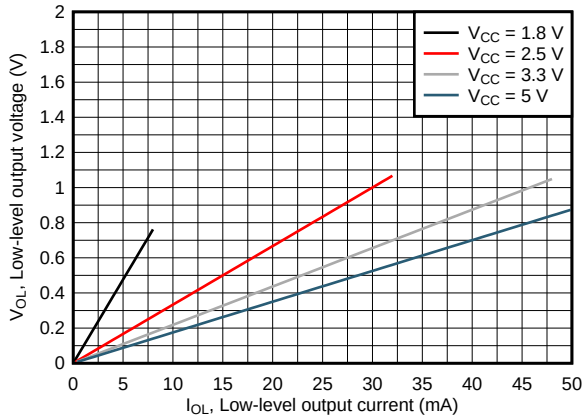
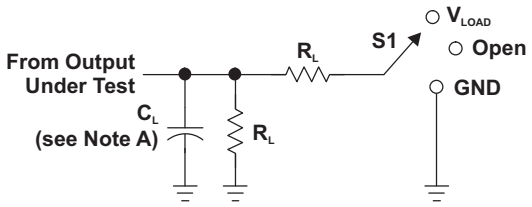


Figure 2. Simulated typical low-level output voltage (V_{OL}) across low-level output current (I_{OL}) at common supply values

Copyright © 1999–2019, Texas Instruments Incorporated

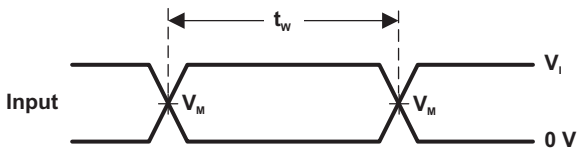
7 Parameter Measurement Information



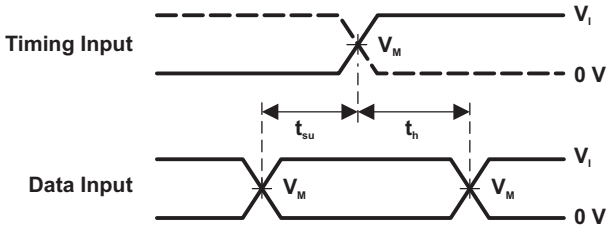
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

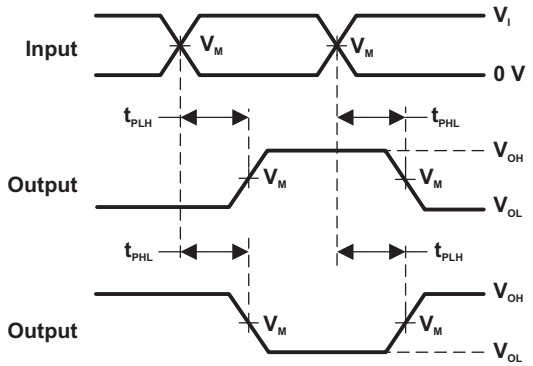
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



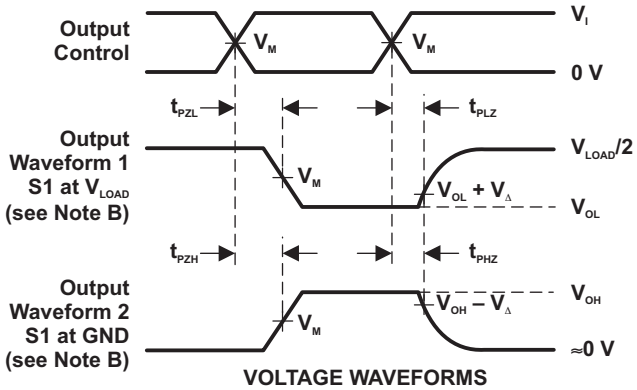
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

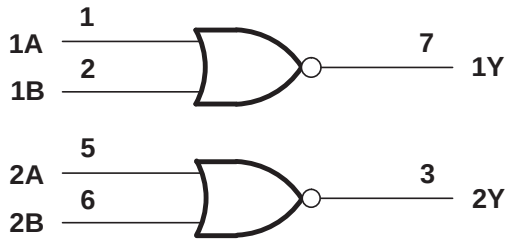
Copyright © 1999–2019, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74LVC2G02 device contains two 2-input positive-NOR gates and each gate performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

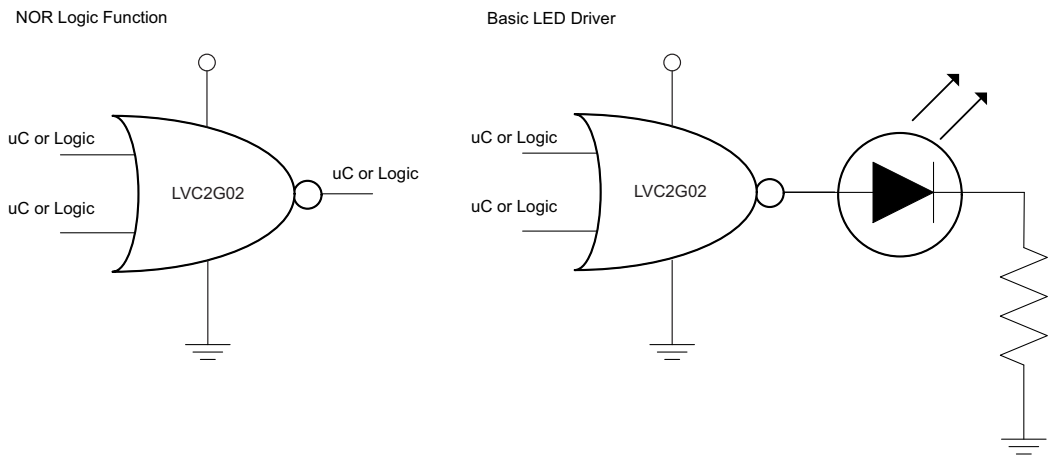
Copyright © 1999–2019, Texas Instruments Incorporated

9 Application and Implementation

9.1 Application Information

The SN74LVC2G02 is a high-drive CMOS device that can be used for implement NOR logic with a high output drive, such as an LED application. It can produce 24-mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 Mhz. The inputs are 5.5-V tolerant allowing translation down to V_{CC}.

9.2 Typical Application



9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above V_{CC}.

Copyright © 1999–2019, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curves

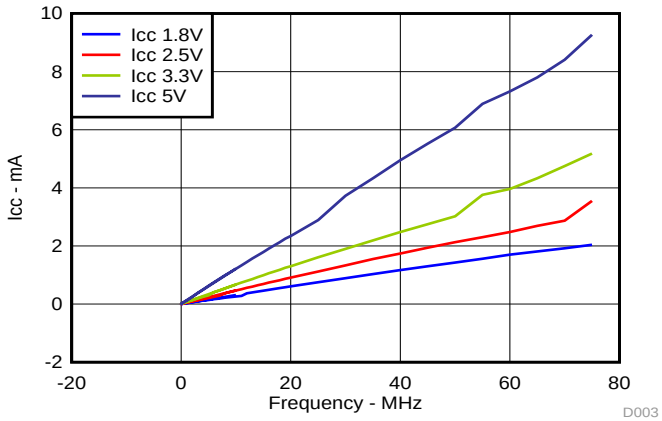


Figure 4. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple VCC pins, then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

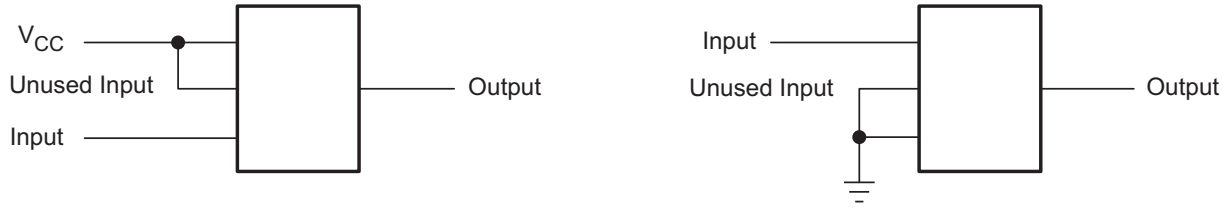
11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

11.2 Layout Example



12 デバイスおよびドキュメントのサポート

12.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商標

NanoFree, E2E are trademarks of Texas Instruments.

12.3 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 1999–2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2G02DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(2WI5, C02) (R, Z)
SN74LVC2G02DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2WI5, C02) (R, Z)
SN74LVC2G02DCTRE4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02 (R, Z)
SN74LVC2G02DCTRE4.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02 (R, Z)
SN74LVC2G02DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C02J, C02Q, C02R)
SN74LVC2G02DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C02J, C02Q, C02R)
SN74LVC2G02DCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C02J, C02Q, C02R)
SN74LVC2G02DCUT.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C02J, C02Q, C02R)
SN74LVC2G02DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02R
SN74LVC2G02YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CBN
SN74LVC2G02YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CBN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G02 :

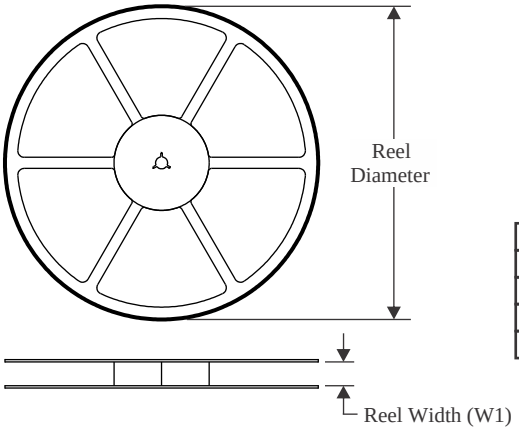
- Enhanced Product : SN74LVC2G02-EP

NOTE: Qualified Version Definitions:

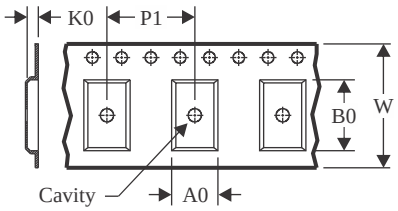
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

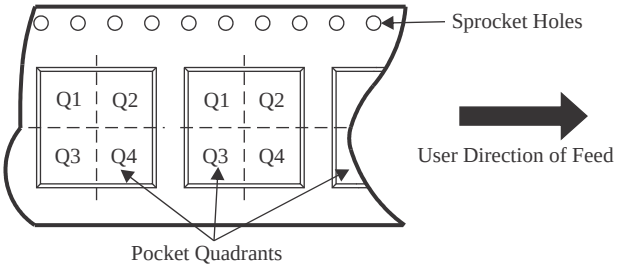


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

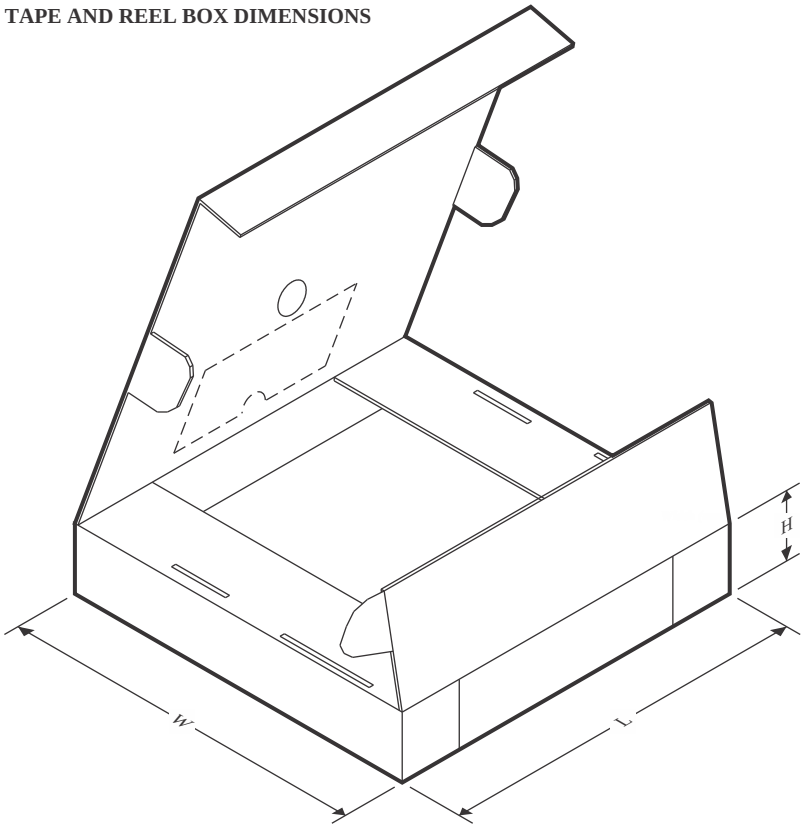
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G02DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC2G02DCTRE4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC2G02DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G02DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G02DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G02YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

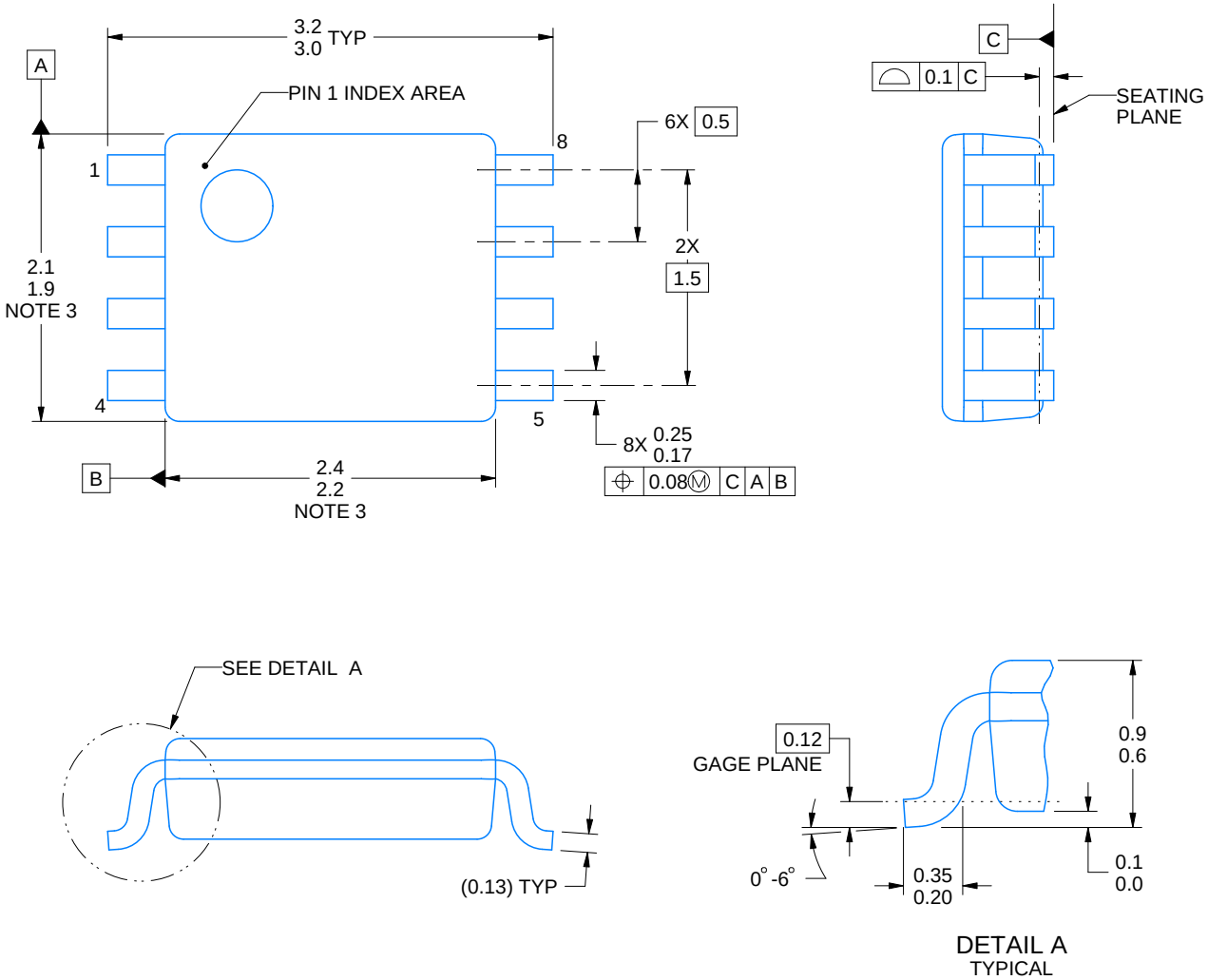
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G02DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC2G02DCTRE4	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74LVC2G02DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G02DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G02DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G02YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

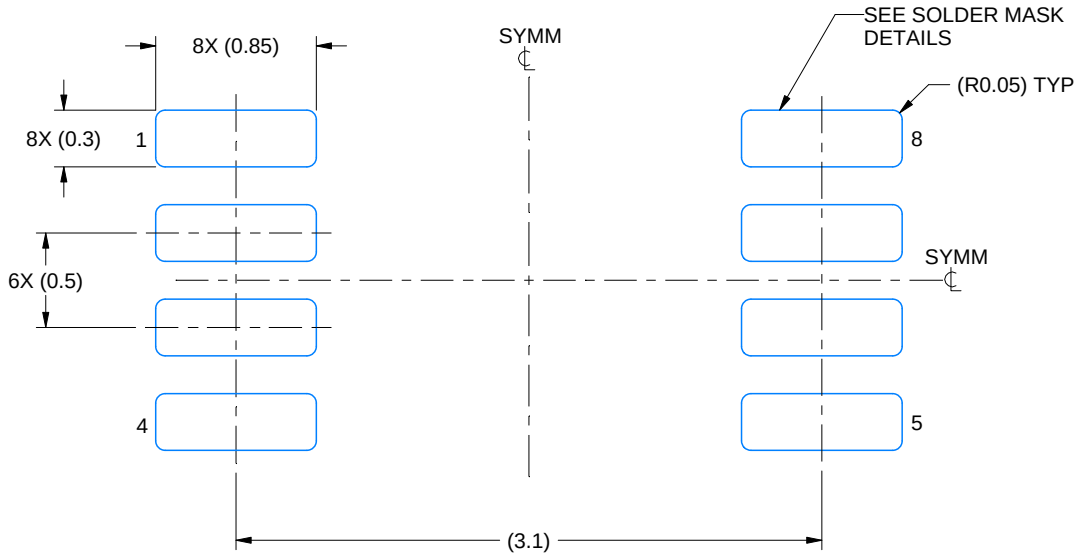
SMALL OUTLINE PACKAGE



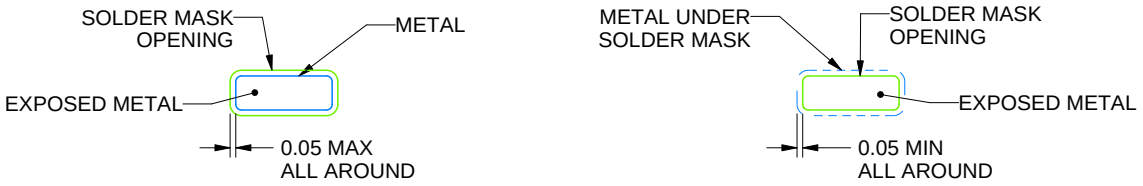
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

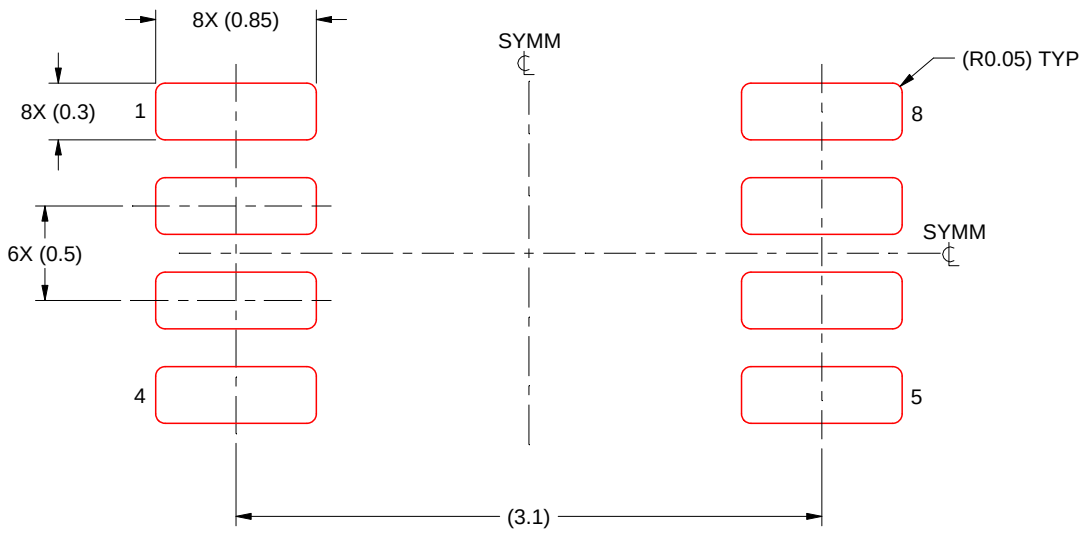


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

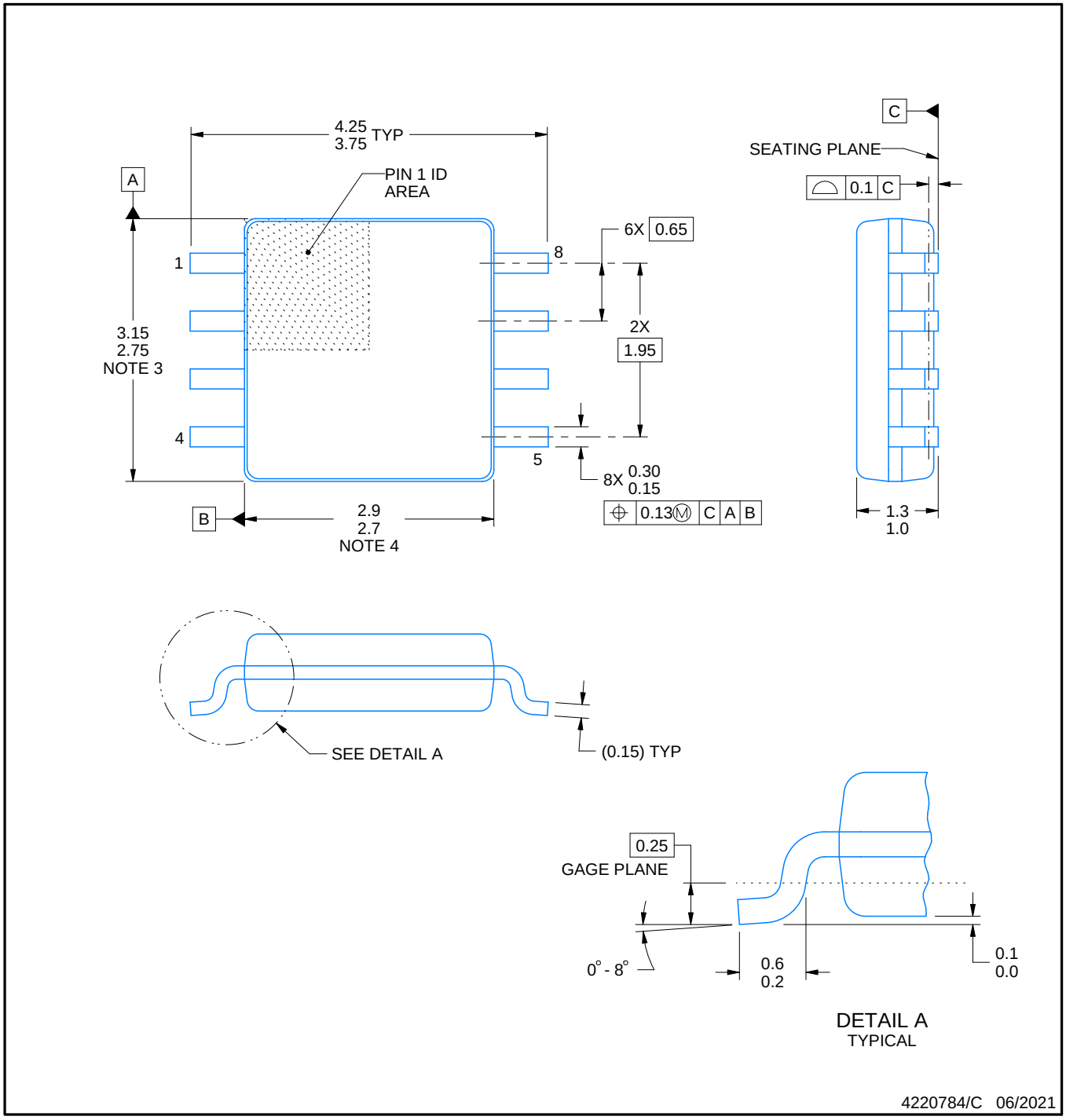


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

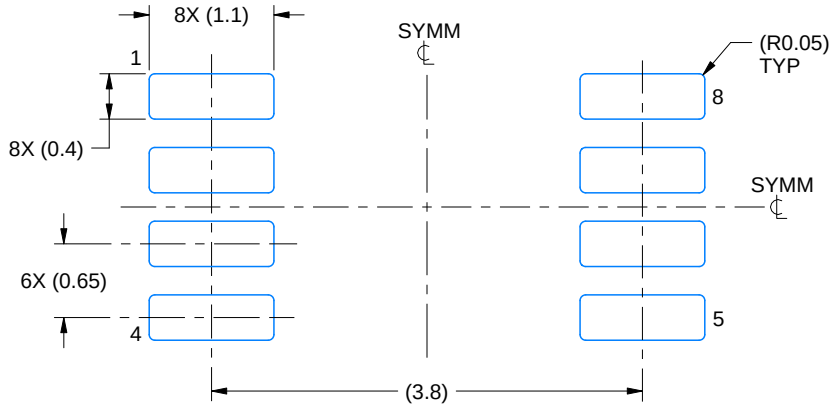
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

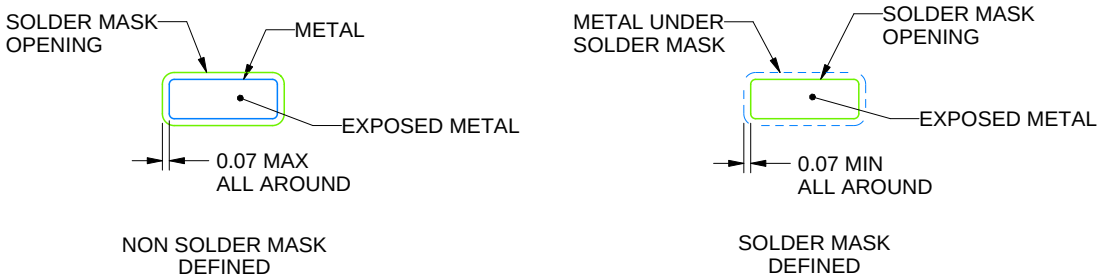


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

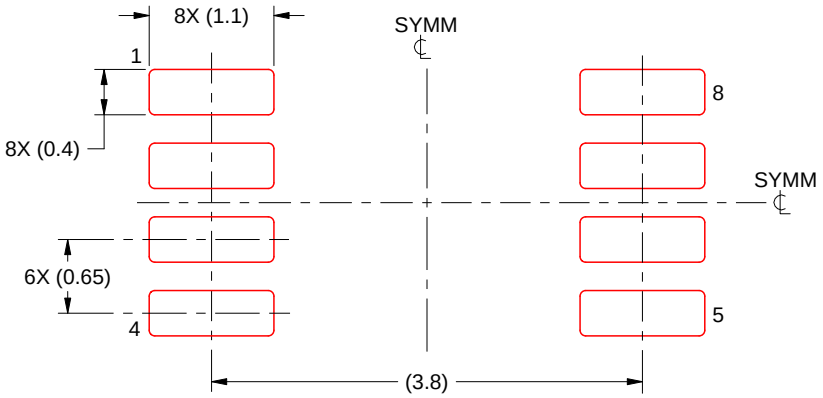


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

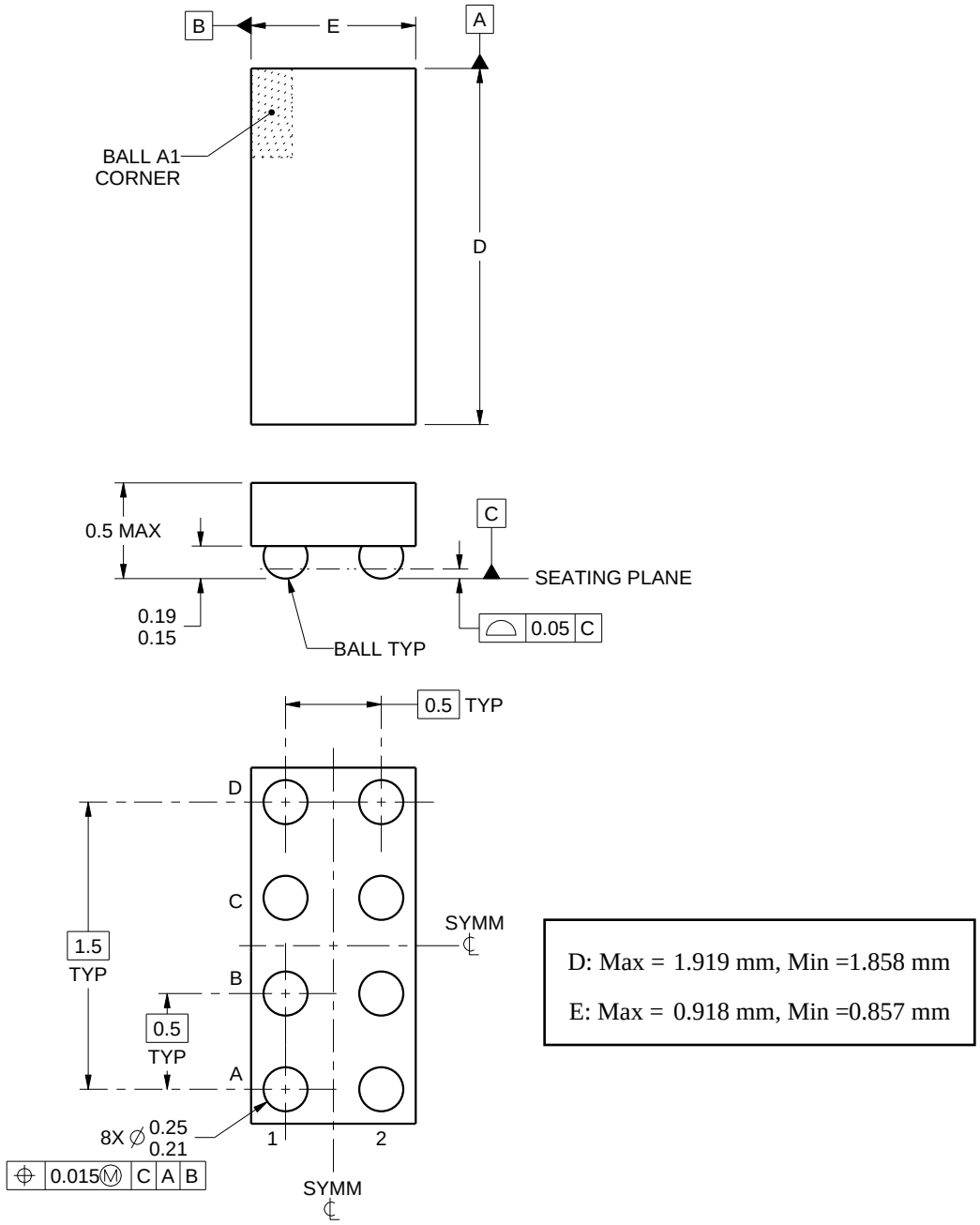


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

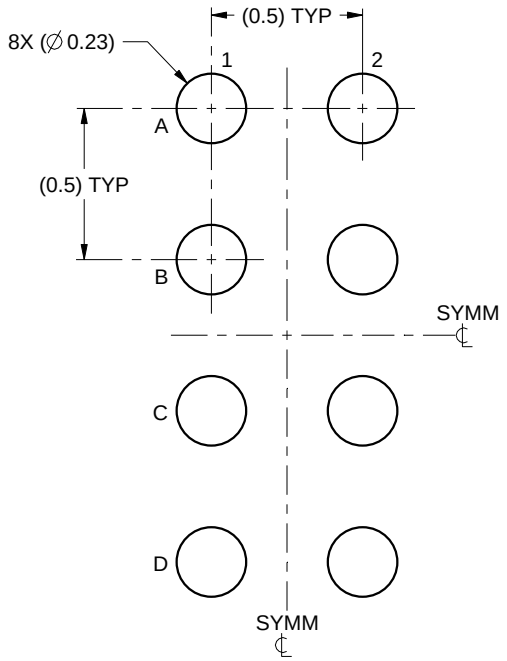
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

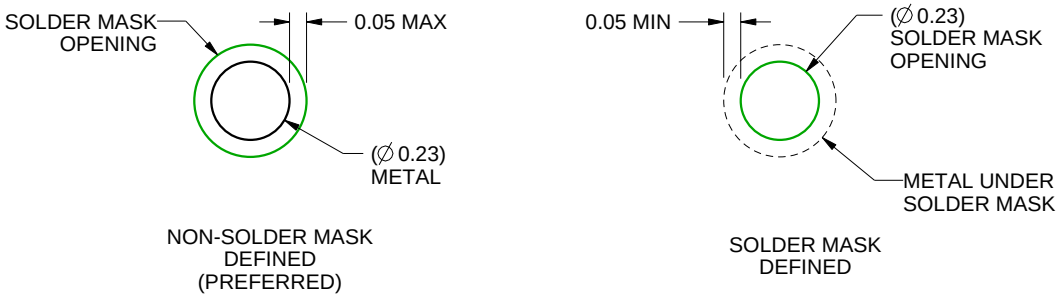


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

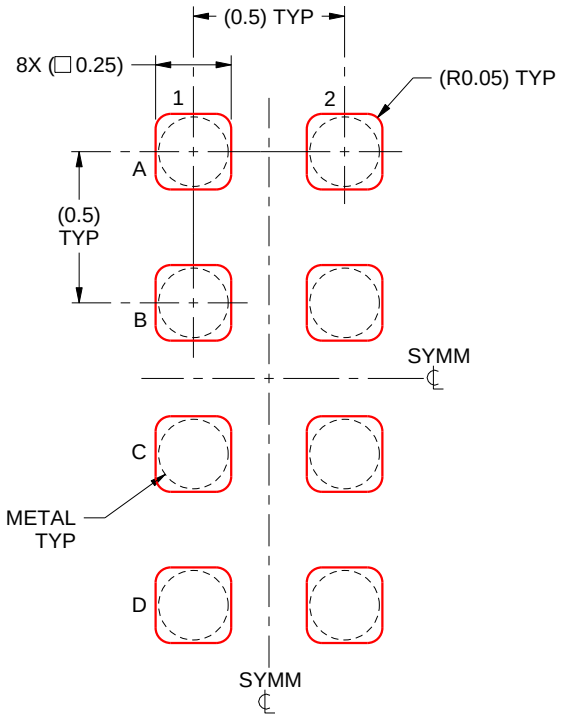


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月