SN74LVC1T45-Q1 車載対応、1.65V～5.5V、シングルビット、デュアル電源レベル シフタ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～+125℃
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C3B
- 完全に構成可能なデュアル レール設計により、1.65V～5.5V の電源電圧の全範囲にわたって各ポートが動作可能
- V_{CC} 絶縁機能:いずれかの V_{CC} 入力が GND レベルになると、両方のポートがハイ インピーダンス状態に移行
- V_{CCA} を基準とする DIR 入力回路
- 3.3V で ±24mA の出力駆動能力
- I_{off} により部分的パワーダウン モードでの動作をサポート
- 最大データ レート:
  - 420Mbps (3.3V から 5V への変換)
  - 210Mbps (3.3V への変換)
  - 140Mbps (2.5V への変換)
  - 75Mbps (1.8V への変換)

2 アプリケーション

- ヘッド・ユニット
- ADAS – カメラ
- テレマティクス

3 概要

SN74LVC1T45-Q1 デバイスは、個別に構成可能な 2 本の電源レールを採用したシングルビット非反転バス トランシーバです。A ポートは V_{CCA} に追従する設計です。V_{CCA} ピンには、1.65V～5.5V の電源電圧を入力できます。B ポートは、V_{CCB} に追従する設計になっています。V_{CCB} ピンには、1.65V～5.5V の電源電圧を入力できます。これにより、1.8V、2.5V、3.3V、5V の任意の電圧ノード間での低電圧双方向変換が可能です。

SN74LVC1T45-Q1 デバイスは、シングルビットの非反転レベル トランスレータです。完全に構成可能なデュアル レール設計により、1.65V～5.5V の電源電圧の全範囲にわたって各ポートが動作可能です。このデバイスは広い双方向変換範囲を必要とするアプリケーションに最適です。

SN74LVC1T45-Q1 は、DIR 入力が V_{CCA} によって給電されるように設計されています。

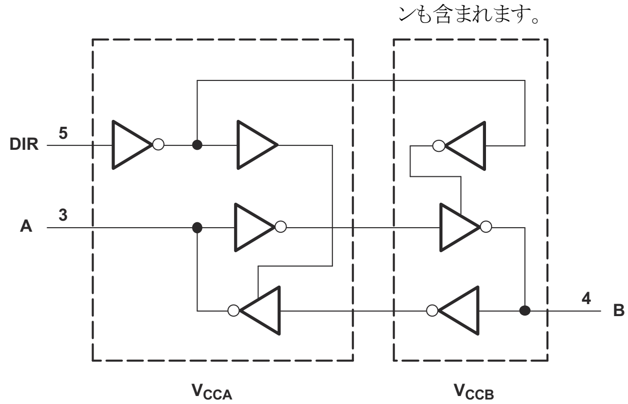
このデバイスは、I_{off} を使用する部分的パワーダウン アプリケーション用の動作が完全に規定されています。I_{off} 回路で出力をディセーブルすることにより、電源切断時にデバイスに電流が逆流して損傷するのを回避できます。

V_{CC} 絶縁機能は、いずれかの V_{CC} 入力が GND レベルになると、両方のポートがハイ インピーダンス状態になるよう設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74LVC1T45-Q1	DCK (SC70、6)	2mm × 2.1mm

(1) 詳細については、セクション 9 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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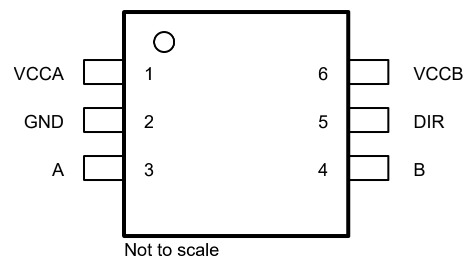
4 Pin Configuration and Functions



See mechanical drawings for dimensions.

図 4-1. DCK Package, 6-Pin SC70 (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	3	I/O	Output level depends on V_{CC1} voltage
B	4	I/O	Input threshold value depends on V_{CC2} voltage
DIR	5	I	GND (low level) determines B-port to A-port direction
GND	2	G	Device GND
V_{CCA}	1	P	SYSTEM-1 supply voltage (1.65V to 5.5V)
V_{CCB}	6	P	SYSTEM-2 supply voltage (1.65V to 5.5V)

(1) G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage, V_{CCA}, V_{CCB}		–0.5	6.5	V
Input voltage, V_I [(2)]		–0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O [(2)]		–0.5	6.5	V
Voltage applied to any output in the high or low state, V_O [(2)] [(3)]	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK} (V_I < 0)			–50	mA
Output clamp current, I_{OK} (V_O < 0)			–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See[(1)] [(2)] [(3)]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	5.5	V
V_{CCB}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage, data inputs[(4)]	V_{CCI} = 1.65V to 1.95V	V_{CCI} × 0.65		V
		V_{CCI} = 2.3V to 2.7V	1.7		
		V_{CCI} = 3V to 3.6V	2		
		V_{CCI} = 4.5V to 5.5V	V_{CCI} × 0.7		
V_{IL}	Low-level input voltage, data inputs[(4)]	V_{CCI} = 1.65V to 1.95V		V_{CCI} × 0.35	V
		V_{CCI} = 2.3V to 2.7V		0.7	
		V_{CCI} = 3V to 3.6V		0.8	
		V_{CCI} = 4.5V to 5.5V		V_{CCI} × 0.3	
V_{IH}	High-level input voltage, DIR (referenced to V_{CCA})[(5)]	V_{CCI} = 1.65V to 1.95V	V_{CCA} × 0.65		V
		V_{CCI} = 2.3V to 2.7V	1.7		
		V_{CCI} = 3V to 3.6V	2		
		V_{CCI} = 4.5V to 5.5V	V_{CCA} × 0.7		

5.3 Recommended Operating Conditions (続き)

See[(1) (2) (3)]

				MIN	MAX	UNIT
V_{IL}	Low-level input voltage, DIR (referenced to V_{CCA})[(5)]		V_{CCI} = 1.65V to 1.95V		V_{CCA} × 0.35	V
			V_{CCI} = 2.3V to 2.7V		0.7	
			V_{CCI} = 3V to 3.6V		0.8	
			V_{CCI} = 4.5V to 5.5V		V_{CCA} × 0.3	
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	V_{CCO}	V
I_{OH}	High-level output current		V_{CCO} = 1.65V to 1.95V		–4	mA
			V_{CCO} = 2.3V to 2.7V		–8	
			V_{CCO} = 3V to 3.6V		–24	
			V_{CCO} = 4.5V to 5.5V		–32	
I_{OL}	Low-level output current		V_{CCO} = 1.65V to 1.95V		4	mA
			V_{CCO} = 2.3V to 2.7V		8	
			V_{CCO} = 3V to 3.6V		24	
			V_{CCO} = 4.5V to 5.5V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	V_{CCI} = 1.65V to 1.95V		20	ns/V
			V_{CCI} = 2.3V to 2.7V		20	
			V_{CCI} = 3V to 3.6V		10	
			V_{CCI} = 4.5V to 5.5V		5	
		Control inputs, V_{CCI} = 1.65V to 5.5V			5	
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

5.4 Thermal Information

THERMAL METRIC[(1)]		SN74LVC1T45-Q1 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	54.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)[(1) (2)]

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$	I_{OH} = –100 µA, V_{CCA} = 1.65V to 4.5V, V_{CCB} = 1.65V to 4.5V		V_{CCO} – 0.1			V
		I_{OH} = –4mA, V_{CCA} = 1.65V, V_{CCB} = 1.65V		1.2			
		I_{OH} = –8mA, V_{CCA} = 2.3V, V_{CCB} = 2.3V		1.9			
		I_{OH} = –24mA, V_{CCA} = 3V, V_{CCB} = 3V		2.3			
		I_{OH} = –32mA, V_{CCA} = 4.5V, V_{CCB} = 4.5V		3.8			
V_{OL}	$V_I = V_{IL}$	I_{OL} = 100 µA, V_{CCA} = 1.65V to 4.5V, V_{CCB} = 1.65V to 4.5V				0.1	V
		I_{OL} = 4mA, V_{CCA} = 1.65V, V_{CCB} = 1.65V				0.45	
		I_{OL} = 8mA, V_{CCA} = 2.3V, V_{CCB} = 2.3V				0.4	
		I_{OL} = 24mA, V_{CCA} = 3V, V_{CCB} = 3V				0.65	
		I_{OL} = 32mA, V_{CCA} = 4.5V, V_{CCB} = 4.5V				0.65	
I_I	DIR at $V_I = V_{CCA}$ or GND, V_{CCA} = 1.65V to 5.5V, V_{CCB} = 1.65V to 5.5V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±4	
I_{off}	V_I or V_O = 0 to 5.5V	A port at V_{CCA} = 0V, V_{CCB} = 0 to 5.5V	T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
		B port at V_{CCA} = 0 to 5.5V, V_{CCB} = 0V	T_A = 25°C			±1	
			T_A = –40°C to 125°C			±10	
I_{OZ}	A or B port at $V_O = V_{CCO}$ or GND, V_{CCA} = 1.65V to 5.5V, V_{CCB} = 1.65V to 5.5V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
I_{CCA}	$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.65V to 5.5V, V_{CCB} = 1.65V to 5.5V				10	µA
		V_{CCA} = 5.5V, V_{CCB} = 0V				4	
		V_{CCA} = 0V, V_{CCB} = 5.5V				–10	
I_{CCB}	$V_I = V_{CCI}$ or GND, I_O = 0	V_{CCA} = 1.65V to 5.5V, V_{CCB} = 1.65V to 5.5V				10	µA
		V_{CCA} = 5.5V, V_{CCB} = 0V				–10	
		V_{CCA} = 0V, V_{CCB} = 5.5V				4	
$I_{CCA} + I_{CCB}$	$V_I = V_{CCI}$ or GND, I_O = 0, V_{CCA} = 1.65V to 5.5V, V_{CCB} = 1.65V to 5.5V					20	µA
ΔI_{CCA}	V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V	A port at V_{CCA} – 0.6V, DIR at V_{CCA}, B port = open				50	µA
		DIR at V_{CCA} – 0.6V, B port = open, A port at V_{CCA} or GND				50	
ΔI_{CCB}	B port at V_{CCB} – 0.6V, DIR at GND, A port = open, V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V					50	µA
C_i	DIR at $V_I = V_{CCA}$ or GND, T_A = 25°C, V_{CCA} = 3.3V, V_{CCB} = 3.3V				2.5		pF
C_{io}	A or B port at $V_O = V_{CCA/B}$ or GND, T_A = 25°C, V_{CCA} = 3.3V, V_{CCB} = 3.3V				6		pF
C_{pdA} [(3)]	C_L = 0pF, f = 10MHz, $t_r = t_f$ = 1ns	A-port input, B-port output	$V_{CCA} = V_{CCB}$ = 1.8V		3		pF
			$V_{CCA} = V_{CCB}$ = 2.5V		4		
			$V_{CCA} = V_{CCB}$ = 3.3V		4		
			$V_{CCA} = V_{CCB}$ = 5V		4		
		B-port input, A-port output	$V_{CCA} = V_{CCB}$ = 1.8V		18		
			$V_{CCA} = V_{CCB}$ = 2.5V		19		
			$V_{CCA} = V_{CCB}$ = 3.3V		20		
			$V_{CCA} = V_{CCB}$ = 5V		21		

5.5 Electrical Characteristics (続き)

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)(1) (2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pdB} (3)	C_L = 0pF, f = 10MHz, t_r = t_f = 1ns	A-port input, B-port output	V_{CCA} = V_{CCB} = 1.8V		18		pF
			V_{CCA} = V_{CCB} = 2.5V		19		
			V_{CCA} = V_{CCB} = 3.3V		20		
			V_{CCA} = V_{CCB} = 5V		21		
		B-port input, A-port output	V_{CCA} = V_{CCB} = 1.8V		3		
			V_{CCA} = V_{CCB} = 2.5V		4		
			V_{CCA} = V_{CCB} = 3.3V		4		
			V_{CCA} = V_{CCB} = 5V		4		

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) Power dissipation capacitance per transceiver

5.6 Switching Characteristics: V_{CCA} = 1.8V ±0.15V

over operating free-air temperature range (unless otherwise noted; see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2	ns
t_{PHL}			2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	
t_{PLH}	B	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	ns
t_{PHL}			2.8	17.3	2.1	15.9	2	15.6	1.8	15.2	
t_{PHZ}	DIR	A	5.2	22.7	4.8	21.5	4.7	21.4	5.1	20.1	ns
t_{PLZ}			2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	
t_{PHZ}	DIR	B	5.2	27.9	4.9	14.5	3.6	13.3	2.3	11.2	ns
t_{PLZ}			4.2	19	2.2	12.2	2.3	11.4	2	9.4	
t_{PZH} (1)	DIR	A		39.7		31.2		29.9		27.5	ns
t_{PZL} (1)				45.2		30.4		28.9		26.4	
t_{PZH} (1)	DIR	B		34.2		26.8		25		24.1	ns
t_{PZL} (1)				40.7		33		31.5		30.1	

(1) The enable time is a calculated value, derived using the formula shown in *セクション 7.1.1* .

5.7 Switching Characteristics: V_{CCA} = 2.5V ±0.2V

over operating free-air temperature range (unless otherwise noted; see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	ns
t_{PHL}			2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	
t_{PLH}	B	A	2.2	13.3	1.5	11.5	1.4	11	1	10.5	ns
t_{PHL}			2.2	11.5	1.4	10.7	1.3	10	0.9	9.2	
t_{PHZ}	DIR	A	3	11.1	3.1	11.1	2.8	11.1	3.2	11.1	ns
t_{PLZ}			1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	
t_{PHZ}	DIR	B	5.2	26.7	4.1	14.4	3.9	13.2	2.4	10.1	ns
t_{PLZ}			3.9	21.9	3.2	12.6	2.8	11.4	1.8	8.3	

5.7 Switching Characteristics: V_{CCA} = 2.5V ±0.2V (続き)

over operating free-air temperature range (unless otherwise noted; see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PZH} (1)	DIR	A		35.2		24.1		22.4		18.8	ns
t_{PZL} (1)				38.2		24.9		23.2		19.3	
t_{PZH} (1)	DIR	B		27.9		20.4		18.3		16.9	ns
t_{PZL} (1)				27		21.6		19.5		18.7	

5.8 Switching Characteristics: V_{CCA} = 3.3V ±0.3V

over operating free-air temperature range (unless otherwise noted; see 図 6-1)

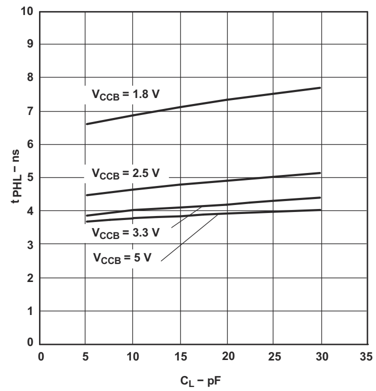
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	ns
t_{PHL}			2	15.6	1.3	10	0.8	8	0.7	7	
t_{PLH}	B	A	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	ns
t_{PHL}			1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	
t_{PHZ}	DIR	A	2.9	10.3	3	10.3	2.8	10.3	3.4	10.3	ns
t_{PLZ}			1.8	8.6	1.6	8.6	2.2	8.7	2.2	8.7	
t_{PHZ}	DIR	B	5.4	27.5	3.9	13.1	2.9	11.8	2.4	9.8	ns
t_{PLZ}			3.3	17.5	2.9	10.8	2.4	10.1	1.7	7.9	
t_{PZH} (1)	DIR	A		26.8		20.2		18.9		16.3	ns
t_{PZL} (1)				37.6		21.5		19.8		17.3	
t_{PZH} (1)	DIR	B		27.1		19.6		17.5		16.1	ns
t_{PZL} (1)				25.9		20.3		18.3		17.3	

5.9 Switching Characteristics: V_{CCA} = 5V ±0.5V

over operating free-air temperature range (unless otherwise noted; see 図 6-1)

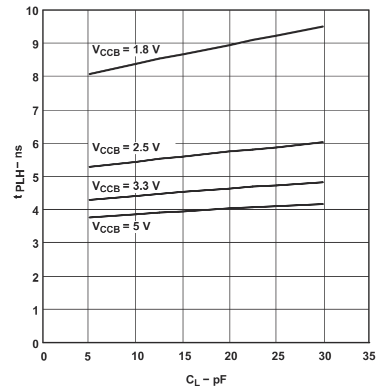
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t_{PHL}			1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	
t_{PLH}	B	A	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	ns
t_{PHL}			1.7	10	0.9	7.6	0.7	7	0.5	6.5	
t_{PHZ}	DIR	A	2.1	8.4	2.2	8.4	2.2	8.5	2.2	8.4	ns
t_{PLZ}			0.9	6.8	1	6.8	0.7	6.7	0.7	6.7	
t_{PHZ}	DIR	B	4.8	26.2	2.5	14.8	1	11.5	2.5	9.5	ns
t_{PLZ}			3.2	17.8	2.5	10.4	2.5	10	1.6	7.5	
t_{PZH} (1)	DIR	A		28		18.5		17.4		14.4	ns
t_{PZL} (1)				36.2		22.4		18.5		16	
t_{PZH} (1)	DIR	B		24.9		17.3		15.1		13.6	ns
t_{PZL} (1)				23.6		17.6		16		14.9	

5.10 Typical Characteristics



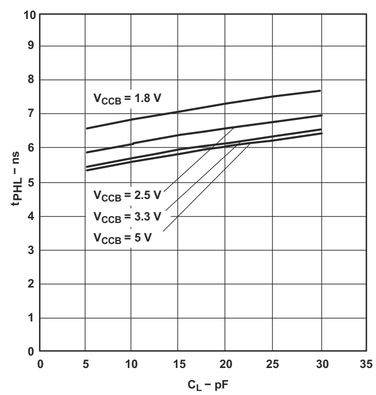
T_A = 25°C, V_{CCA} = 1.8V

図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



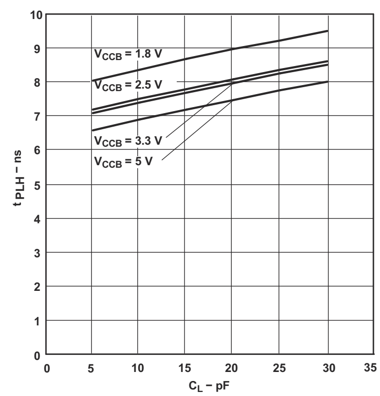
T_A = 25°C, V_{CCA} = 1.8V

図 5-2. Typical Propagation Delay (A to B) vs Load Capacitance



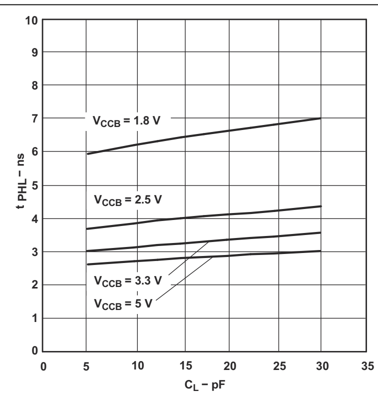
T_A = 25°C, V_{CCA} = 1.8V

図 5-3. Typical Propagation Delay (B to A) vs Load Capacitance



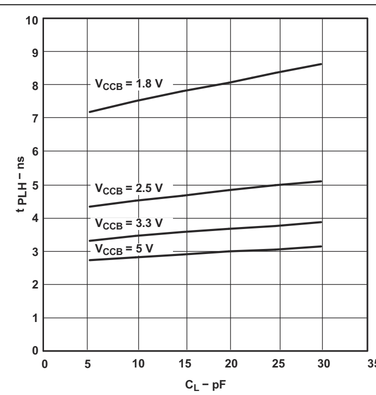
T_A = 25°C, V_{CCA} = 1.8V

図 5-4. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5V

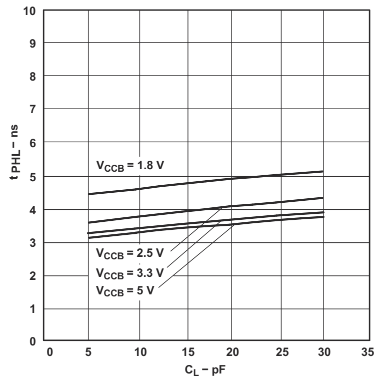
図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5V

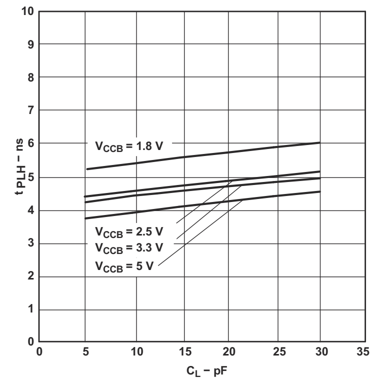
図 5-6. Typical Propagation Delay (A to B) vs Load Capacitance

5.10 Typical Characteristics (continued)



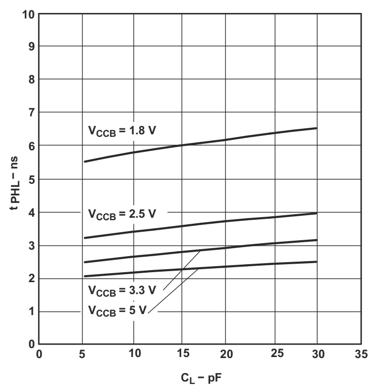
T_A = 25°C, V_{CCA} = 2.5V

図 5-7. Typical Propagation Delay (B to A) vs Load Capacitance



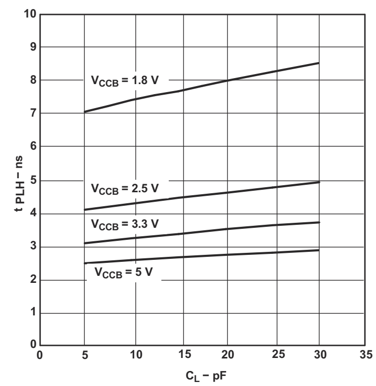
T_A = 25°C, V_{CCA} = 2.5V

図 5-8. Typical Propagation Delay (B to A) vs Load Capacitance



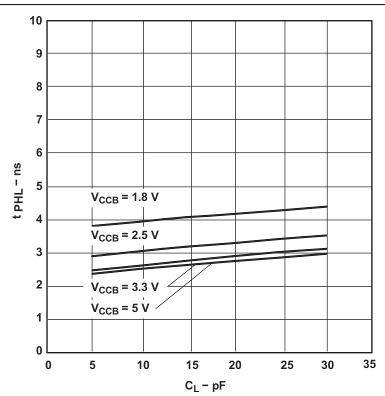
T_A = 25°C, V_{CCA} = 3.3V

図 5-9. Typical Propagation Delay (A to B) vs Load Capacitance



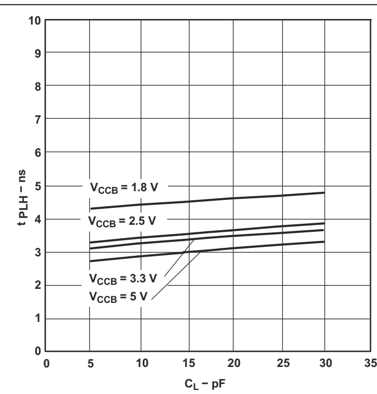
T_A = 25°C, V_{CCA} = 3.3V

図 5-10. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3V

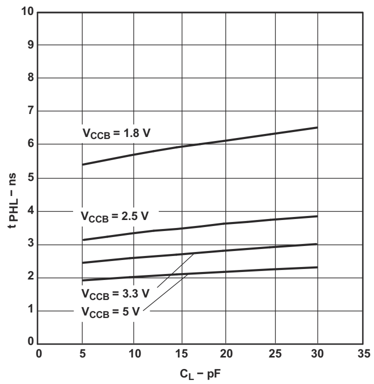
図 5-11. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3V

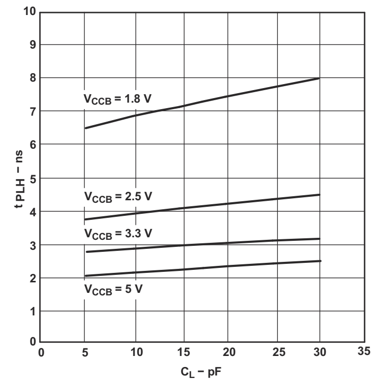
図 5-12. Typical Propagation Delay (B to A) vs Load Capacitance

5.10 Typical Characteristics (continued)



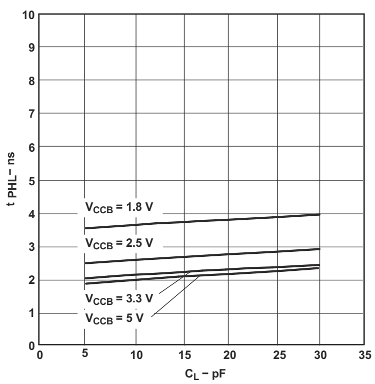
T_A = 25°C, V_{CCA} = 5V

図 5-13. Typical Propagation Delay (A to B) vs Load Capacitance



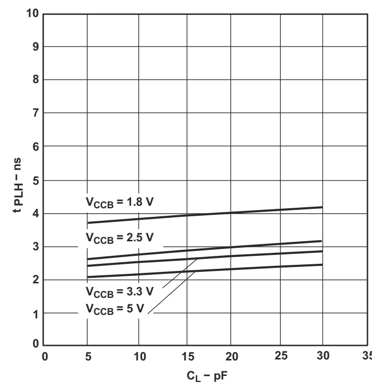
T_A = 25°C, V_{CCA} = 5V

図 5-14. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5V

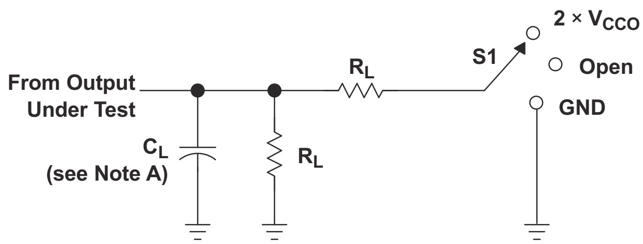
図 5-15. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5V

図 5-16. Typical Propagation Delay (B to A) vs Load Capacitance

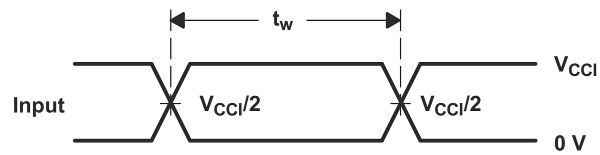
Parameter Measurement Information



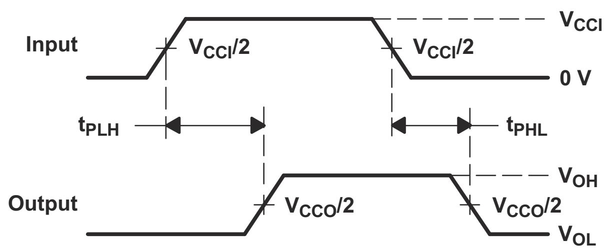
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

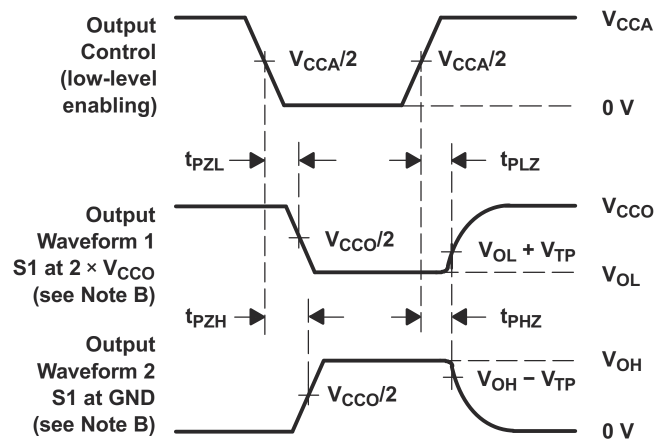
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The SN74LVC1T45-Q1 is single-bit, dual-supply, non-inverting voltage level translation. Pin A and that direction control pin (DIR) are supported by V_{CCA} and pin B is supported by V_{CCB}. The A port can accept I/O voltages ranging from 1.65V to 5.5V, while the B port can accept I/O voltages from 1.65V to 5.5V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

6.2 Functional Block Diagram

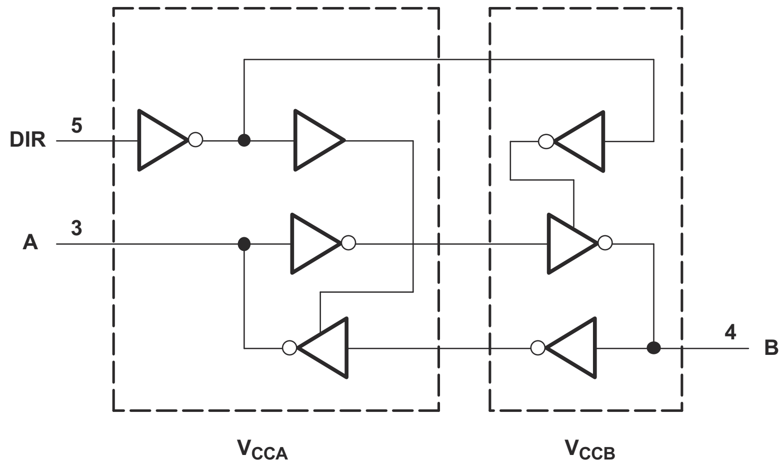


図 6-1. Logic Diagram (Positive Logic)

6.3 Feature Description

The SN74LVC1T45-Q1 has a fully configurable dual-rail design that allows each port to operate over the full 1.65V to 5.5V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65V and 5.5V, making the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V, and 5V).

SN74LVC1T45-Q1 can support high data rate applications. The translated signal data rate can be up to 420Mbps when the signal is translated from 3.3V to 5V.

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

6.3.1 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

6.4 Device Functional Modes

表 6-1 lists the operational modes of SN74LVC1T45-Q1.

表 6-1. Function Table (1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The SN74LVC1T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 420Mbps when device translates signals from 3.3V to 5V.

1.1 Enable Times

Calculate the enable times for the SN74LVC1T45-Q1 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

2 Typical Applications

2.1 Unidirectional Logic Level-Shifting Application

図 7-1 shows an example of the SN74LVC1T45-Q1 being used in a unidirectional logic level-shifting application.

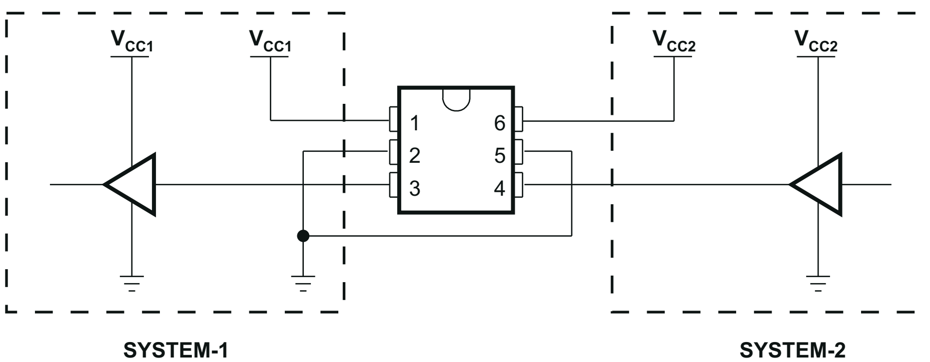


図 7-1. Unidirectional Logic Level-Shifting Application

2.1.1 Design Requirements

For this design example, use the parameters listed in 表 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Input voltage	1.65V to 5.5V
Output voltage	1.65V to 5.5V

2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC1T45-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC1T45-Q1 device is driving to determine the output voltage range.

2.1.3 Application Curves

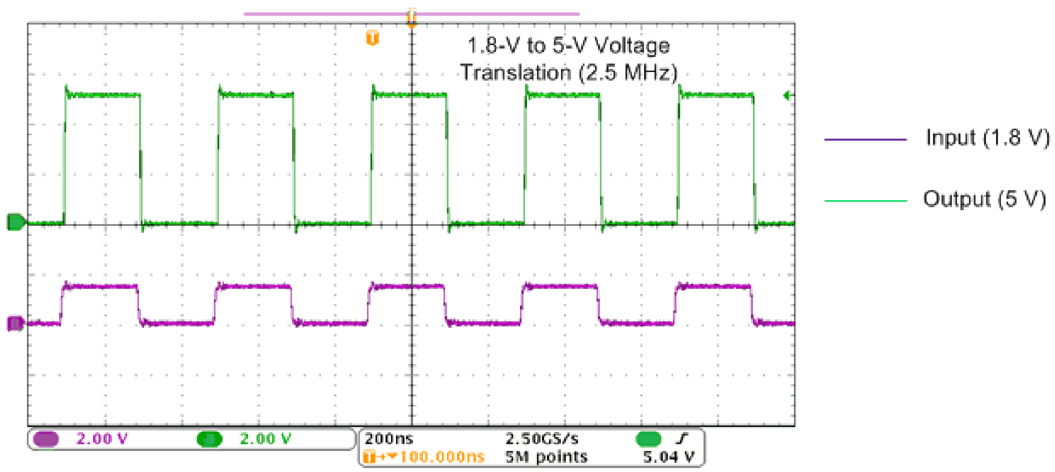


図 7-2. Translation Up (1.8V to 5V) at 2.5MHz

2.2 Bidirectional Logic Level-Shifting Application

図 7-3 shows the SN74LVC1T45-Q1 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45-Q1 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

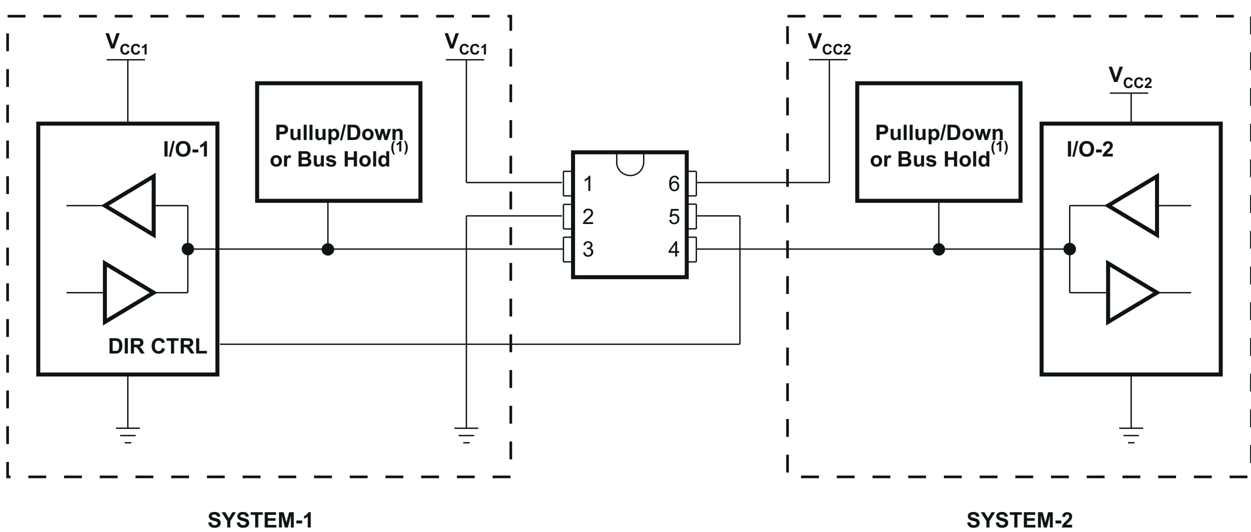


図 7-3. Bidirectional Logic Level-Shifting Application

2.2.1 Detailed Design Procedure

表 7-2 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 7-2. Data Transmission

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

2.2.2 Application Curves

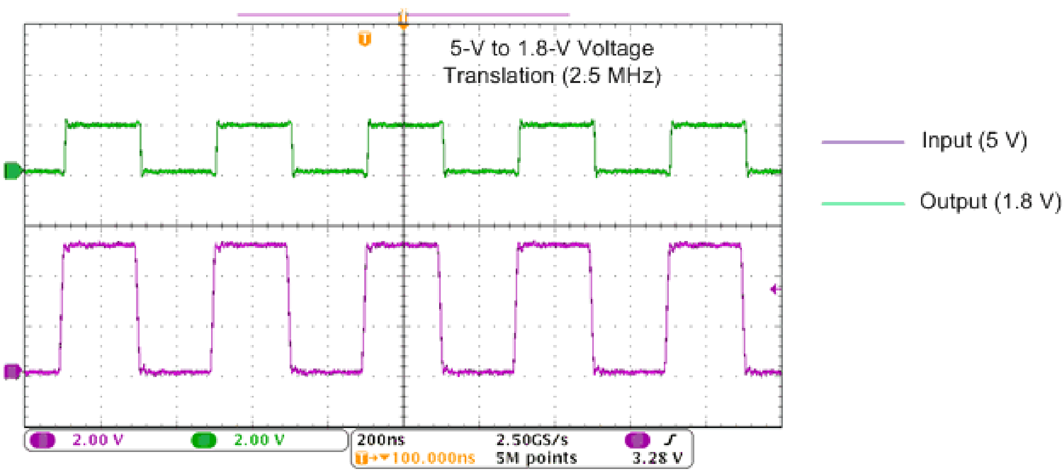


図 7-4. Translation Down (5V to 1.8V) at 2.5MHz

3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in *Glitch-free Power Supply Sequencing* .

4 Layout

4.1 Layout Guidelines

For device reliability, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements.

4.2 Layout Example

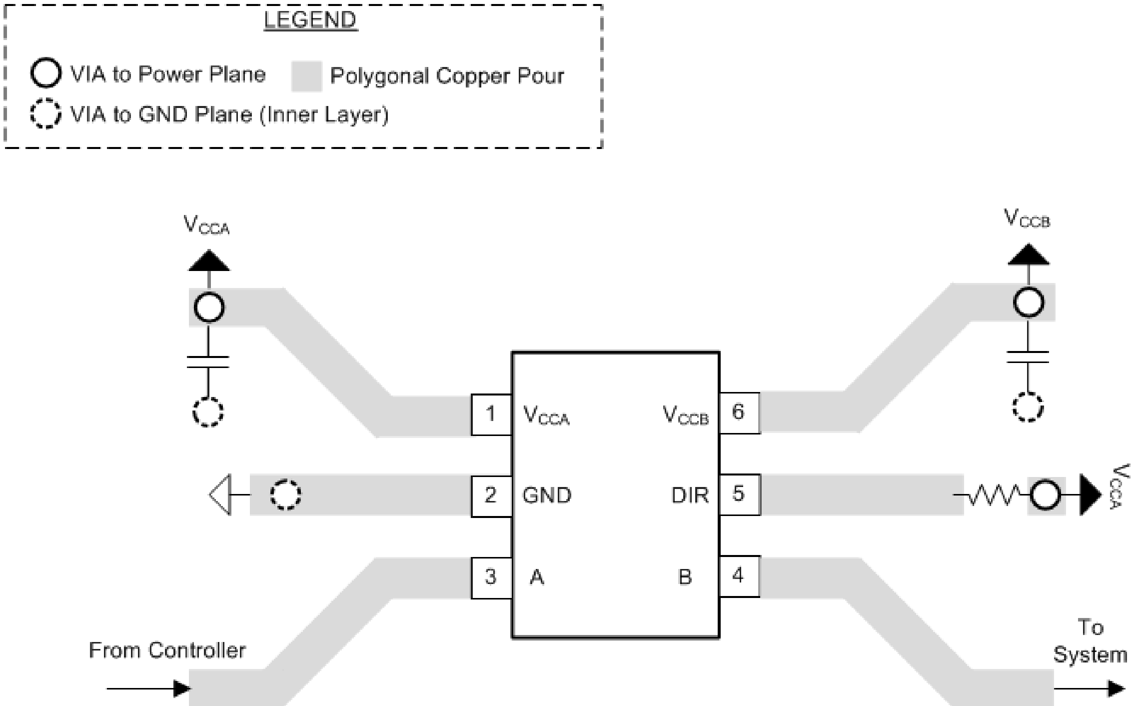


図 7-5. Layout Schematic

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

7.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

7.3 サポート・リソース

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7.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (December 2022) to Revision F (June 2024) — **Page**

- パッケージ リード サイズを含めるよう「パッケージ情報」表を更新 1
- Updated the *Power Supply Recommendations* section.......... 15

Changes from Revision D (July 2017) to Revision E (December 2022) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.......... 1
- Updated the thermals in the *Thermal Information* section.......... 4
- Updated the *Switching Characteristics* sections: extended some minimum specifications for lower delays......6

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1T45QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR
SN74LVC1T45QDCKRQ1.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR
SN74LVC1T45QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1T45-Q1 :

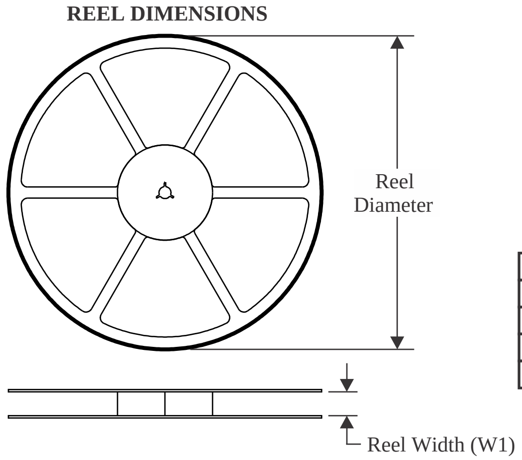
- Catalog : SN74LVC1T45

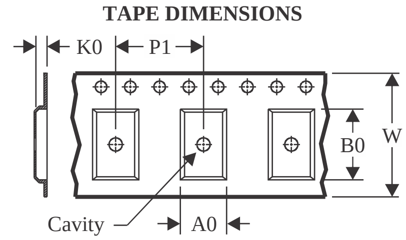
- Enhanced Product : SN74LVC1T45-EP

NOTE: Qualified Version Definitions:

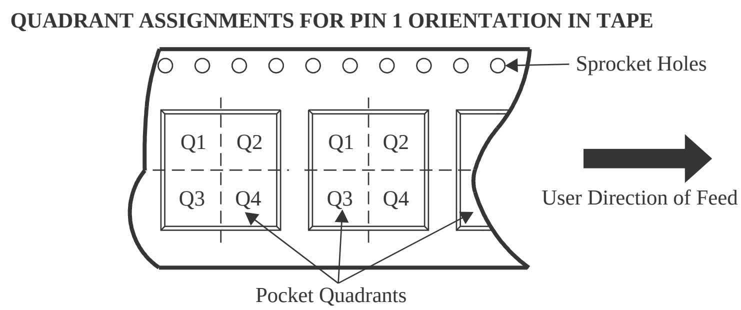
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION





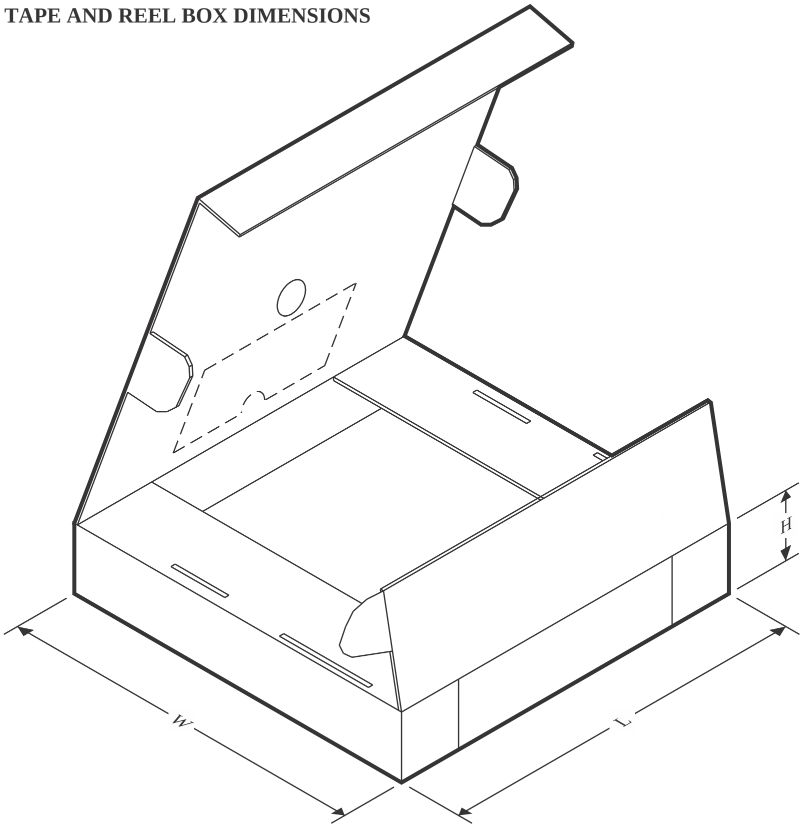
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

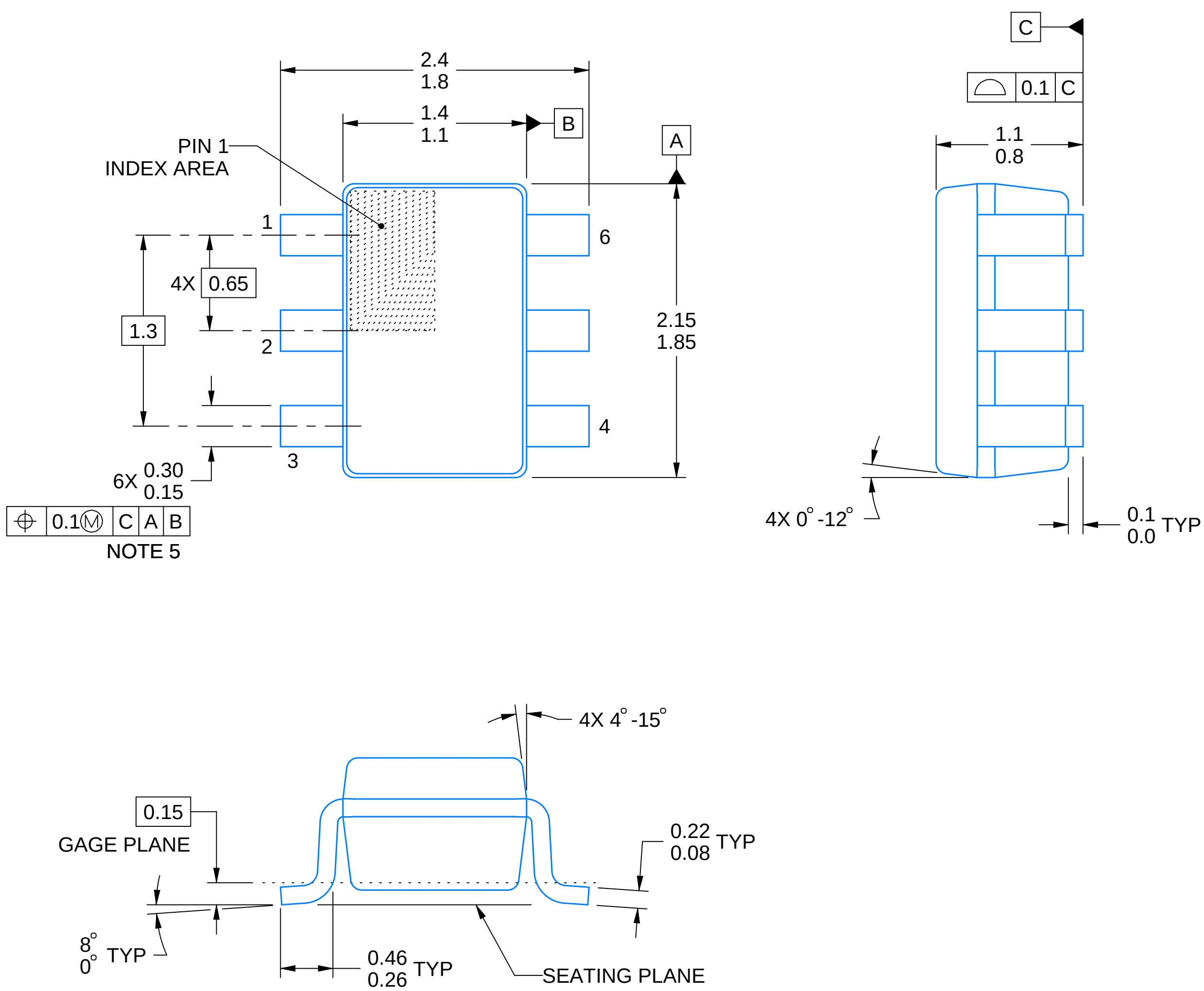
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0



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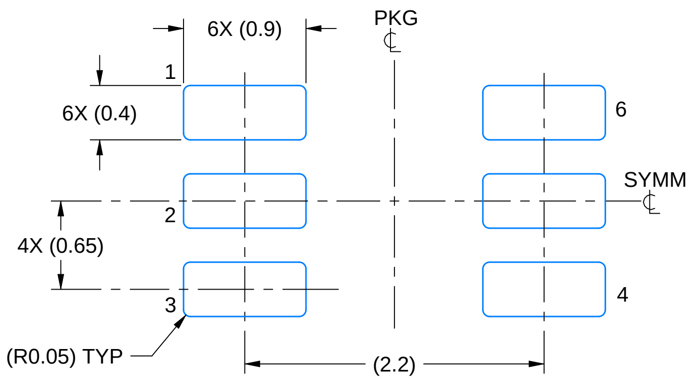
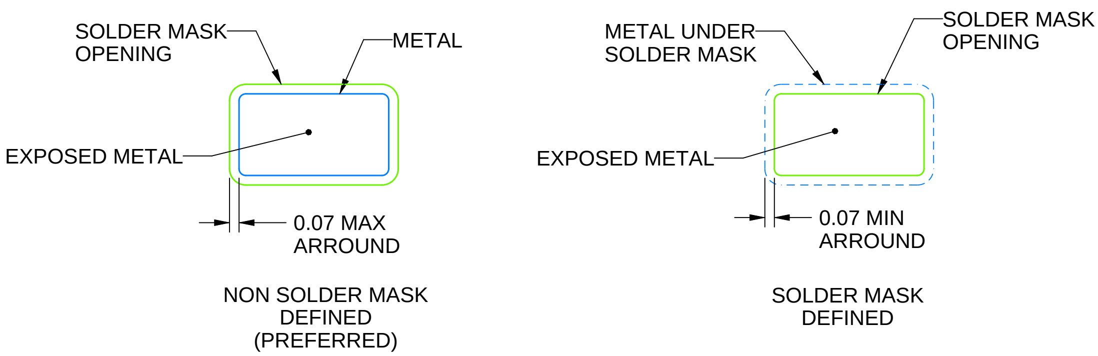
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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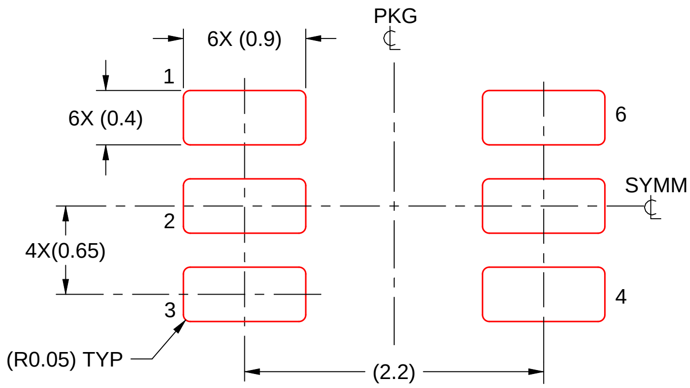
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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