SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

FEATURES

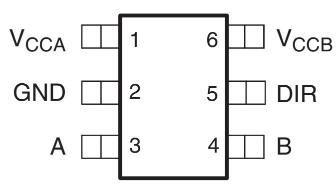
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **DIR Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 4-μA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Max Data Rates**
  - **420 Mbps (3.3-V to 5-V Translation)**
  - **210 Mbps (Translate to 3.3 V)**
  - **140 Mbps (Translate to 2.5 V)**
  - **75 Mbps (Translate to 1.8 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**[1]
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges are available – contact factory

DCK PACKAGE
(TOP VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–55°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1T45MDCKREP	NXG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(3) The actual top-side marking has one additional character that designates the assembly/test site.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74LVC1T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74LVC1T45 is designed so that the DIR input is powered by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

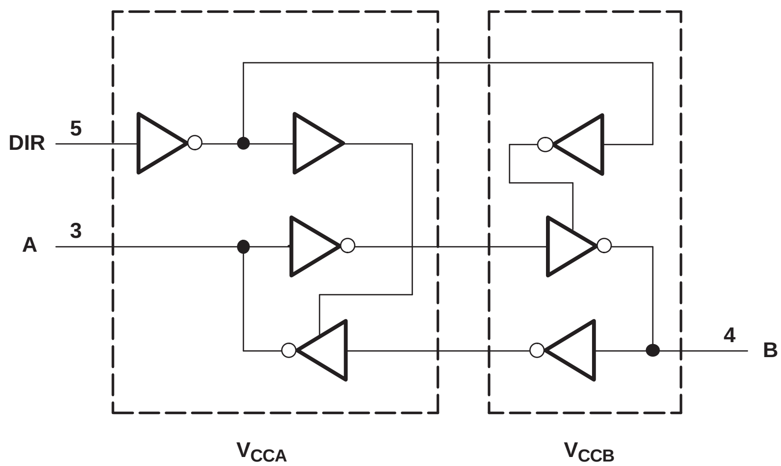
The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

FUNCTION TABLE(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]			259	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1][2][3]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs[4]	1.65 V to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
V_{IL}	Low-level input voltage	Data inputs[4]	1.65 V to 1.95 V			$V_{CCI} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCI} \times 0.3$	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})[5]	1.65 V to 1.95 V		$V_{CCA} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[5]	1.65 V to 1.95 V			$V_{CCA} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
V_I	Input voltage				0	5.5	V
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
		Control inputs	1.65 V to 5.5 V			5	
T_A	Operating free-air temperature				–55	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.

Electrical Characteristics[1][2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C MIN	TYP	MAX	–55°C to 125°C MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} – 0.1		V
		I_{OH} = –4 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –8 mA		2.3 V	2.3 V				1.9		
		I_{OH} = –24 mA		3 V	3 V				2.4		
		I_{OH} = –32 mA		4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA		2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA		3 V	3 V					0.55	
		I_{OL} = 32 mA		4.5 V	4.5 V					0.55	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	µA
I_{off}	A port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V			±1		±6	µA
	B port			0 to 5.5 V	0 V			±1		±6	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±6	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					4	µA
				5.5 V	0 V					2	
				0 V	5.5 V					-4	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					4	µA
				5.5 V	0 V					-4	
				0 V	5.5 V					2	
$I_{CCA} + I_{CCB}$ (see Table 1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					4	µA
ΔI_{CCA}	A port	A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open		3 V to 5.5 V	3 V to 5.5 V					50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	B port at V_{CCB} – 0.6 V, DIR at GND, A port = open		3 V to 5.5 V	3 V to 5.5 V					50	µA
C_i	DIR	$V_I = V_{CCA}$ or GND		3.3 V	3.3 V		2.5				pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND		3.3 V	3.3 V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2	ns
t_{PHL}			2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	
t_{PLH}	B	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	ns
t_{PHL}			2.8	17.3	2.1	15.9	2	18.6	1.8	15.2	
t_{PHZ}	DIR	A	5.2	22.4	4.8	21.5	4.7	21.4	5.1	20.1	ns
t_{PLZ}			2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	
t_{PHZ}	DIR	B	7.4	24.9	4.9	14.5	4.6	13.3	2.8	11.2	ns
t_{PLZ}			4.2	19	3.7	12.2	3.3	11.4	2.4	10.4	
t_{PZH} (1)	DIR	A		39.7		31.2		29.9		27.5	ns
t_{PZL} (1)				42.2		30.4		28.9		26.4	
t_{PZH} (1)	DIR	B		34.2		26.8		25		24.1	ns
t_{PZL} (1)				39.7		33		31.5		30.1	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	ns
t_{PHL}			2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	
t_{PLH}	B	A	2.2	13.3	1.5	11.5	1.4	11	1	10.5	ns
t_{PHL}			2.2	11.5	1.4	10.5	1.3	10	0.9	9.2	
t_{PHZ}	DIR	A	3	11.1	3.1	11.1	2.8	11.1	3.2	11.1	ns
t_{PLZ}			1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	
t_{PHZ}	DIR	B	6.5	26.7	4.1	14.4	3.9	13.2	2.4	10.1	ns
t_{PLZ}			3.9	21.9	3.2	12.6	2.8	11.4	1.8	8.3	
t_{PZH} (1)	DIR	A		35.2		24.1		22.4		18.8	ns
t_{PZL} (1)				38.2		24.9		23.2		19.3	
t_{PZH} (1)	DIR	B		27.9		20.4		18.3		16.9	ns
t_{PZL} (1)				27		21.6		19.5		18.7	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	ns
t_{PHL}			2	15.6	1.3	10	0.8	8	0.7	7	
t_{PLH}	B	A	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	ns
t_{PHL}			1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	
t_{PHZ}	DIR	A	2.9	10.3	3	10.3	2.8	10.3	3.4	10.3	ns
t_{PLZ}			1.8	8.6	1.6	8.6	2.2	8.7	2.2	8.7	
t_{PHZ}	DIR	B	5.4	23.5	3.9	13.1	2.9	11.8	2.4	9.8	ns
t_{PLZ}			3.3	17.5	2.9	10.8	2.4	10.1	1.7	7.9	
t_{PZH} (1)	DIR	A		28.8		20.2		18.9		16.3	ns
t_{PZL} (1)				31.6		21.5		19.8		17.3	
t_{PZH} (1)	DIR	B		27.1		19.6		17.5		16.1	ns
t_{PZL} (1)				25.9		20.3		18.3		17.3	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t_{PHL}			1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	
t_{PLH}	B	A	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	ns
t_{PHL}			1.7	10	0.9	7.6	0.7	7	0.5	6.5	
t_{PHZ}	DIR	A	2.1	8.4	2.2	8.4	2.2	8.5	2.2	8.4	ns
t_{PLZ}			0.9	6.8	1	6.8	1	6.7	0.9	6.7	
t_{PHZ}	DIR	B	4.8	23.2	2.5	12.8	1	11.5	2.5	9.5	ns
t_{PLZ}			4.2	17.8	2.5	10.4	2.5	10	1.6	7.5	
t_{PZH} (1)	DIR	A		28		18.5		17.4		14.4	ns
t_{PZL} (1)				31.2		20.4		18.5		16	
t_{PZH} (1)	DIR	B		24.9		17.3		15.1		13.6	ns
t_{PZL} (1)				23.6		17.6		16		14.6	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
C_{pdB} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver

Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

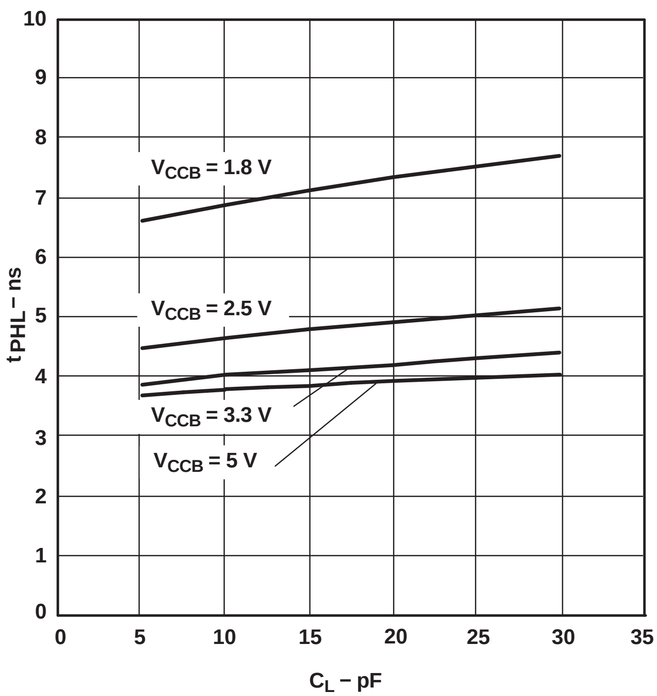
1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

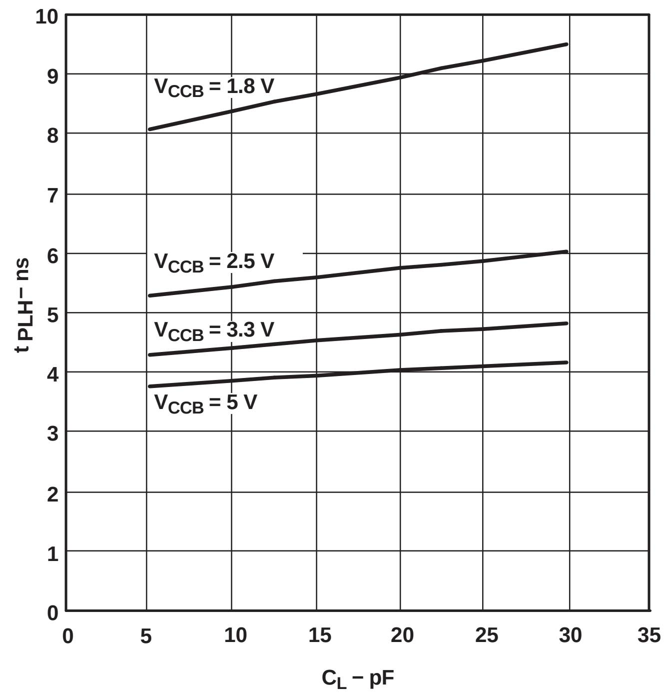
Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}					UNIT
	0 V	1.8 V	2.5 V	3.3 V	5 V	
0 V	0	<1	<1	<1	<1	µA
1.8 V	<1	<2	<2	<2	2	
2.5 V	<1	<2	<2	<2	<2	
3.3 V	<1	<2	<2	<2	<2	
5 V	<1	2	<2	<2	<2	

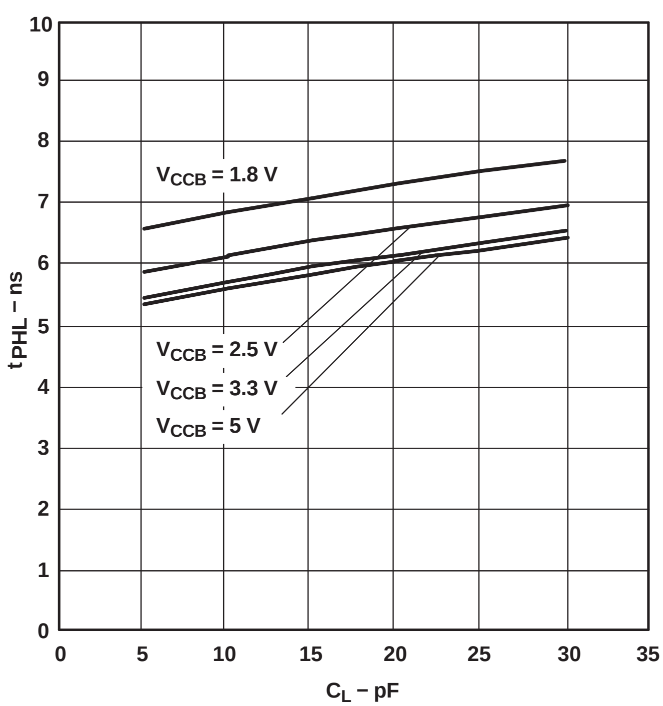
TYPICAL CHARACTERISTICS

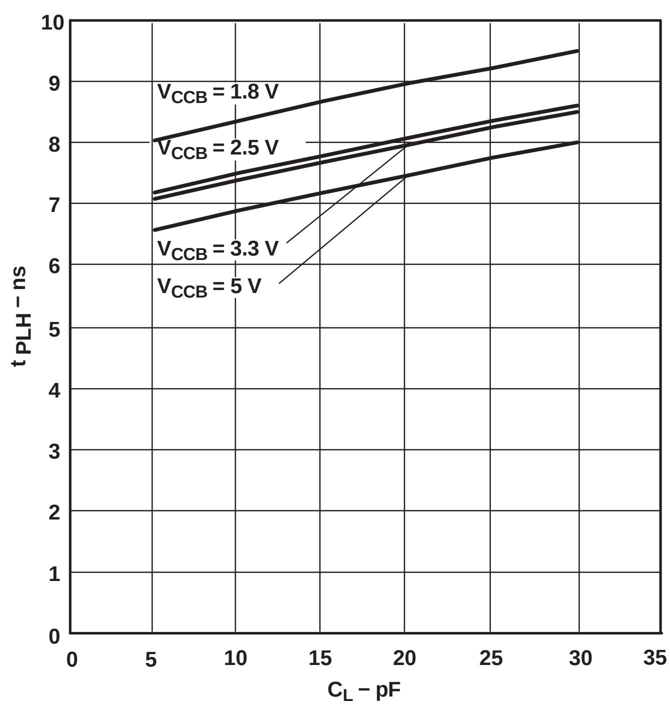
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 1.8 V





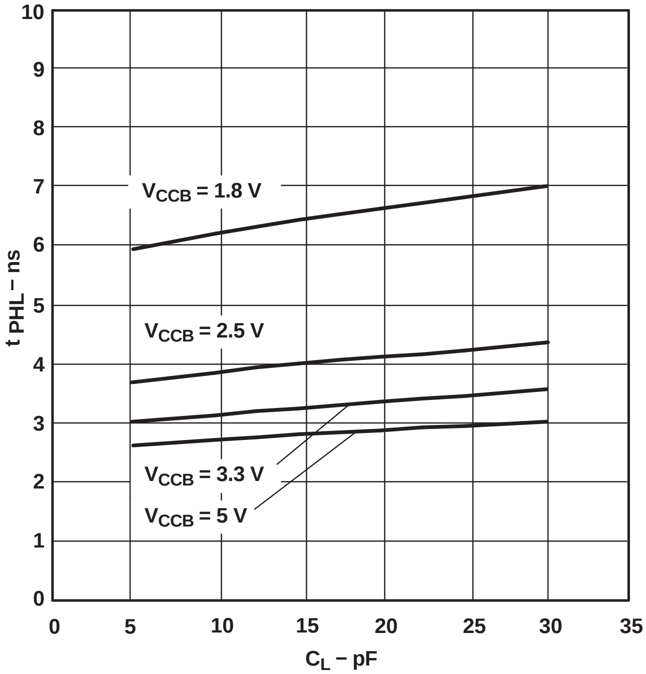
TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 1.8 V

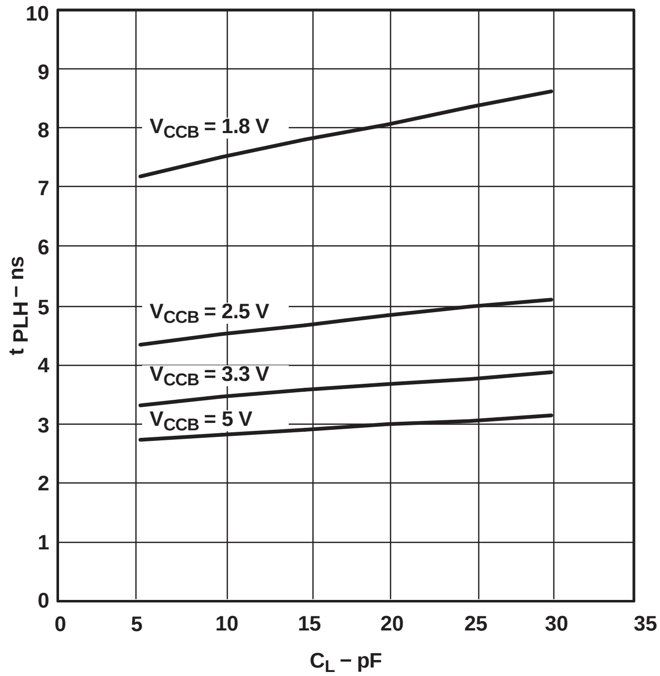




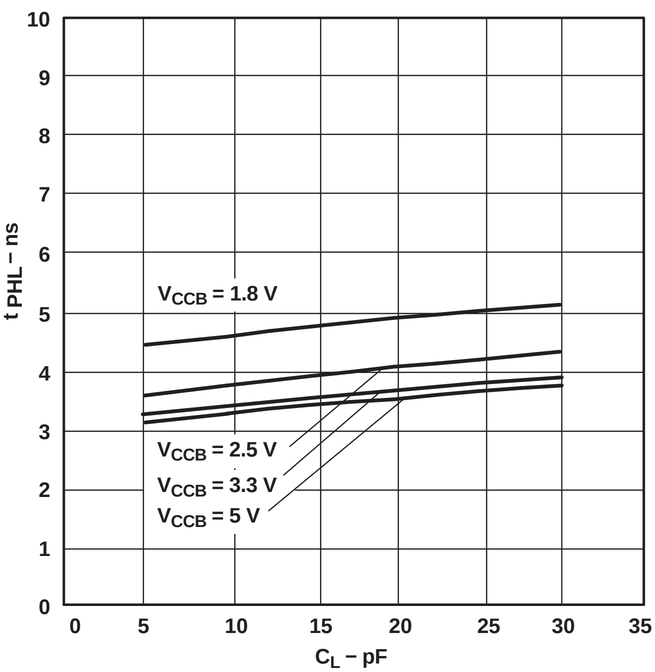
TYPICAL CHARACTERISTICS (continued)

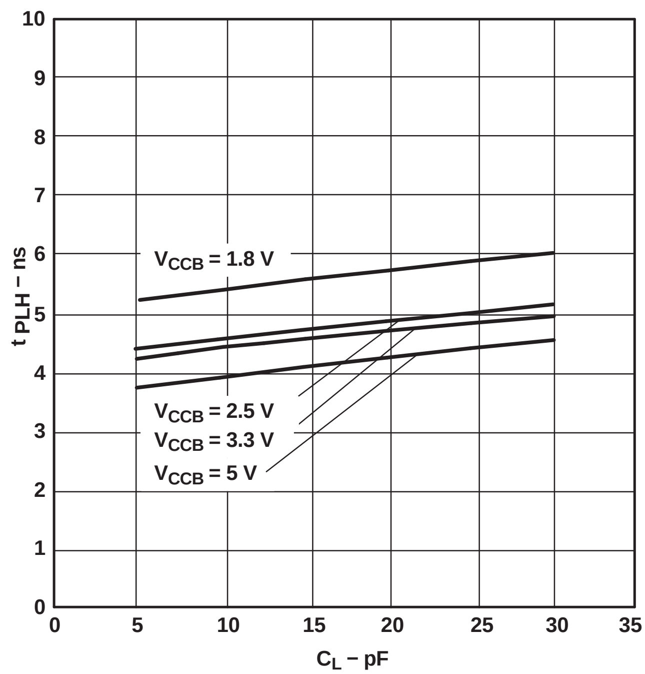
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 2.5 V





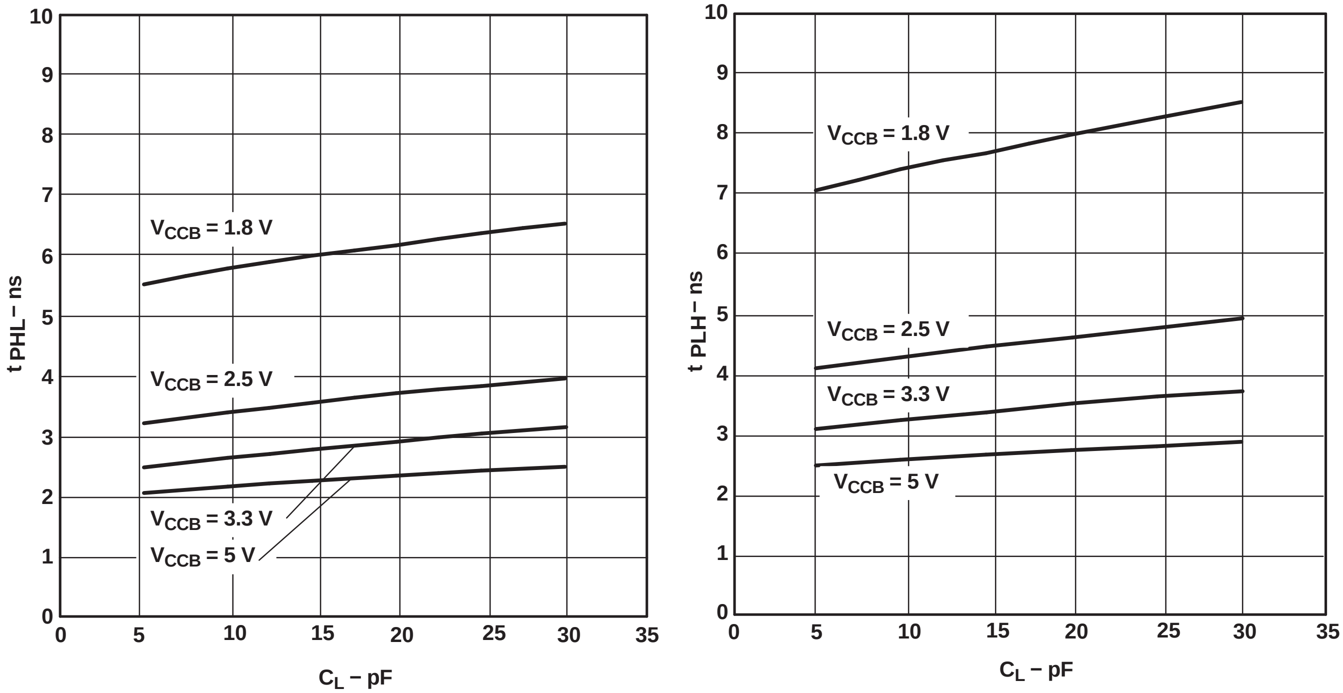
TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 2.5 V



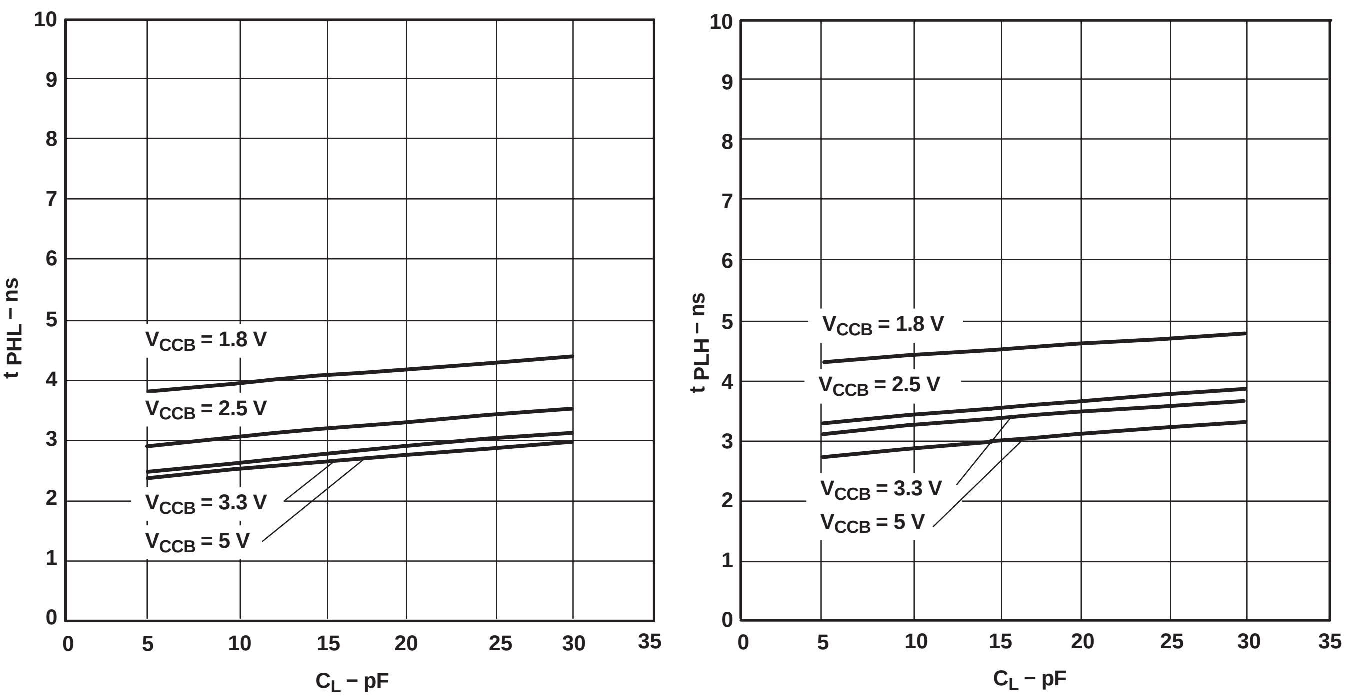


TYPICAL CHARACTERISTICS (continued)

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 3.3 V

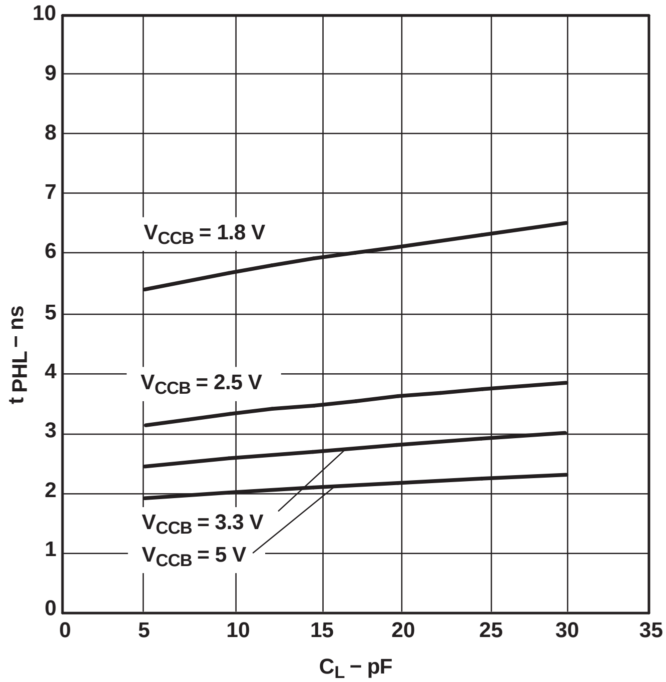


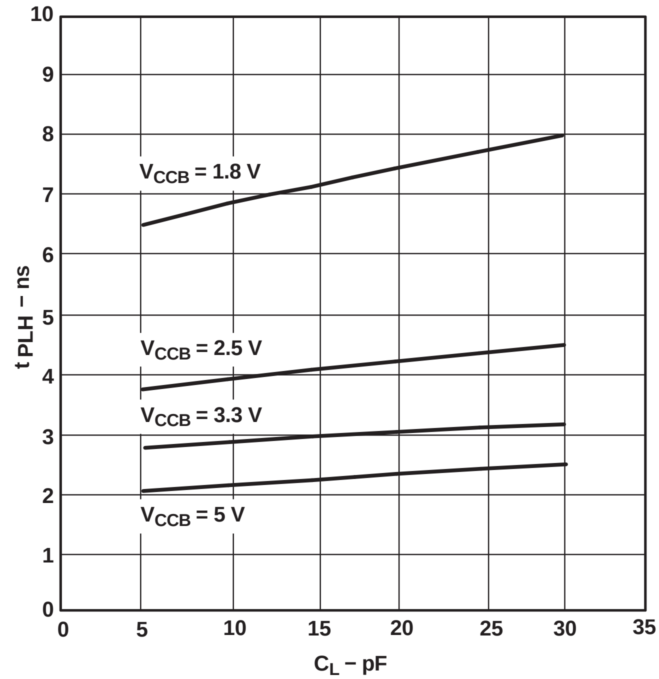
TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 3.3 V



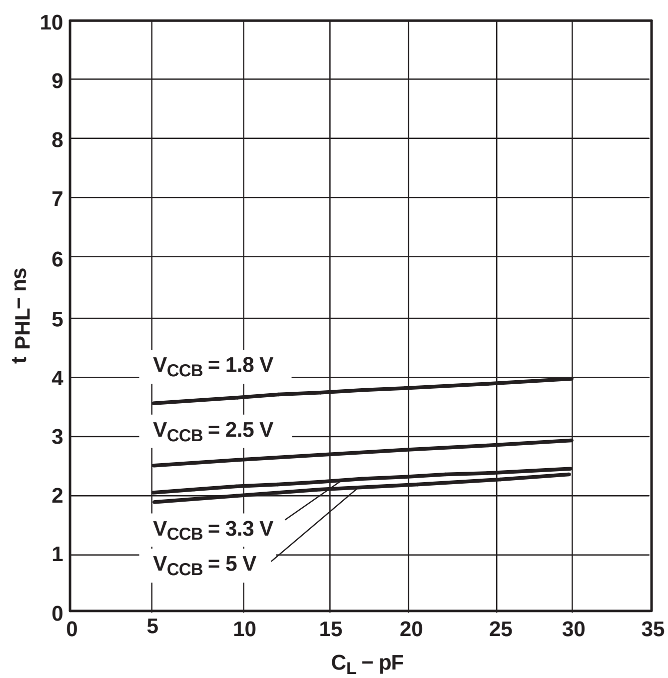
TYPICAL CHARACTERISTICS (continued)

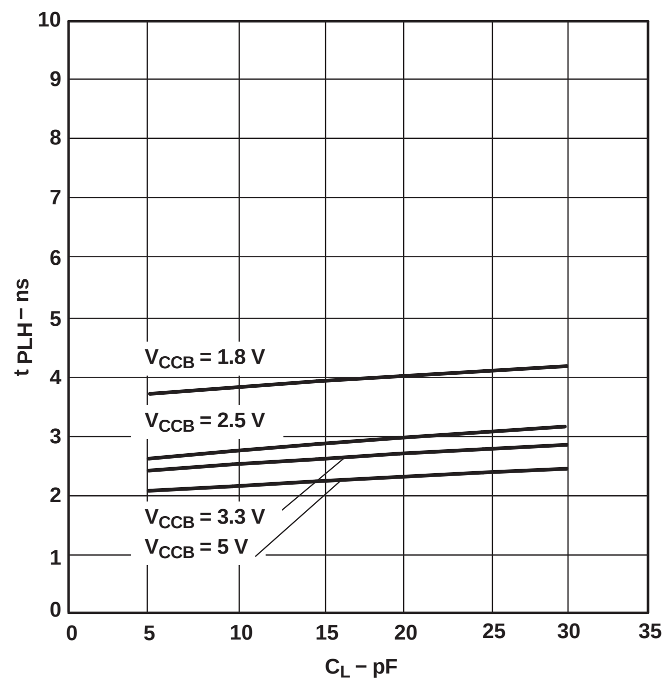
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 5 V



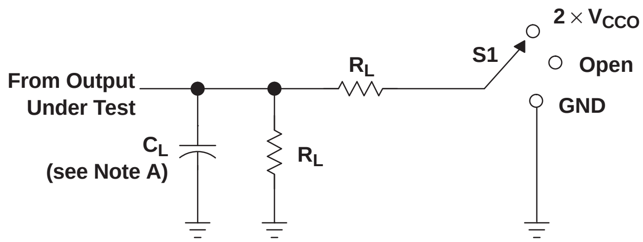


TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
T_A = 25°C, V_{CCA} = 5 V





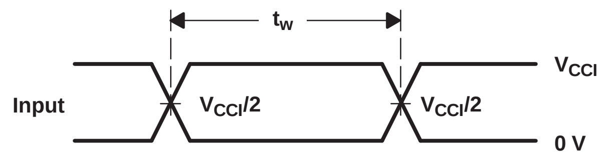
PARAMETER MEASUREMENT INFORMATION



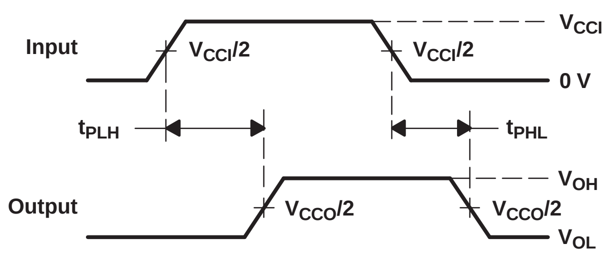
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

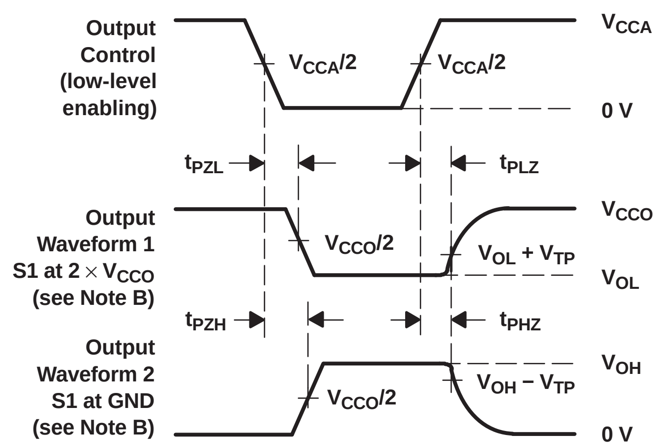
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



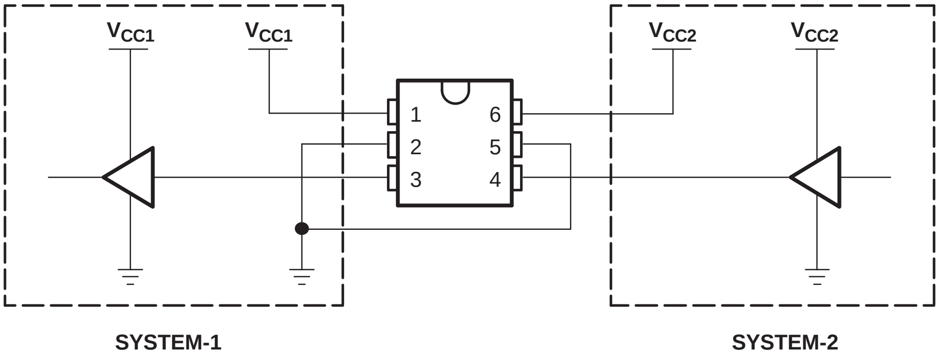
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 2 shows an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.

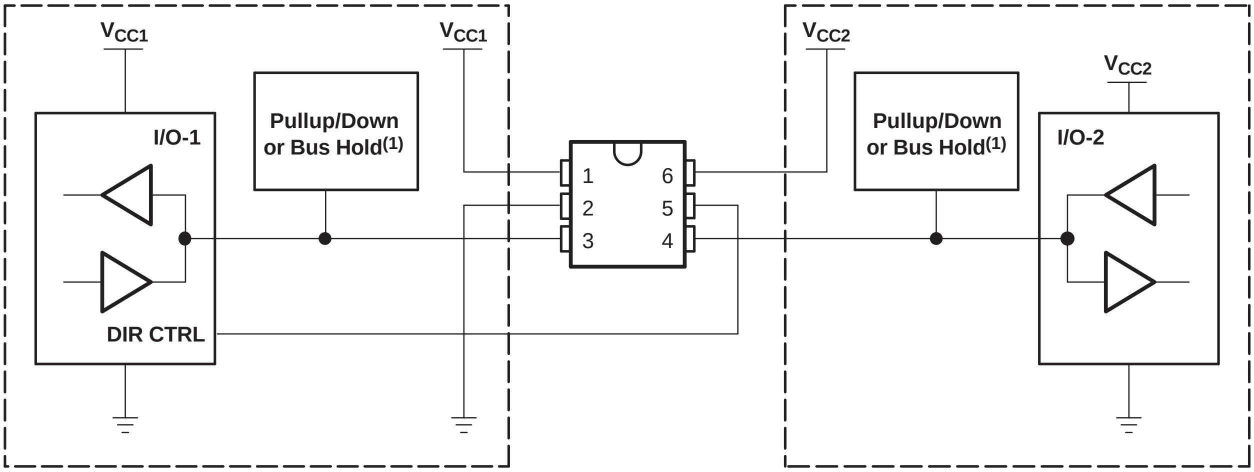


PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage.
4	B	IN	Input threshold value depends on V_{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

Figure 2. Unidirectional Logic Level-Shifting Application

APPLICATION INFORMATION

Figure 3 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 3. Bidirectional Logic Level-Shifting Application

Enable Times

Calculate the enable times for the SN74LVC1T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1T45MDCKREP	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXG
V62/09608-01XE	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1T45-EP :

- Catalog : SN74LVC1T45

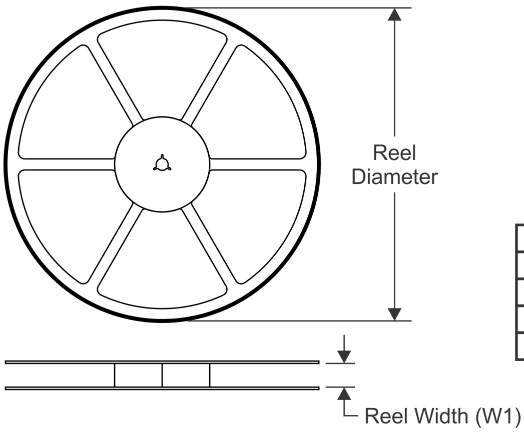
- Automotive : SN74LVC1T45-Q1

NOTE: Qualified Version Definitions:

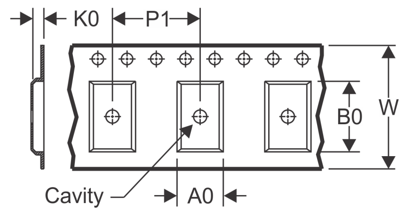
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

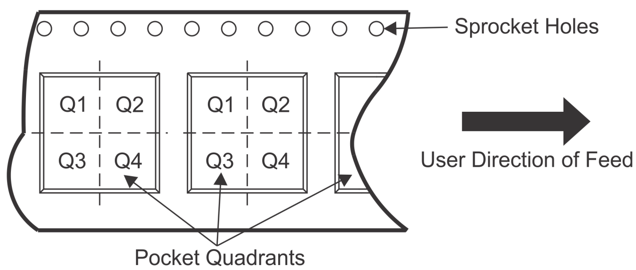


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

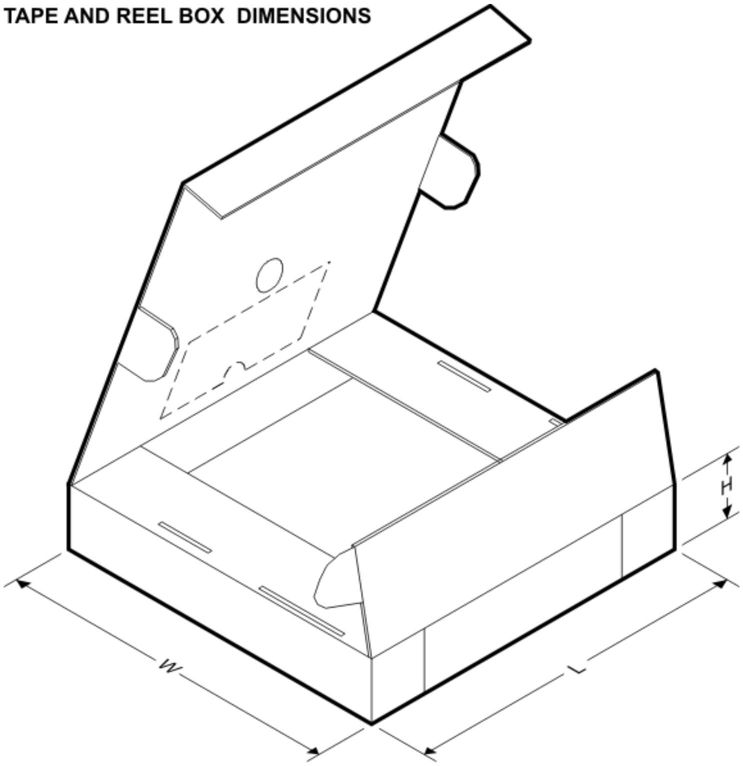
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45MDCKREP	SC70	DCK	6	3000	180.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



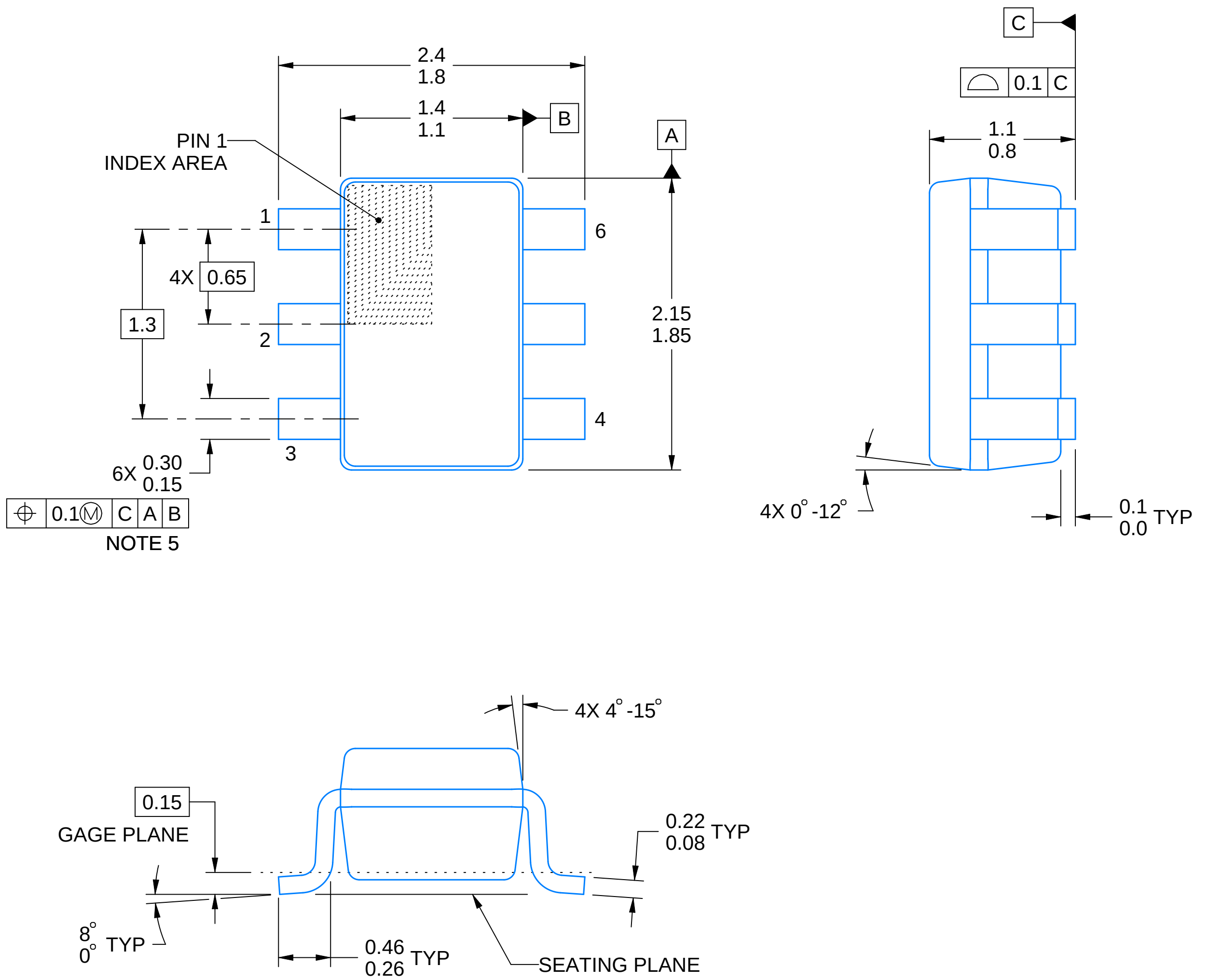
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45MDCKREP	SC70	DCK	6	3000	202.0	201.0	28.0

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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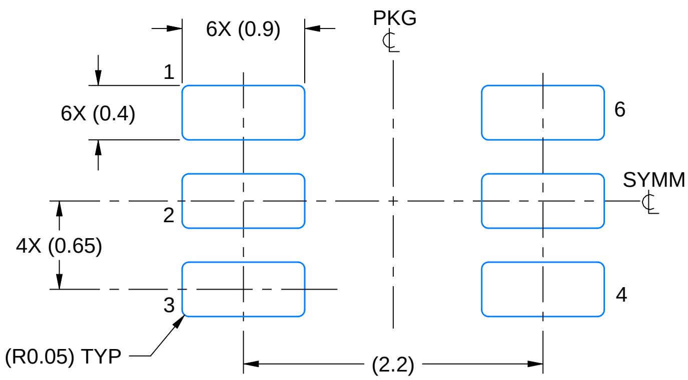
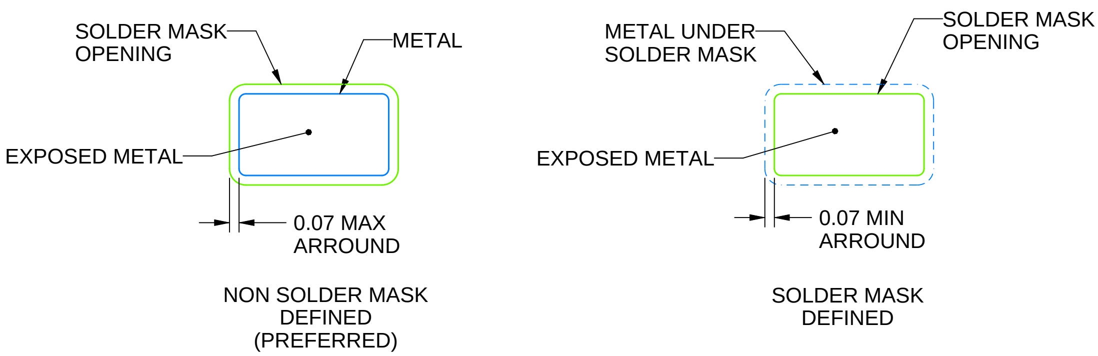
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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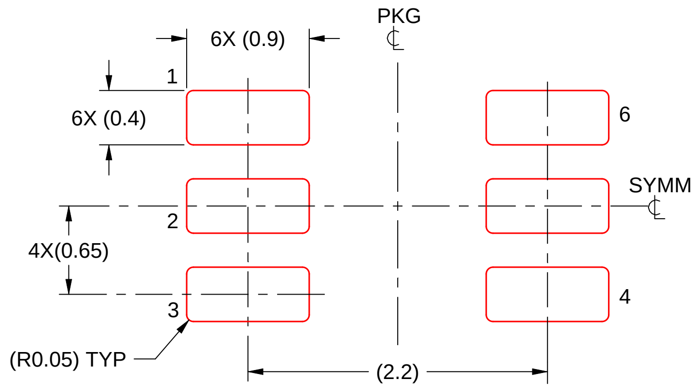
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.