

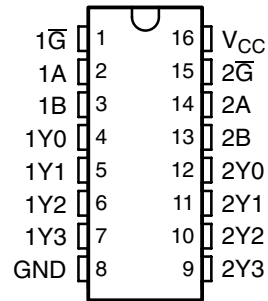
SN74LVC139A-Q1

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS782B – SEPTEMBER 2004 – REVISED JANUARY 2008

- Qualified for Automotive Applications
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.2 ns
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Level Per AEC-Q100 Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

This dual 2-line to 4-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION†

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Reel of 2500 | SN74LVC139AQDRQ1 | LVC139AQ |
| | TSSOP – PW | Reel of 2000 | SN74LVC139AQPWRQ1 | LC139AQ |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE
(each decoder/demultiplexer)

| INPUTS | | | OUTPUTS | | | |
|----------------|--------|---|---------|----|----|----|
| \overline{G} | SELECT | | | | | |
| | B | A | Y3 | Y2 | Y1 | Y0 |
| L | L | L | H | H | H | L |
| L | L | H | H | H | L | H |
| L | H | L | H | L | H | H |
| L | H | H | L | H | H | H |
| H | X | X | H | H | H | H |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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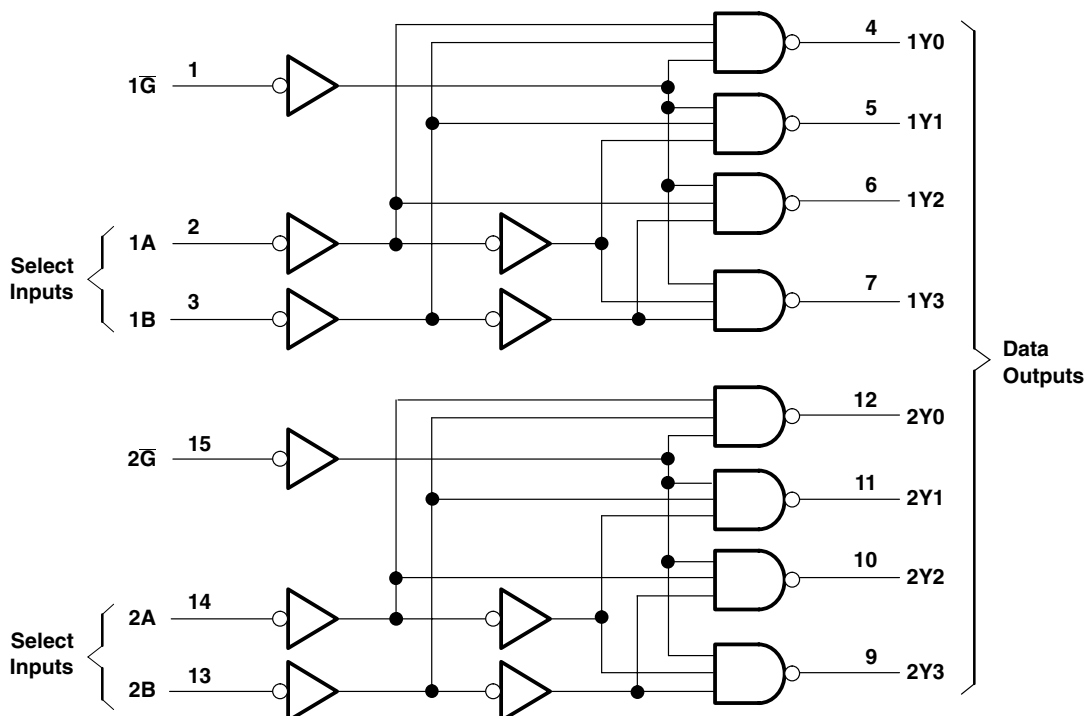
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SN74LVC139A-Q1

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS782B – SEPTEMBER 2004 – REVISED JANUARY 2008

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 6.5 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 6.5 V |
| Output voltage range, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O | ±50 mA |
| Continuous current through V_{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 73°C/W |
| (see Note 3): PW package | 108°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC139A-Q1

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS782B – SEPTEMBER 2004 – REVISED JANUARY 2008

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|--|---|----------------------|----------------------|------|
| V_{CC} Supply voltage | Operating | 1.65 | 3.6 | V |
| | Data retention only | 1.5 | | |
| V_{IH} High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | | |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | |
| V_{IL} Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | | $0.35 \times V_{CC}$ | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 0.7 | |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | |
| V_I Input voltage | | 0 | 5.5 | V |
| V_O Output voltage | | 0 | V_{CC} | V |
| I_{OH} High-level output current | $V_{CC} = 1.65\text{ V}$ | | -4 | mA |
| | $V_{CC} = 2.3\text{ V}$ | | -8 | |
| | $V_{CC} = 2.7\text{ V}$ | | -12 | |
| | $V_{CC} = 3\text{ V}$ | | -24 | |
| I_{OL} Low-level output current | $V_{CC} = 1.65\text{ V}$ | | 4 | mA |
| | $V_{CC} = 2.3\text{ V}$ | | 8 | |
| | $V_{CC} = 2.7\text{ V}$ | | 12 | |
| | $V_{CC} = 3\text{ V}$ | | 24 | |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | | 10 | ns/V |
| T_A Operating free-air temperature | | -40 | 125 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = -40^\circ\text{C to }125^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | | UNIT |
|------------------|--|-----------------|--|------|---------|---|------|---------|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{OH} | $I_{OH} = -100\text{ }\mu\text{A}$ | 1.65 V to 3.6 V | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | | V |
| | $I_{OH} = -4\text{ mA}$ | 1.65 V | 1.2 | | | 1.2 | | | |
| | $I_{OH} = -8\text{ mA}$ | 2.3 V | 1.7 | | | 1.7 | | | |
| | $I_{OH} = -12\text{ mA}$ | 2.7 V | 2.1 | | | 2.2 | | | |
| | | 3 V | 2.3 | | | 2.4 | | | |
| | $I_{OH} = -24\text{ mA}$ | 3 V | 2.1 | | | 2.2 | | | |
| V_{OL} | $I_{OL} = 100\text{ }\mu\text{A}$ | 1.65 V to 3.6 V | | | 0.2 | | | 0.2 | V |
| | $I_{OL} = 4\text{ mA}$ | 1.65 V | | | 0.45 | | | 0.45 | |
| | $I_{OL} = 8\text{ mA}$ | 2.3 V | | | 0.7 | | | 0.7 | |
| | $I_{OL} = 12\text{ mA}$ | 2.7 V | | | 0.4 | | | 0.4 | |
| | $I_{OL} = 24\text{ mA}$ | 3 V | | | 0.55 | | | 0.55 | |
| I_I All inputs | $V_I = 5.5\text{ V or GND}$ | 3.6 V | | | ± 5 | | | ± 5 | μA |
| I_{CC} | $V_I = V_{CC}\text{ or GND, } I_O = 0$ | 3.6 V | | | 10 | | | 10 | μA |
| ΔI_{CC} | One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | 2.7 V to 3.6 V | | | 500 | | | 500 | μA |
| C_i | $V_I = V_{CC}\text{ or GND}$ | 3.3 V | | 5 | | | 5 | | pF |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



SN74LVC139A-Q1

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS782B – SEPTEMBER 2004 – REVISED JANUARY 2008

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|--------------------|-----------------|----------------|-------------------------|-----|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 1 | 8.8 | 1 | 7.7 | ns |
| | \overline{G} | | 1 | 6.7 | 1 | 6.2 | |
| t _{sk(o)} | | | | | | 1 | ns |

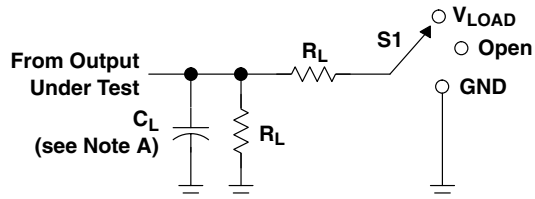
operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|---|--------------------|-------------------------|-------------------------|-------------------------|------|
| | | TYP | TYP | TYP | |
| C _{pd} Power dissipation capacitance | f = 10 MHz | 28.5 | 29.5 | 30.5 | pF |



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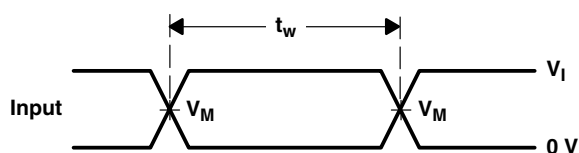
PARAMETER MEASUREMENT INFORMATION



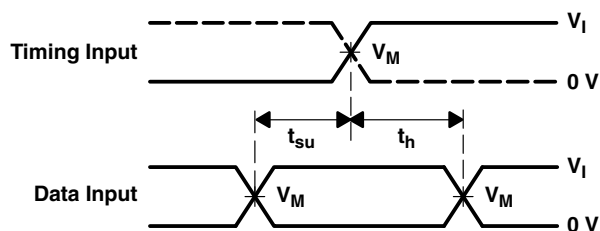
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

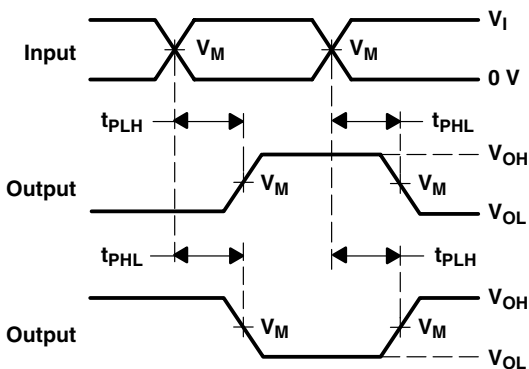
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|-----------------------------------|--------|---------------|-------|------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



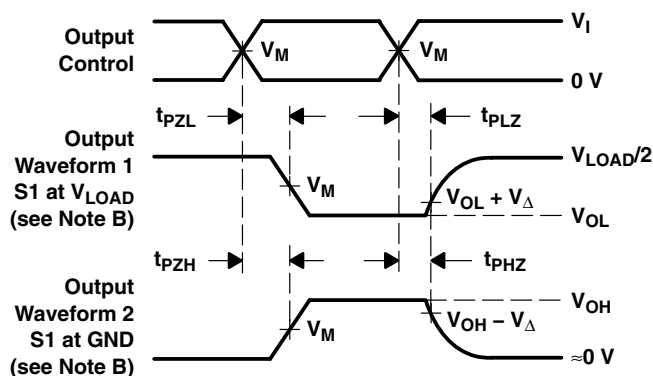
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CLVC139AQPWRG4Q1 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC139AQ |
| CLVC139AQPWRG4Q1.B | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC139AQ |
| SN74LVC139AQPWRQ1 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC139AQ |
| SN74LVC139AQPWRQ1.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC139AQ |
| SN74LVC139AQPWRQ1.B | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC139AQ |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC139A-Q1 :

- Catalog : [SN74LVC139A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVC139AQPWRG4Q1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC139AQPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CLVC139AQPWRG4Q1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC139AQPWRQ1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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