![Texas Instruments logo] **TEXAS INSTRUMENTS**

# SN74LV8T574 Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs and Integrated Level Translation

## 1 Features

- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- Up to 150Mbps with 5V or 3.3V $V_{CC}$
- Supports standard function pinout
- Latch-up performance exceeds 250mA per JESD 17
- Supports defense and aerospace applications:
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability

## 2 Applications

- Parallel data synchronization
- Parallel data storage
- Shift register
- Pattern generators

## 3 Description

The SN74LV8T574 contains eight D-type flip-flops. All channels share a latch enable (LE) input and output enable ($\overline{OE}$) input. This device has a flow-through pinout which allows for easier bus routing.

The input is designed with a reduced threshold circuit to support up translation when the supply voltage is larger than the input voltage. Additionally, the 5V tolerant input pins enable down translation when the input voltage is larger than the supply voltage. The output level is always referenced to the supply voltage ($V_{CC}$) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.
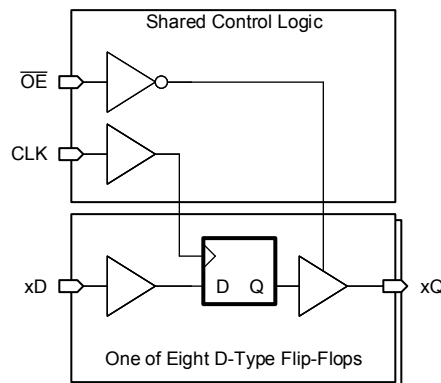
### Device Information

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE[3] |
|---|---|---|---|
| SN74LV8T574 | PW (TSSOP, 20) | 6.5mm × 6.4mm | 6.5mm x 4.4mm |
| | DGS (VSSOP, 20) | 5.1mm × 4.9mm | 5.1mm × 3.0mm |
| | RKS (VQFN, 20) | 4.5mm × 2.5mm | 4.5mm × 2.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



**Functional Block Diagram**

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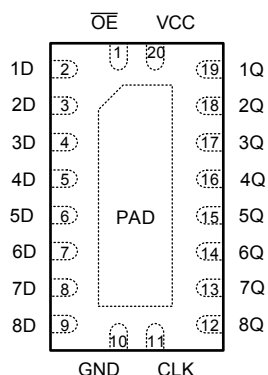
# 4 Pin Configuration and Functions



Figure 4-1. SN74LV8T574 RKS Package (Top View)
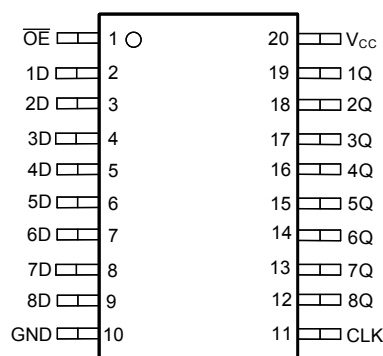


Figure 4-2. SN74LV8T574 PW , DGS Package (Top View)

**Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{\text{OE}}$ | 1 | Input | Output enable for all channels, active low |
| D1 | 2 | Input | Input for channel 1 |
| D2 | 3 | Input | Input for channel 2 |
| D3 | 4 | Input | Input for channel 3 |
| D4 | 5 | Input | Input for channel 4 |
| D5 | 6 | Input | Input for channel 5 |
| D6 | 7 | Input | Input for channel 6 |
| D7 | 8 | Input | Input for channel 7 |
| D8 | 9 | Input | Input for channel 8 |
| GND | 10 | — | Ground |
| CLK | 11 | Input | Clock input for all channels, rising edge triggered |
| Q8 | 12 | Output | Output for channel 8 |
| Q7 | 13 | Output | Output for channel 7 |
| Q6 | 14 | Output | Output for channel 6 |
| Q5 | 15 | Output | Output for channel 5 |
| Q4 | 16 | Output | Output for channel 4 |
| Q3 | 17 | Output | Output for channel 3 |
| Q2 | 18 | Output | Output for channel 2 |
| Q1 | 19 | Output | Output for channel 1 |
| $V_{CC}$ | 20 | — | Postive supply |
| Thermal Pad[2] | | — | The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply. |

(1)   Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2)   RKS package only.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | −0.5 | 7 | V |
| $V_I$ | Input voltage range[2] | | −0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state[2] | | −0.5 | 7 | V |
| $V_O$ | Output voltage range[2] | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5V | | -20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1)    Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2)    The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ±1000 | |

(1)    JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)    JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Thermal Information

| PACKAGE | PINS | THERMAL METRIC[1] | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| DGS (VSSOP) | 20 | 131.6 | 69.5 | 86.7 | 10.9 | 85.9 | N/A | °C/W |
| PW (TSSOP) | 20 | 116.8 | 58.5 | 78.7 | 12.6 | 77.9 | N/A | °C/W |
| RKS (VQFN) | 20 | 90.4 | 92.2 | 63.4 | 29 | 63.5 | 41.3 | °C/W |

(1)    For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65V to 2 V | 1.1 | | V |
| | | $V_{CC}$ = 2.25V to 2.75V | 1.28 | | |
| | | $V_{CC}$ = 3 V to 3.6V | 1.45 | | |
| | | $V_{CC}$ = 4.5V to 5.5V | 2 | | |

over operating free-air temperature range (unless otherwise noted)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65V to 2 V | | 0.51 | V |
| | | $V_{CC}$ = 2.25V to 2.75V | | 0.65 | |
| | | $V_{CC}$ = 3 V to 3.6V | | 0.75 | |
| | | $V_{CC}$ = 4.5V to 5.5V | | 0.8 | |
| $I_O$ | Output current | $V_{CC}$ = 1.6V to 2 V | | ±8 | mA |
| | | $V_{CC}$ = 2.25V to 2.75V | | ±15 | |
| | | $V_{CC}$ = 3.3 V to 5.0V | | ±25 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.6 V to 5.0V | | 20 | ns/V |
| Δt/Δ$V_{CC}$ | Safe supply ramp rate for POR | $V_{CC}$ = 1.6 V to 5.5 V | 6 | | μs/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = -50μA | 1.65V to 5.5V | $V_{CC}$-0.1 | | | $V_{CC}$-0.1 | $V_{CC}$-0.01 | | V |
| | $I_{OH}$ = -2mA | 1.65V to 2V | 1.28 | 1.7[1] | | 1.21 | 1.7[1] | | |
| | $I_{OH}$ = -3mA | 2.25V to 2.75V | 2 | 2.4[1] | | 1.93 | 2.4[1] | | |
| | $I_{OH}$ = -5.5mA | 3V to 3.6V | 2.6 | 3.08[1] | | 2.49 | 3.08[1] | | |
| | $I_{OH}$ = -8mA | 4.5V to 5.5V | 4.1 | 4.65[1] | | 3.95 | 4.65[1] | | |
| $V_{OL}$ | $I_{OL}$ = 50μA | 1.65V to 5.5V | | | 0.1 | | 0.01 | 0.1 | V |
| | $I_{OL}$ = 2mA | 1.65V to 2V | | 0.1[1] | 0.2 | | 0.1[1] | 0.25 | |
| | $I_{OL}$ = 3mA | 2.25V to 2.75V | | 0.15[1] | 0.17 | | 0.15[1] | 0.2 | |
| | $I_{OL}$ = 5.5mA | 3V to 3.6V | | 0.2[1] | 0.23 | | 0.2[1] | 0.25 | |
| | $I_{OL}$ = 8mA | 4.5V to 5.5V | | 0.3[1] | 0.3 | | 0.3[1] | 0.35 | |
| $I_I$ | $V_I$ = 0V or $V_{CC}$ | 0V to 5.5V | | | ±0.1 | | ±0.001 | ±1 | μA |
| $I_{CC}$ | $V_I$ = 0V or $V_{CC}$, $I_O$ = 0; open on loading | 1.65V to 5.5V | | | 2 | | 0.2 | 20 | μA |
| Δ$I_{CC}$ | One input at 0.3V or 3.4V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 5.5V | | | 1.35 | | 0.1 | 1.5 | mA |
| | One input at 0.3V or 1.1V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 1.8V | | | 10 | | 3.4 | 20 | μA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND and $V_{CC}$ = 5.5V | 5.5V | | | ±0.25 | | | ±2.5 | μA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5V | | 4 | 10 | | | 10 | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5V | | 3 | | | | | pF |
| $C_{PD}$ | No load, F = 1MHz | 5V | | 10 | | | | | pF |
| $V_{POR}$ | $V_{CC}$ ramp rate of 6μs/V to 100ms/V | 1.65V to 5.5V | | | 1.5 | | | 1.5 | V |

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)

## 5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $V_{CC}$ | $T_A$ = 25°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_W$ | Pulse duration | CLK | 1.8V | 3.7 | | 3.7 | | 3.7 | | ns |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | $V_{CC}$ | $T_A$ = 25°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{SU}$ | Setup time | Data before CLK rising edge | 1.8V | 1.9 | | 2.1 | | 2.2 | | ns |
| $t_H$ | Hold time | Data after CLK rising edge | 1.8V | 1 | | 1.1 | | 1.1 | | ns |
| $t_W$ | Pulse duration | CLK | 2.5V | 3.7 | | 3.7 | | 3.7 | | ns |
| $t_{SU}$ | Setup time | Data before CLK rising edge | 2.5V | 1.5 | | 1.7 | | 1.8 | | ns |
| $t_H$ | Hold time | Data after CLK rising edge | 2.5V | 0.6 | | 0.7 | | 0.7 | | ns |
| $t_W$ | Pulse duration | CLK | 3.3V | 3.7 | | 3.7 | | 3.7 | | ns |
| $t_{SU}$ | Setup time | Data before CLK rising edge | 3.3V | 1.3 | | 1.6 | | 1.6 | | ns |
| $t_H$ | Hold time | Data after CLK rising edge | 3.3V | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_W$ | Pulse duration | CLK | 5V | 3.7 | | 3.7 | | 3.7 | | ns |
| $t_{SU}$ | Setup time | Data before CLK rising edge | 5V | 0.2 | | 0.6 | | 0.6 | | ns |
| $t_H$ | Hold time | Data after CLK rising edge | 5V | 0.4 | | 0.4 | | 0.4 | | ns |

## 5.7 Switching Characteristics

$C_L$ = 50pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 85°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{max}$ | | | $C_L$ = 15pF | 1.8V | 98.1 | | | 89.3 | | | 85 | | | MHz |
| $f_{max}$ | | | $C_L$ = 15pF | 2.5V | 170.3 | | | 150.9 | | | 139.6 | | | MHz |
| $f_{max}$ | | | $C_L$ = 15pF | 3.3V | 185.6 | | | 183.1 | | | 170 | | | MHz |
| $f_{max}$ | | | $C_L$ = 15pF | 5V | 246.8 | | | 231.2 | | | 219.3 | | | MHz |
| $f_{max}$ | | | $C_L$ = 50pF | 1.8V | 71.8 | | | 67.5 | | | 67.5 | | | MHz |
| $f_{max}$ | | | $C_L$ = 50pF | 2.5V | 116.8 | | | 108.4 | | | 105.6 | | | MHz |
| $f_{max}$ | | | $C_L$ = 50pF | 3.3V | 133.1 | | | 124.3 | | | 120 | | | MHz |
| $f_{max}$ | | | $C_L$ = 50pF | 5V | 171.8 | | | 159.3 | | | 150 | | | MHz |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15pF | 1.8V | 8.6 | | 16.9 | 7.6 | | 18.5 | 7.4 | | 19.3 | ns |
| $t_{PHL}$ | | | | 1.8V | 9 | | 19 | 8 | | 20.5 | 7.7 | | 21.3 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 1.8V | 8.2 | | 15.8 | 7.5 | | 16.8 | 7.3 | | 17.3 | ns |
| $t_{PZH}$ | | | | 1.8V | 9.2 | | 16.8 | 8.3 | | 18.1 | 8.1 | | 18.8 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 1.8V | 7.7 | | 11.1 | 7.2 | | 11.9 | 7.1 | | 12.3 | ns |
| $t_{PHZ}$ | | | | 1.8V | 8 | | 12.6 | 7.2 | | 13.7 | 7.1 | | 14.4 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15pF | 2.5V | 6 | | 10.1 | 5.3 | | 11.2 | 5.2 | | 12 | ns |
| $t_{PHL}$ | | | | 2.5V | 5.9 | | 10.9 | 5.2 | | 12 | 5 | | 12.9 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 2.5V | 5.9 | | 9.7 | 5.4 | | 10.6 | 5.3 | | 11.2 | ns |
| $t_{PZH}$ | | | | 2.5V | 6.7 | | 10.6 | 6.1 | | 11.6 | 5.9 | | 12.2 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 2.5V | 5.8 | | 7.4 | 5.4 | | 8 | 5.2 | | 8.4 | ns |
| $t_{PHZ}$ | | | | 2.5V | 5.6 | | 8 | 5.1 | | 8.8 | 5 | | 9.3 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15pF | 3.3V | 5.2 | | 8.2 | 4.6 | | 9.2 | 4.5 | | 9.8 | ns |
| $t_{PHL}$ | | | | 3.3V | 4.9 | | 8.5 | 4.3 | | 9.5 | 4.1 | | 10.1 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 3.3V | 5.1 | | 8 | 4.7 | | 8.7 | 4.6 | | 9.2 | ns |
| $t_{PZH}$ | | | | 3.3V | 5.9 | | 8.7 | 5.4 | | 9.6 | 5.2 | | 10.1 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 3.3V | 5 | | 6.3 | 4.7 | | 6.7 | 4.6 | | 7 | ns |
| $t_{PHZ}$ | | | | 3.3V | 4.3 | | 6.4 | 3.8 | | 7.1 | 3.7 | | 7.5 | ns |

Product Folder Links: *SN74LV8T574*

$C_L$ = 50pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 85°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15pF | 5V | 4.6 | | 6.5 | 4.2 | | 7.1 | 4.1 | | 7.6 | ns |
| $t_{PHL}$ | | | | 5V | 4 | | 6.2 | 3.5 | | 6.9 | 3.5 | | 7.3 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 5V | 3.8 | | 5.5 | 3.4 | | 6 | 3.4 | | 6.4 | ns |
| $t_{PZH}$ | | | | 5V | 4.5 | | 6.1 | 4.1 | | 6.7 | 3.9 | | 7.2 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 15pF | 5V | 4.8 | | 5.6 | 4.7 | | 5.9 | 4.6 | | 6.2 | ns |
| $t_{PHZ}$ | | | | 5V | 3.6 | | 4.7 | 3.2 | | 5.2 | 3.2 | | 5.5 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50pF | 1.8V | 10.8 | | 20.9 | 9.6 | | 22.7 | 9.3 | | 23.6 | ns |
| $t_{PHL}$ | | | | 1.8V | 10.9 | | 22.5 | 9.8 | | 24.3 | 9.5 | | 25.3 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 1.8V | 10.6 | | 19.5 | 9.7 | | 20.8 | 9.5 | | 21.6 | ns |
| $t_{PZH}$ | | | | 1.8V | 11.7 | | 21.1 | 10.6 | | 22.7 | 10.4 | | 23.5 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 1.8V | 14.2 | | 17.8 | 13.7 | | 18.6 | 13.6 | | 19.1 | ns |
| $t_{PHZ}$ | | | | 1.8V | 14.5 | | 19.3 | 13.8 | | 20.4 | 13.6 | | 21.1 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50pF | 2.5V | 7.6 | | 12.7 | 6.7 | | 14.1 | 6.5 | | 15 | ns |
| $t_{PHL}$ | | | | 2.5V | 7.4 | | 13.3 | 6.6 | | 14.6 | 6.4 | | 15.6 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 2.5V | 8 | | 12.5 | 7.3 | | 13.5 | 7.2 | | 14.2 | ns |
| $t_{PZH}$ | | | | 2.5V | 8.7 | | 13.5 | 7.9 | | 14.7 | 7.6 | | 15.4 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 2.5V | 10.2 | | 11.9 | 9.6 | | 12.5 | 9.6 | | 12.9 | ns |
| $t_{PHZ}$ | | | | 2.5V | 10.1 | | 12.4 | 9.4 | | 13.2 | 9.2 | | 13.7 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50pF | 3.3V | 6.5 | | 10.3 | 5.8 | | 11.5 | 5.6 | | 12.2 | ns |
| $t_{PHL}$ | | | | 3.3V | 6.2 | | 10.6 | 5.6 | | 11.8 | 5.4 | | 12.4 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 3.3V | 7 | | 10.4 | 6.6 | | 11.3 | 6.5 | | 11.8 | ns |
| $t_{PZH}$ | | | | 3.3V | 7.7 | | 11.2 | 7 | | 12.2 | 6.8 | | 12.9 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 3.3V | 8.6 | | 9.9 | 8.3 | | 10.4 | 8.3 | | 10.7 | ns |
| $t_{PHZ}$ | | | | 3.3V | 7.9 | | 9.8 | 7.5 | | 10.5 | 7.4 | | 10.9 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50pF | 5V | 5.6 | | 8.1 | 5.1 | | 8.8 | 4.9 | | 9.4 | ns |
| $t_{PHL}$ | | | | 5V | 5.1 | | 7.8 | 4.7 | | 8.6 | 4.6 | | 9.2 | ns |
| $t_{PZL}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 5V | 5.4 | | 7.4 | 5 | | 8.1 | 4.9 | | 8.5 | ns |
| $t_{PZH}$ | | | | 5V | 5.8 | | 8.1 | 5.3 | | 8.8 | 5.2 | | 9.4 | ns |
| $t_{PLZ}$ | $\overline{OE}$ | Q | $C_L$ = 50pF | 5V | 7 | | 7.8 | 6.8 | | 8.2 | 6.8 | | 8.4 | ns |
| $t_{PHZ}$ | | | | 5V | 5.6 | | 6.8 | 5.3 | | 7.2 | 5.2 | | 7.6 | ns |
| $t_{sk(o)}$ | | | $C_L$ = 50pF | 1.8V | | | 0.4 | | | 0.4 | | | 0.3 | ns |
| $t_{sk(o)}$ | | | $C_L$ = 50pF | 2.5V | | | 0.3 | | | 0.3 | | | 0.3 | ns |
| $t_{sk(o)}$ | | | $C_L$ = 50pF | 3.3V | | | 0.3 | | | 0.3 | | | 0.3 | ns |
| $t_{sk(o)}$ | | | $C_L$ = 50pF | 5V | | | 0.4 | | | 0.4 | | | 0.3 | ns |

## 5.8 Noise Characteristics

$V_{CC}$ = 5V, $C_L$ = 50pF, $T_A$ = 25°C

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | -0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | | 2 | | V |

$V_{CC}$ = 5V, $C_L$ = 50pF, $T_A$ = 25°C

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

## 5.9 Typical Characteristics

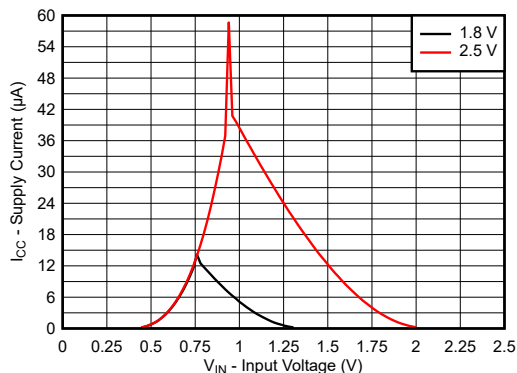$T_A$ = 25°C (unless otherwise noted)



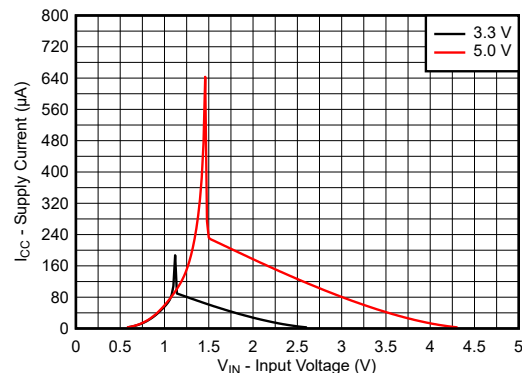Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply



Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply
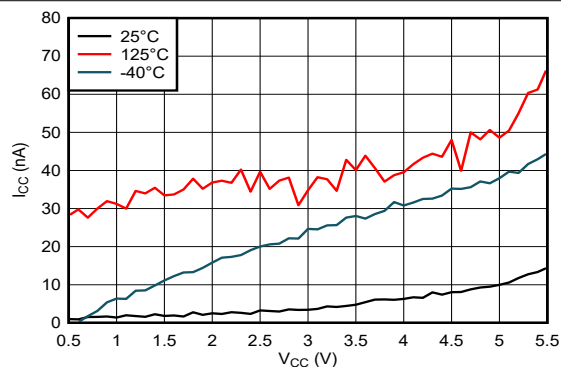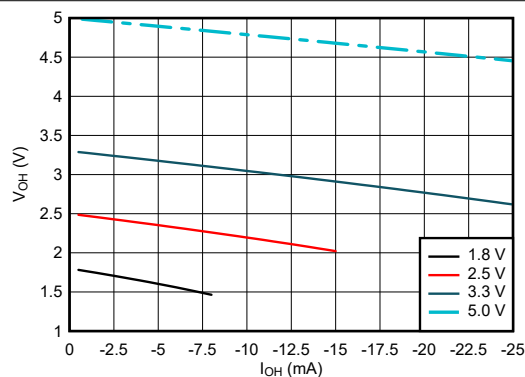


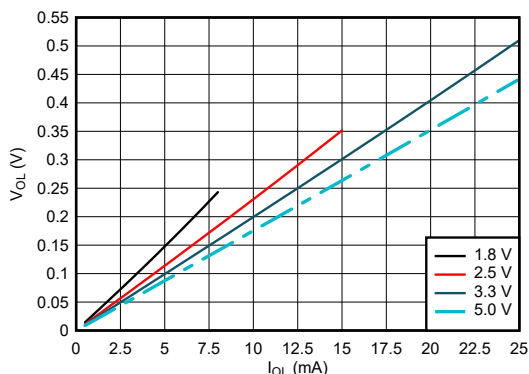Figure 5-3. Supply Current Across Supply Voltage



Figure 5-4. Output Voltage vs Current in HIGH State



Figure 5-5. Output Voltage vs Current in LOW State
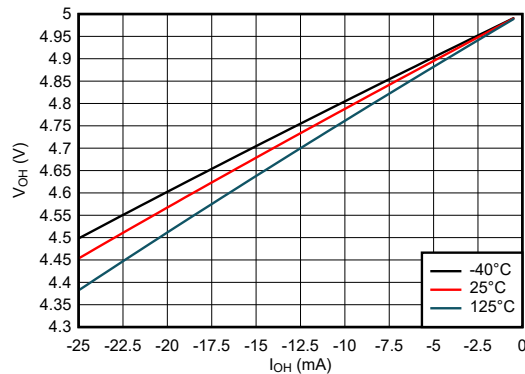


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

Product Folder Links: *SN74LV8T574*

## 5.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)



Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply
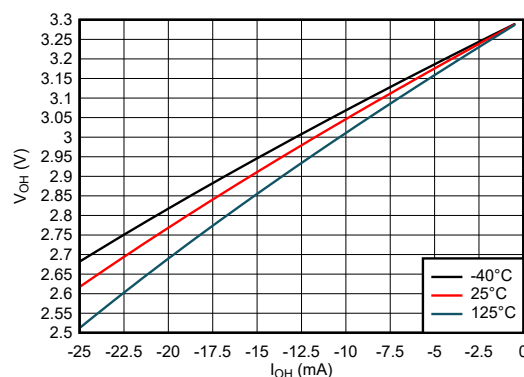


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply
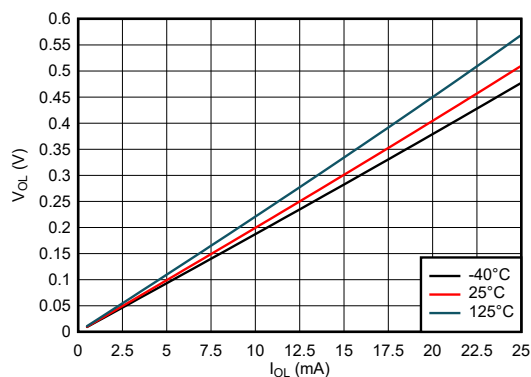


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply
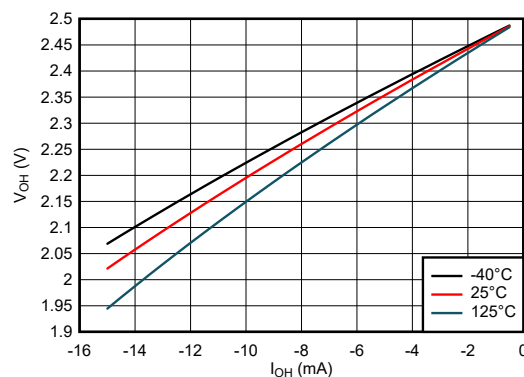


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply
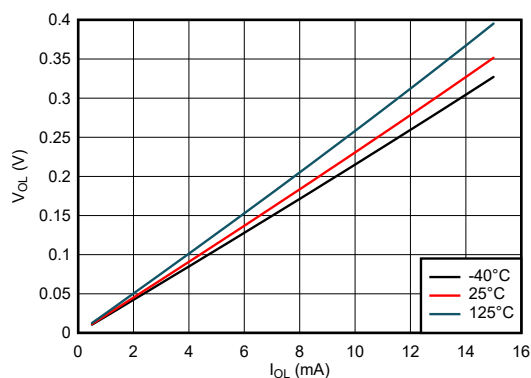


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply
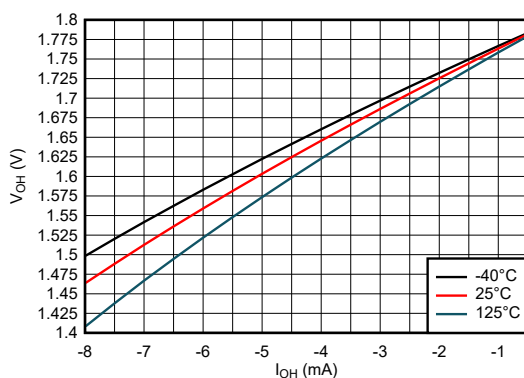


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

## 5.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)
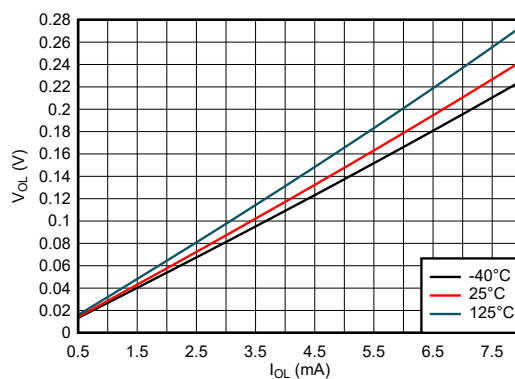


**Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

Product Folder Links: *SN74LV8T574*

# 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 2.5ns.

The outputs are measured individually with one input transition per measurement.

| TEST | S1 | S2 | $R_L$ | $C_L$ | ΔV | $V_{CC}$ |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | OPEN | OPEN | — | 15pF, 50pF | — | ALL |
| $t_{PLZ}$, $t_{PZL}$ | CLOSED | OPEN | 1kΩ | 15pF, 50pF | 0.15V | ≤ 2.5V |
| $t_{PHZ}$, $t_{PZH}$ | OPEN | CLOSED | 1kΩ | 15pF, 50pF | 0.15V | ≤ 2.5V |
| $t_{PLZ}$, $t_{PZL}$ | CLOSED | OPEN | 1kΩ | 15pF, 50pF | 0.3V | > 2.5V |
| $t_{PHZ}$, $t_{PZH}$ | OPEN | CLOSED | 1kΩ | 15pF, 50pF | 0.3V | > 2.5V |
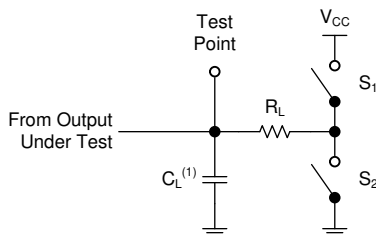


(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**
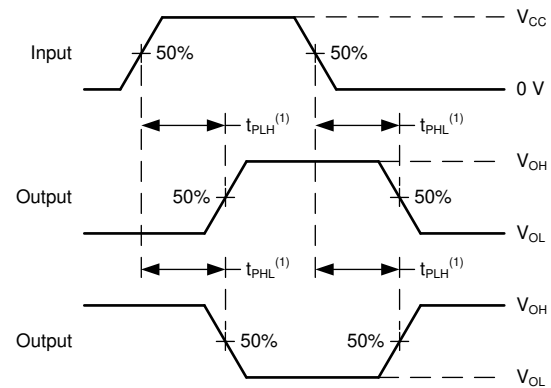


(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**
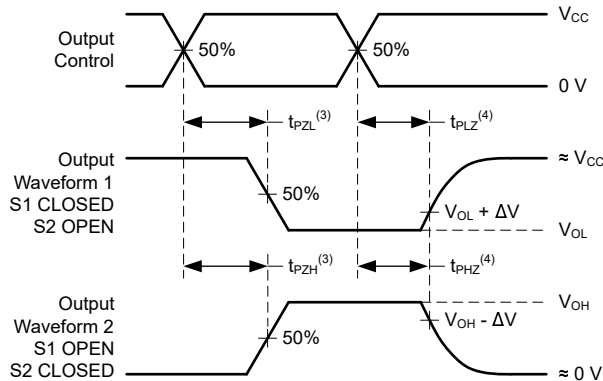


(3) The greater between $t_{PZL}$ and $t_{PZH}$ is the same as $t_{en}$.
(4) The greater between $t_{PLZ}$ and $t_{PHZ}$ is the same as $t_{dis}$.

**Figure 6-3. Voltage Waveforms Propagation Delays**
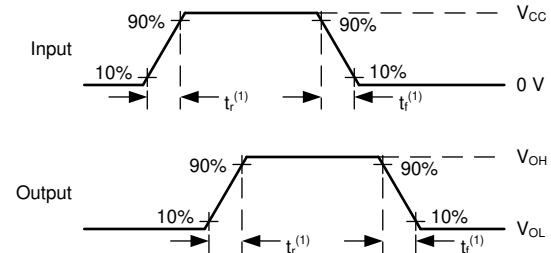


(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**Figure 6-4. Voltage Waveforms, Input and Output Transition Times**

# 7 Detailed Description

## 7.1 Overview

These 8-bit flip-flops feature 3-state outputs. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN74LV8T574 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Product Folder Links: *SN74LV8T574*

## 7.2 Feature Description

### 7.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 7.2.2 Latching Logic with Known Power-Up State

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory. In typical logic devices, the output state of each latching circuit is unknown after power is initially applied; however, this device includes an added Power On Reset (POR) circuit which sets the states of all included latching circuits during the power-up ramp prior to the device starting normal functionality.
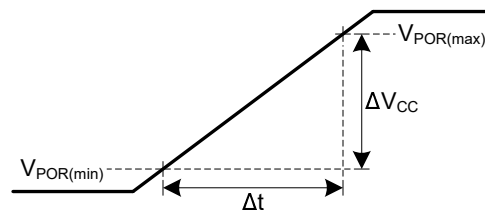


**Figure 7-1. Supply ($V_{CC}$) Ramp Characteristics for Known Power-Up State**

Figure 7-1 shows a correct supply voltage turn-on ramp and defines values used in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Prior to starting the power-on ramp, the supply must be completely off ($V_{CC} \leq V_{POR(min)}$).

The supply voltage must ramp at a rate within the range provided in the *Recommended Operating Conditions* table.

The output state of each latching logic circuit only remains stable as long as power is applied to the device ($V_{CC} \geq V_{POR(max)}$).

Variation from these recommendations will result in the device having an unknown power-up state.

### 7.2.3 LVxT Enhanced Input Voltage

The SN74LV8T574 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 7-2 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.
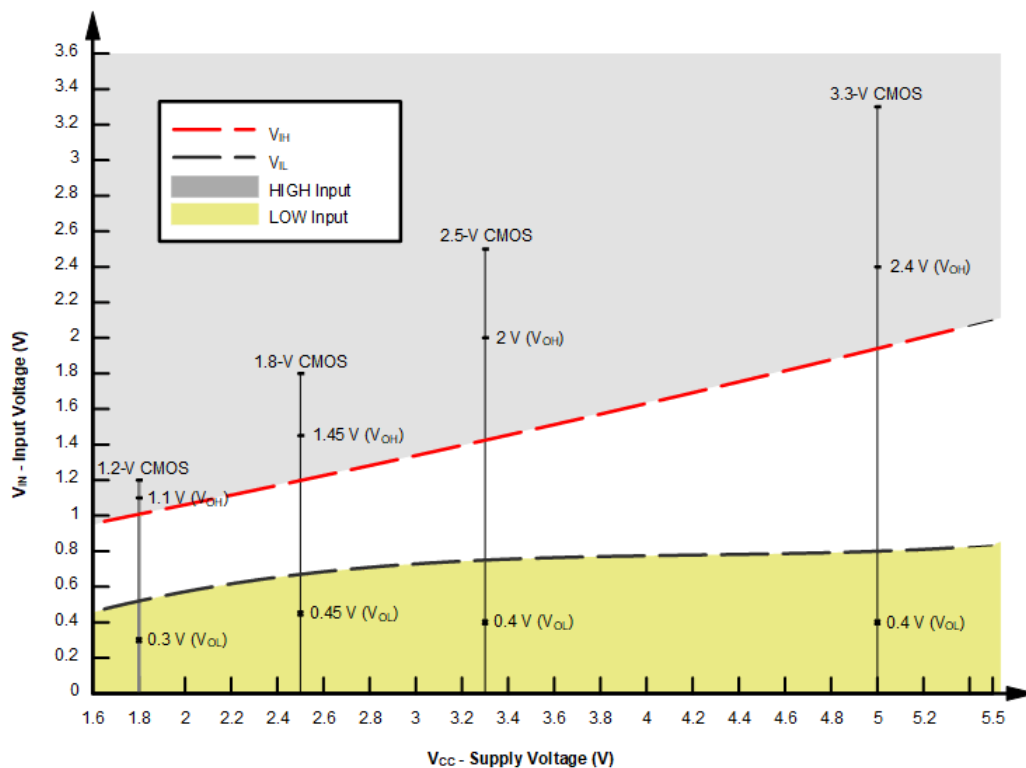


**Figure 7-2. LVxT Input Voltage Levels**

Product Folder Links: *SN74LV8T574*

### 7.2.3.1 Up Translation

Input signals can be up translated using the SN74LV8T574. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a $V_{IH(MIN)}$ of 3.5V. For the SN74LV8T574, $V_{IH(MIN)}$ with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-3.

*Up Translation Combinations* are as follows:
- 1.8V $V_{CC}$ – Inputs from 1.2V
- 2.5V $V_{CC}$ – Inputs from 1.8V
- 3.3V $V_{CC}$ – Inputs from 1.8V and 2.5V
- 5.0V $V_{CC}$ – Inputs from 2.5V and 3.3V
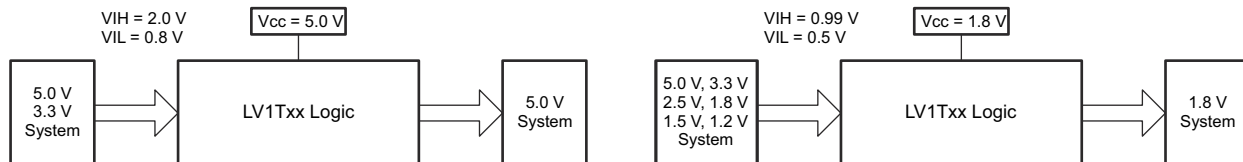


**Figure 7-3. LVxT Up and Down Translation Example**

### 7.2.3.2 Down Translation

Signals can be translated down using the SN74LV8T574. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V $V_{CC}$. See Figure 7-3.

*Down Translation Combinations* are as follows:
- 1.8V $V_{CC}$ – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V $V_{CC}$ – Inputs from 3.3V and 5.0V
- 3.3V $V_{CC}$ – Inputs from 5.0V

### 7.2.4 Clamp Diode Structure

As Figure 7-4 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

---

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
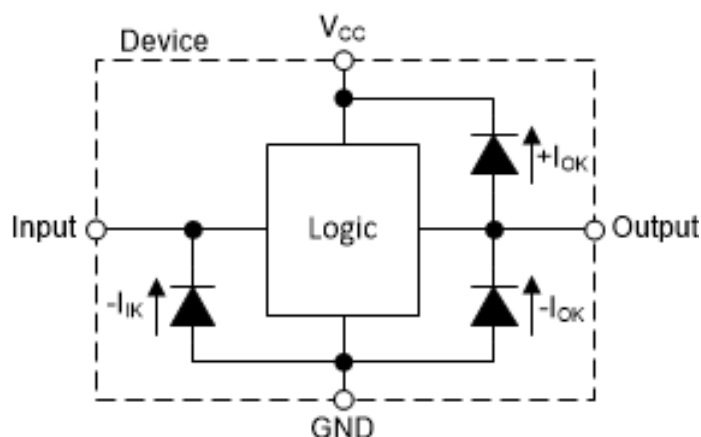
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**Figure 7-4. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.3 Functional Block Diagram
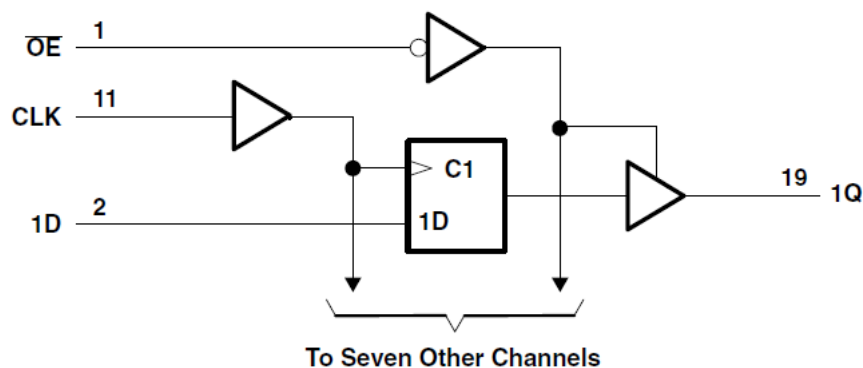


**Figure 7-5. Logic Diagram (Positive Logic)**

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS[1] | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L, H, ↓ | X | $Q_0$ |
| H | X | X | Z |

(1)　H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

# 8 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 8.1 Application Information

The SN74LV8T574 device is a high drive CMOS device that can be used for a variety of bus-interface type applications where the data needs to be retained or latched.

## 8.2 Typical Application
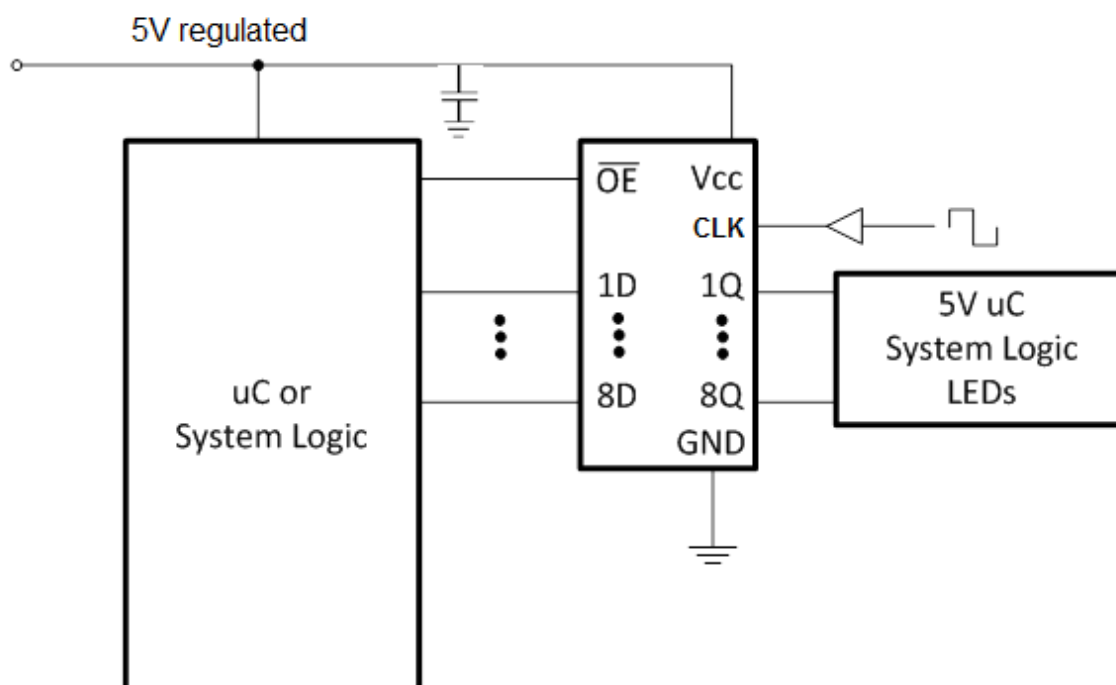


**Figure 8-1. Typical Application Schematic**

### *8.2.1 Design Requirements*

#### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV8T574 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T574 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T574 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T574 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

> **CAUTION**
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV8T574 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T574 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

### 8.2.3 Application Curves
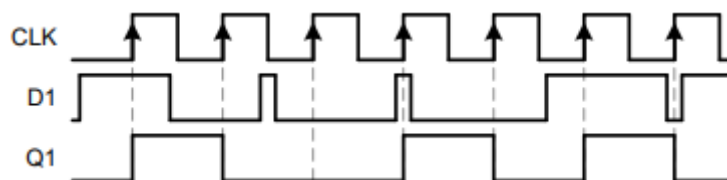


**Figure 8-2. Simplified Functional Diagram Showing Clock Operation**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

### 8.4.2 Layout Example
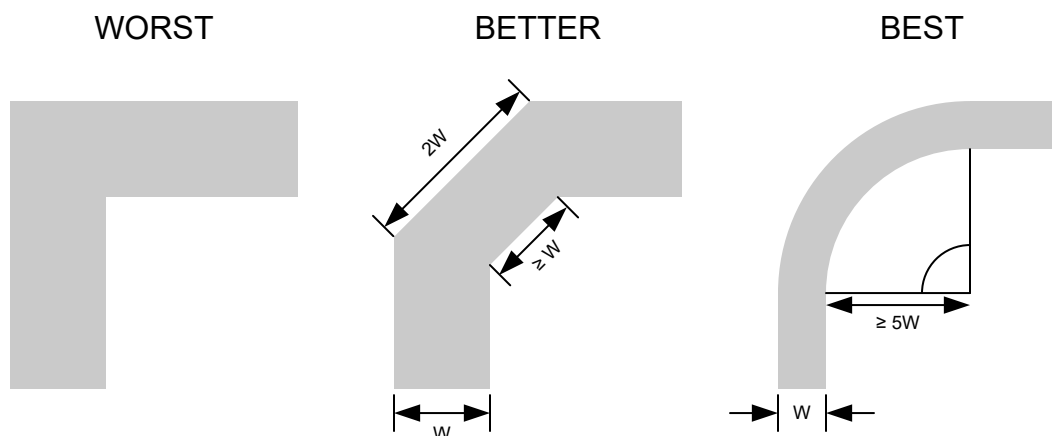


**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

![Texas Instruments logo]
**www.ti.com**
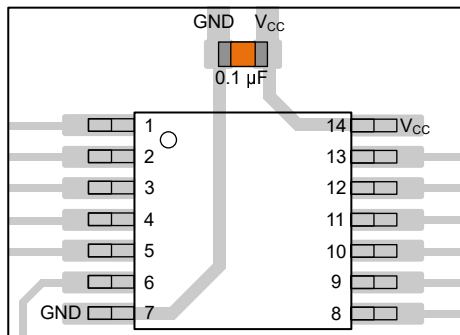


**Figure 8-4. Example Bypass Capacitor Placement
for TSSOP and Similar Packages**
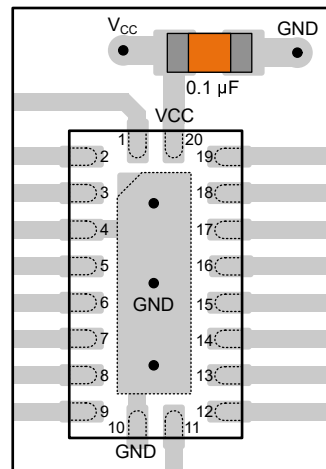


**Figure 8-5. Example Bypass Capacitor Placement
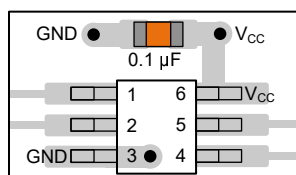for WQFN and Similar Packages**



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**
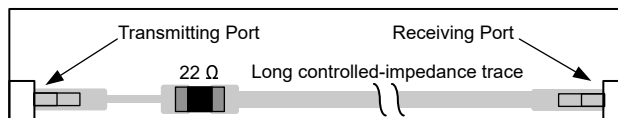


**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

Product Folder Links: *SN74LV8T574*

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

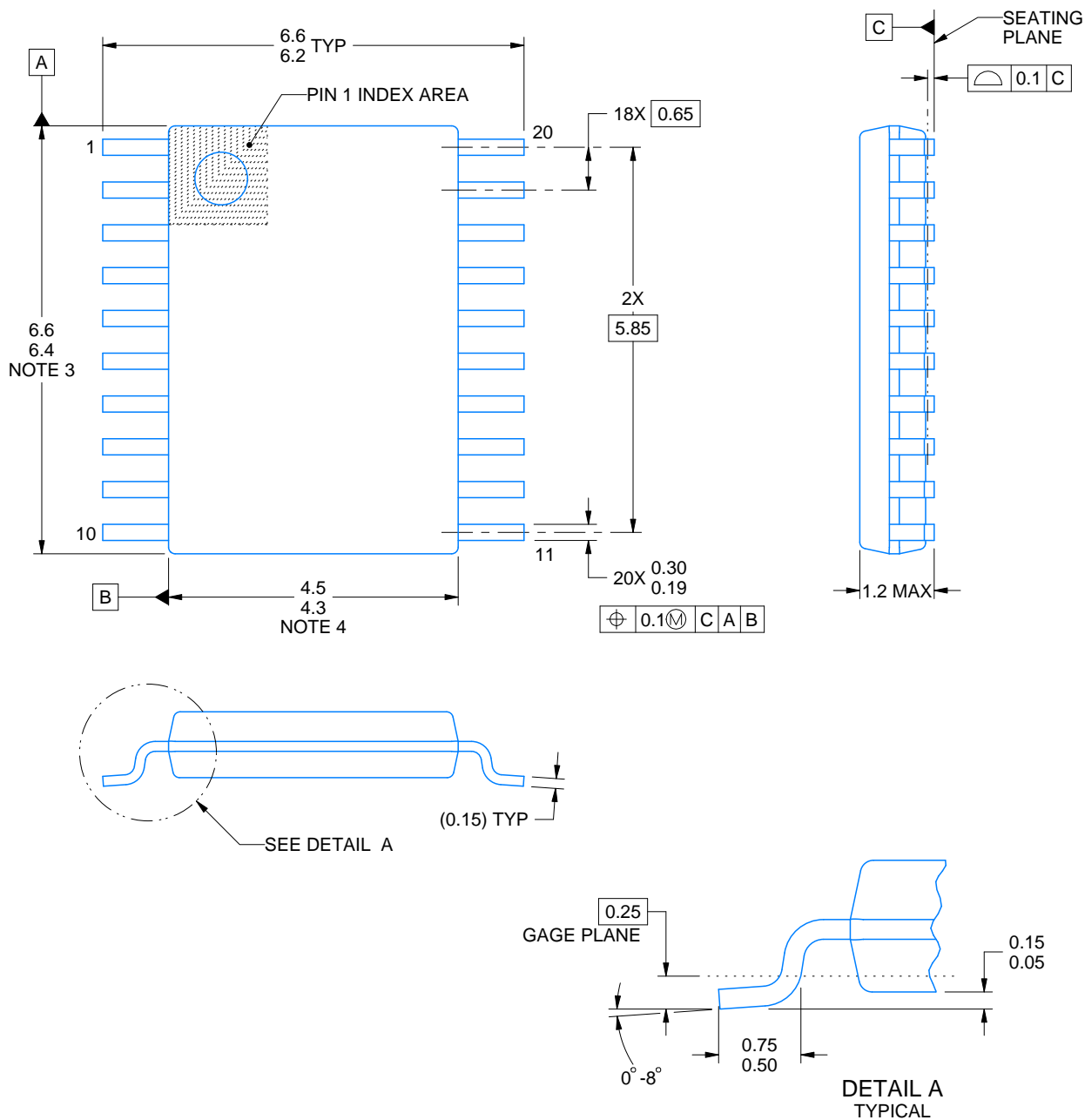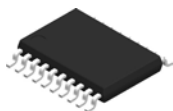TI Glossary      This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| September 2025 | * | Initial Release |

**Texas Instruments**
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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
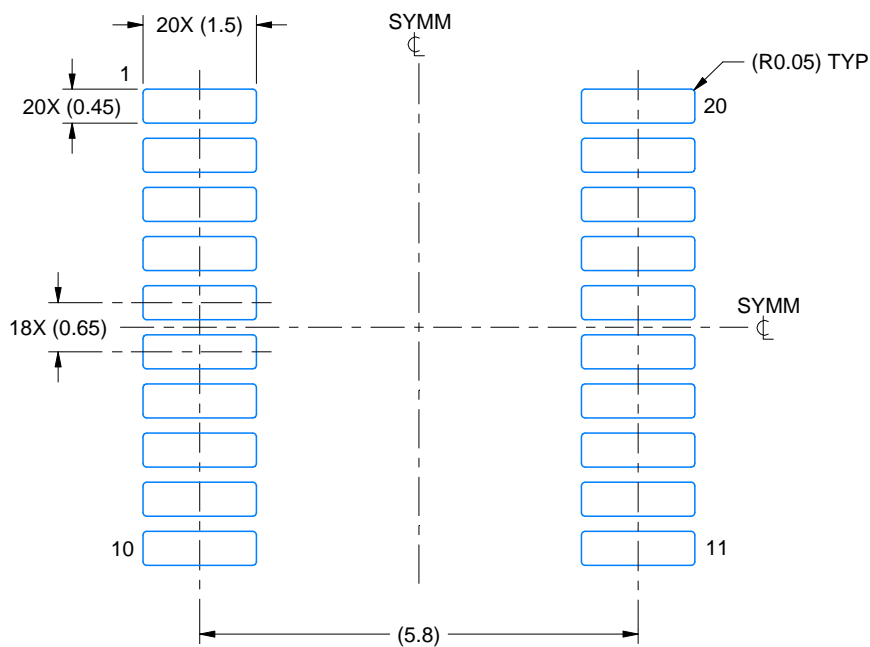
A

6.6
6.2 TYP

PIN 1 INDEX AREA

1

20

18X 0.65

6.6
6.4
NOTE 3

2X

5.85

10

11

B

4.5
4.3
NOTE 4

20X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C

SEATING
PLANE

◯ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

**DETAIL A**
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**
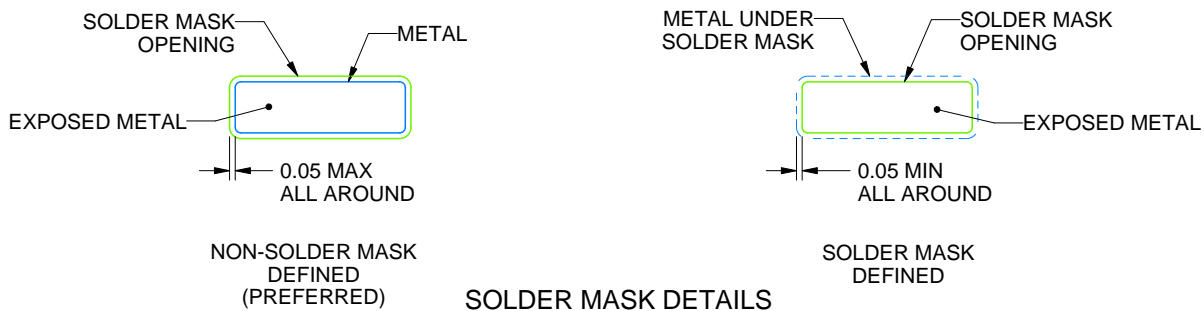
4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)
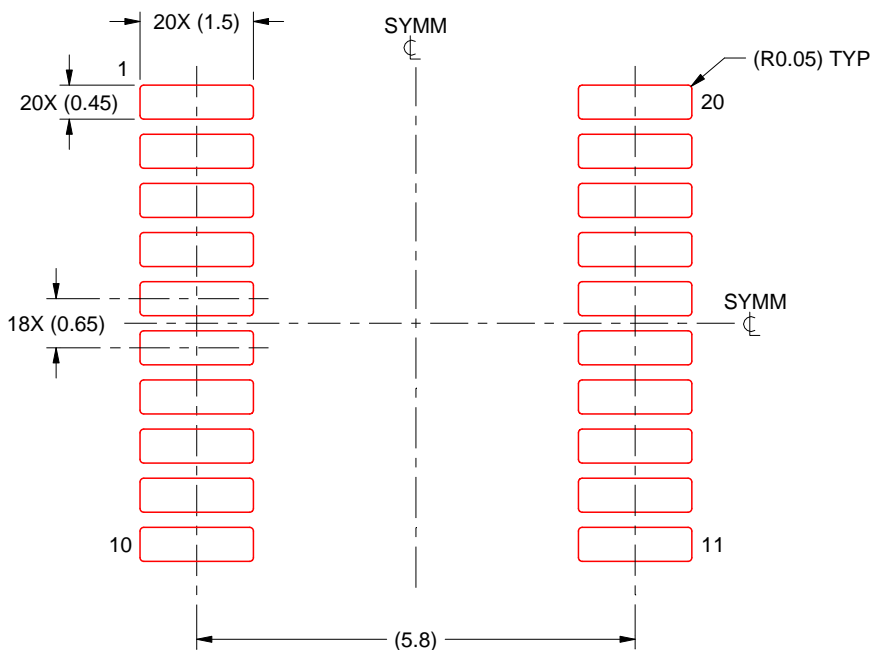
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.