SN74LV8T541-Q1 車載用 3 ステート出力、ロジック レベル シフタ搭載、オクタル バッファ / ドライバ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 幅広い動作範囲:1.65V～5.5V
- 5.5V 耐圧入力ピン
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」を参照):
  - 昇圧変換:
    - 1.2V から 1.8V
    - 1.5V から 2.5V
    - 1.8V から 3.3V
    - 3.3V から 5.0V
  - 降圧変換:
    - 5.0V、3.3V、2.5V から 1.8V
    - 5.0V、3.3V から 2.5V
    - 5.0V から 3.3V
- 5V または 3.3V の V_{CC} で最大 150Mbps
- 標準機能ピン配置をサポート
- JESD 17 準拠で
  250mA 超のラッチアップ性能

2 アプリケーション

- デジタル サイネージ
- インジケータ LED の制御
- マイクロコントローラの出力数増加

3 概要

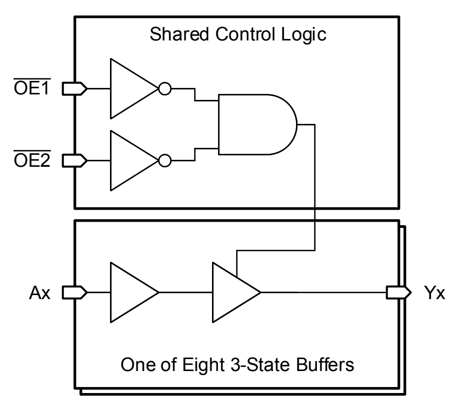
SN74LV8T541-Q1 は 3 ステート出力を備えた 8 個のバッファを搭載しています。アクティブ Low の出力イネーブル ピン ($\overline{OE1}$、$\overline{OE2}$) は 8 つのチャネルをすべて制御し、この両方が Low のときのみ出力がアクティブになるよう構成されています。

入力は、スレッショルドを低減した回路を使用して設計されており、電源電圧が入力電圧より高い場合の昇圧変換をサポートします。また、5V 許容の入力ピンにより、入力電圧が電源電圧より高い場合の降圧変換が可能です。出力レベルは常に電源電圧 (V_{CC}) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (公称) (3)
SN74LV8T541-Q1	PW (TSSOP、20)	6.5mm × 6.4mm	6.5mm × 4.4mm

(1) 詳細については、セクション 13 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



概略論理図 (正論理)

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4 Pin Configuration and Functions

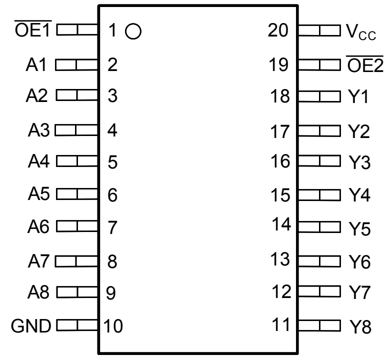

図 4-1. PW Package, 20-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{OE1}$	1	I	Output enable input 1, active low
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
Y8	11	O	Output for channel 8
Y7	12	O	Output for channel 7
Y6	13	O	Output for channel 6
Y5	14	O	Output for channel 5
Y4	15	O	Output for channel 4
Y3	16	O	Output for channel 3
Y2	17	O	Output for channel 2
Y1	18	O	Output for channel 1
$\overline{OE2}$	19	I	Output enable input 2, active low
V_{CC}	20	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	7	V
V_O	Output voltage range[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 2V	1.1		V
		V_{CC} = 2.25V to 2.75V	1.28		
		V_{CC} = 3V to 3.6V	1.45		
		V_{CC} = 4.5V to 5.5V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V to 2V		0.51	V
		V_{CC} = 2.25V to 2.75V		0.65	
		V_{CC} = 3V to 3.6V		0.75	
		V_{CC} = 4.5V to 5.5V		0.8	
I_O	Output current	V_{CC} = 1.6V to 2V		±8	mA
		V_{CC} = 2.25V to 2.75V		±15	
		V_{CC} = 3.3V to 5.0V		±25	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.6V to 5.0V		20	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		PW (TSSOP)	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -50µA	1.65V to 5.5V	V_{CC}-0.1			V_{CC}-0.1			V
	I_{OH} = -2mA	1.65V to 2V	1.28	1.7 [1]		1.21			
	I_{OH} = -3mA	2.25V to 2.75V	2	2.4[1]		1.93			
	I_{OH} = -5.5mA	3V to 3.6V	2.6	3.08 [1]		2.49			
	I_{OH} = -8mA	4.5V to 5.5V	4.1	4.65 [1]		3.95			
V_{OL}	I_{OL} = 50 uA	1.65V to 5.5V			0.1			0.1	V
	I_{OL} = 2mA	1.65V to 2V		0.1[1]	0.2			0.25	
	I_{OL} = 3mA	2.25V to 2.75V		0.15 [1]	0.17			0.2	
	I_{OL} = 5.5mA	3V to 3.6V		0.2[1]	0.23			0.25	
	I_{OL} = 8mA	4.5V to 5.5V		0.3[1]	0.3			0.35	
I_I	V_I = 0V or V_{CC}	0V to 5.5V			±0.1			±1	µA
I_{CC}	V_I = 0V or V_{CC}, I_O = 0; open on loading	1.65V to 5.5V			2			20	µA
ΔI_{CC}	One input at 0.3V or 3.4V, other inputs at 0 or V_{CC}, I_O = 0	5.5V			1.35			1.5	mA
	One input at 0.3V or 1.1V, other inputs at 0 or V_{CC}, I_O = 0	1.8V			10			20	µA
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5V	5.5V			±0.25			±2.5	µA
C_I	V_I = V_{CC} or GND	5V		4	10			10	pF
C_O	V_O = V_{CC} or GND	5V		5					pF
C_{PD}	No load, F = 1MHz	5V		17					pF

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)

ADVANCE INFORMATION

5.6 Switching Characteristics

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	C_L = 15pF	1.8V	5.3		12.1	4.8		13.4	ns
t_{PHL}					6.7		15.8	5.9		17.4	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	1.8V	9		20.5	7.9		23	ns
t_{PZL}					8.1		19.3	7.1		21.4	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	1.8V	7		13.2	6.3		15	ns
t_{PLZ}					6.7		11.7	6.3		12.9	ns
t_{PLH}	A	Y	C_L = 50pF	1.8V	7.3		16.4	6.5		18.2	ns
t_{PHL}					8.4		19.6	7.5		21.7	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	1.8V	11.4		25.1	9.9		28.2	ns
t_{PZL}					10.1		23.5	9		26	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	1.8V	12.8		20.5	12		22.5	ns
t_{PLZ}					12.6		19	12		20.3	ns
$t_{sk(o)}$			C_L = 50pF	1.8V			0.3			0.3	ns
t_{PLH}	A	Y	C_L = 15pF	2.5V	3.9		7.7	3.4		8.7	ns
t_{PHL}					4.9		9.8	4.3		11.2	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	2.5V	6.6		12.6	5.7		14.7	ns
t_{PZL}					5.8		11.6	5		13.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	2.5V	5		8.5	4.4		9.8	ns
t_{PLZ}					5.1		7.9	4.6		8.8	ns
t_{PLH}	A	Y	C_L = 50pF	2.5V	5.3		10.6	4.7		12	ns
t_{PHL}					6.2		12.5	5.5		14.2	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	2.5V	8.4		15.9	7.3		18.3	ns
t_{PZL}					7.5		14.7	6.7		16.9	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	2.5V	8.8		13.4	8.1		14.8	ns
t_{PLZ}					9		12.8	8.5		13.8	ns
$t_{sk(o)}$			C_L = 50pF	2.5V			0.3			0.3	ns
t_{PLH}	A	Y	C_L = 15pF	3.3V	3.4		6.3	3		7.3	ns
t_{PHL}					4.2		8.1	3.7		9.3	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	3.3V	5.7		10.3	5		11.9	ns
t_{PZL}					5		9.5	4.4		11	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	3.3V	3.7		6.7	3.2		7.9	ns
t_{PLZ}					4.4		6.6	4.1		7.4	ns
t_{PLH}	A	Y	C_L = 50pF	3.3V	4.6		8.8	4		10	ns
t_{PHL}					5.5		10.4	4.9		11.9	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	3.3V	7.4		13.1	6.4		15.1	ns
t_{PZL}					6.7		12.1	6		14	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	3.3V	7		10.5	6.5		11.7	ns
t_{PLZ}					7.6		10.6	7.3		11.4	ns
$t_{sk(o)}$			C_L = 50pF	3.3V			0.2			0.2	ns
t_{PLH}	A	Y	C_L = 15pF	5V	3.1		5.4	2.9		6.1	ns
t_{PHL}					3.1		5.5	2.8		6.3	ns

5.6 Switching Characteristics (続き)

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	5V	4.3		7.1	3.7		8.4	ns
t_{PZL}					3.6		6.4	3.2		7.6	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	5V	3.1		5	2.7		5.8	ns
t_{PLZ}					4.3		6	4		6.5	ns
t_{PLH}	A	Y	C_L = 50pF	5V	4.1		7.2	3.7		8.1	ns
t_{PHL}					4.2		7.2	3.8		8.4	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	5V	5.6		9.4	4.9		10.9	ns
t_{PZL}					5		8.6	4.5		9.9	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	5V	4.9		7.3	4.6		8.1	ns
t_{PLZ}					6.3		8.4	6.1		8.9	ns
$t_{sk(o)}$			C_L = 50pF	5V			0.3			0.3	ns

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

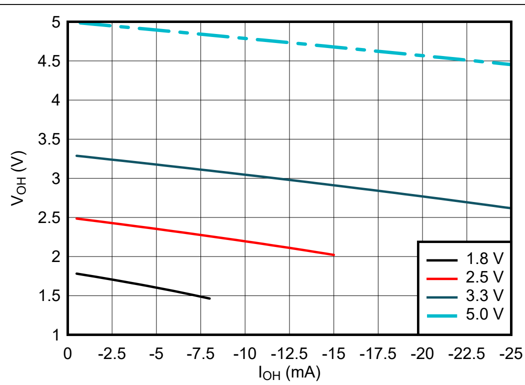

図 5-1. Output Voltage vs Current in HIGH State

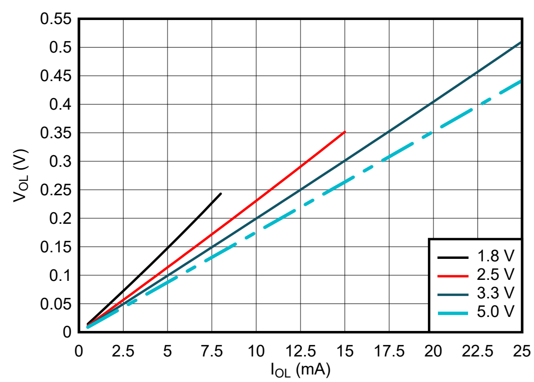

図 5-2. Output Voltage vs Current in LOW State

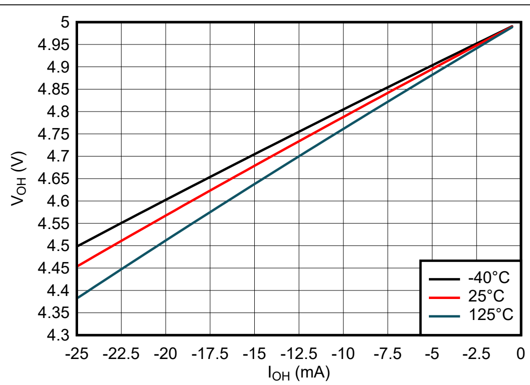

図 5-3. Output Voltage vs Current in HIGH State; 5-V Supply

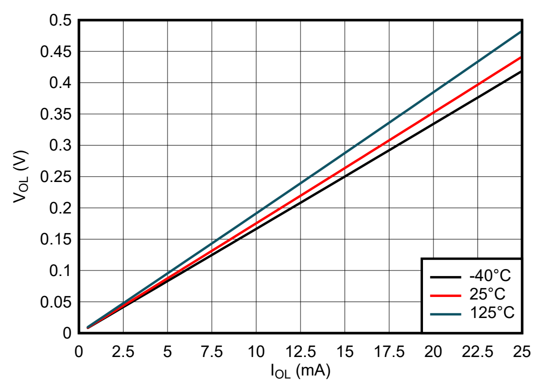

図 5-4. Output Voltage vs Current in LOW State; 5-V Supply

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5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

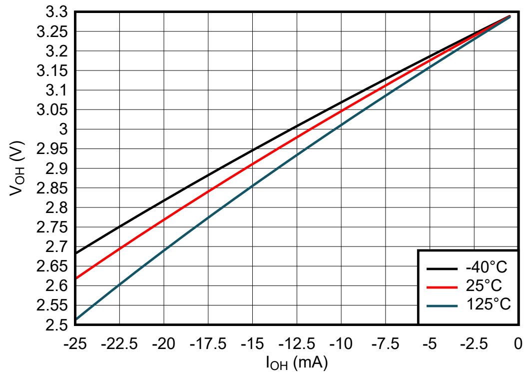


図 5-5. Output Voltage vs Current in HIGH State; 3.3-V Supply

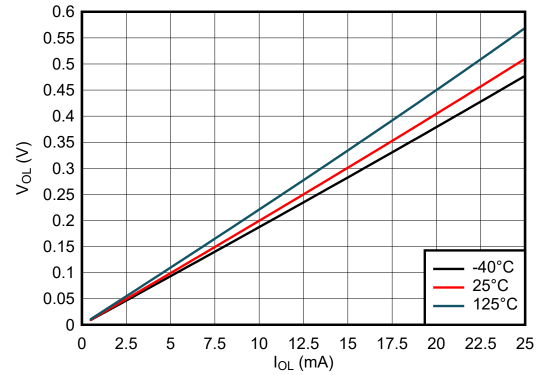


図 5-6. Output Voltage vs Current in LOW State; 3.3-V Supply

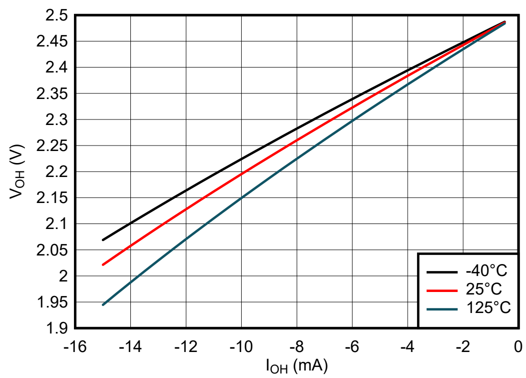


図 5-7. Output Voltage vs Current in HIGH State; 2.5-V Supply

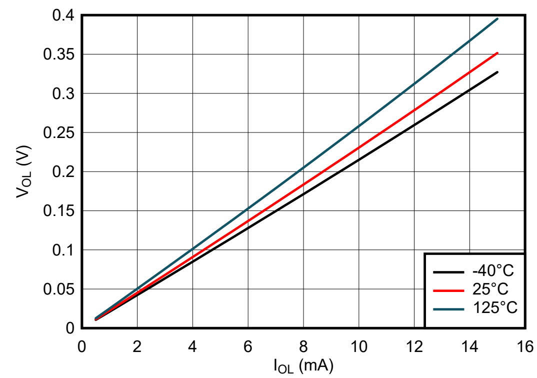


図 5-8. Output Voltage vs Current in LOW State; 2.5-V Supply

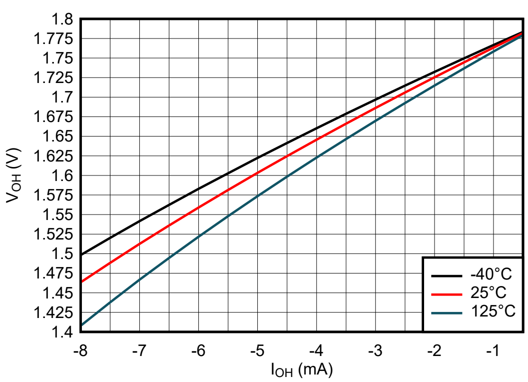


図 5-9. Output Voltage vs Current in HIGH State; 1.8-V Supply

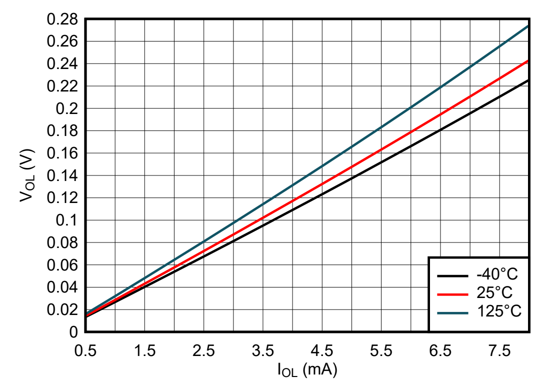


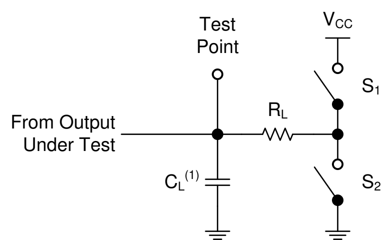
図 5-10. Output Voltage vs Current in LOW State; 1.8-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

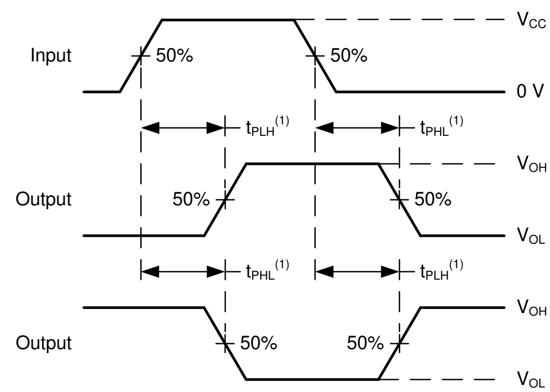
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.3V	> 2.5V



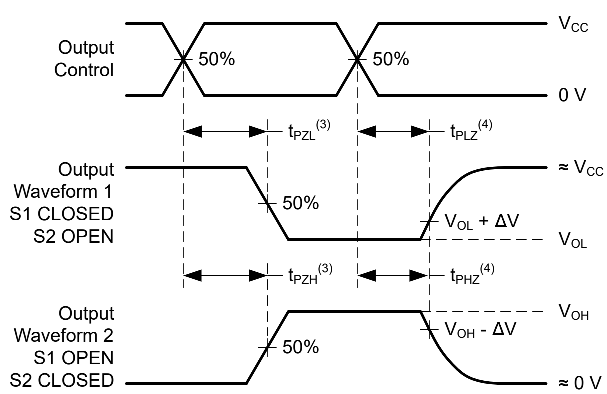
(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

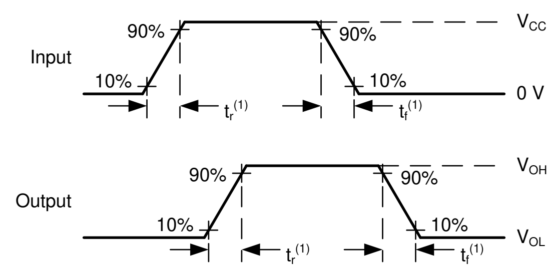
図 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

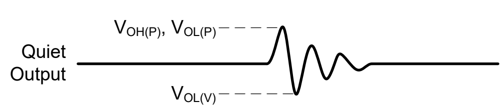
(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

図 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

図 6-4. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

図 6-5. Voltage Waveforms, Noise

7 Detailed Description

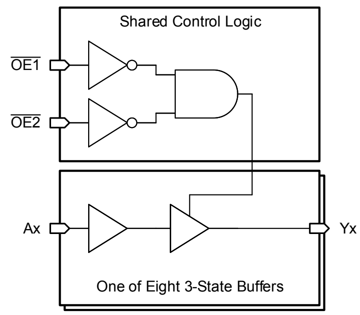
7.1 Overview

The SN74LV8T541-Q1 contains eight buffers with 3-state outputs. The active low output enable pins ($\overline{OE1}$ and $\overline{OE2}$) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.

7.2 Functional Block Diagram



8 Feature Description

8.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.2 LVxT Enhanced Input Voltage

The SN74LV8T541-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 図 8-1 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

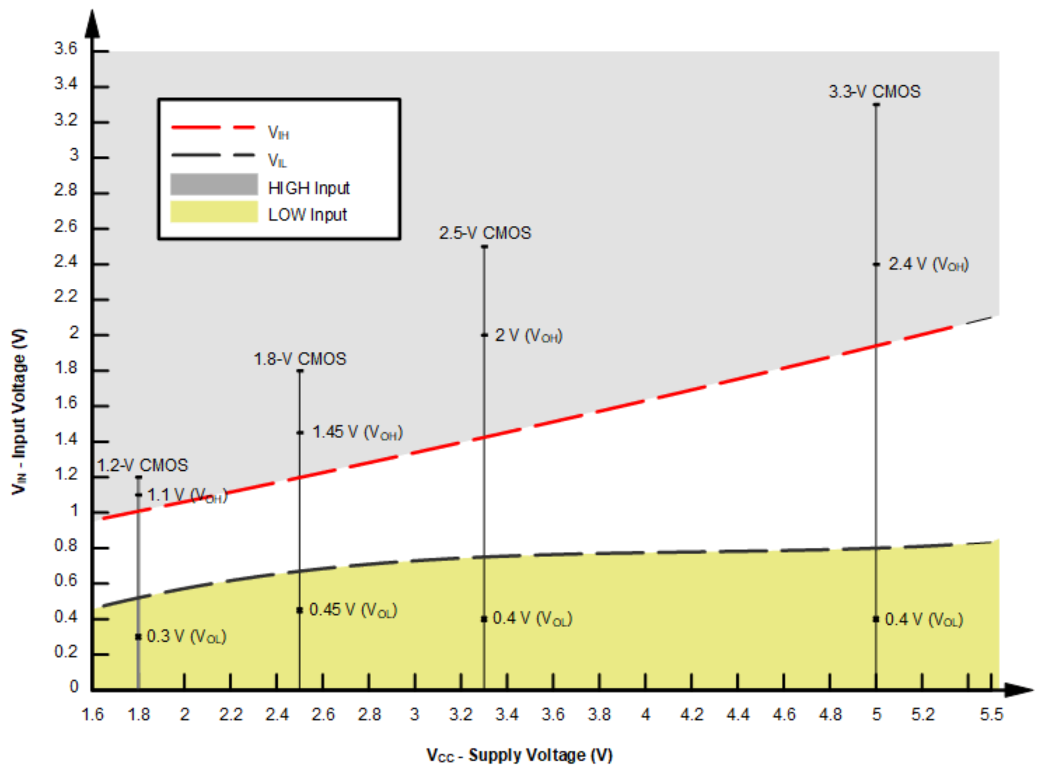


図 8-1. LVxT Input Voltage Levels

8.3 Clamp Diode Structure

As 図 8-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

> 注意
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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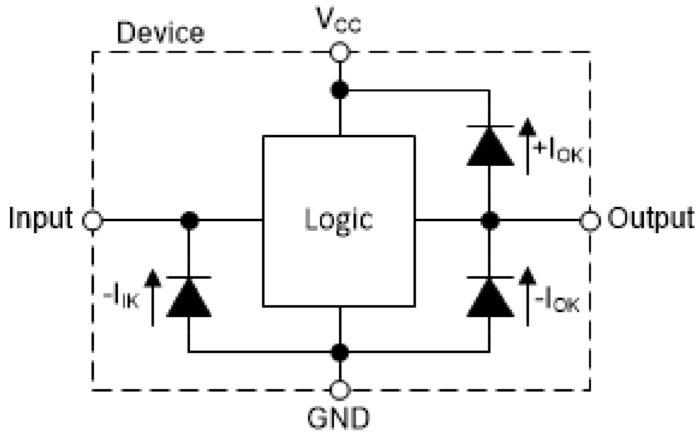

図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

9 Device Functional Modes

表 9-1 lists the functional modes of the SN74LV8T541-Q1.

表 9-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

(1) L = input low, H = input high, X = don't care
(2) L = output low, H = output high, Z = high impedance

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The SN74LV8T541-Q1 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

10.2 Typical Application

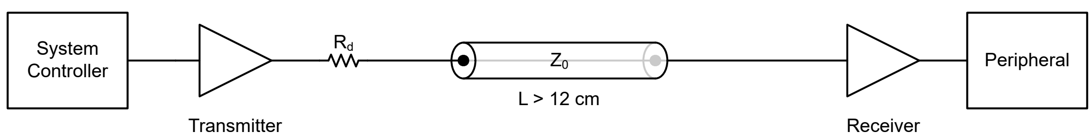

図 10-1. Typical Application Block Diagram

10.2.1 Design Requirements

10.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV8T541-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T541-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T541-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T541-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

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> 注意
>
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

10.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LV8T541-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10kΩ resistor value is often used due to these factors.

The SN74LV8T541-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

10.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

10.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T541-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

10.2.3 Application Curves

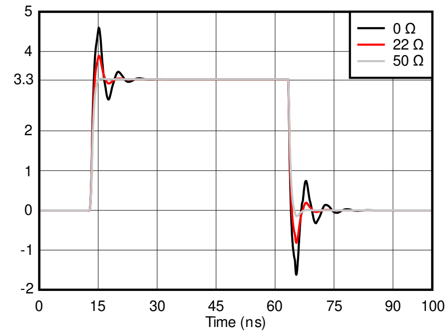

図 10-2. Simulated Signal Integrity at the Receiver with Different Damping Resistor (R_d) Values

10.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. As shown in the following layout example, install the bypass capacitor as close to the power terminal as possible for best results.

10.4 Layout

10.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10.4.2 Layout Example

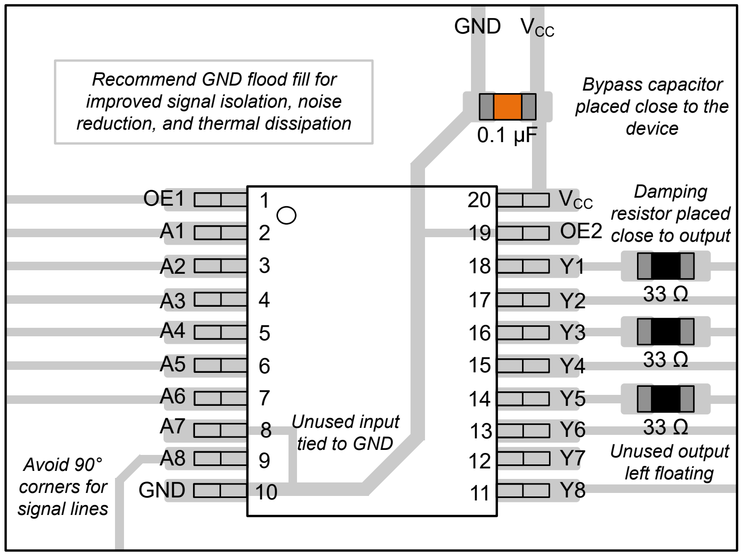

図 10-3. Example Layout for the SN74LV8T541-Q1 in TSSOP

ADVANCE INFORMATION

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

11.2 ドキュメントの更新通知を受け取る方法

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

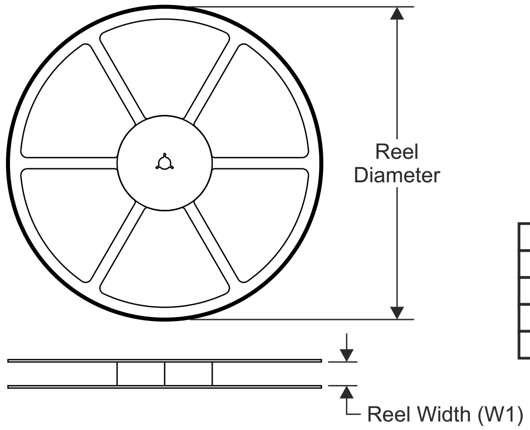
DATE	REVISION	NOTES
March 2024	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

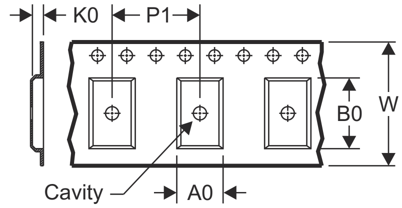
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

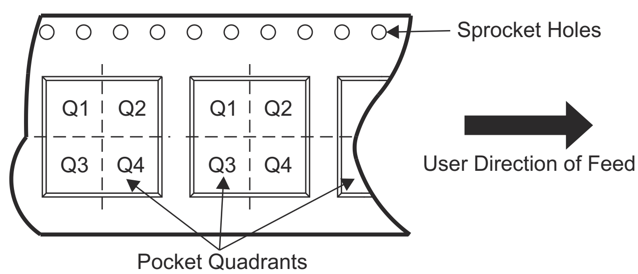


TAPE DIMENSIONS



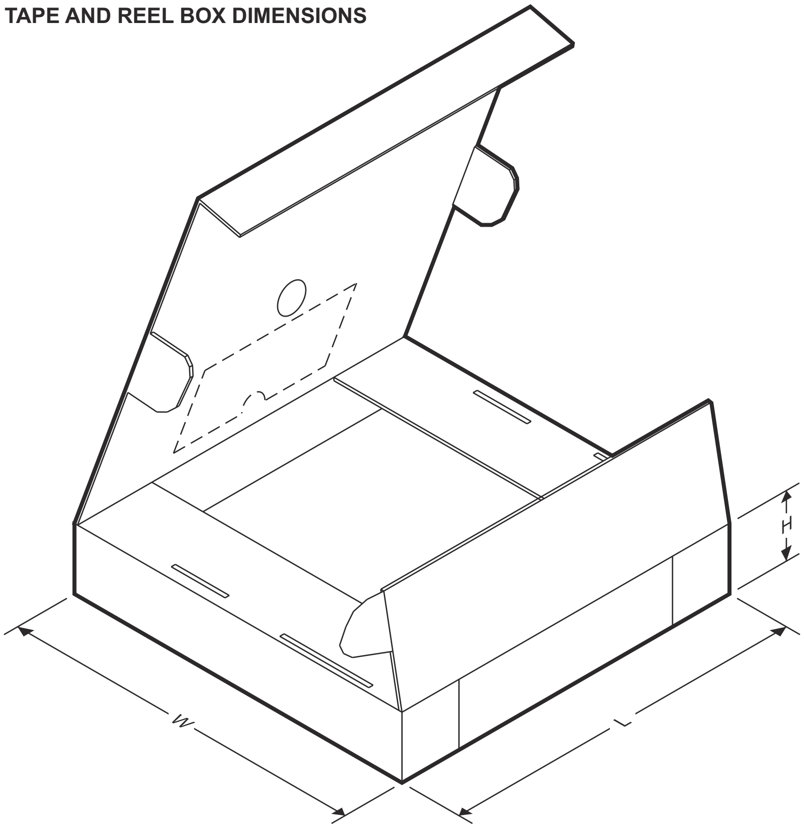
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P1I8T541QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.00	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P1I8T541QPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

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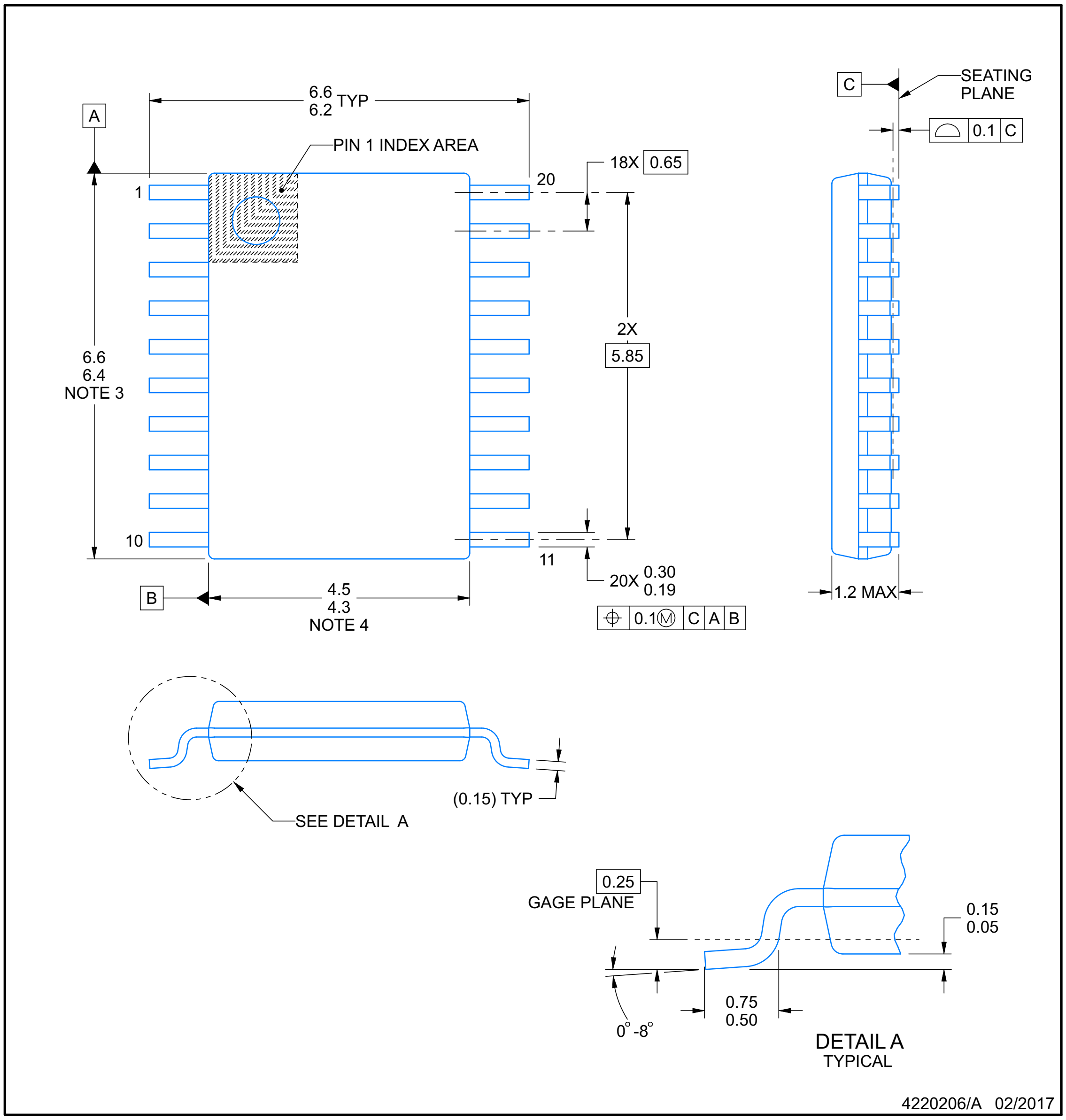
13.2 Mechanical Data

PACKAGE OUTLINE

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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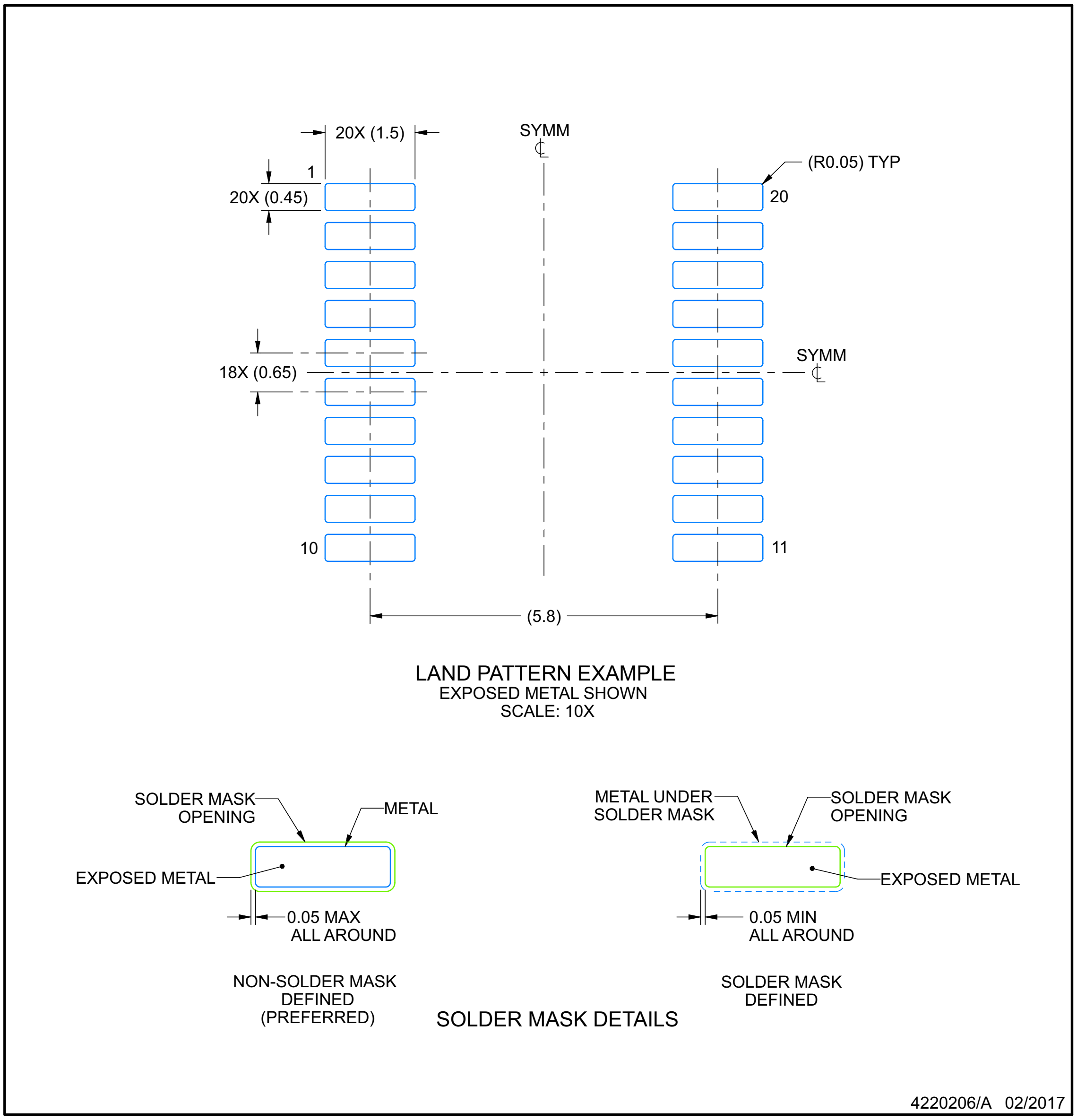
EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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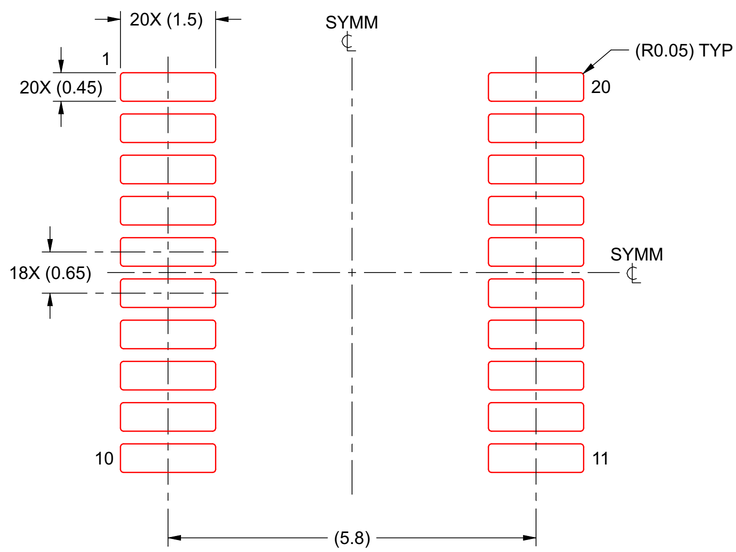
EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74LV8T541QPWRQ1	Active	Preproduction	TSSOP (PW) | 20	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74LV8T541QPWRQ1.A	Active	Preproduction	TSSOP (PW) | 20	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV8T541-Q1 :

- Enhanced Product : SN74LV8T541-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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