





参考資料





SN74LV6T14-Q1 JAJSQO1 - JUNE 2023 - REVISED JUNE 2023

SN74LV6T14-Q1 車載用へキサ・シュミット・トリガ・インバータ、統合変換 機能付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - デバイス温度グレード 1:-40℃~+125℃
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- ウェッタブル・フランク QFN (WBQA) パッケージで供 給されます
- 幅広い動作範囲:1.8V~5.5V
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」 を参照):
 - 昇圧変換:
 - 1.2V から 1.8V
 - 1.5V から 2.5V
 - 1.8V から 3.3V
 - 3.3V から 5.0V
 - 降圧変換:
 - 5.0V、3.3V、2.5V から 1.8V
 - 5.0V、3.3V から 2.5V
 - 5.0V から 3.3V
- 5.5V 許容入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の V_{CC} で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- 反転クロック入力の同期
- スイッチのデバウンス
- デジタル信号の反転

3 概要

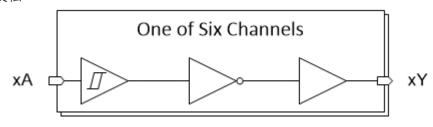
SN74LV6T14-Q1 デバイスは、シュミット・トリガ入力採用 の6つの独立したインバータを内蔵しています。各ゲート はブール関数 Y = A を正論理で実行します。出力レベル は電源電圧 (V_{CC}) を基準としており、1.8V、2.5V、3.3V、 5VのCMOSレベルをサポートしています。

入力は低スレッショルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例:1.2V 入力から 1.8V 出力、 1.8V 入力から 3.3V 出力) をサポートします。 また、5V 許 容の入力ピンにより、降圧変換 (例:3.3V から 2.5V 出力) が可能です。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ・サイズ (2)	本体サイズ (公称)(3)
SN74LV6T14-Q1	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
3N/4EV0114-Q1	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの 末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合は ピンも含まれます。
- 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



概略論理図 (正論理)



Table of Contents

1 特長	1	8.3 Feature Description	<mark>1</mark> 1
2 アプリケーション		8.4 Device Functional Modes	14
3 概要		9 Application and Implementation	15
4 Revision History		9.1 Application Information	15
5 Pin Configuration and Functions		9.2 Typical Application	15
6 Specifications		10 Power Supply Recommendations	17
6.1 Absolute Maximum Ratings		11 Layout	17
6.2 ESD Ratings		11.1 Layout Guidelines	17
6.3 Recommended Operating Conditions		11.2 Layout Example	18
6.4 Thermal Information		12 Device and Documentation Support	19
6.5 Electrical Characteristics	6	12.1 Documentation Support	19
6.6 Switching Characteristics		12.2ドキュメントの更新通知を受け取る方法	19
6.7 Noise Characteristics		12.3 サポート・リソース	19
6.8 Typical Characteristics		12.4 Trademarks	19
7 Parameter Measurement Information		12.5 静電気放電に関する注意事項	19
8 Detailed Description	11	12.6 用語集	19
8.1 Overview		13 Mechanical, Packaging, and Orderable	
8.2 Functional Block Diagram		Information	19

4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial Release



5 Pin Configuration and Functions

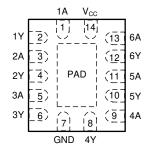


図 5-1. SN74LV6T14-Q1 BQA Package, 14-Pin WQFN (Top View)

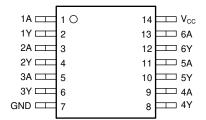


図 5-2. SN74LV6T14-Q1 PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

	PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	BQA	PW	ITPE\"	DESCRIPTION
1A			I	Channel 1, Input A
1Y			0	Channel 1, Ouput Y
2A			I	Channel 2, Input A
2Y			0	Channel 2, Ouput Y
3A _{CC}			I	Channel 3, Input A
3Y			0	Channel 3, Ouput Y
GND			G	Ground
4Y			0	Channel 4, Output Y
4A			I	Channel 4, Input A
5Y			0	Channel 5, Output Y
5A			I	Channel 5, Input A
6Y			0	Channel 6, Output Y
6A			I	Channel 6, Input A
V _{CC}			Р	Positive Supply
Thermal Pa	nd ⁽²⁾	1		The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

⁽¹⁾ I = input, O = output, I/O = input or output, G = ground, P = power.

⁽²⁾ BQA package only.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any outp	out in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
Vo	Output voltage range ⁽²⁾	Output voltage range ⁽²⁾		V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < -0.5 V		-20	mA
I _{OK}	Output clamp current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC +} 0.5 \text{ V}$		±20	mA
Io	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous output current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature	Storage temperature		150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
	Electrostatic	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	
V _(ESD)	discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.6	5.5	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V to 2 V	1.1		
\	High level input voltage	V _{CC} = 2.25 V to 2.75 V	1.28		V
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	1.45		V
		V _{CC} = 4.5 V to 5.5 V	2		
		V _{CC} = 1.65 V to 2 V		0.5	
\		V _{CC} = 2.25 V to 2.75 V		0.65	V
V_{IL}	Low-Level input voltage	V _{CC} = 3 V to 3.6 V		0.75	V
		V _{CC} = 4.5 V to 5.5 V		0.85	
		V _{CC} = 1.6 V to 2 V		±3	
lo	Output current	V _{CC} = 2.25 V to 2.75 V		±7	mA
		V _{CC} = 3.3 V to 5.0 V		±15	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 1.6 V to 5.0 V		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

6.4 Thermal Information

		SN74L\	SN74LV6T14-Q1			
	THERMAL METRIC ⁽¹⁾	BQA (WQFN)	PW (TSSOP)	UNIT		
		14 PINS	14 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	88.3	151.0	°C/W		
R ₀ JC(top)	Junction-to-case (top) thermal resistance	90.9	80.0	°C/W		
R _{θJB}	Junction-to-board thermal resistance	56.8	94.2	°C/W		
Ψ_{JT}	Junction-to-top characterization parameter	9.9	28.0	°C/W		
Y _{JB}	Junction-to-board characterization parameter	56.7	93.6	°C/W		
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	33.4	N/A	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	T _A =	: 25°C	-40°C t	UNIT		
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP MAX	MIN	TYP MAX	UNII	
		1.65 V to 2 V	0.6	1.2	0.5	1.27		
\/	Positive-going input threshold	2.25 V to 2.75 V	0.73	1.39	0.64	1.44	V	
V_{T+}	voltage	3 V to 3.6 V	0.88	1.59	0.80	1.63	V	
		4.5 V to 5.5 V	1.15	2.03	1.1	2.07		
		1.65 V to 2 V	0.225	0.685	0.185	0.755		
	Negative-going input threshold	2.25 V to 2.75 V	0.295	0.775	0.265	0.805	V	
V _{T-}	voltage	3 V to 3.6 V	0.385	0.875	0.345	0.895	V	
		4.5 V to 5.5 V	0.535	1.075	0.495	1.085		
		1.65 V to 2 V	0.35	0.68	0.28	0.8		
A) /	Libertana dia O.C.	2.25 V to 2.75 V	0.4	0.77	0.33	0.87	,,	
ΔV_T	Hysteresis (V _{T+} - V _{T-})	3 V to 3.6 V	0.44	0.88	0.38	0.91	V	
		4.5 V to 5.5 V	0.53	1.2	0.51	1.4		
	I _{OH} = -50 uA	1.65 V to 5.5 V	V _{CC} -0.1		V _{CC} -0.1			
	I _{OH} = -2 mA	1.65 V to 2 V	1.28	1.7 (1)	1.21			
	I _{OH} = -3 mA	2.25 V to 2.75 V	2	2.4 ⁽¹⁾	1.93			
V_{OH}	I _{OH} = -5.5 mA	3 V to 3.6 V	2.6	3.08	2.49		V	
	I _{OH} = -8 mA	4.5 V to 5.5 V	4.1	4.65 (1)	3.95			
	I _{OL} = 50 uA	1.65 V to 5.5 V		0.1		0.1		
	I _{OL} = 2 mA	1.65 V to 2 V		0.1(1) 0.2		0.25		
V_{OL}	I _{OL} = 3 mA	2.25 V to 2.75 V		0.1 ⁽¹⁾ 0.15		0.2	V	
	I _{OL} = 5.5 mA	3 V to 3.6 V		0.2 ⁽¹⁾ 0.2		0.25		
	I _{OL} = 8 mA	4.5 V to 5.5 V		0.3(1) 0.3		0.35		
I _I	V _I = 0 V or V _{CC}	0 V to 5.5 V		±0.1		±1	μΑ	
I _{cc}	$V_I = 0 \text{ V or } V_{CC}, I_O = 0; \text{ open on loading}$	1.65 V to 5.5 V		2		20	μΑ	
ΔI _{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V_{CC} , $I_{O} = 0$	5.5 V		1.35		1.5	mA	
	One input at 0.3 V or 1.1 V, other inputs at 0 or V _{CC} , I _O = 0	1.8 V		10		20	μΑ	
Cı	V _I = V _{CC} or GND	5 V		4 10		10	pF	
Co	V _O = V _{CC} or GND	5 V		3			pF	
C _{PD} (2) (3)	No load, F = 1Mhz	5 V		14			pF	

 ⁽¹⁾ Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
 (2) C_{PD} is used to determine the dynamic power consumption, per channel.
 (3) P_D= V_{CC} ²xF_Ix(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage.

6.6 Switching Characteristics

over operating free-air temperature range; (unless otherwise noted). See Parameter Measurement Information

PARAMETER	FROM	TO (OUTPUT)	V	LOAD	T	= 25°	C	-40°C	to 12	5°C	UNIT			
FANAMETER	(INPUT)	10 (0011-01)	V _{CC}	CAPACITANCE	MIN	TYP	MAX	MIN	TYP	MAX	ONI			
			1.8 V	C _L = 15 pF	8.85	14	19.7	7.45	15.5	22.8				
			1.0 V	C _L = 50 pF	10.8	17.1	23.3	9.07	18.4	26.7				
		Y	2.5 V	C _L = 15 pF	6.44	8.9	11	5.42	9.6	13.4				
t	A			C _L = 50 pF	7.94	10.8	13.2	6.59	11.7	16	nS			
t _{PD}			'	'		3.3 V	C _L = 15 pF	5.24	6.9	8.4	4.42	7.5	10.2	113
			3.3 V	C _L = 50 pF	6.58	8.5	10.1	5.41	9.1	12.2				
			5 V	C _L = 15 pF	4.09	5.1	6.2	3.29	5.5	7.7				
			3 V	C _L = 50 pF	5.06	6.4	7.7	4.07	6.9	9.4				

6.7 Noise Characteristics

VCC = 5 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.9	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.8	-0.3		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4	5		V
V _{IH(D)}	High-level dynamic input voltage	2.1			V
V _{IL(D)}	Low-level dynamic input voltage			0.5	V

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

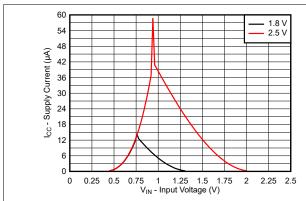


図 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

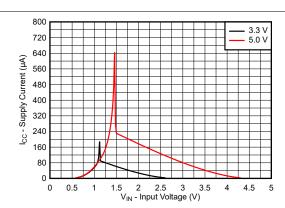
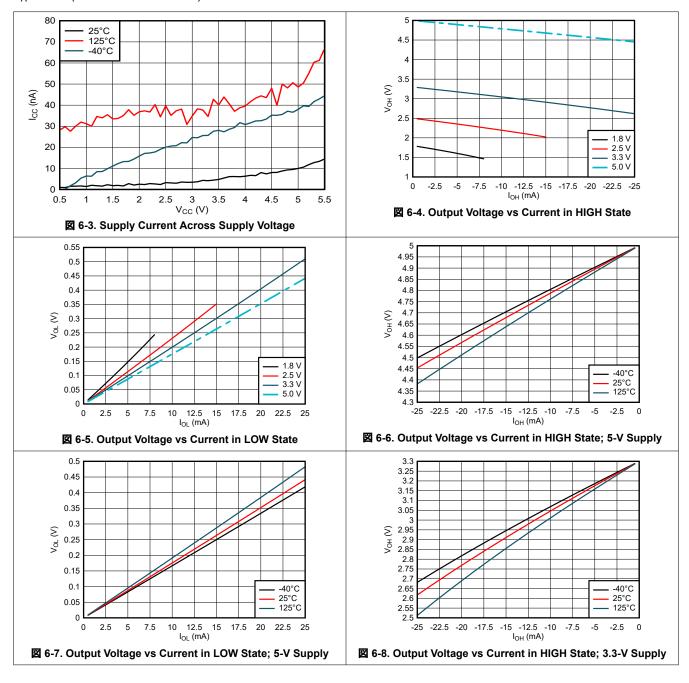


図 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply



6.8 Typical Characteristics (continued)

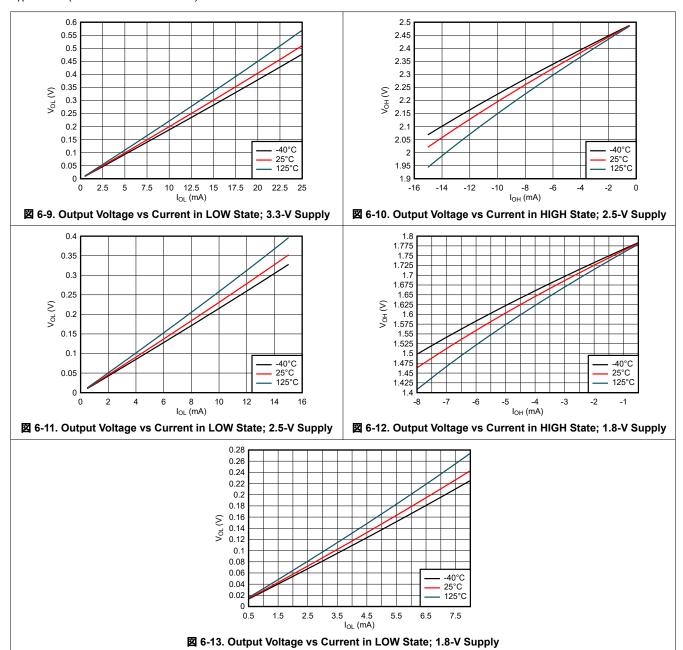
T_A = 25°C (unless otherwise noted)





6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



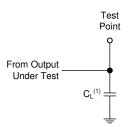


7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω .

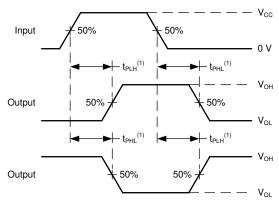
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



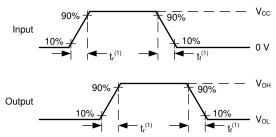
(1) C_L includes probe and test-fixture capacitance.

図 7-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

図 7-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

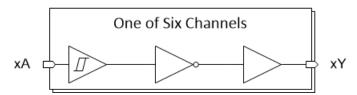
図 7-3. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

The SN74LV6T14-Q1 device contains six independent Inverter with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A}$ in positive logic. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 平衡な CMOS プッシュプル出力

このデバイスには、平衡な CMOS プッシュプル出力が内蔵されています。「平衡な」という用語は、デバイスが同様の電流をシンクおよびソースできることを示します。このデバイスは駆動能力を備えており、軽負荷に高速エッジが生成されるため、リンギングを防ぐために配線と負荷の条件を考慮する必要があります。さらに、このデバイスの出力は、デバイスを損傷することなく維持できる以上に大きな電流を駆動できます。過電流による損傷を防止するため、デバイスの出力電力を制限することが重要です。「絶対最大定格」で定義されている電気的および熱的制限を常に順守してください。

未使用のプッシュプル CMOS 出力は、未接続のままにする必要があります。

8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in \boxtimes 8-1.

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

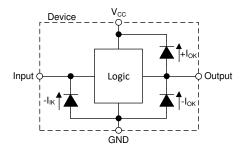


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.3 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much

Copyright © 2023 Texas Instruments Incorporated

Submit Document Feedback

slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

8.3.4 LVxT Enhanced Input Voltage

The SN74LV6T14-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. \boxtimes 8-2 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a $10-k\Omega$ resistor is recommended and will typically meet all requirements.

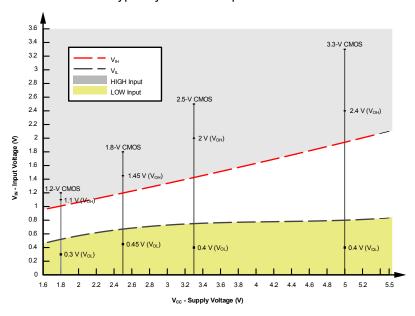


図 8-2. LVxT Input Voltage Levels

8.3.4.1 Down Translation

Signals can be translated down using the SN74LV6T14-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Submit Document Feedback

Copyright © 2023 Texas Instruments Incorporated

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. As shown in \boxtimes 8-2, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in \boxtimes 8-3 for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC}.

Down Translation Combinations are as follows:

- 1.8-V V_{CC} Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V V_{CC} Inputs from 3.3 V and 5.0 V
- 3.3-V V_{CC} Inputs from 5.0 V

8.3.4.2 Up Translation

Input signals can be up translated using the SN74LV6T14-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV6T14-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in \boxtimes 8-3, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} Inputs from 1.2 V
- 2.5-V V_{CC} Inputs from 1.8 V
- 3.3-V V_{CC} Inputs from 1.8 V and 2.5 V
- 5.0-V V_{CC} Inputs from 2.5 V and 3.3 V

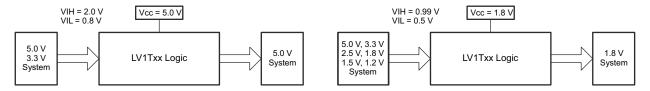


図 8-3. LVxT Up and Down Translation Example

8.3.5 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.



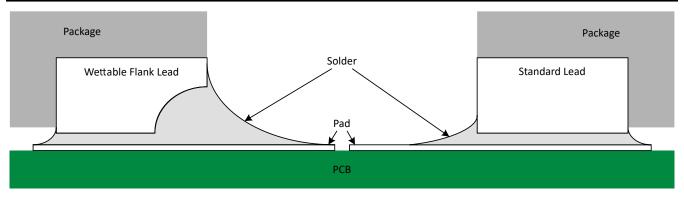


図 8-4. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 🗵 8-4, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV6T14-Q1.

表 8-1. Function Table

INPUTS ⁽¹⁾	ОИТРИТ
Α	Y
Н	L
L	Н

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance



9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV6T14-Q1 can be used to add an additional stage to a counter with an external flip-flop. Because counters use a negative edge trigger, the flip-flop's clock input must be inverted to provide this function. Having Schmitt-trigger inputs is important in this application to eliminate any noise issues that could impact the counting function which could lead to incorrect frequency division. This function only requires one of the six available inverters in the SN74LV6T14-Q1 device, so the remaining channels can be used for other applications needing an inverted signal or improved signal integrity. Unused inputs must be terminated at V_{CC} or GND. Unused outputs can be left floating.

9.2 Typical Application

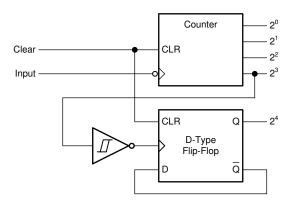


図 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV6T14-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV6T14-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV6T14-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.



The SN74LV6T14-Q1 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the CMOS Power Consumption and Cpd Calculation application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

注意

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV6T14-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV6T14-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Product Folder Links: SN74LV6T14-Q1

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV6T14-Q1 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.3 Application Curves

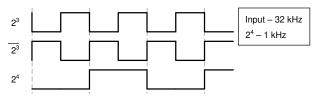


図 9-2. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.



11.2 Layout Example

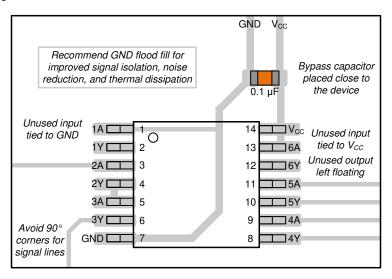


図 11-1. Example Layout for the SN74LV6T14-Q1



12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LV6T14-Q1

Copyright © 2023 Texas Instruments Incorporated

Submit Document Feedback

www.ti.com 9-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LV6T14QPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT14Q
SN74LV6T14QPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT14Q
SN74LV6T14QWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT14Q
SN74LV6T14QWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT14Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents Tl's knowledge and belief as of the date that it is provided. Tl bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. Tl has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. Tl and Tl suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV6T14-Q1:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

• Catalog : SN74LV6T14

● Enhanced Product : SN74LV6T14-EP

NOTE: Qualified Version Definitions:

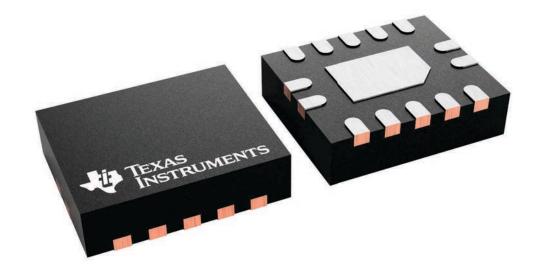
Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

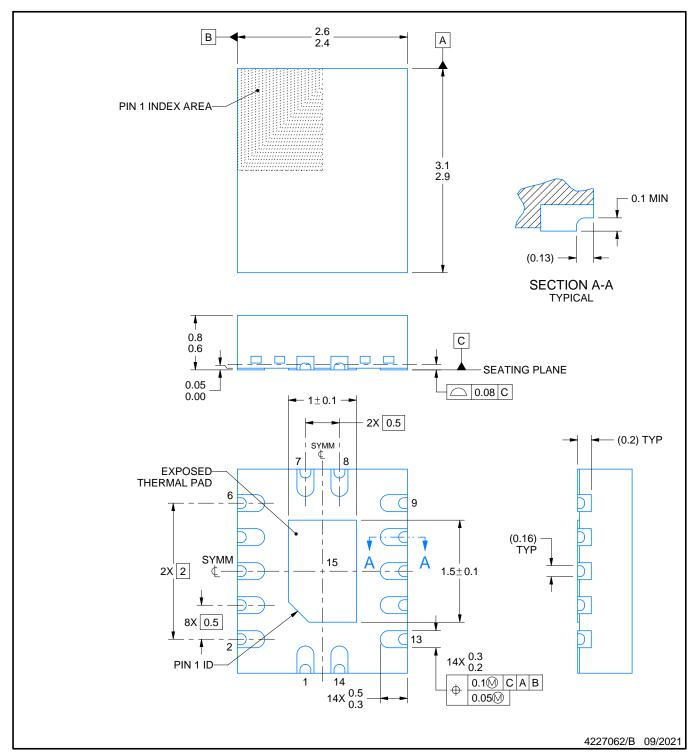
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD

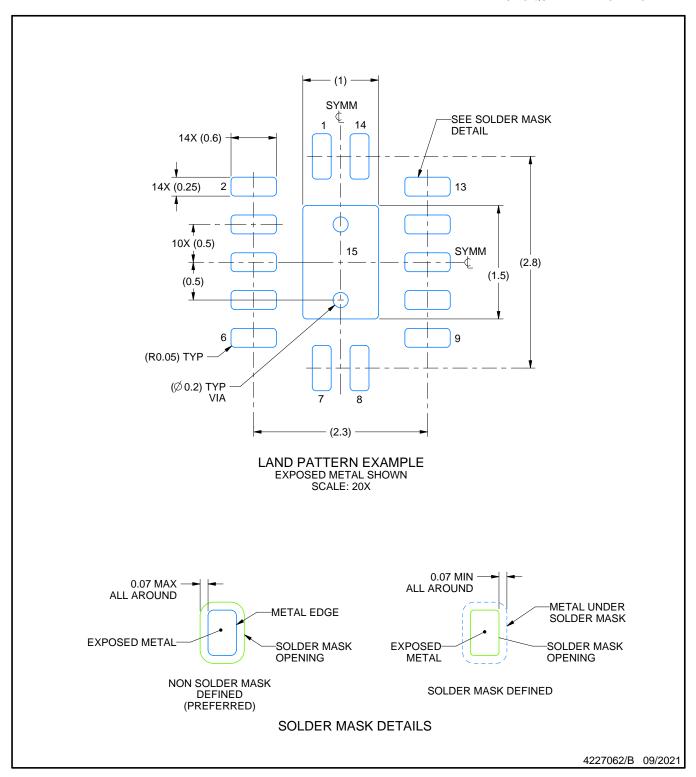


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

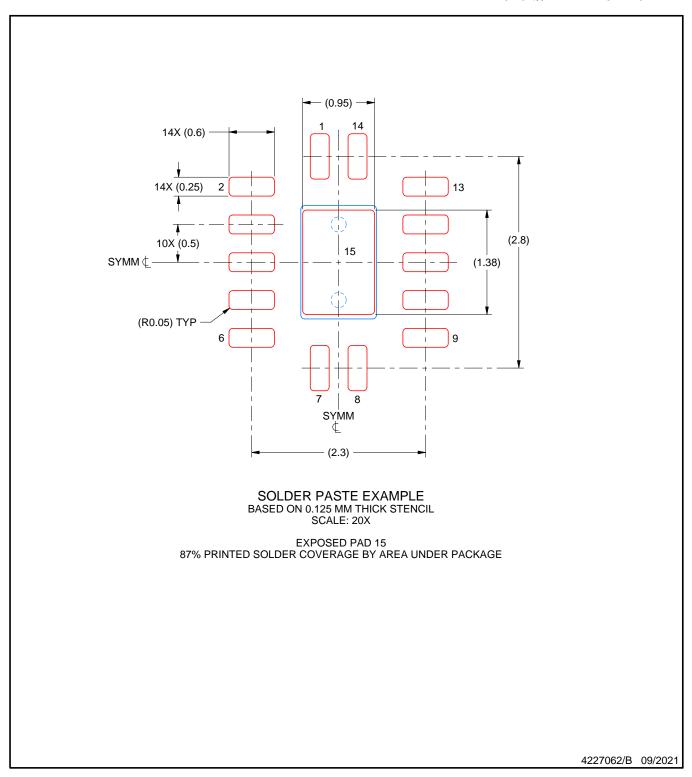


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



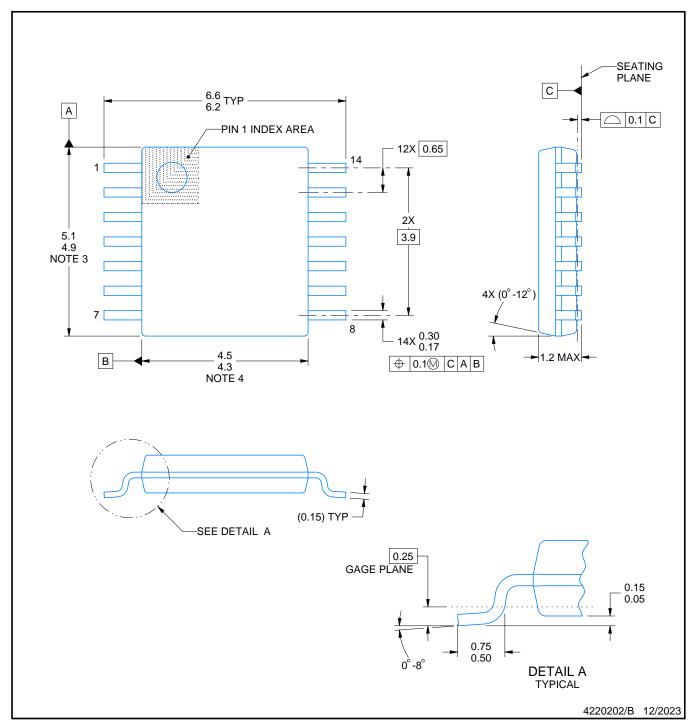
NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

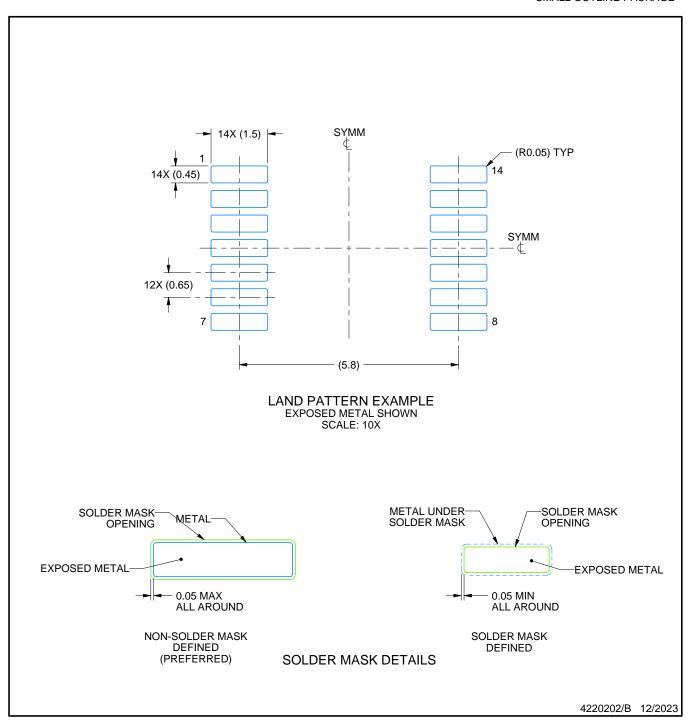
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



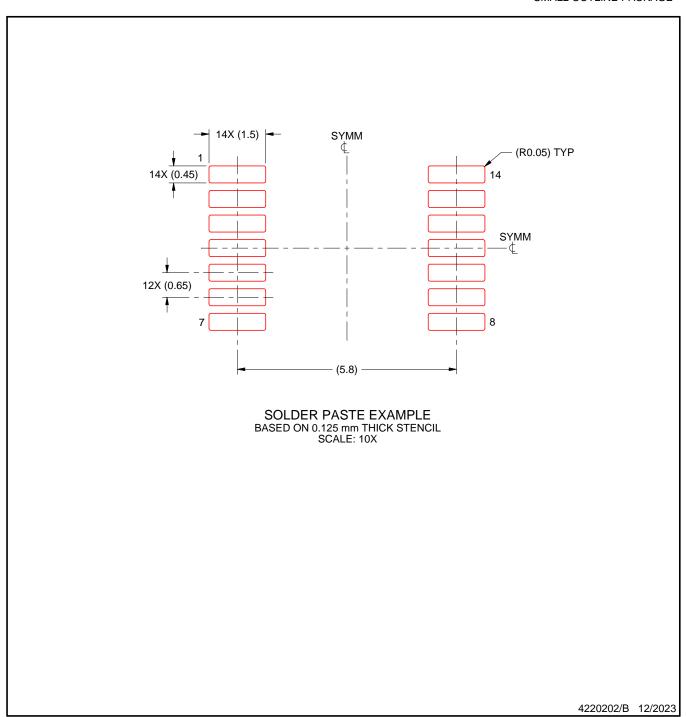
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TIの製品は、TIの販売条件、TIの総合的な品質ガイドライン、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TIはそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日: 2025 年 10 月