# SN74LV6T14 ヘキサ・シュミット・トリガ・インバータ、内蔵変換機能付き

## 1 特長

- 幅広い動作範囲：1.8V～5.5V
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」を参照)：
  - 昇圧変換：
    - 1.2V から 1.8V
    - 1.5V から 2.5V
    - 1.8V から 3.3V
    - 3.3V から 5.0V
  - 降圧変換：
    - 5.0V、3.3V、2.5V から 1.8V
    - 5.0V、3.3V から 2.5V
    - 5.0V から 3.3V
- 5.5V 許容入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の $V_{CC}$ で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- 反転クロック入力の同期
- スイッチのデバウンス
- デジタル信号の反転

## 3 概要

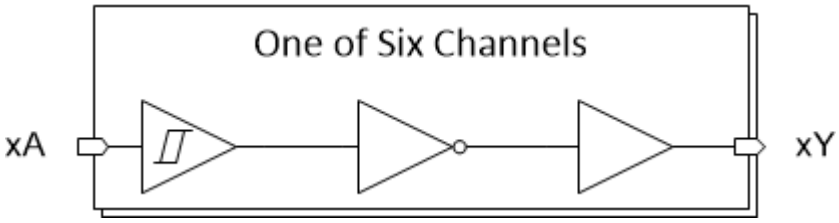
SN74LV6T14 デバイスは、シュミット・トリガ入力採用の 6 つの独立したインバータを内蔵しています。各ゲートはブール関数 $Y = \overline{A}$ を正論理で実行します。出力レベルは電源電圧 ($V_{CC}$) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

入力は低スレッショルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例：1.2V 入力から 1.8V 出力、1.8V 入力から 3.3V 出力) をサポートします。また、5V 許容の入力ピンにより、降圧変換 (例：3.3V から 2.5V 出力) が可能です。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ・サイズ (2) | 本体サイズ (公称)(3) |
|---|---|---|---|
| SN74LV6T14 | BQA (WQFN、14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | PW (TSSOP、14) | 5mm × 6.4mm | 5mm × 4.4mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。




**概略論理図 (正論理)**

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## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| June 2023 | * | Initial Release |

# 5 Pin Configuration and Functions

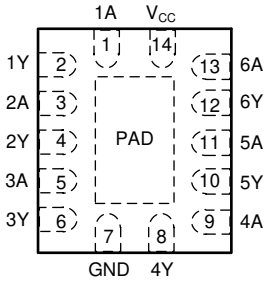



**図 5-1. SN74LV6T14 BQA Package, 14-Pin WQFN (Top View)**

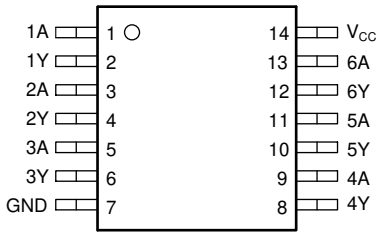



**図 5-2. SN74LV6T14 PW Package, 14-Pin TSSOP (Top View)**

**表 5-1. Pin Functions**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | BQA | PW | | |
| 1A | | | I | Channel 1, Input A |
| 1Y | | | O | Channel 1, Ouput Y |
| 2A | | | I | Channel 2, Input A |
| 2Y | | | O | Channel 2, Ouput Y |
| $3A_{CC}$ | | | I | Channel 3, Input A |
| 3Y | | | O | Channel 3, Ouput Y |
| GND | | | G | Ground |
| 4Y | | | O | Channel 4, Output Y |
| 4A | | | I | Channel 4, Input A |
| 5Y | | | O | Channel 5, Output Y |
| 5A | | | I | Channel 5, Input A |
| 6Y | | | O | Channel 6, Output Y |
| 6A | | | I | Channel 6, Input A |
| $V_{CC}$ | | | P | Positive Supply |
| Thermal Pad[2] | | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) I = input, O = output, I/O = input or output, G = ground, P = power.
(2) BQA package only.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5 V | | -20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.6 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 2 V | 1.1 | | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | 1.28 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 1.45 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65 V to 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | 0.65 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.75 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.85 | |
| $I_O$ | Output current | $V_{CC}$ = 1.6 V to 2 V | | ±3 | mA |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | ±7 | |
| | | $V_{CC}$ = 3.3 V to 5.0 V | | ±15 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.6 V to 5.0 V | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LV6T14 | | UNIT |
|---|---|---|---|---|
| | | BQA (WQFN) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 88.3 | 151.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 90.9 | 80.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.8 | 94.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 9.9 | 28.0 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 56.7 | 93.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 33.4 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ | Positive-going input threshold voltage | 1.65 V to 2 V | 0.6 | | 1.2 | 0.5 | | 1.27 | V |
| | | 2.25 V to 2.75 V | 0.73 | | 1.39 | 0.64 | | 1.44 | |
| | | 3 V to 3.6 V | 0.88 | | 1.59 | 0.80 | | 1.63 | |
| | | 4.5 V to 5.5 V | 1.15 | | 2.03 | 1.1 | | 2.07 | |
| $V_{T-}$ | Negative-going input threshold voltage | 1.65 V to 2 V | 0.225 | | 0.685 | 0.185 | | 0.755 | V |
| | | 2.25 V to 2.75 V | 0.295 | | 0.775 | 0.265 | | 0.805 | |
| | | 3 V to 3.6 V | 0.385 | | 0.875 | 0.345 | | 0.895 | |
| | | 4.5 V to 5.5 V | 0.535 | | 1.075 | 0.495 | | 1.085 | |
| $\Delta V_T$ | Hysteresis ($V_{T+} - V_{T-}$) | 1.65 V to 2 V | 0.35 | | 0.68 | 0.28 | | 0.8 | V |
| | | 2.25 V to 2.75 V | 0.4 | | 0.77 | 0.33 | | 0.87 | |
| | | 3 V to 3.6 V | 0.44 | | 0.88 | 0.38 | | 0.91 | |
| | | 4.5 V to 5.5 V | 0.53 | | 1.2 | 0.51 | | 1.4 | |
| $V_{OH}$ | $I_{OH}$ = -50 uA | 1.65 V to 5.5 V | $V_{CC}$-0.1 | | | $V_{CC}$-0.1 | | | V |
| | $I_{OH}$ = -2 mA | 1.65 V to 2 V | 1.28 | 1.7 (1) | | 1.21 | | | |
| | $I_{OH}$ = -3 mA | 2.25 V to 2.75 V | 2 | 2.4(1) | | 1.93 | | | |
| | $I_{OH}$ = -5.5 mA | 3 V to 3.6 V | 2.6 | 3.08 (1) | | 2.49 | | | |
| | $I_{OH}$ = -8 mA | 4.5 V to 5.5 V | 4.1 | 4.65 (1) | | 3.95 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 uA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 1.65 V to 2 V | | 0.1(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 3 mA | 2.25 V to 2.75 V | | 0.1(1) | 0.15 | | | 0.2 | |
| | $I_{OL}$ = 5.5 mA | 3 V to 3.6 V | | 0.2(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 8 mA | 4.5 V to 5.5 V | | 0.3(1) | 0.3 | | | 0.35 | |
| $I_I$ | $V_I$ = 0 V or $V_{CC}$ | 0 V to 5.5 V | | | ±0.1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = 0 V or $V_{CC}$, $I_O$ = 0; open on loading | 1.65 V to 5.5 V | | | 2 | | | 20 | µA |
| $\Delta I_{CC}$ | One input at 0.3 V or 3.4 V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 5.5 V | | | 1.35 | | | 1.5 | mA |
| | One input at 0.3 V or 1.1 V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 1.8 V | | | 10 | | | 20 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | 10 | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 3 | | | | | pF |
| $C_{PD}$ (2) (3) | No load, F = 1Mhz | 5 V | | 14 | | | | | pF |

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
(2) $C_{PD}$ is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}{}^2 x F_I x (C_{PD} + C_L)$ where $F_I$= input frequency, $C_L$= output load capacitance, $V_{CC}$= supply voltage.

## 6.6 Switching Characteristics

over operating free-air temperature range; (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PD}$ | A | Y | 1.8 V | $C_L$ = 15 pF | 8.85 | 14 | 19.7 | 7.45 | 15.5 | 22.8 | nS |
| | | | | $C_L$ = 50 pF | 10.8 | 17.1 | 23.3 | 9.07 | 18.4 | 26.7 | |
| | | | 2.5 V | $C_L$ = 15 pF | 6.44 | 8.9 | 11 | 5.42 | 9.6 | 13.4 | |
| | | | | $C_L$ = 50 pF | 7.94 | 10.8 | 13.2 | 6.59 | 11.7 | 16 | |
| | | | 3.3 V | $C_L$ = 15 pF | 5.24 | 6.9 | 8.4 | 4.42 | 7.5 | 10.2 | |
| | | | | $C_L$ = 50 pF | 6.58 | 8.5 | 10.1 | 5.41 | 9.1 | 12.2 | |
| | | | 5 V | $C_L$ = 15 pF | 4.09 | 5.1 | 6.2 | 3.29 | 5.5 | 7.7 | |
| | | | | $C_L$ = 50 pF | 5.06 | 6.4 | 7.7 | 4.07 | 6.9 | 9.4 | |

## 6.7 Noise Characteristics

VCC = 5 V, CL = 50 pF, TA = 25°C

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | -0.8 | -0.3 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.4 | 5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.1 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.5 | V |

## 6.8 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

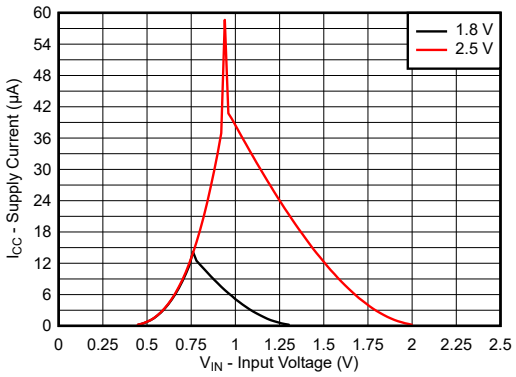



**図 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply**

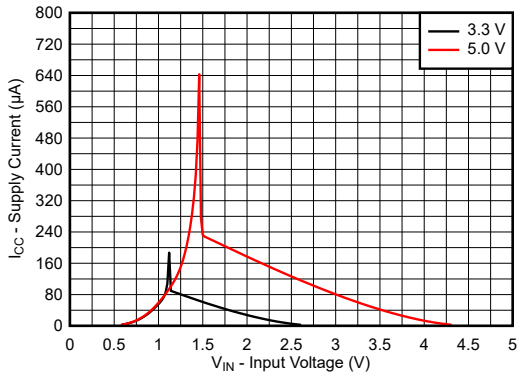



**図 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply**

## 6.8 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

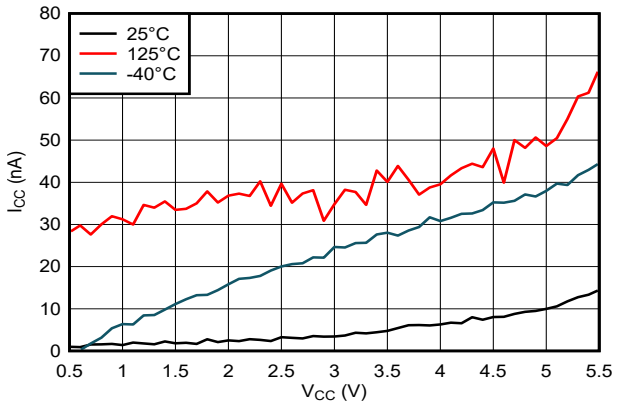



図 6-3. Supply Current Across Supply Voltage

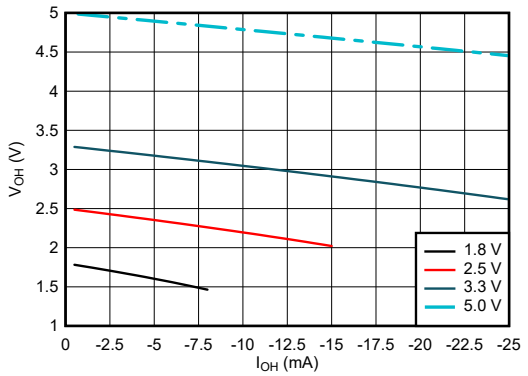



図 6-4. Output Voltage vs Current in HIGH State

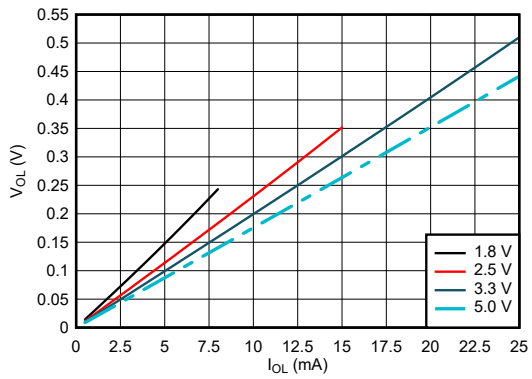



図 6-5. Output Voltage vs Current in LOW State

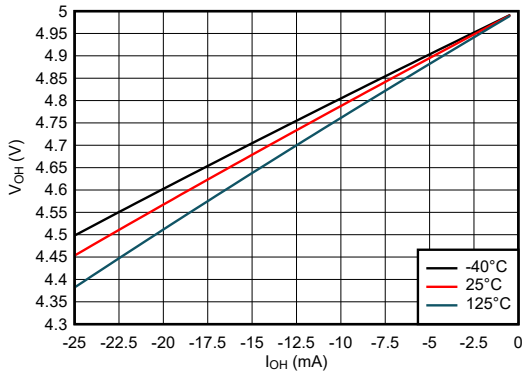



図 6-6. Output Voltage vs Current in HIGH State; 5-V Supply

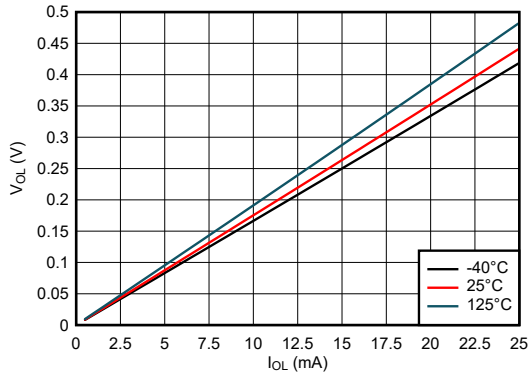



図 6-7. Output Voltage vs Current in LOW State; 5-V Supply

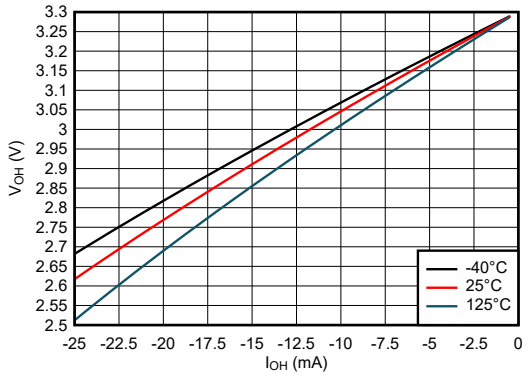



図 6-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

## 6.8 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

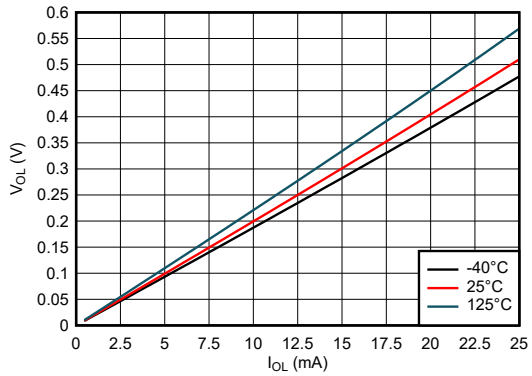



**図 6-9. Output Voltage vs Current in LOW State; 3.3-V Supply**

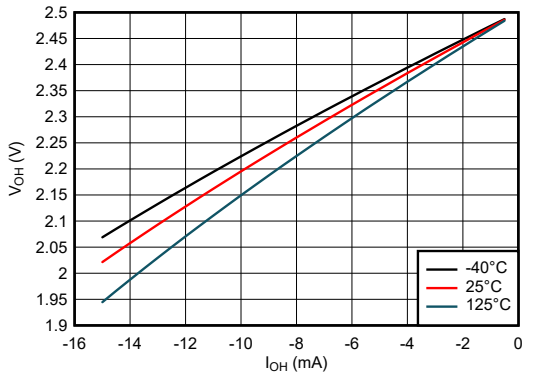



**図 6-10. Output Voltage vs Current in HIGH State; 2.5-V Supply**

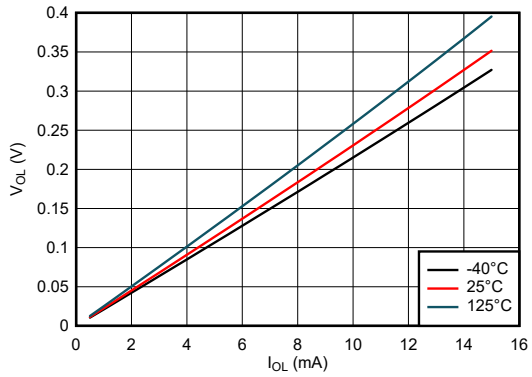



**図 6-11. Output Voltage vs Current in LOW State; 2.5-V Supply**

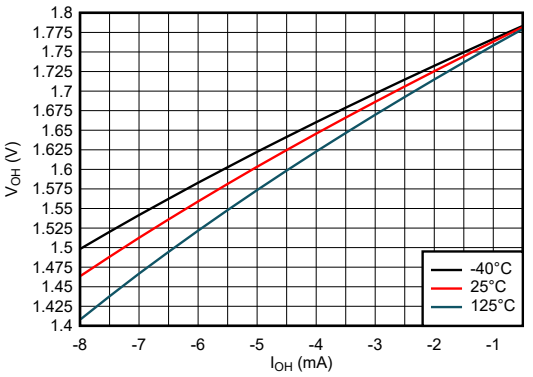



**図 6-12. Output Voltage vs Current in HIGH State; 1.8-V Supply**

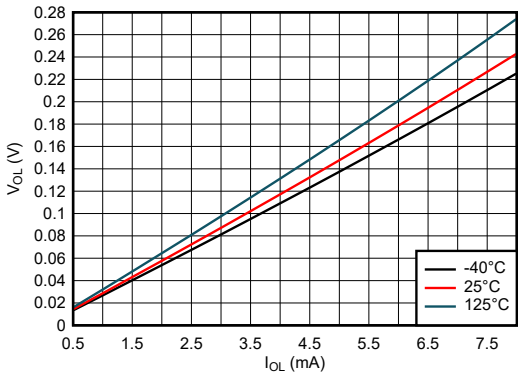


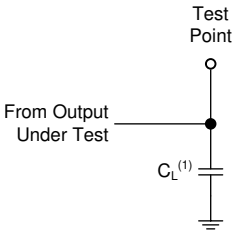

**図 6-13. Output Voltage vs Current in LOW State; 1.8-V Supply**

# 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω.

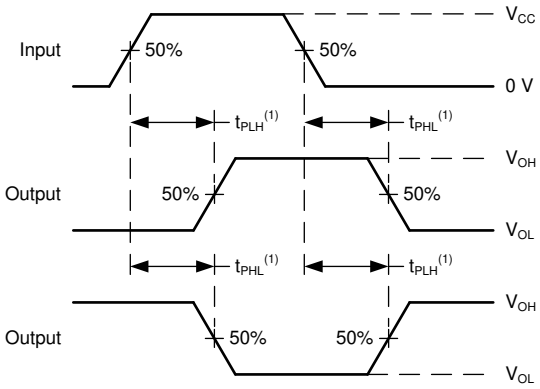
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



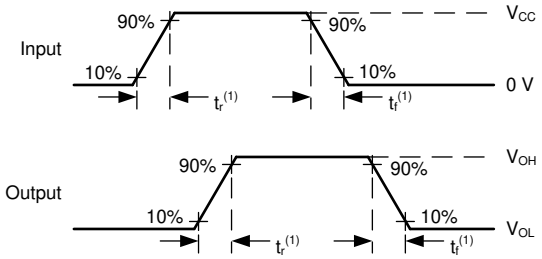

(1) $C_L$ includes probe and test-fixture capacitance.

**図 7-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 7-2. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

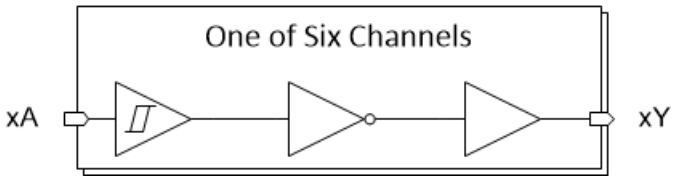
**図 7-3. Voltage Waveforms, Input and Output Transition Times**

# 8 Detailed Description

## 8.1 Overview

The SN74LV6T14 device contains six independent Inverter with Schmitt-trigger inputs. Each gate performs the Boolean function Y = $\overline{A}$ in positive logic. The output level is referenced to the supply voltage ($V_{CC}$) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 平衡な CMOS プッシュプル出力

このデバイスには、平衡な CMOS プッシュプル出力が内蔵されています。「平衡な」という用語 は、デバイスが同様の電流をシンクおよびソースできることを示します。 このデバイスは駆動能力を備えており、軽負荷に高速エッジが生成されるため、リンギングを防ぐために配線と負荷の条件を考慮する必要があります。さらに、このデバイスの出力は、デバイスを損傷することなく維持できる以上に大きな電流を駆動できます。過電流による損傷を防止するため、デバイスの出力電力を制限することが重要です。「絶対最大定格」で定義されている電気的および熱的制限を常に順守してください。

未使用のプッシュプル CMOS 出力は、未接続のままにする必要があります。

### 8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in 図 8-1.

**注意**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

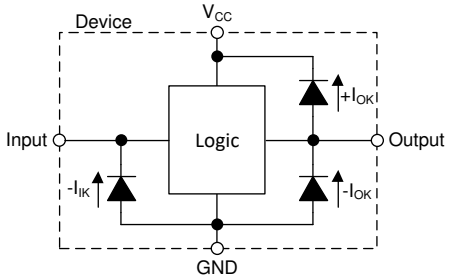



**図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.3 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much

slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

### 8.3.4 LVxT Enhanced Input Voltage

The SN74LV6T14 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ($V_{CC}$), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 図 8-2 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

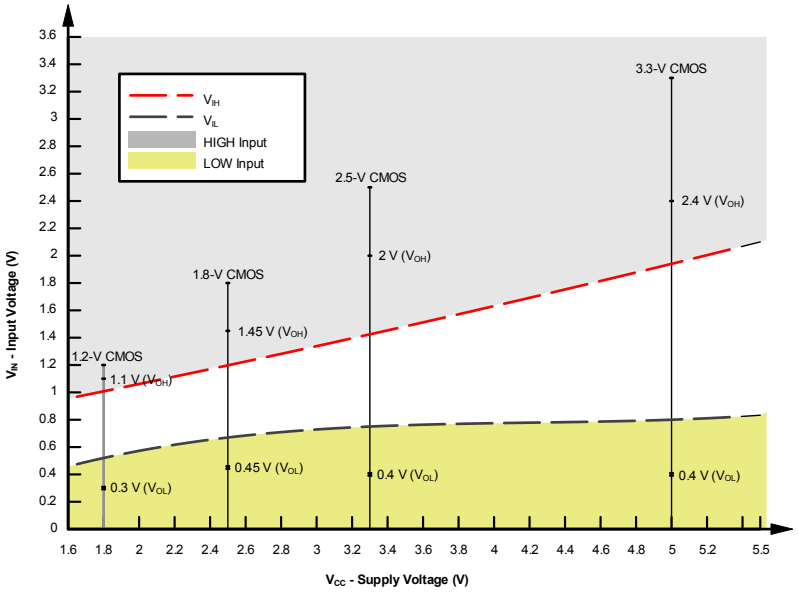



**図 8-2. LVxT Input Voltage Levels**

#### *8.3.4.1 Down Translation*

Signals can be translated down using the SN74LV6T14. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state. As shown in 図 8-2, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in 図 8-3 for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V $V_{CC}$.

*Down Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V $V_{CC}$ – Inputs from 3.3 V and 5.0 V
- 3.3-V $V_{CC}$ – Inputs from 5.0 V

### *8.3.4.2 Up Translation*

Input signals can be up translated using the SN74LV6T14. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV6T14, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in 図 8-3, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

*Up Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 1.2 V
- 2.5-V $V_{CC}$ – Inputs from 1.8 V
- 3.3-V $V_{CC}$ – Inputs from 1.8 V and 2.5 V
- 5.0-V $V_{CC}$ – Inputs from 2.5 V and 3.3 V

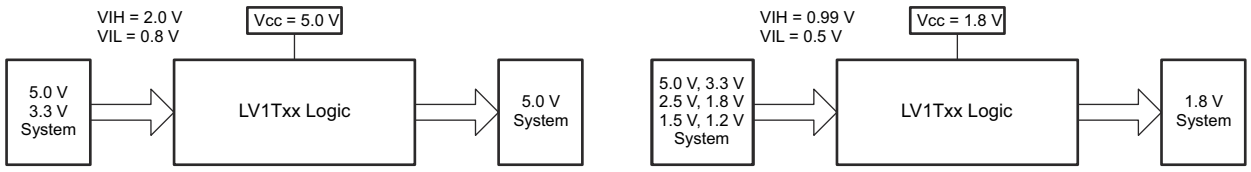



**図 8-3. LVxT Up and Down Translation Example**

## 8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV6T14.

**表 8-1. Function Table**

| INPUTS(1) | OUTPUT |
|---|---|
| A | Y |
| H | L |
| L | H |

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

# 9 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV6T14 can be used to add an additional stage to a counter with an external flip-flop. Because counters use a negative edge trigger, the flip-flop's clock input must be inverted to provide this function. Having Schmitt-trigger inputs is important in this application to eliminate any noise issues that could impact the counting function which could lead to incorrect frequency division. This function only requires one of the six available inverters in the SN74LV6T14 device, so the remaining channels can be used for other applications needing an inverted signal or improved signal integrity. Unused inputs must be terminated at $V_{CC}$ or GND. Unused outputs can be left floating.

## 9.2 Typical Application

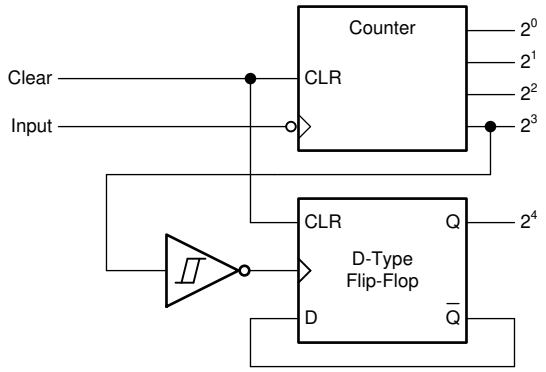



**図 9-1. Typical Application Block Diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV6T14 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV6T14 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV6T14 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV6T14 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

**注意**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV6T14 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV6T14 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV6T14 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.3 Application Curves

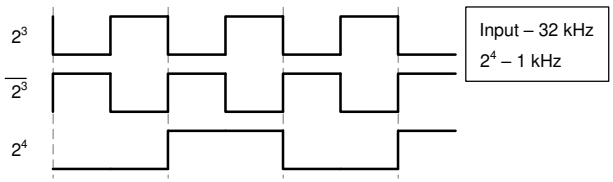



**図 9-2. Application Timing Diagram**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

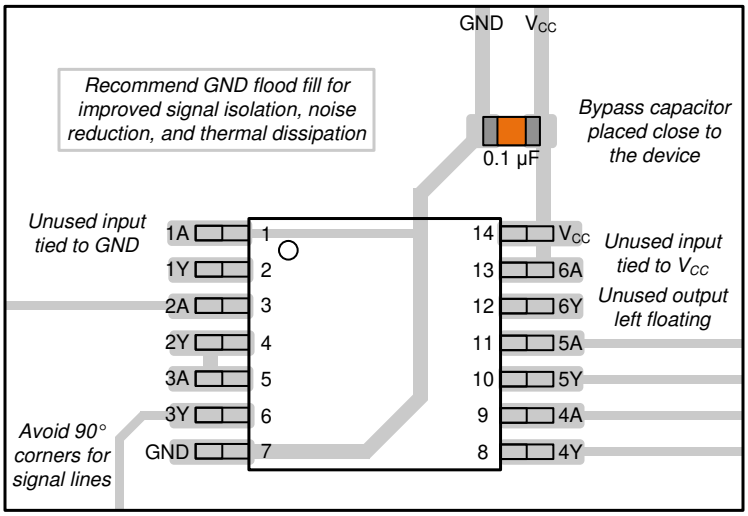



**図 11-1. Example Layout for the SN74LV6T14**

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 12.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

## 12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 12.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV6T14BQAR | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | SELECTIVE AG (TOP SIDE) | Level-1-260C-UNLIM | -40 to 125 | LV6T14 |
| SN74LV6T14BQAR.A | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | SELECTIVE AG (TOP SIDE) | Level-1-260C-UNLIM | -40 to 125 | LV6T14 |
| SN74LV6T14PWR | Active | Production | TSSOP (PW) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV6T14 |
| SN74LV6T14PWR.A | Active | Production | TSSOP (PW) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV6T14 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN74LV6T14 :**

- Automotive : SN74LV6T14-Q1
- Enhanced Product : SN74LV6T14-EP

NOTE: Qualified Version Definitions:

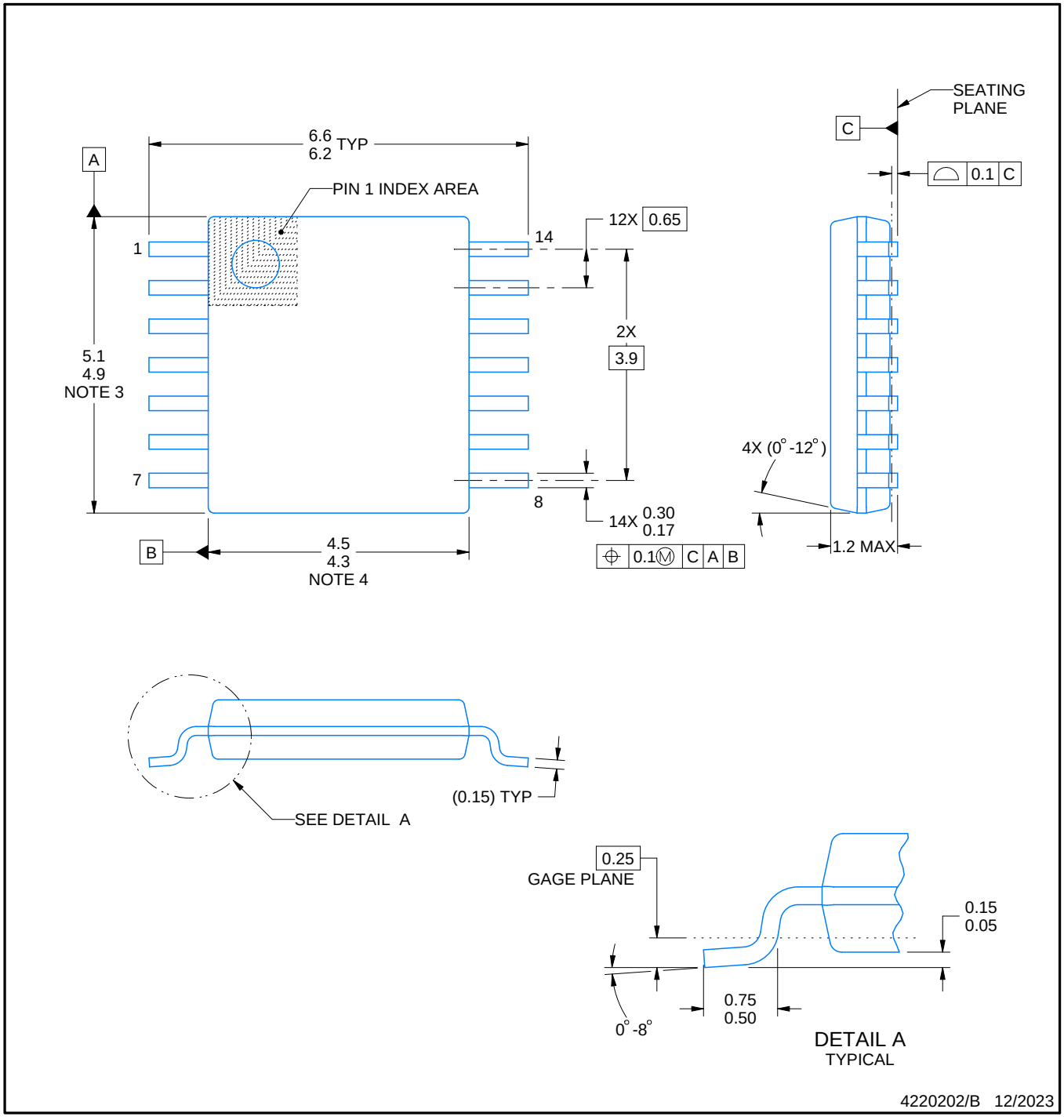
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

# PACKAGE OUTLINE

## PW0014A

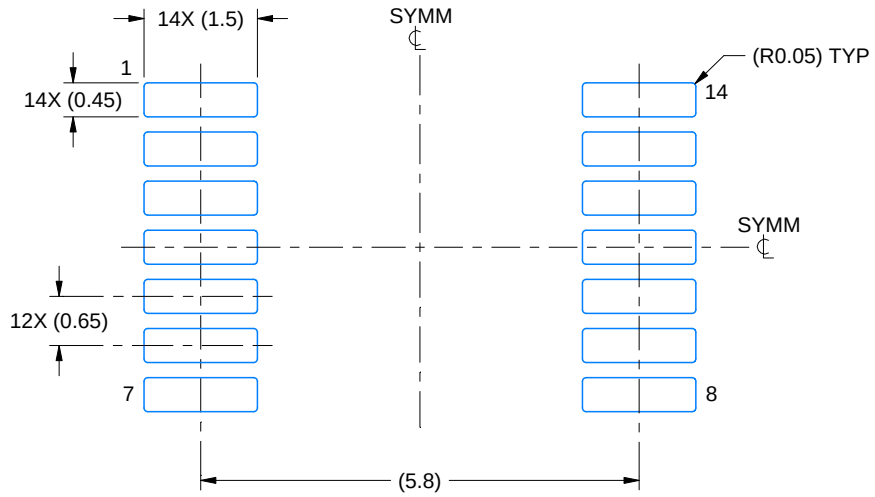
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

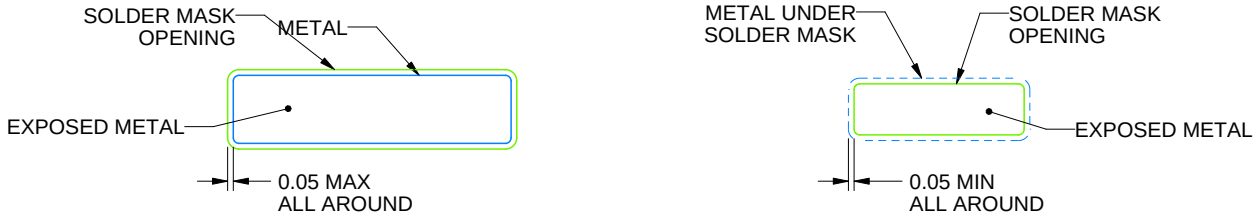



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

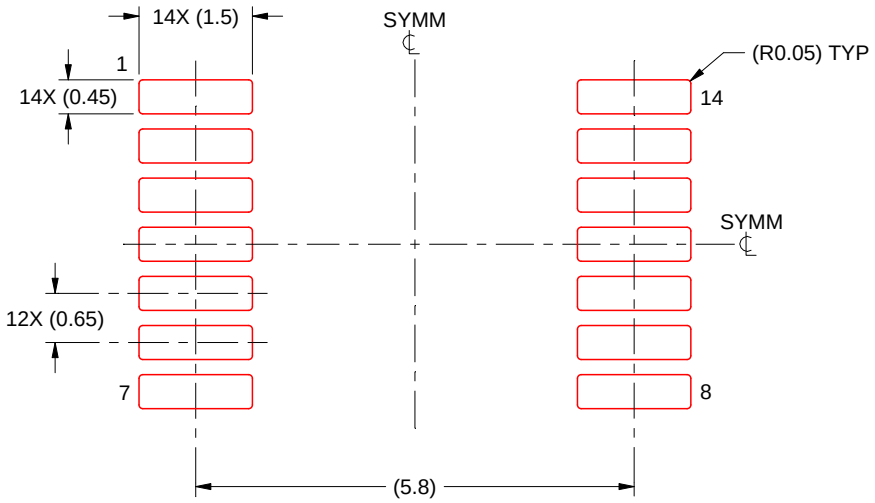



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

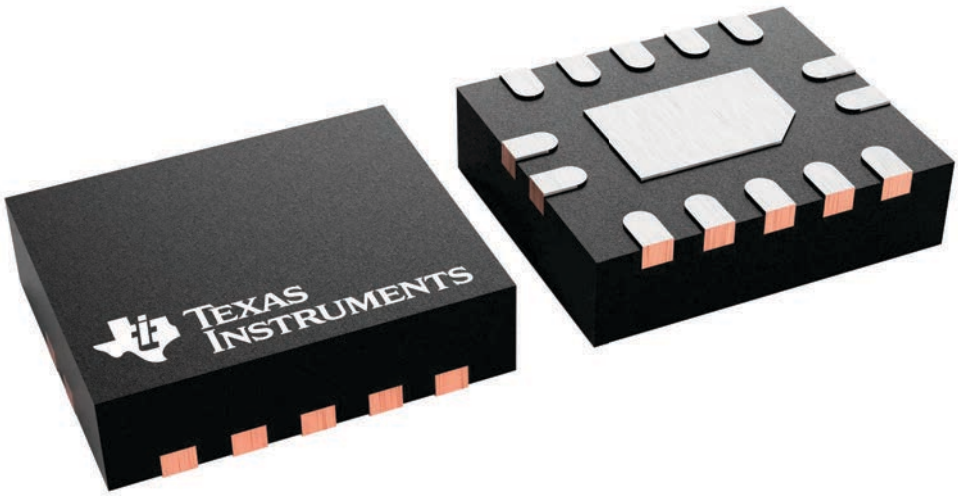
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

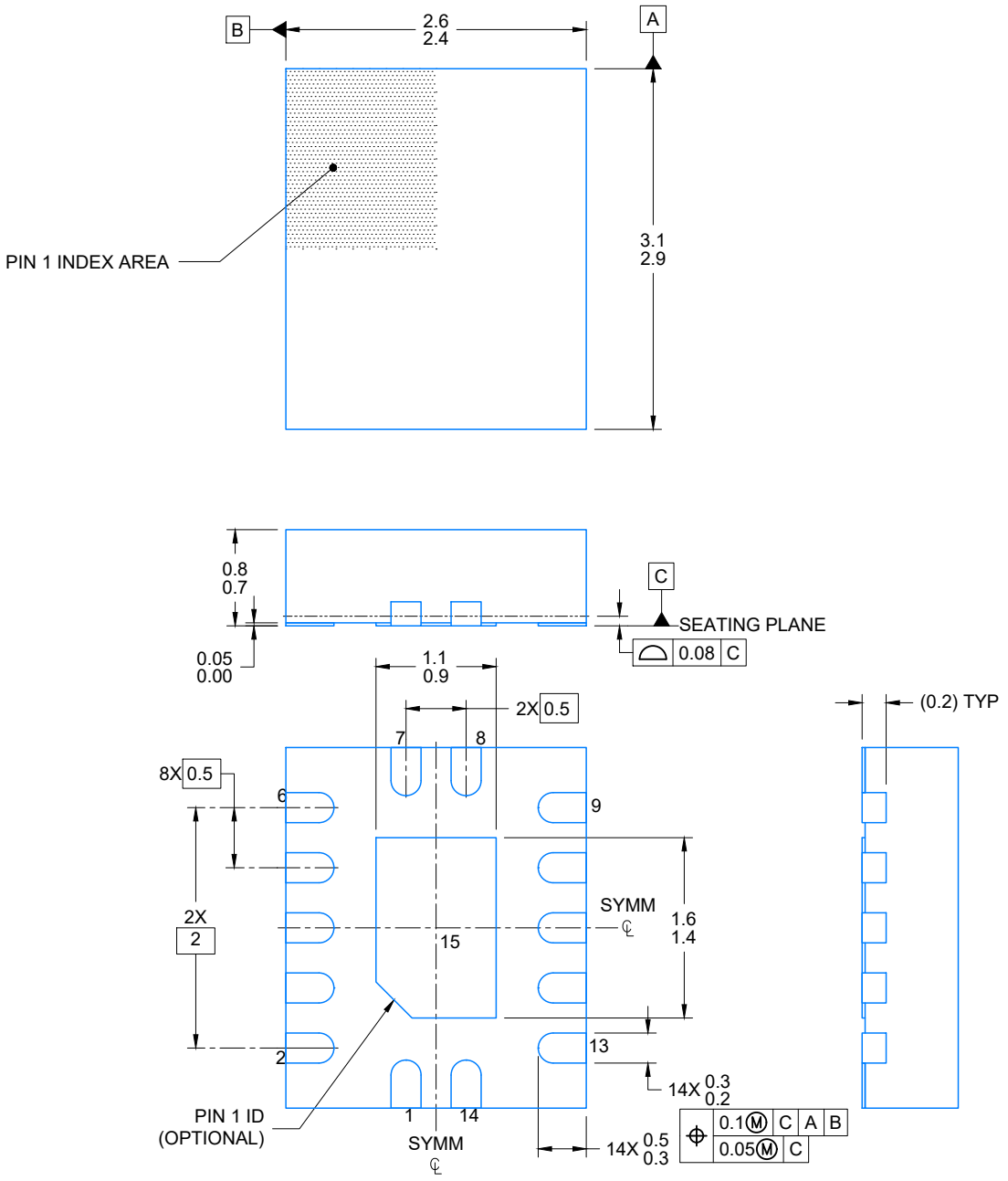


# PACKAGE OUTLINE

## BQA0014A

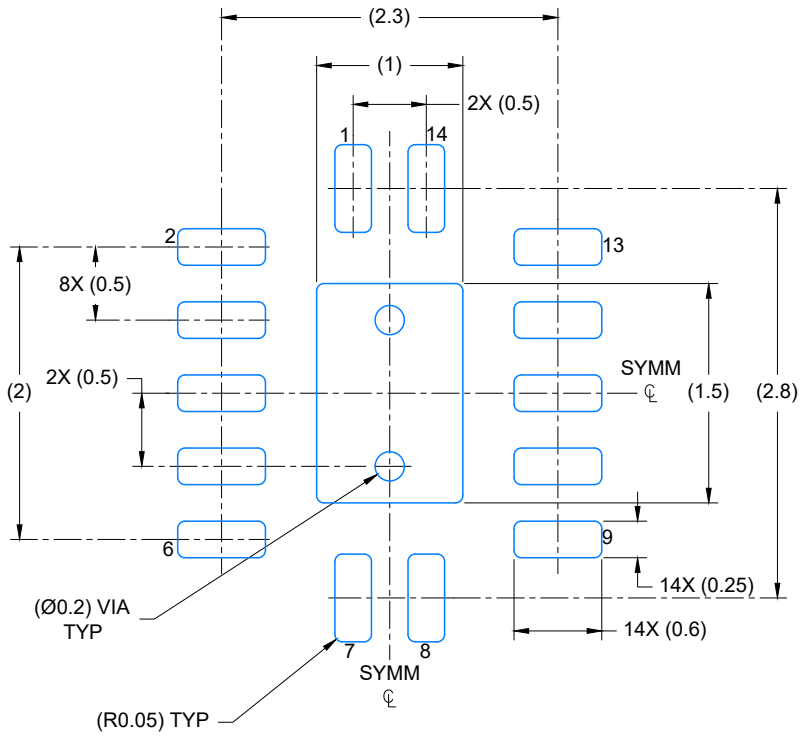
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

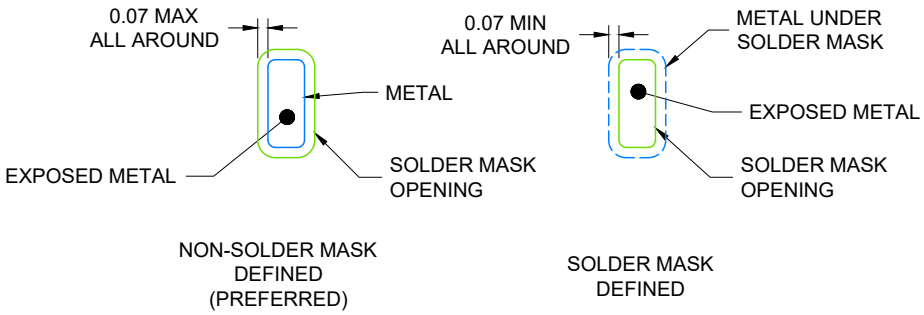



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

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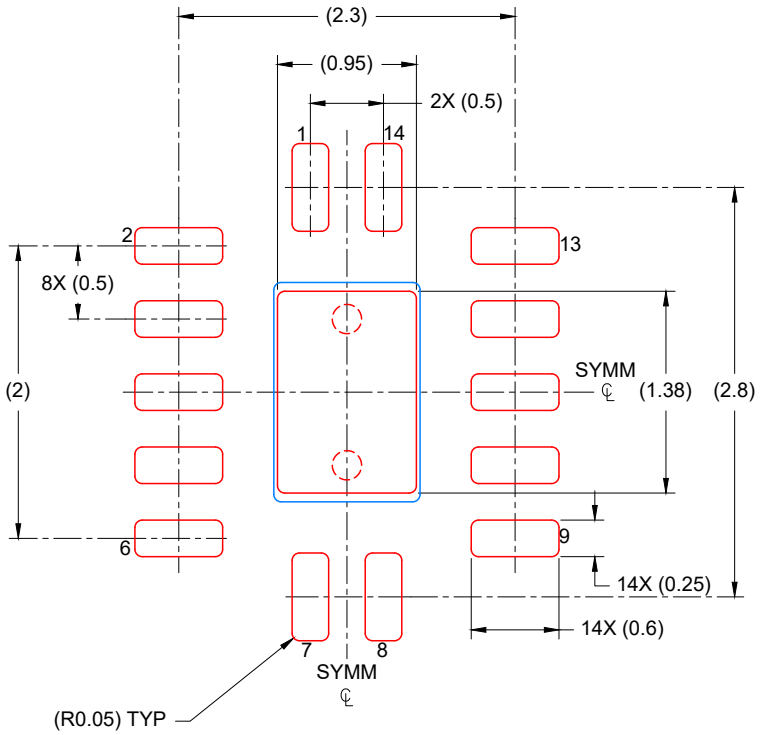
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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