

SN74LV4066A クワッド双方向アナログスイッチ

1 特長

- 1.65V～5.5V の V_{CC} で動作
- すべてのポートで混在モード電圧動作をサポート
- 高いオン / オフ出力電圧比
- スイッチ間の低いクロストーク
- スイッチの個別制御
- 非常に低い入力電流
- JESD 22 を上回る ESD 保護:
 - 2000V 人体モデル (A114-A)
 - マシン モデルで 200V (A115-A)
 - 750V 荷電デバイス モデル (C101)

2 アプリケーション

- [テレコミュニケーション](#)
- [eCall](#) (車載用緊急通報システム)
- [インフォテインメント](#)

3 概要

このクワッド シリコンゲート CMOS アナログ スイッチは、1.65V～5.5V の V_{CC} で動作するように設計されています。

このスイッチは、アナログとデジタルの両方の信号を扱うことができます。各スイッチは、最大 5.5V (ピーク) までの振幅の信号をどちらの方向にも伝送できます。

それぞれのスイッチ セクションには、独自のイネーブル入力制御 (C) が存在します。C に HIGH レベルの電圧が印加されると、対応するスイッチ セクションがオンになります。

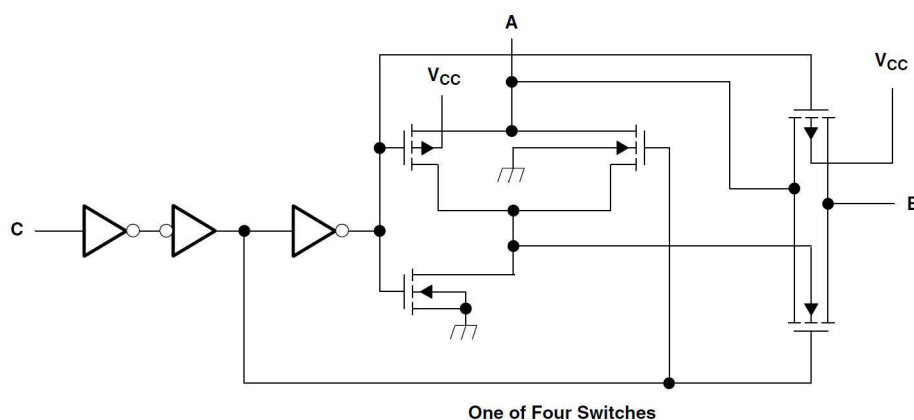
信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN74LV4066A	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	RGY (QFN, 14)	3.5mm × 3.5mm

(1) 詳細については、[セクション 10](#) を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)



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4 Pin Configuration and Functions

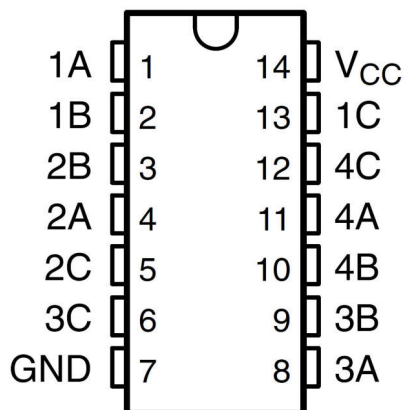


図 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

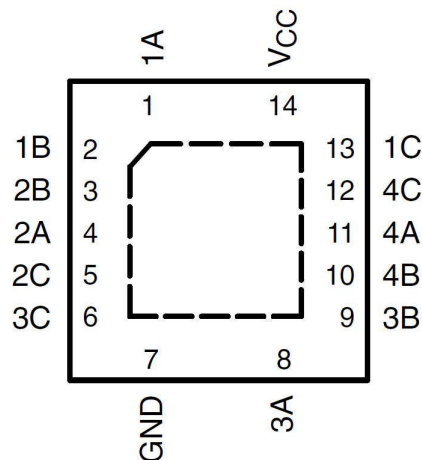


図 4-2. RGY Package, 14-Pin QFN (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I/O	Input/Output to switch channel 1
1B	2	I/O	Input/Output to switch channel 1
2B	3	I/O	Input/Output to switch channel 2
2A	4	I/O	Input/Output to switch channel 2
2C	5	I	Control line for channel 2. Switch is ON when control pin is high.
3C	6	I	Control line for channel 3. Switch is ON when control pin is high.
GND	7	—	Ground (0V) reference
3A	8	I/O	Input/Output to switch channel 3
3B	9	I/O	Input/Output to switch channel 3
4B	10	I/O	Input/Output to switch channel 4
4A	11	I/O	Input/Output to switch channel 4
4C	12	I	Control line for channel 4. Switch is ON when control pin is high.
1C	13	I	Control line for channel 1. Switch is ON when control pin is high.
V _{CC}	14	—	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VDD and GND.
Thermal pad		—	It is recommended to tie the pad to GND for the best performance.

(1) Signal types: I = input, O = output, I/O = input or output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	7.0	V
V _I	Logic input voltage range		−0.5	7.0	V
V _{IO}	Switch I/O voltage range ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Logic input clamp current	V _I < 0	−20		mA
I _{IOK}	Switch path diode clamp current	V _{IO} < 0 or V _{IO} > V _{CC}	−50	50	mA
I _T	Switch continuous current	V _{IO} = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{std}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information: SN74LV4066A

THERMAL METRIC ⁽¹⁾		SN74LV4066A			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.8	150.6	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		1.65		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 2V	1.5		5.5	V
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.7		5.5	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.7		5.5	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.7		5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 2V	0		0.5	V
		V _{CC} = 2.3V to 2.7V	0	V _{CC} × 0.3		
		V _{CC} = 3V to 3.6V	0	V _{CC} × 0.3		
		V _{CC} = 4.5V to 5.5V	0	V _{CC} × 0.3		
V _I	Logic control input voltage		0		5.5	V
V _{IO}	Switch input or output voltage		0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 2.3V to 2.7V			200	ns/V
		V _{CC} = 3V to 3.6V			100	
		V _{CC} = 4.5V to 5.5V			20	
T _A	Ambient temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.5 Electrical Characteristics (LV)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 6-1)	1.65V	25°C	60	150	Ω
				–40°C to 85°C		225	
				–40°C to 125°C		225	
			2.3V	25°C	38	180	
				–40°C to 85°C		225	
				–40°C to 125°C		225	
			3V	25°C	29	150	Ω
				–40°C to 85°C		190	
				–40°C to 125°C		190	
			4.5V	25°C	21	75	Ω
				–40°C to 85°C		100	
				–40°C to 125°C		100	

5.5 Electrical Characteristics (LV) (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C		130	600	Ω
			–40°C to 85°C			700	
			–40°C to 125°C			700	
			25°C		143	500	
			–40°C to 85°C			600	
			–40°C to 125°C			600	
		3V	25°C		57	180	Ω
			–40°C to 85°C			225	
			–40°C to 125°C			225	
		4.5V	25°C		31	100	Ω
			–40°C to 85°C			125	
			–40°C to 125°C			125	
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C		2.5		Ω
			–40°C to 85°C		3		
			–40°C to 125°C		3		
			25°C		3	30	
			–40°C to 85°C			40	
			–40°C to 125°C			40	
		3V	25°C		3	20	Ω
			–40°C to 85°C			30	
			–40°C to 125°C			30	
		4.5V	25°C		2	15	Ω
			–40°C to 85°C			20	
			–40°C to 125°C			20	
I _{IH} I _{IL}	Control input current	V _I = 5.5V or GND	25°C			0.1	μA
			–40°C to 85°C	0 to 5.5V		1	
			–40°C to 125°C			1	
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see 6-2)	25°C			±0.1	μA
			–40°C to 85°C	5.5V		±1	
			–40°C to 125°C			±1	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see 6-3)	25°C			±0.1	μA
			–40°C to 85°C	5.5V		±1	
			–40°C to 125°C			±1	
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0V	25°C		0.01		μA
			–40°C to 85°C	5.5V		20	
			–40°C to 125°C			20	
C _{IC}	Control input capacitance	f = 10MHz	25°C	3.3V	4		pF
C _{IS}	Switch terminal capacitance	f = 10MHz	25°C	3.3V	5.5		pF
C _{OS(on)}	Common terminal ON-capacitance	f = 10MHz	25°C	3.3V	5.5		pF

5.5 Electrical Characteristics (LV) (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _F	Feedthrough capacitance	f = 10MHz	25°C	3.3V		0.5		pF
C _{PD}	Power dissipation capacitance	C _L = 50pF, f = 10MHz	25°C	3.3V		4.5		pF

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted)

V_{CC} = 2V ± 0.2V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF (see 6-4)	25°C		1.2	10	ns
					–40°C to 85°C			16	
					–40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF (see 6-5)	25°C		3.3	15	ns
					–40°C to 85°C			20	
					–40°C to 125°C			20	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF (see 6-5)	25°C		6	15	ns
					–40°C to 85°C			23	
					–40°C to 125°C			23	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF (see 6-4)	25°C		2.6	12	ns
					–40°C to 85°C			18	
					–40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50pF (see 6-5)	25°C		4.2	25	ns
					–40°C to 85°C			32	
					–40°C to 125°C			32	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50pF (see 6-5)	25°C		9.6	25	ns
					–40°C to 85°C			32	
					–40°C to 125°C			32	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)

V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF (see 6-4)	25°C		0.8	6	ns
					–40°C to 85°C			10	
					–40°C to 125°C			10	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF (see 6-5)	25°C		2.3	11	ns
					–40°C to 85°C			15	
					–40°C to 125°C			15	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF (see 6-5)	25°C		4.5	11	ns
					–40°C to 85°C			15	
					–40°C to 125°C			15	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF (see 6-4)	25°C		1.5	9	ns
					–40°C to 85°C			12	
					–40°C to 125°C			12	

5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ (続き)

over recommended operating free-air temperature range (unless otherwise noted)

$V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$ (see 図 6-5)	25°C		8	18	ns
					–40°C to 85°C			22	
					–40°C to 125°C			22	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$ (see 図 6-5)	25°C		7.2	18	ns
					–40°C to 85°C			22	
					–40°C to 125°C			22	

5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range (unless otherwise noted)

$V_{CC} = 5V \pm 0.5V$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15pF$ (see 図 6-4)	25°C		0.6	4	ns
					–40°C to 85°C			7	
					–40°C to 125°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15pF$ (see 図 6-5)	25°C		3.5	8	ns
					–40°C to 85°C			10	
					–40°C to 125°C			11	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15pF$ (see 図 6-5)	25°C		4.4	8	ns
					–40°C to 85°C			10	
					–40°C to 125°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$ (see 図 6-4)	25°C		0.8	6	ns
					–40°C to 85°C			8	
					–40°C to 125°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$ (see 図 6-5)	25°C		7	13	ns
					–40°C to 85°C			16	
					–40°C to 125°C			16	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$ (see 図 6-5)	25°C		6.2	13	ns
					–40°C to 85°C			16	
					–40°C to 125°C			16	

5.9 AC Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	4066	$C_L = 50pF$, $R_L = 50\Omega$, $F_{in} = 1MHz$ (sine wave) (see 図 6-6)(1)	$V_{CC} = 2.3V$		60		MHz
					$V_{CC} = 3V$		75		
					$V_{CC} = 4.5V$		100		
Charge Injection (control input to signal output)	INH	COM or Yn	ALL	$C_L = 50pF$, $F_{in} = 1MHz$ (sine wave) (see 図 6-7)	$V_{CC} = 2.3V$		15		mV
					$V_{CC} = 3V$		20		
					$V_{CC} = 4.5V$		50		

5.9 AC Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 50Ω, F _{in} = 1MHz (sine wave) (see Figure 6-8(2))	V _{CC} = 2.3V	–40		dB
					V _{CC} = 3V	–40		
					V _{CC} = 4.5V	–40		
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 50Ω, F _{in} = 1MHz (sine wave) (see Figure 6-9(2))	V _{CC} = 2.3V	–45		dB
					V _{CC} = 3V	–45		
					V _{CC} = 4.5V	–45		
Sine-wave distortion	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 10kΩ, F _{in} = 1kHz (sine wave) (see Figure 6-10)	V _I = 2V _{p-p} V _{CC} = 2.3V	0.1		%
					V _I = 2.5V _{p-p} V _{CC} = 3V	0.1		
					V _I = 4V _{p-p} V _{CC} = 4.5V	0.1		

6 Parameter Measurement Information

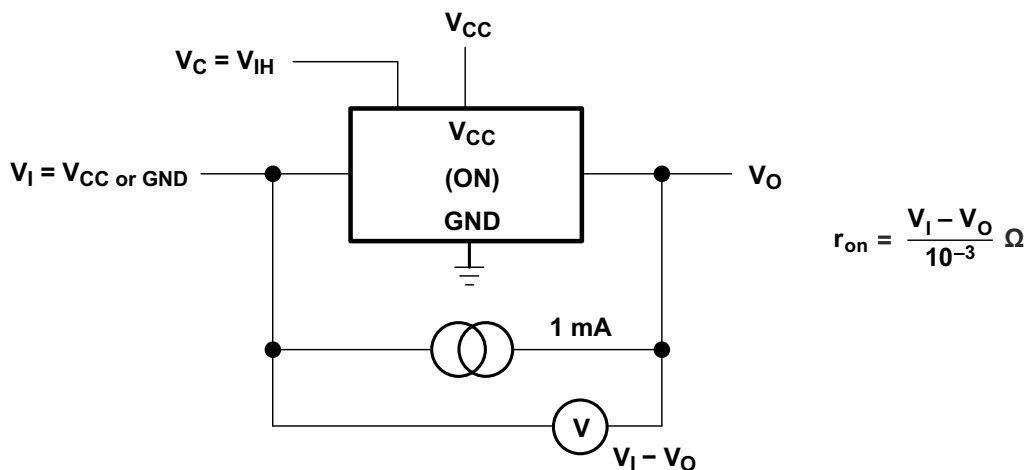


図 6-1. ON-State Resistance Test Circuit

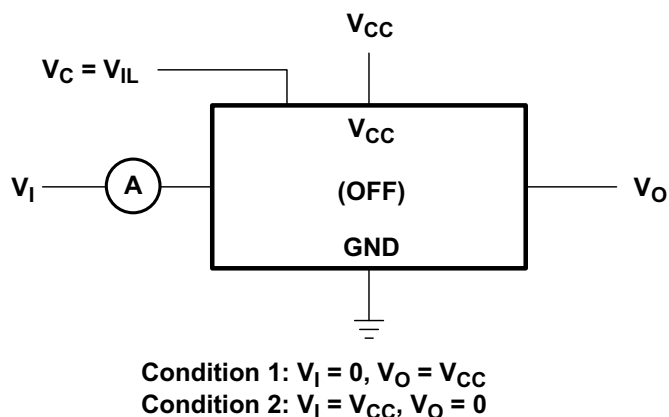


図 6-2. OFF-State Switch Leakage-Current Test Circuit

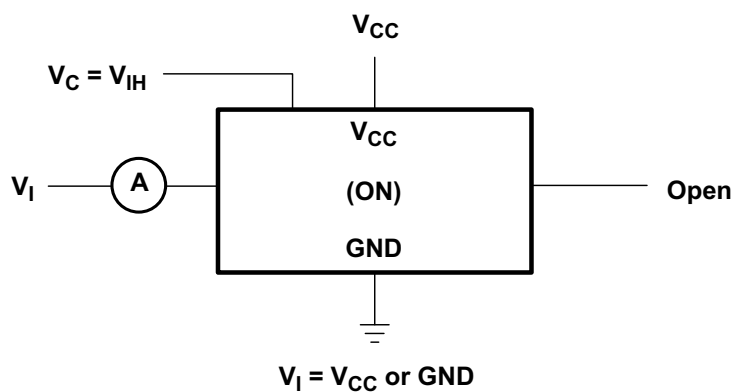
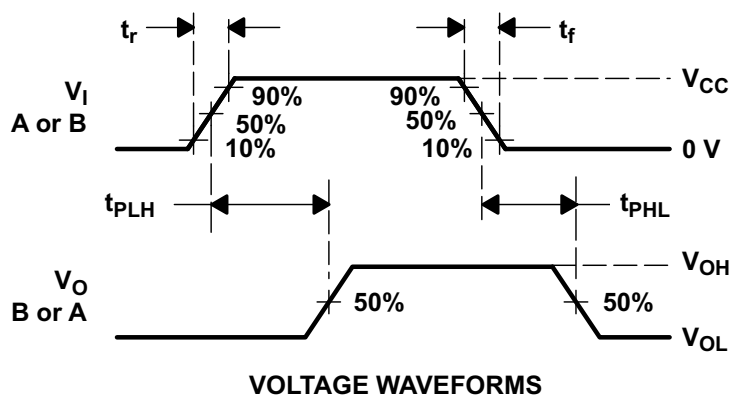
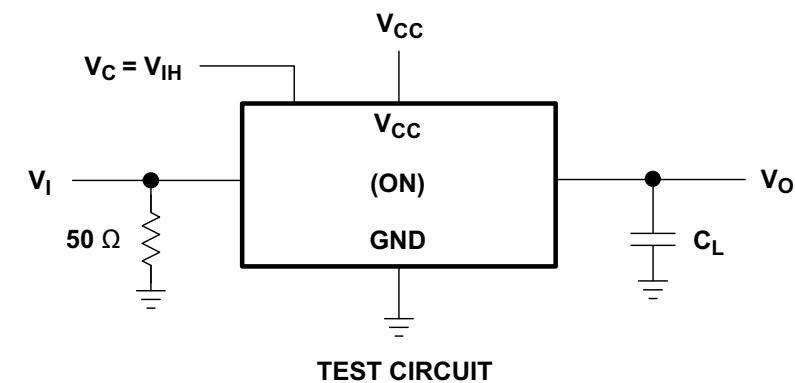
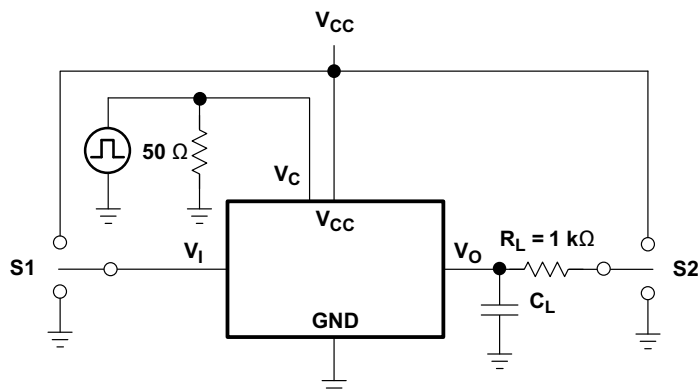


図 6-3. ON-State Leakage-Current Test Circuit

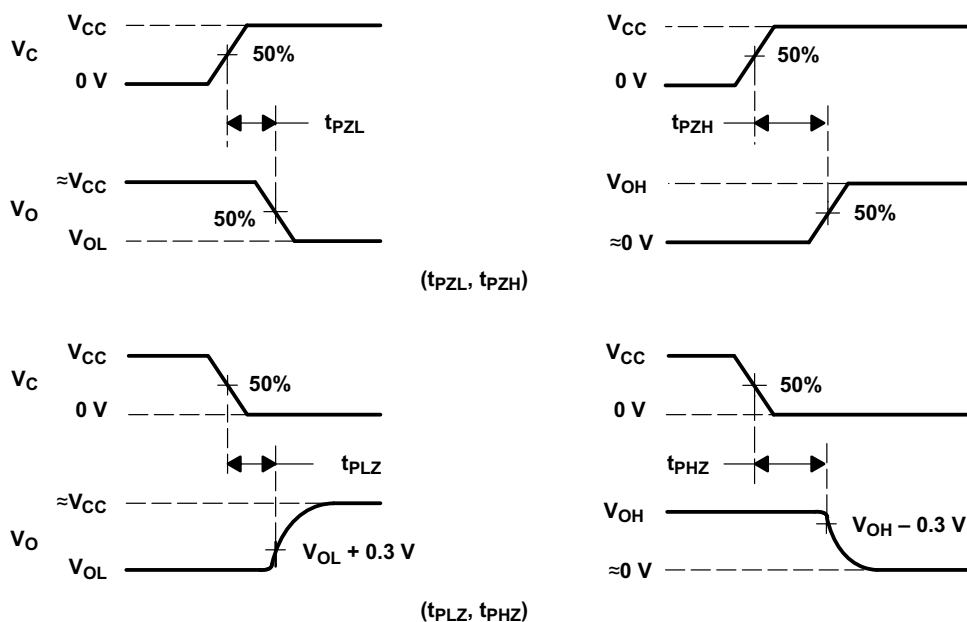


✎ 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST CIRCUIT

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

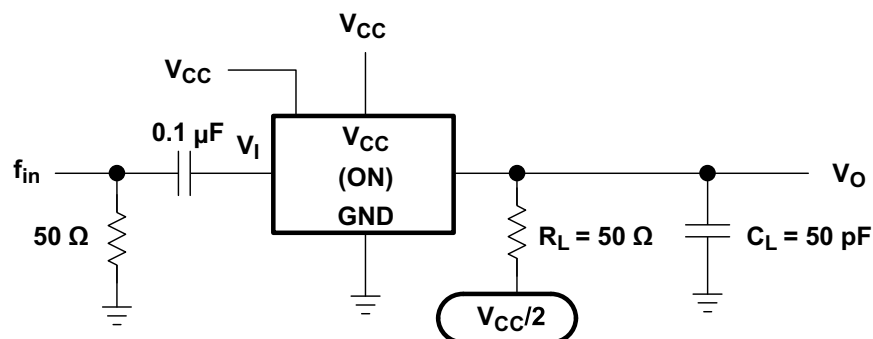
图 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

图 6-6. Frequency Response (Switch ON)

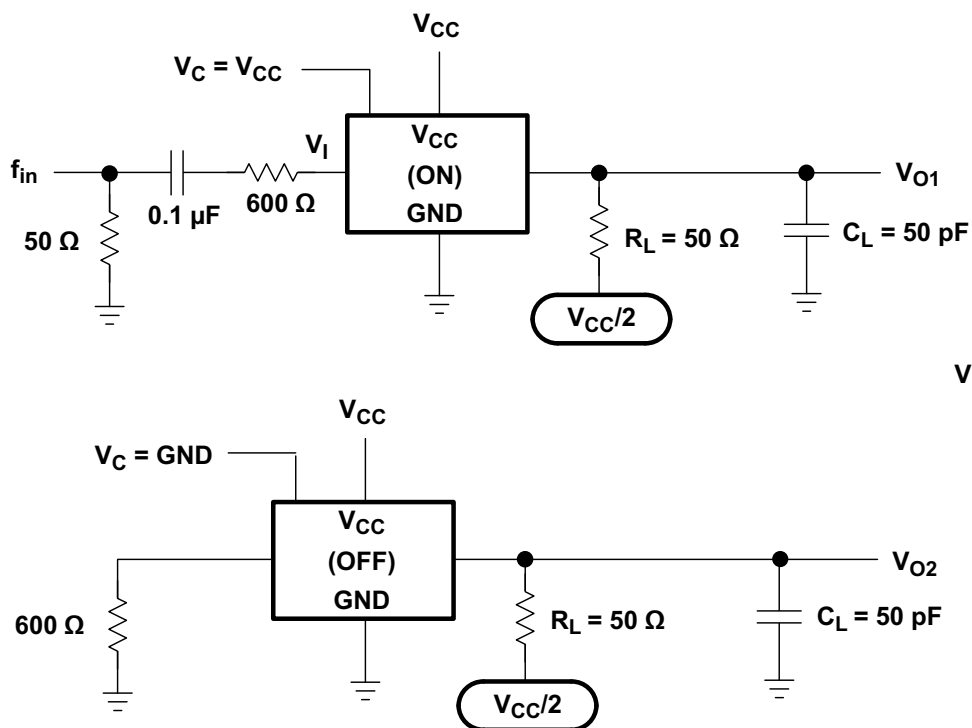


図 6-7. Crosstalk Between Any Two Switches

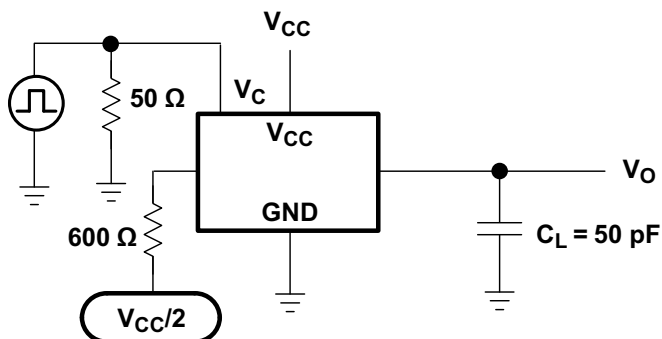


図 6-8. Crosstalk (Control Input – Switch Output)

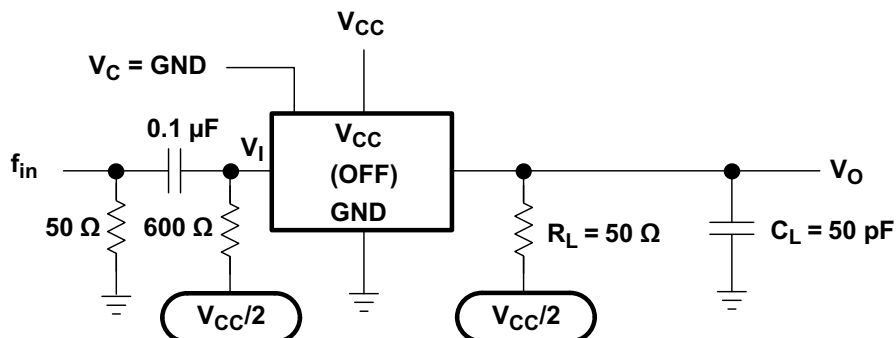


図 6-9. Feed-Through Attenuation (Switch OFF)

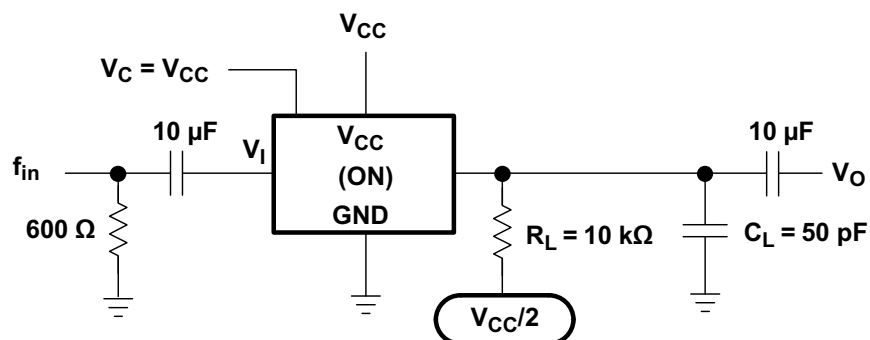


図 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Functional Block Diagram

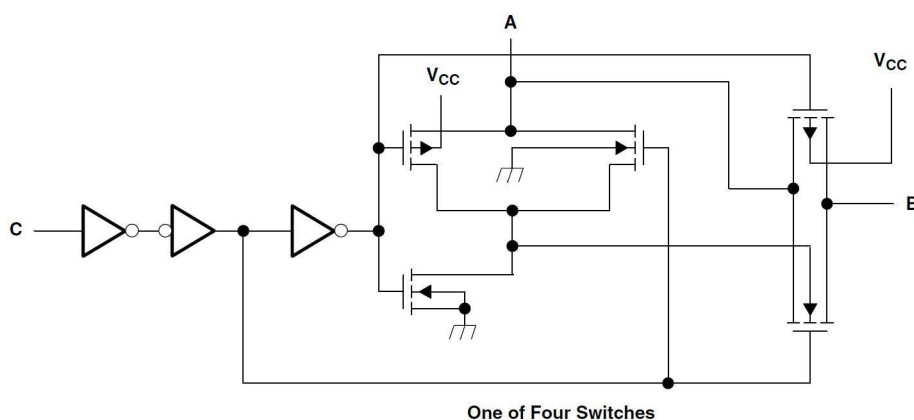


図 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table

Input Control (C)	Switch
L	OFF
H	ON

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.3 Trademarks

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8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (April 2006) to Revision J (February 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
データシートから SN54LV4066A の情報を削除.....	1
V _{CC} 動作を「2V~5.5V」から「1.65V~5.5V」に変更、それに応じて、r _{ON} 、r _{ON(p)} 、Δr _{ON} などの仕様を更新.....	1
Changed RL value from: 600Ω to: 50Ω for frequency response, crosstalk, and feed-through attenuation, and their associated figures.....	10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4066AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LV4066A
SN74LV4066ADBR	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADBR.A	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADGVR	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADGVR.A	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066AN	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4066AN
SN74LV4066AN.A	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4066AN
SN74LV4066ANSR	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4066A
SN74LV4066ANSR.A	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4066A
SN74LV4066APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW066A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4066ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4066ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4066ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV4066ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV4066APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4066ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4066ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV4066ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV4066ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV4066ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV4066APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV4066ARGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

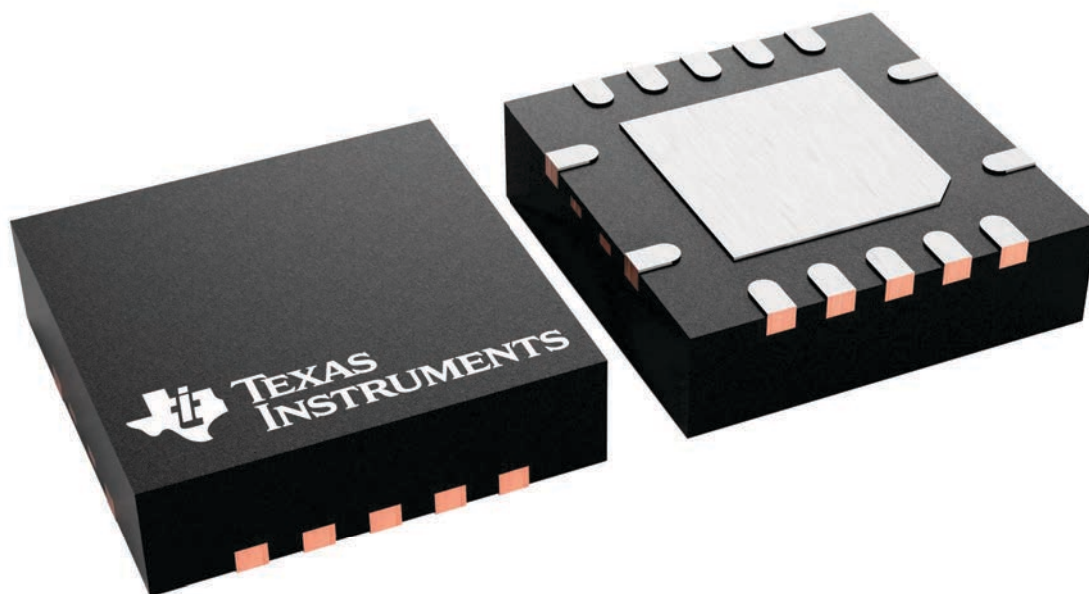
RGY 14

VQFN - 1 mm max height

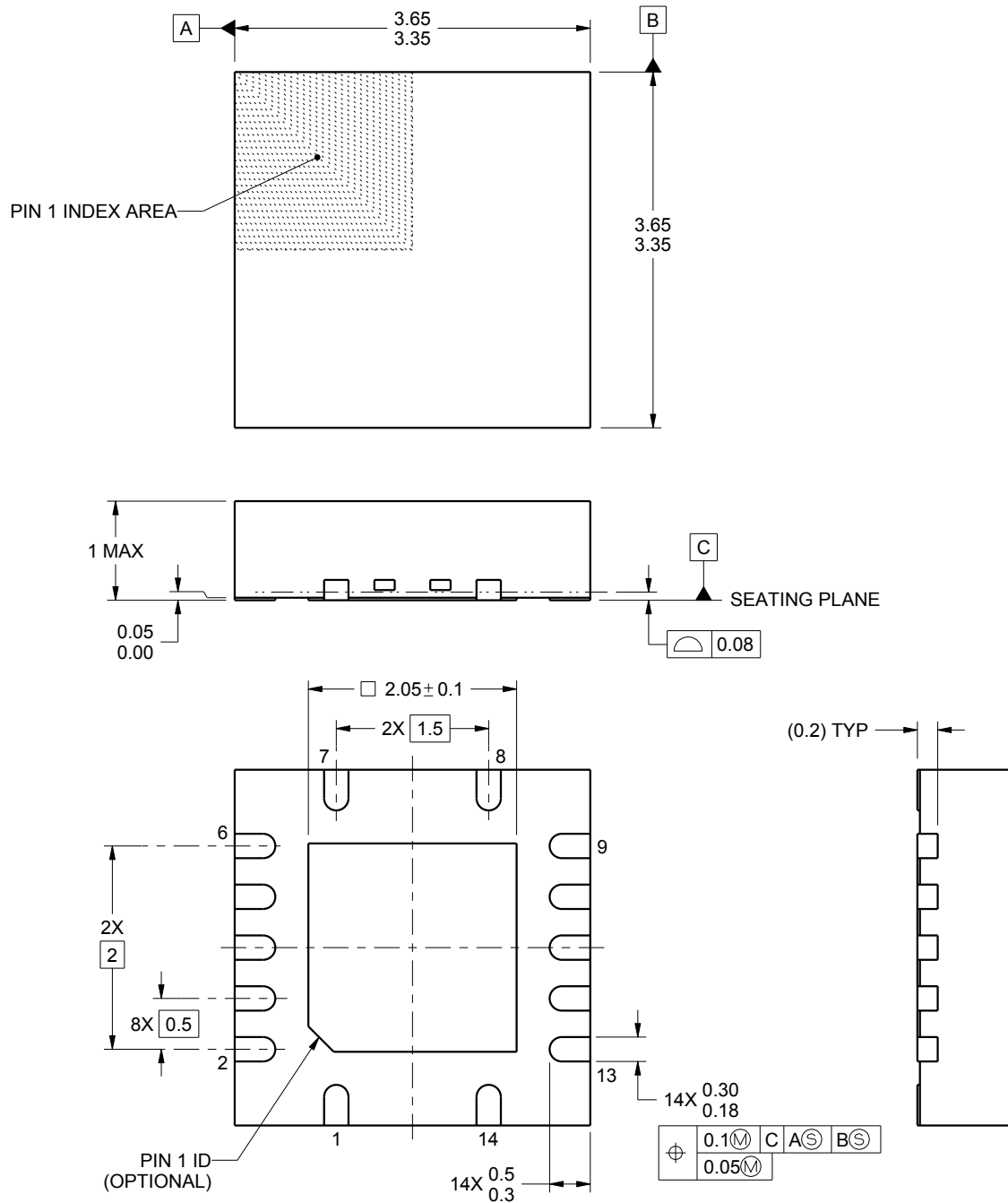
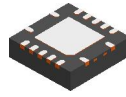
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A



4219040/A 09/2015

NOTES:

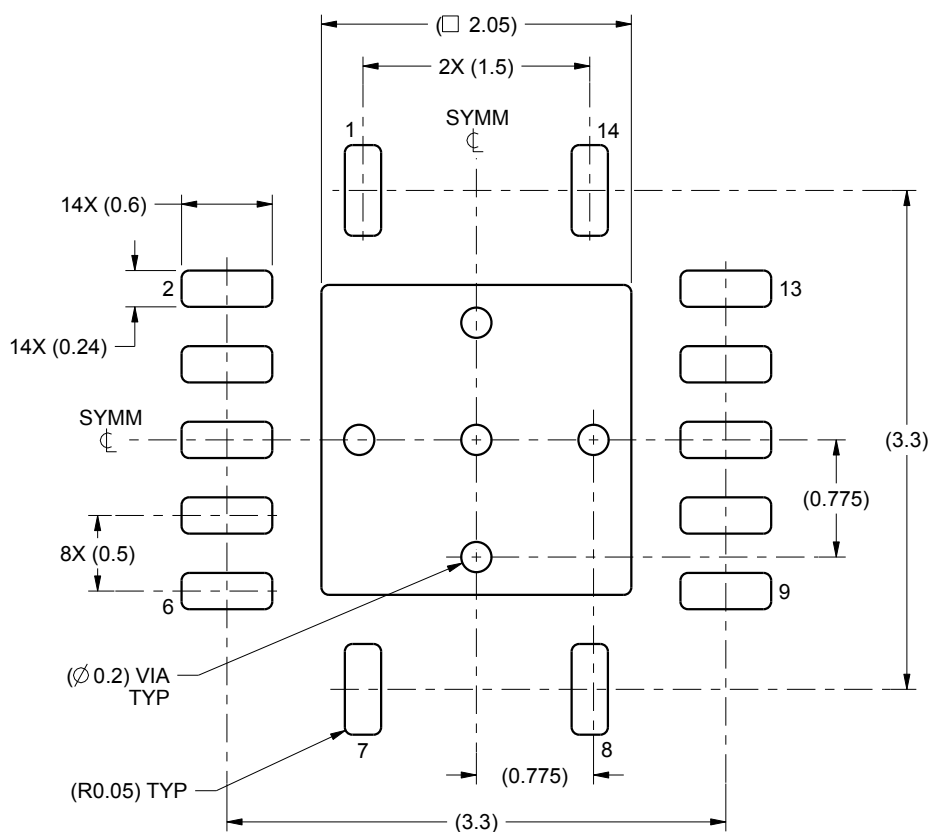
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

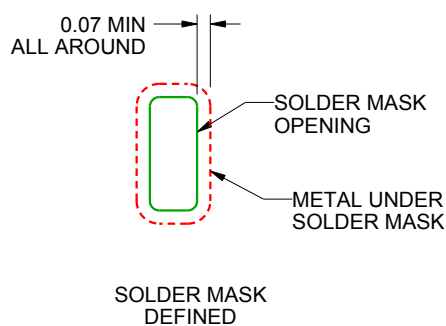
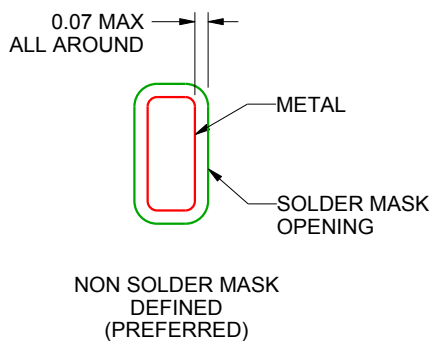
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

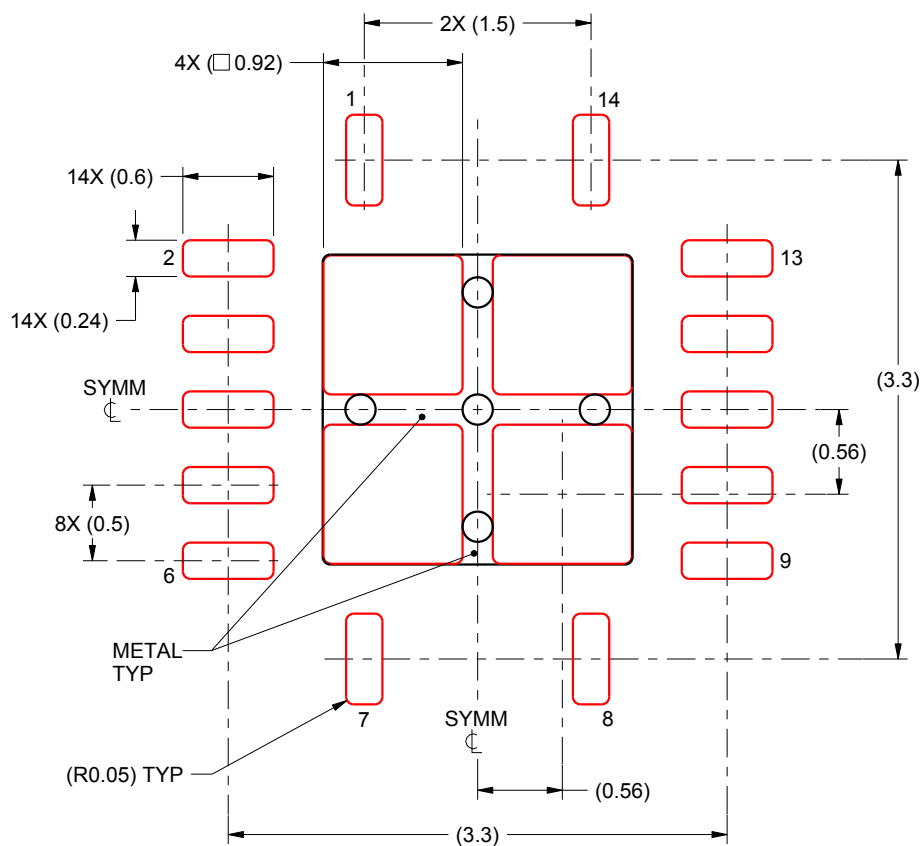
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

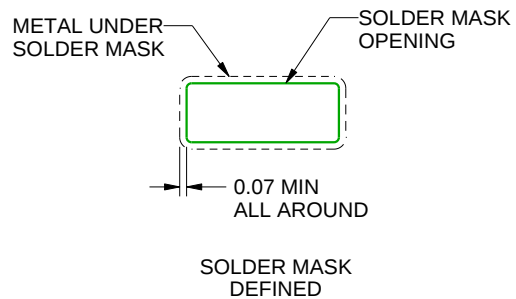
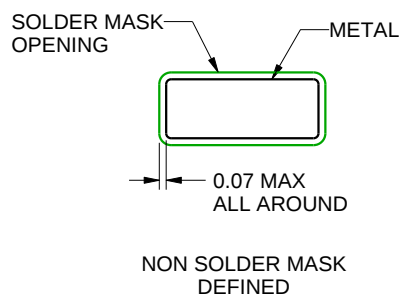
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

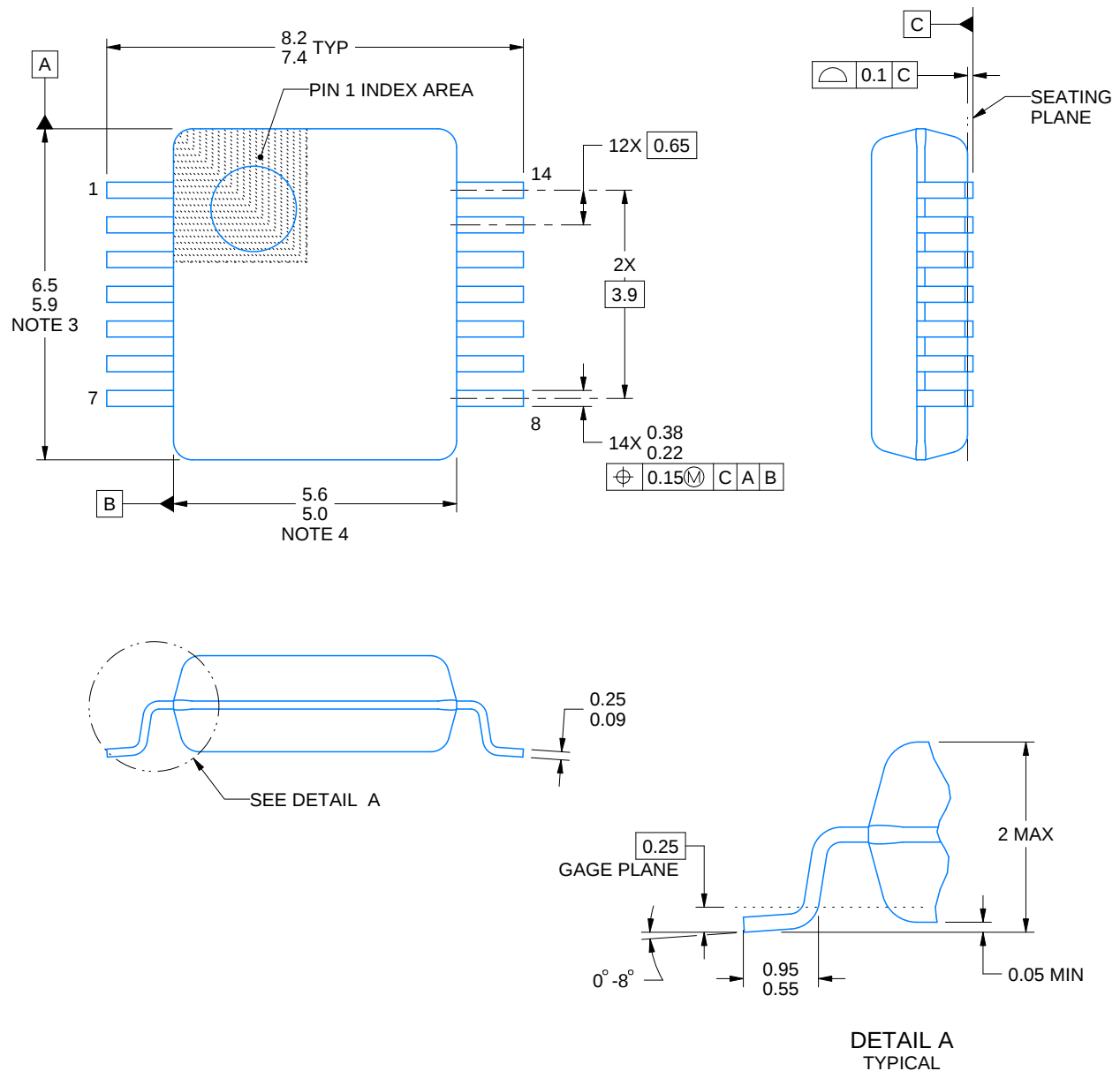
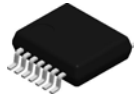
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

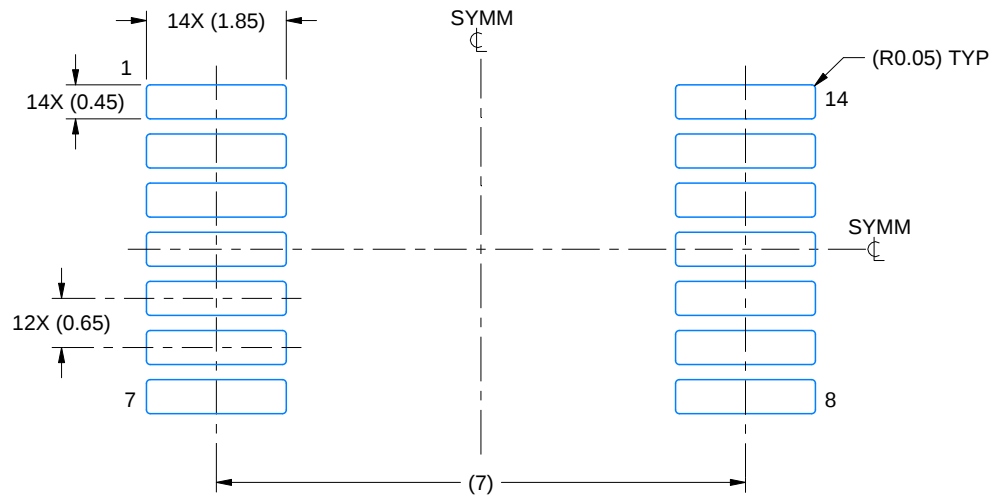
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

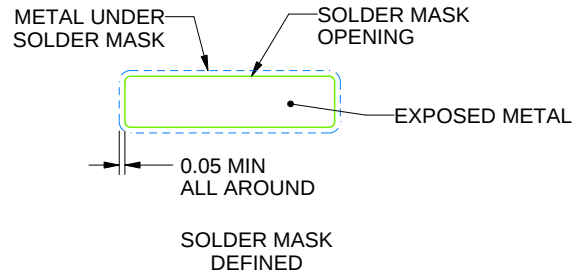
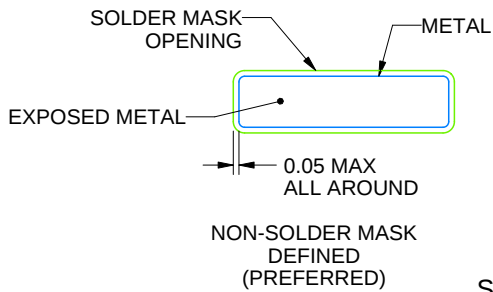
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

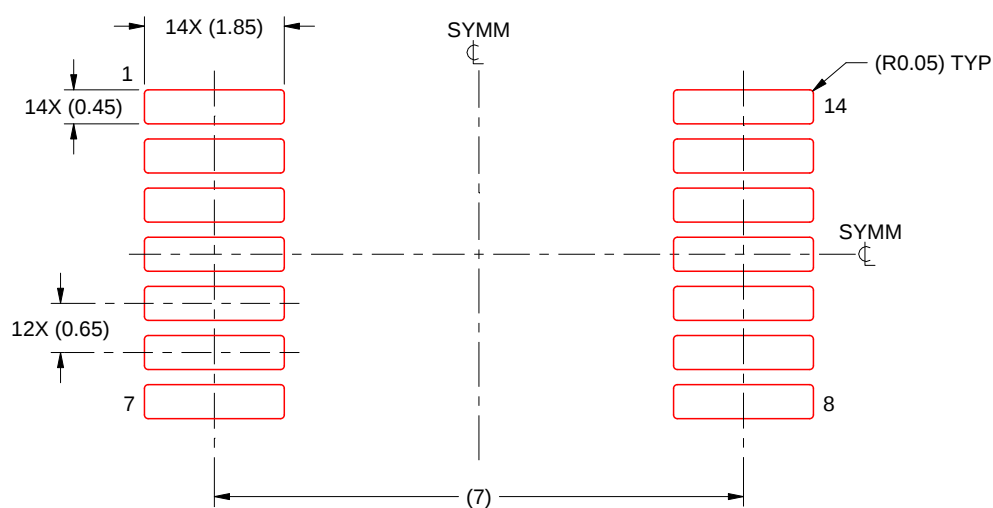
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

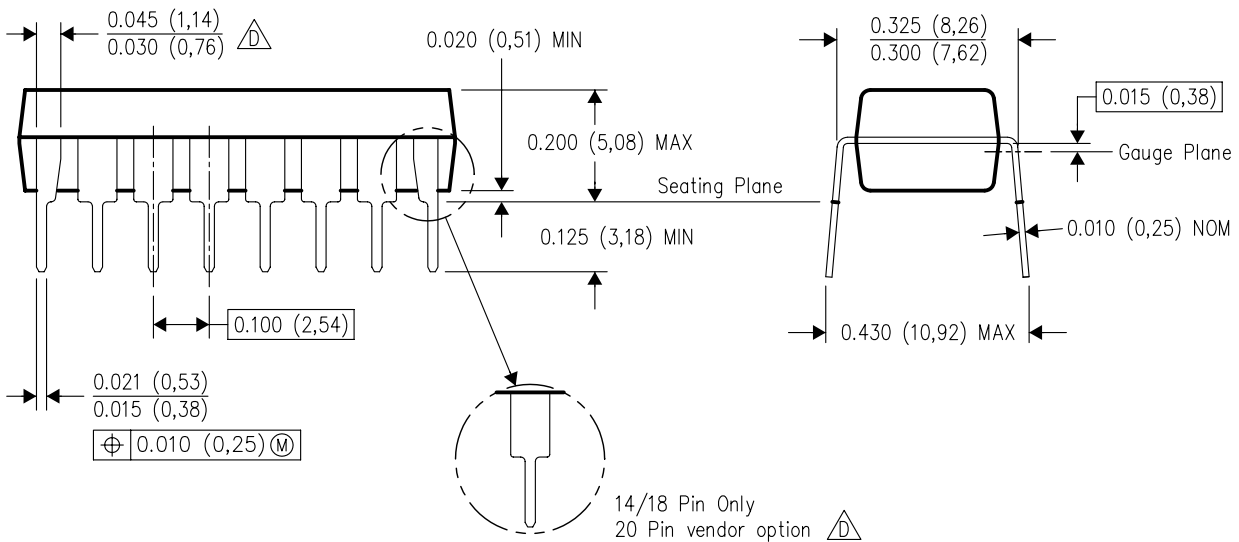
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



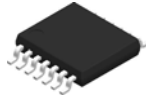
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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