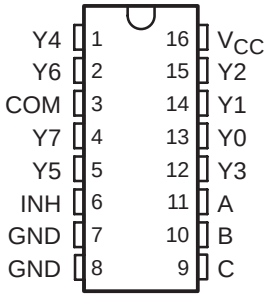
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 5.5-V $V_{CC}$ Operation**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**D, DW, OR PW PACKAGE**
**(TOP VIEW)**




## description/ordering information

This 8-channel CMOS analog multiplexer/demultiplexer is designed for 2-V to 5.5-V $V_{CC}$ operation.

The SN74LV4051A handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

**ORDERING INFORMATION**

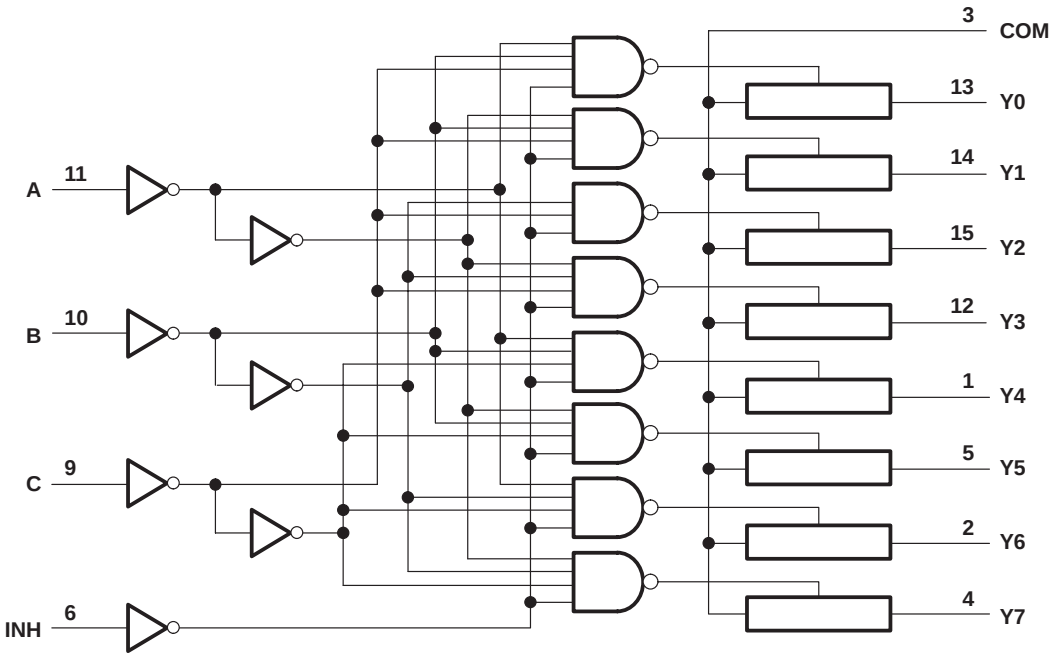
| $T_A$ | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 105°C | SOIC − D | Tape and reel | SN74LV4051ATDREP | LV4051ATEP |
| | SOIC − DW | Tape and reel | SN74LV4051ATDWREP§ | LV4051ATEP |
| | TSSOP − PW | Tape and reel | SN74LV4051ATPWREP | L4051EP |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
§ Product Preview.

**FUNCTION TABLE**

| INPUTS | | | | ON CHANNEL |
|---|---|---|---|---|
| INH | C | B | A | |
| L | L | L | L | Y0 |
| L | L | L | H | Y1 |
| L | L | H | L | Y2 |
| L | L | H | H | Y3 |
| L | H | L | L | Y4 |
| L | H | L | H | Y5 |
| L | H | H | L | Y6 |
| L | H | H | H | Y7 |
| H | X | X | X | None |

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7.0 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7.0 V
Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −20 mA
I/O diode current, $I_{IOK}$ ($V_{IO}$ < 0) . . . . . −50 mA
Switch through current, $I_T$ ($V_{IO}$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 73°C/W
DW package . . . . . 57°C/W
PW package . . . . . 108°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2‡ | 5.5 | V |
| $V_{IH}$ | High-level input voltage, control inputs | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage, control inputs | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | |
| $V_I$ | Control input voltage | | 0 | 5.5 | V |
| $V_{IO}$ | Input/output voltage | | 0 | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | −40 | 105 | °C |

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $r_{on}$ | On-state switch resistance | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$, (see Figure 1) | 2.3 V | | 38 | 180 | | 225 | Ω |
| | | | 3 V | | 30 | 150 | | 190 | |
| | | | 4.5 V | | 22 | 75 | | 100 | |
| $r_{on(p)}$ | Peak on-state resistance | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ to GND, $V_{INH}$ = $V_{IL}$ | 2.3 V | | 113 | 500 | | 600 | Ω |
| | | | 3 V | | 54 | 180 | | 225 | |
| | | | 4.5 V | | 31 | 100 | | 125 | |
| $\Delta r_{on}$ | Difference in on-state resistance between switches | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ to GND, $V_{INH}$ = $V_{IL}$ | 2.3 V | | 2.1 | 30 | | 40 | Ω |
| | | | 3 V | | 1.4 | 20 | | 30 | |
| | | | 4.5 V | | 1.3 | 15 | | 20 | |
| $I_I$ | Control input current | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{S(off)}$ | Off-state switch leakage current | $V_I$ = $V_{CC}$ and $V_O$ = GND, or $V_I$ = GND and $V_O$ = $V_{CC}$, $V_{INH}$ = $V_{IH}$, (see Figure 2) | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{S(on)}$ | On-state switch leakage current | $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$ (see Figure 3) | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | | | 20 | µA |
| $C_{IC}$ | Control input capacitance | f = 10 MHz | 3.3 V | | 2 | | | | pF |
| $C_{IS}$ | Common terminal capacitance | | 3.3 V | | 23.4 | | | | pF |
| $C_{OS}$ | Switch terminal capacitance | | 3.3 V | | 5.7 | | | | pF |
| $C_F$ | Feedthrough capacitance | | 3.3 V | | 0.5 | | | | pF |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 15 pF, (see Figure 4) | | 1.9 | 10 | | 16 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 6.6 | 18 | | 23 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 7.4 | 18 | | 23 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 50 pF, (see Figure 5) | | 3.8 | 12 | | 18 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 7.8 | 28 | | 35 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 11.5 | 28 | | 35 | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 15 pF, (see Figure 4) | | 1.2 | 6 | | 10 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 4.7 | 12 | | 15 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 5.7 | 12 | | 15 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 50 pF, (see Figure 4) | | 2.5 | 9 | | 12 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 5.5 | 20 | | 25 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 8.8 | 20 | | 25 | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 15 pF, (see Figure 4) | | 0.6 | 4 | | 7 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 3.5 | 8 | | 10 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 15 pF, (see Figure 5) | | 4.4 | 8 | | 10 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 50 pF, (see Figure 4) | | 1.5 | 6 | | 8 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 4 | 14 | | 18 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 50 pF, (see Figure 5) | | 6.2 | 14 | | 18 | ns |

### analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

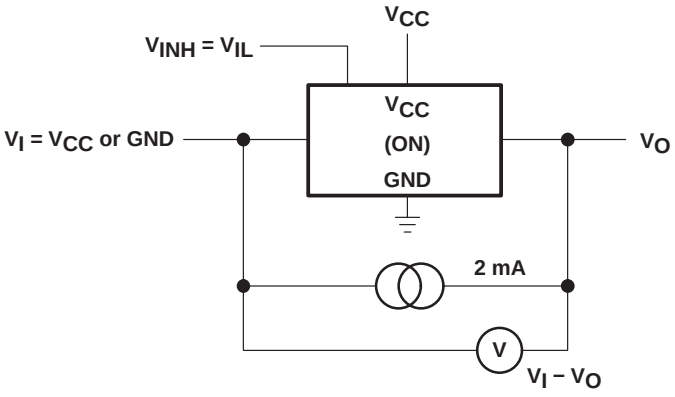
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Frequency response (switch on) | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave) (see Note 5 and Figure 6) | | 2.3 V | | 20 | | MHz |
| | | | | | 3 V | | 25 | | |
| | | | | | 4.5 V | | 35 | | |
| Crosstalk (control input to signal output) | INH | COM or Yn | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (square wave) (see Figure 7) | | 2.3 V | | 20 | | mV |
| | | | | | 3 V | | 35 | | |
| | | | | | 4.5 V | | 60 | | |
| Feedthrough attenuation (switch off) | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (see Note 6 and Figure 8) | | 2.3 V | | −45 | | dB |
| | | | | | 3 V | | −45 | | |
| | | | | | 4.5 V | | −45 | | |
| Sine-wave distortion | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave) (see Figure 9) | $V_I$ = 2 $V_{p-p}$ | 2.3 V | | 0.1 | | % |
| | | | | $V_I$ = 2.5 $V_{p-p}$ | 3 V | | 0.1 | | |
| | | | | $V_I$ = 4 $V_{p-p}$ | 4.5 V | | 0.1 | | |

NOTES: 5. Adjust $f_{in}$ voltage to obtain 0-dBm output. Increase $f_{in}$ frequency until dB meter reads −3 dB.
6. Adjust $f_{in}$ voltage to obtain 0-dBm input.

### operating characteristics, $V_{CC}$ = 3.3 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 5.9 | pF |

## PARAMETER MEASUREMENT INFORMATION




$$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}}\ \Omega$$

**Figure 1. On-State Resistance Test Circuit**

## PARAMETER MEASUREMENT INFORMATION

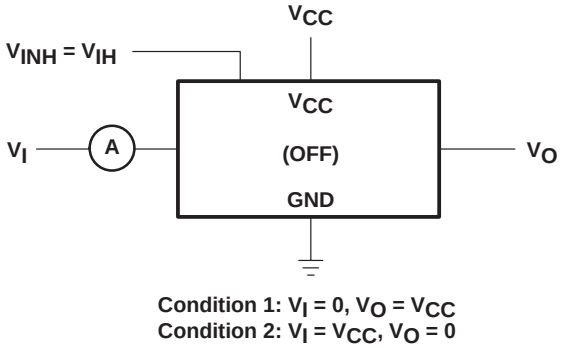



**Figure 2. Off-State Switch Leakage-Current Test Circuit**

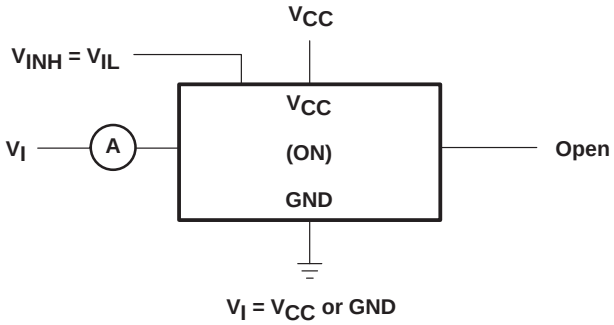



**Figure 3. On-State Switch Leakage-Current Test Circuit**

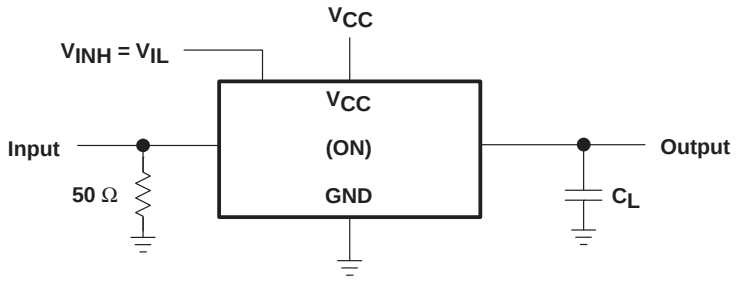
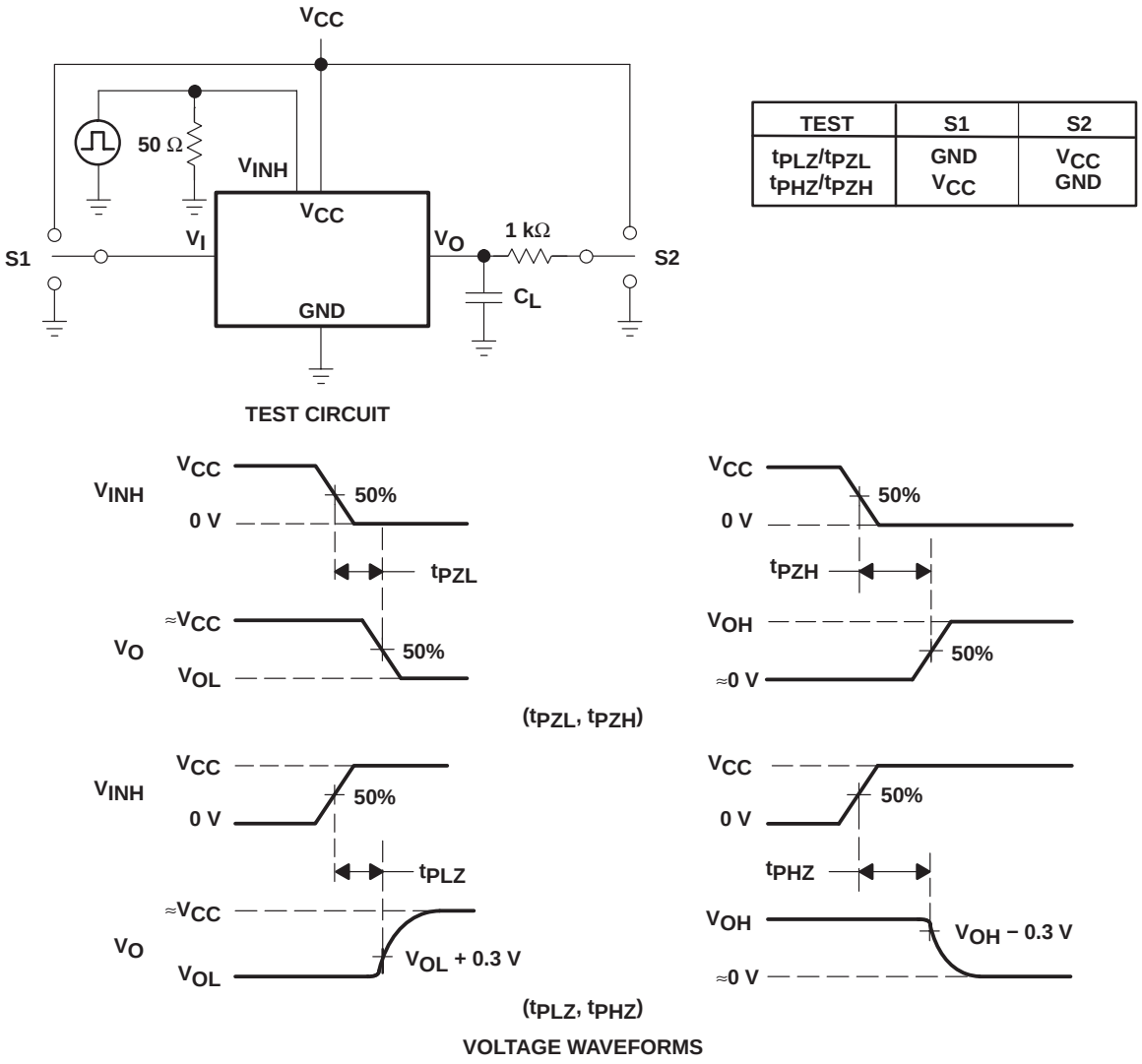


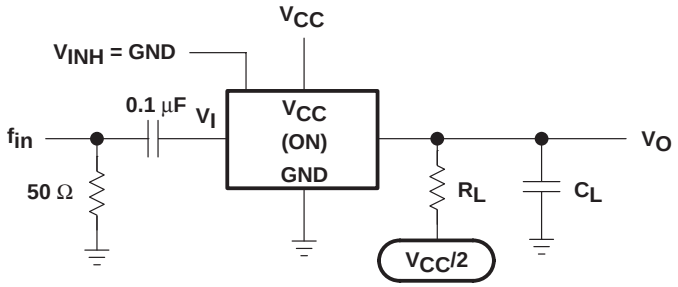

**Figure 4. Propagation Delay Time, Signal Input to Signal Output**

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 | S2 |
|---|---|---|
| $t_{PLZ}/t_{PZL}$ | GND | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | $V_{CC}$ | GND |

**Figure 5. Switching Time ($t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$), Control to Signal Output**




NOTE A: $f_{in}$ is a sine wave.

**Figure 6. Frequency Response (Switch On)**

## PARAMETER MEASUREMENT INFORMATION

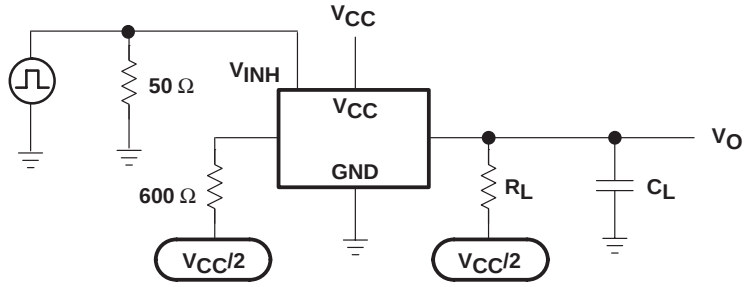



**Figure 7. Crosstalk (Control Input, Switch Output)**

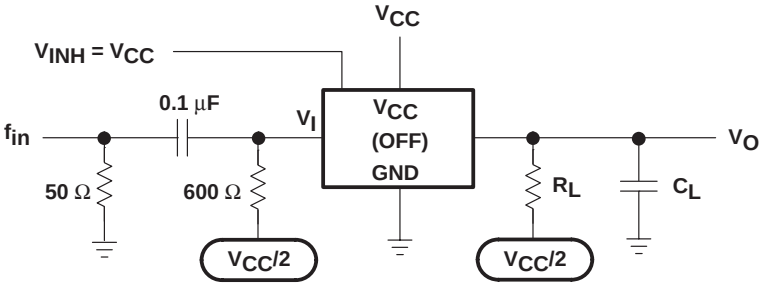



**Figure 8. Feedthrough Attenuation (Switch Off)**

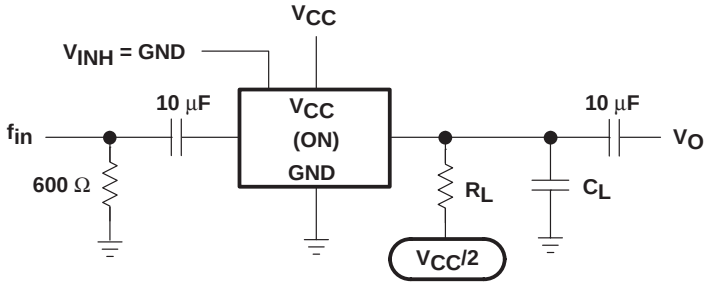



**Figure 9. Sine-Wave Distortion**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV4051ATDREP | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LV4051ATEP |
| SN74LV4051ATDREP.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LV4051ATEP |
| SN74LV4051ATPWREP | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051EP |
| SN74LV4051ATPWREP.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051EP |
| V62/03664-01XE | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051EP |
| V62/03664-01YE | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LV4051ATEP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN74LV4051A-EP :**

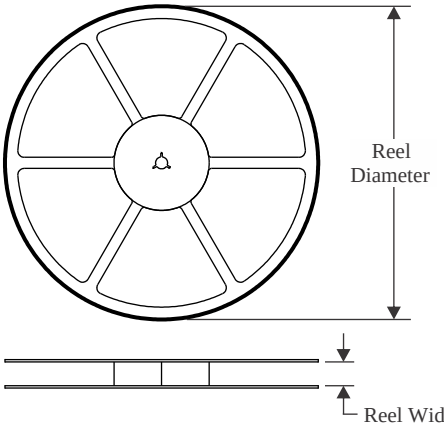
- Catalog : SN74LV4051A
- Automotive : SN74LV4051A-Q1

NOTE: Qualified Version Definitions:

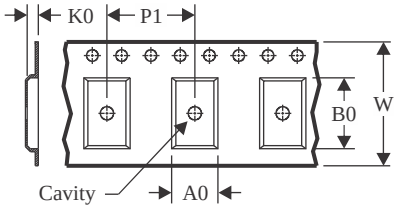
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

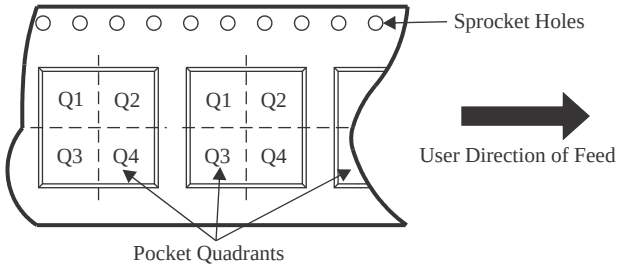



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

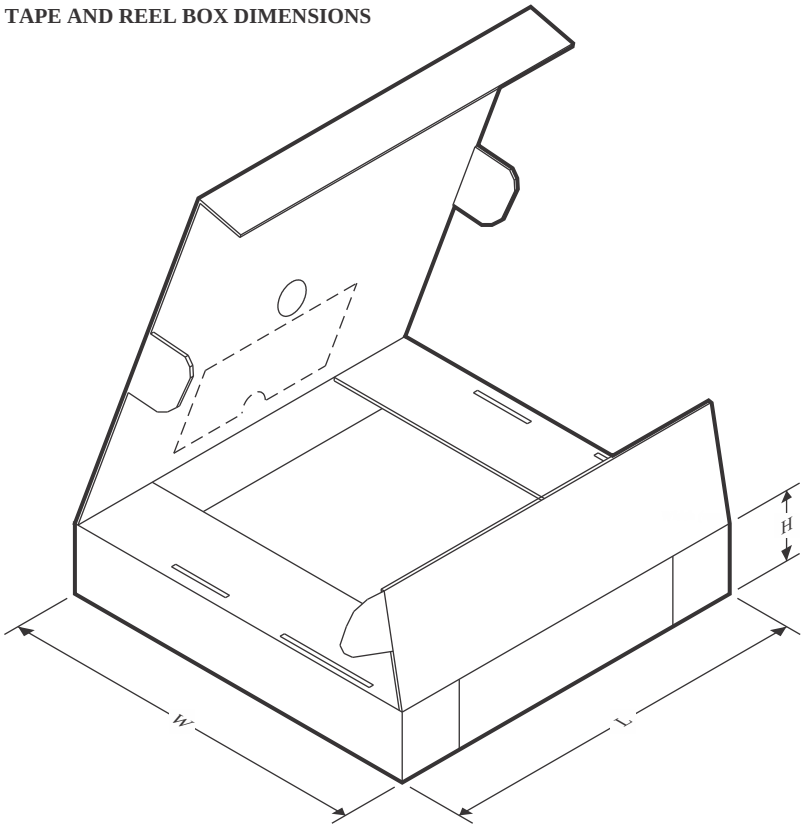
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV4051ATDREP | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV4051ATPWREP | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

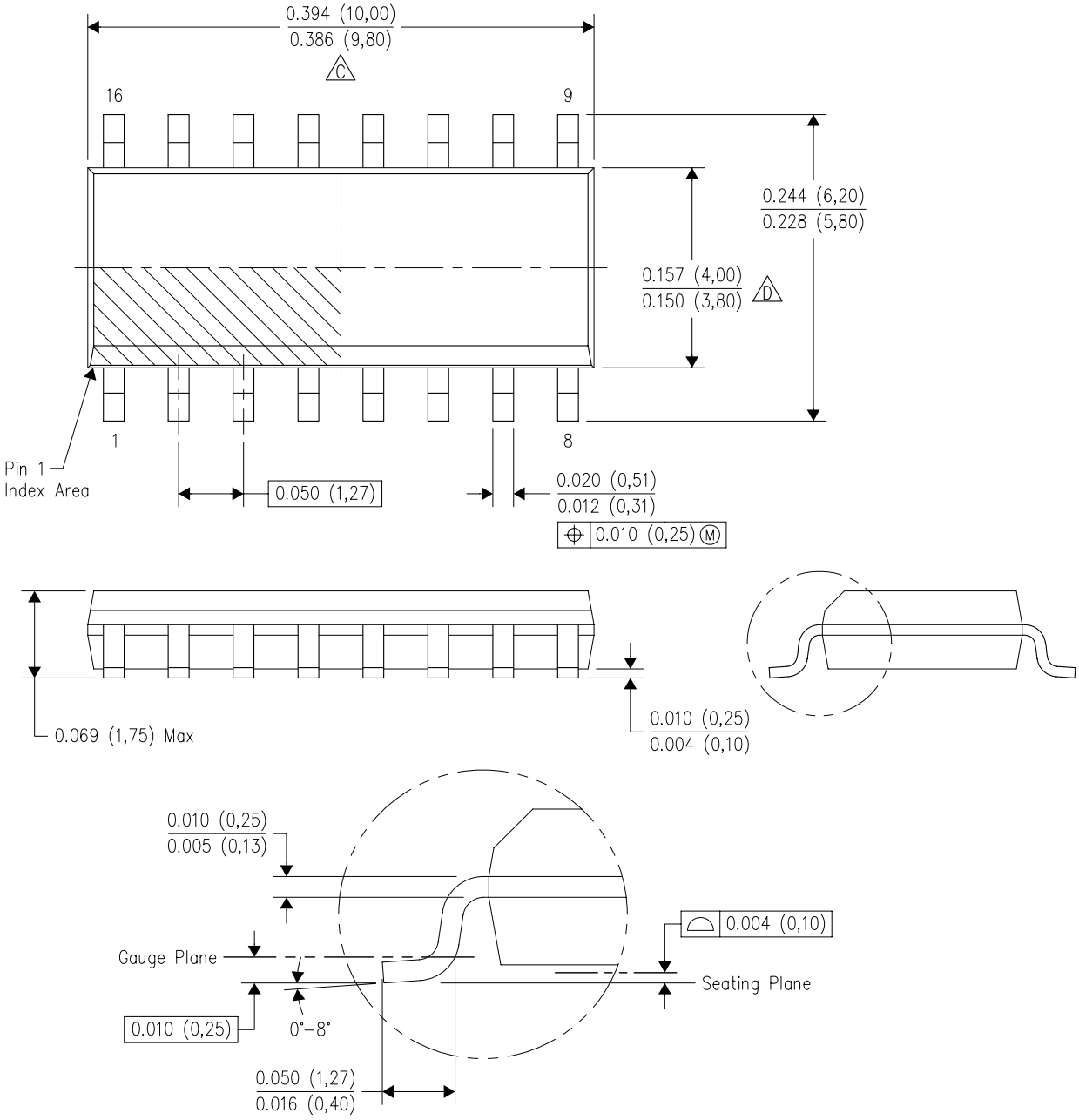
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV4051ATDREP | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV4051ATPWREP | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



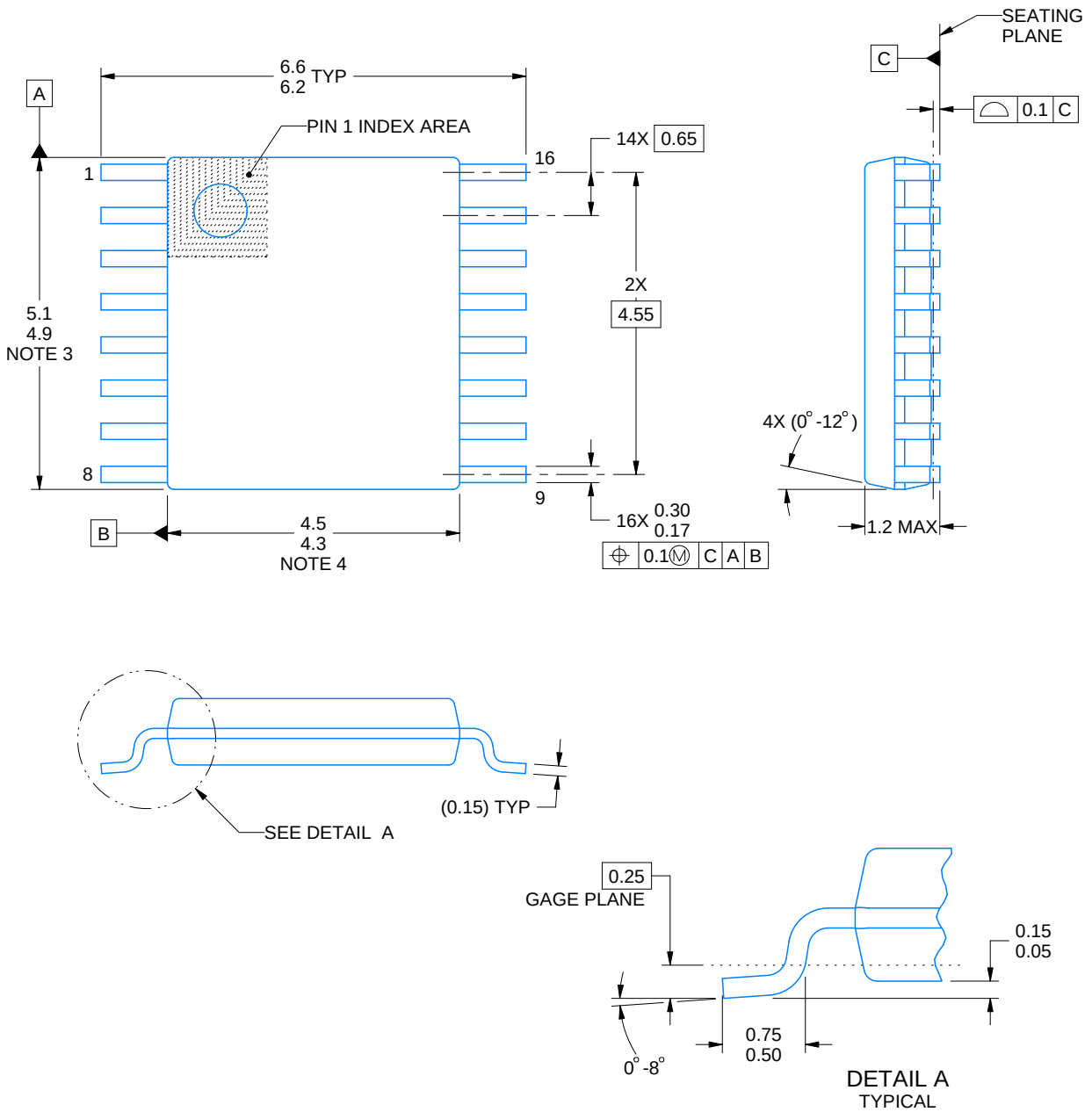

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## PW0016A

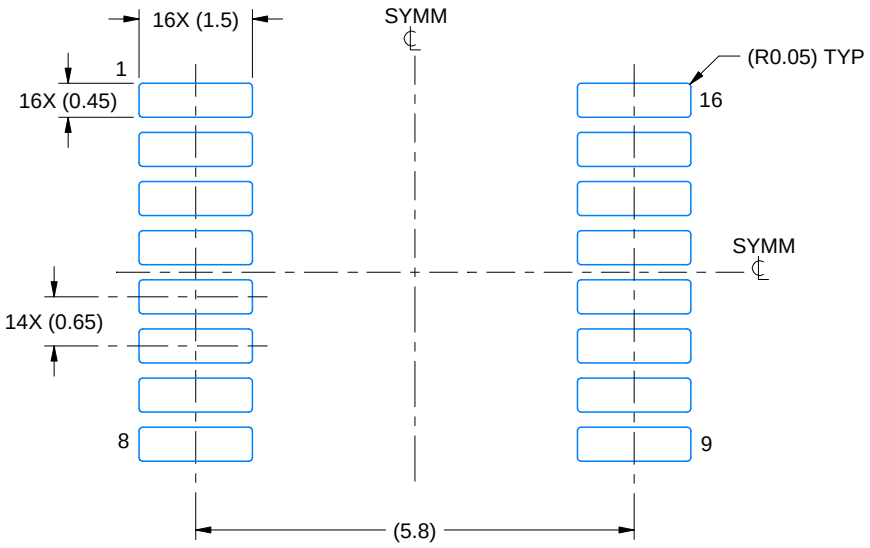
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

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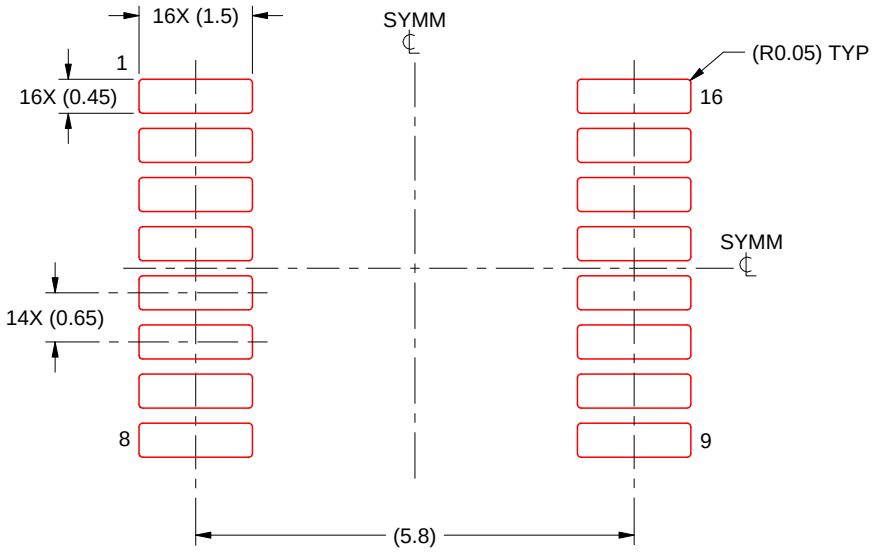
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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