

SN74LV4051A 8 チャンネル アナログ マルチプレクサ / デマルチプレクサ

1 特長

- 1.65V～5.5V の V_{CC} で動作
- すべてのポートで混在モード電圧動作をサポート
- 高いオン / オフ出力電圧比
- スイッチ間の低いクロストーク
- スイッチの個別制御
- 非常に低い入力電流
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン モデル (A115-A)
 - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- [テレコミュニケーション](#)
- [eCall](#) (車載用緊急通報システム)
- [インフォテインメント](#)

3 概要

SN74LV4051A 8 チャンネルの CMOS アナログ マルチプレクサおよびデマルチプレクサは、1.65V ～ 5.5V の V_{CC} で動作するように設計されています。

SN74LV4051A は、アナログとデジタルの両方の信号を扱います。各スイッチは、最大 5.5V (ピーク) の振幅の信号をどちらの方向にも伝送できます。

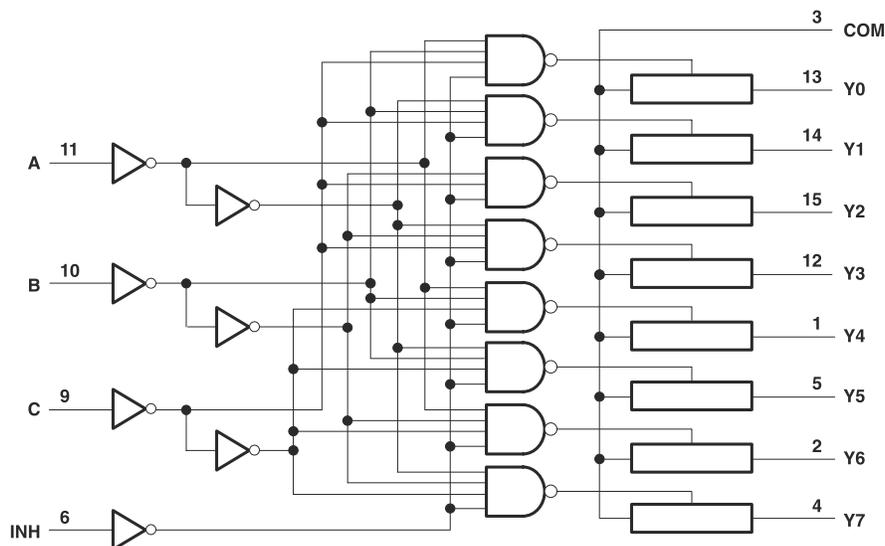
信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN74LV4051A	PW (TSSOP, 16)	5mm × 6.4 mm
	D (SOIC, 16)	9.9mm × 6 mm
	RGY (VQFN, 16)	4mm × 3.5 mm
	DYY (SOT-23-THIN, 16)	4.2 mm × 3.26mm

(1) 詳細については、[セクション 10](#) を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)



Table of Contents

1 特長	1	7 Detailed Description	15
2 アプリケーション	1	7.1 Overview.....	15
3 概要	1	7.2 Functional Block Diagram.....	15
4 Pin Configuration and Functions	3	7.3 Feature Description.....	15
5 Specifications	4	7.4 Device Functional Modes.....	15
5.1 Absolute Maximum Ratings.....	4	8 Device and Documentation Support	16
5.2 ESD Ratings.....	4	8.1 Documentation Support.....	16
5.3 Thermal Information: SN74LV4051A.....	5	8.2 ドキュメントの更新通知を受け取る方法.....	16
5.4 Recommended Operating Conditions.....	6	8.3 サポート・リソース.....	16
5.5 Electrical Characteristics.....	6	8.4 Trademarks.....	16
5.6 Timing Characteristics $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	8	8.5 静電気放電に関する注意事項.....	16
5.7 Timing Characteristics $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	8	8.6 用語集.....	16
5.8 Timing Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	9	9 Revision History	16
5.9 AC Characteristics.....	9	10 Mechanical, Packaging, and Orderable Information	17
5.10 Typical Characteristics.....	11		
6 Parameter Measurement Information	12		

4 Pin Configuration and Functions

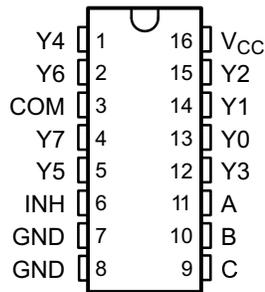


図 4-1. D, PW, or DYY Packages, 16-Pin SOIC, TSSOP, or SOT-23-THIN (Top View)

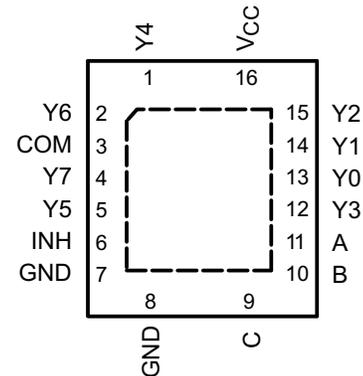


図 4-2. RGY Package 16-Pin VQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽²⁾	DESCRIPTION
NAME	NO.		
A	11	I	Selector line A for outputs (see セクション 7.4 for specific information)
B	10	I	Selector line B for outputs (see セクション 7.4 for specific information)
C	9	I	Selector line C for outputs (see セクション 7.4 for specific information)
COM	3	O/I ⁽¹⁾	Output/Input of mux
GND	7, 8	—	Ground
INH	6	I ⁽¹⁾	Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off.
Y0	13	I/O ⁽¹⁾	Input/Output to mux
Y1	14	I/O ⁽¹⁾	Input/Output to mux
Y2	15	I/O ⁽¹⁾	Input/Output to mux
Y3	12	I/O ⁽¹⁾	Input/Output to mux
Y4	1	I/O ⁽¹⁾	Input/Output of mux
Y5	5	I/O ⁽¹⁾	Input/Output to mux
Y6	2	I/O ⁽¹⁾	Input/Output to mux
Y7	4	I/O ⁽¹⁾	Input/Output to mux
V _{CC}	16	—	Device power

- (1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).
- (2) I = inputs, O = outputs

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7.0	V
V _I	Logic input voltage range		-0.5	7.0	V
V _{IO}	Switch I/O voltage range ^{(2) (3)}		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-20		mA
I _{IOK}	Switch IO diode clamp current	V _{IO} < 0 or V _{IO} > V _{CC}	-50	50	mA
I _T	Switch continuous current	V _{IO} = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5 V maximum

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4051A

THERMAL METRIC ⁽¹⁾		SN74LV4051A	SN74LV4051A	SN74LV4051A	SN74LV4051A	UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	140.2	89.4	199.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.0	72.6	89.7	121.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.6	98.7	65.4	129	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	31.3	13.4	25.0	24.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.7	97.3	65.2	126.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	48.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	1 ⁽²⁾		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 1.65		5.5	V
		V _{CC} = 2 V	1.5	5.5	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	5.5	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	5.5	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 1.65	0	0.4	V
		V _{CC} = 2 V	0	0.5	
		V _{CC} = 2.3 V to 2.7 V	0	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	0	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	0	V _{CC} × 0.3	
V _I	Logic control input voltage	0		5.5	V
V _{IO}	Switch input or output voltage	0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	ns/V
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Ambient temperature	–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

(2) When using a V_{CC} of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	1.65 V		60 150	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	–40°C to 85°C	1.65 V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	–40°C to 125°C	1.65 V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	2.3 V		38 180	Ω
			–40°C to 85°C			225	
			–40°C to 125°C			225	
			25°C	3 V		30 150	Ω
			–40°C to 85°C			190	
			–40°C to 125°C			190	
			25°C	4.5 V		22 75	Ω
			–40°C to 85°C			100	
			–40°C to 125°C			100	
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V		220 600	Ω

5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65 V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 125°C	1.65 V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3 V		113	500	Ω
			–40°C to 85°C				600	
			–40°C to 125°C				600	
			25°C	3 V		54	180	Ω
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	4.5 V		31	100	Ω
			–40°C to 85°C				125	
			–40°C to 125°C				125	
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V		3	40	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65 V			50	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65 V			50	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3 V		2.1	30	Ω
			–40°C to 85°C				40	
			–40°C to 125°C				40	
			25°C	3 V		1.4	20	Ω
			–40°C to 85°C				30	
			–40°C to 125°C				30	
			25°C	4.5 V		1.3	15	Ω
			–40°C to 85°C				20	
			–40°C to 125°C				20	
I _{IH} I _{IL}	Control input current	V _I = 5.5 V or GND	25°C	0 to 5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH}	25°C	5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure4)	25°C	5.5 V			0.1	μA
			–40°C to 85°C				1	
			–40°C to 125°C				2	
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0 V	25°C	5.5 V		0.01		μA
			–40°C to 85°C				20	
			–40°C to 125°C				40	

5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _{IC}	Control input capacitance	f = 10 MHz	25°C	3.3 V		2		pF
C _{OS}	Switch terminal capacitance	f = 10 MHz	25°C	3.3 V		5		pF
C _{IS}	Common terminal capacitance	f = 10 MHz	25°C	3.3 V		23		pF
C _{OS(on)}	Common terminal ON-capacitance	f = 10 MHz	25°C	3.3 V		23		pF
C _F	Feedthrough capacitance	f = 10 MHz	25°C	3.3 V		0.5		pF
C _{PD}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	25°C	3.3 V		6		pF

5.6 Timing Characteristics V_{CC} = 2.5 V ± 0.2 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15 pF	25°C		1.9	10	ns
					-40°C to 85°C			16	
					-40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15 pF	25°C		6.6	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15 pF	25°C		7.4	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50 pF	25°C		3.8	12	ns
					-40°C to 85°C			18	
					-40°C to 125°C			20	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50 pF	25°C		7.8	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50 pF	25°C		11.5	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15 pF	25°C		1.2	6	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15 pF	25°C		4.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	

5.7 Timing Characteristics $V_{CC} = 3.3 V \pm 0.3 V$ (続き)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15 \text{ pF}$	25°C		5.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50 \text{ pF}$	25°C		2.5	9	ns
					-40°C to 85°C			12	
					-40°C to 125°C			14	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50 \text{ pF}$	25°C		5.5	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50 \text{ pF}$	25°C		8.8	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	

5.8 Timing Characteristics $V_{CC} = 5 V \pm 0.5 V$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15 \text{ pF}$	25°C		0.6	4	ns
					-40°C to 85°C			7	
					-40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15 \text{ pF}$	25°C		3.5	8	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15 \text{ pF}$	25°C		4.4	10	ns
					-40°C to 85°C			11	
					-40°C to 125°C			12	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50 \text{ pF}$	25°C		1.5	6	ns
					-40°C to 85°C			8	
					-40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50 \text{ pF}$	25°C		4	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50 \text{ pF}$	25°C		6.2	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4051	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $F_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 7)(1)	$V_{CC} = 2.3 \text{ V}$		20	MHz
					$V_{CC} = 3 \text{ V}$		25	
					$V_{CC} = 4.5 \text{ V}$		35	
Charge Injection (control input to signal output)	INH	COM or Yn		$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $F_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 9)	$V_{CC} = 2.3 \text{ V}$		20	mV
					$V_{CC} = 3 \text{ V}$		35	
					$V_{CC} = 4.5 \text{ V}$		60	

5.9 AC Characteristics (続き)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM		C _L = 50 pF, R _L = 600 Ω, F _{in} = 1 MHz (sine wave) (see Figure 10) (2)	V _{CC} = 2.3 V		-45	dB
					V _{CC} = 3 V		-45	
					V _{CC} = 4.5 V		-45	
Crosstalk (between any switches)	COM or Yn	Yn or COM		C _L = 50 pF, R _L = 600 Ω, F _{in} = 1 MHz (sine wave) (see Figure 8)(2)	V _{CC} = 2.3 V		-45	dB
					V _{CC} = 3 V		-45	
					V _{CC} = 4.5 V		-45	
Sine-wave distortion	COM or Yn	Yn or COM		C _L = 50 pF, R _L = 10 kΩ, F _{in} = 1 kHz (sine wave) (see Figure 11)	V _I = 2 V _{p-p} V _{CC} = 2.3 V		0.1	%
					V _I = 2.5 V _{p-p} V _{CC} = 3 V		0.1	
					V _I = 4 V _{p-p} V _{CC} = 4.5 V		0.1	

5.10 Typical Characteristics

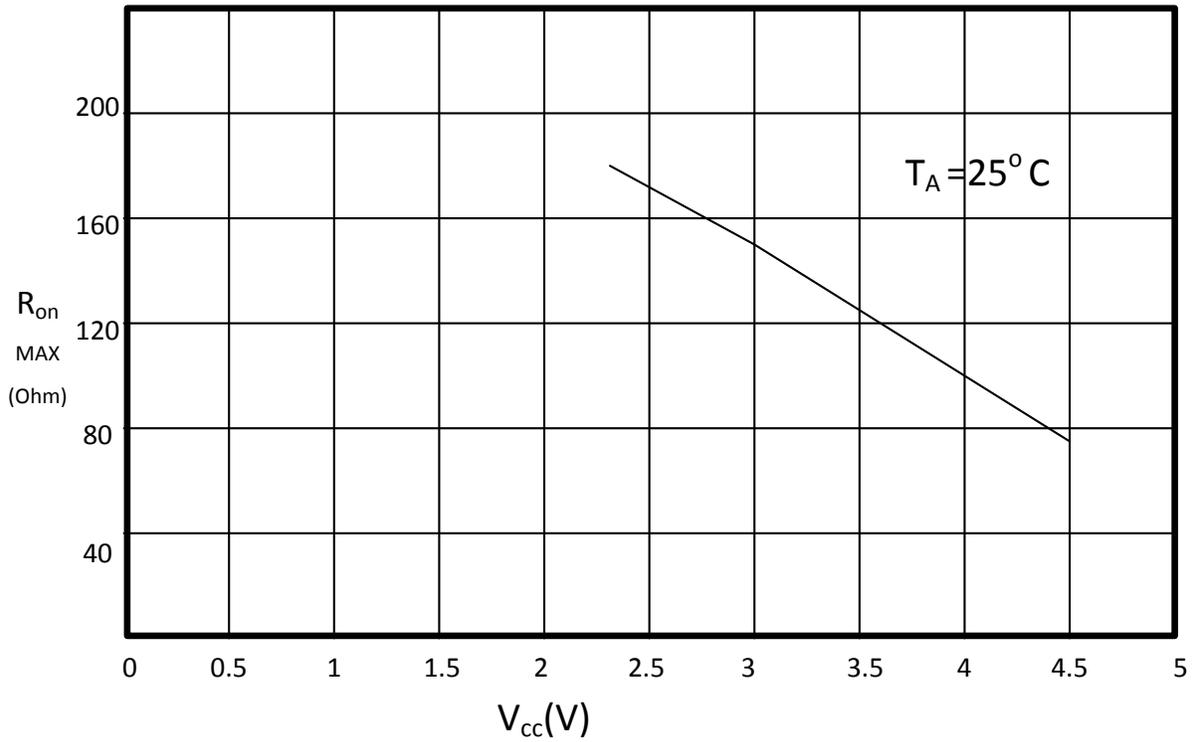


図 5-1. Plot at 25°C for V_{CC} vs Max R_{ON}

6 Parameter Measurement Information

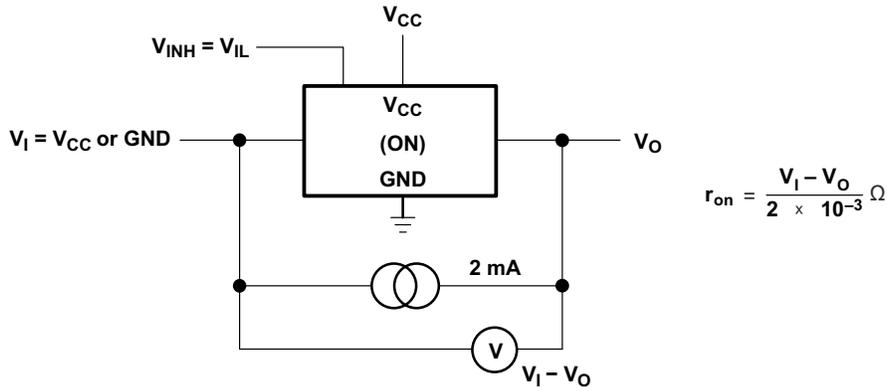
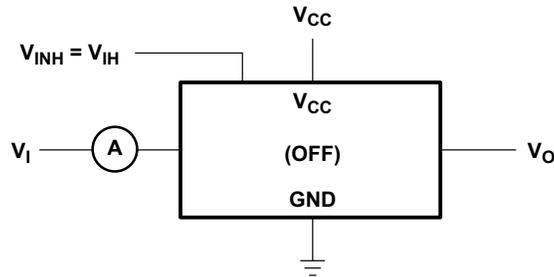


図 6-1. On-State Resistance Test Circuit



Condition 1: \$V_I = 0, V_O = V_{CC}\$
Condition 2: \$V_I = V_{CC}, V_O = 0\$

図 6-2. Off-State Switch Leakage-Current Test Circuit

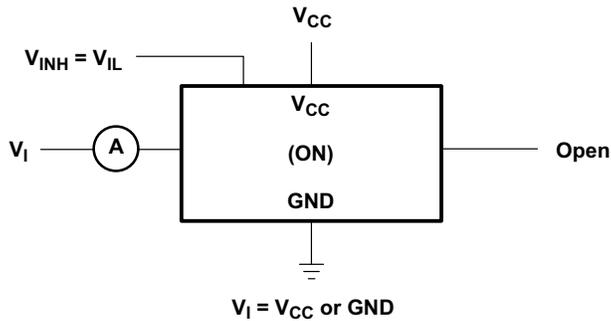


図 6-3. On-State Switch Leakage-Current Test Circuit

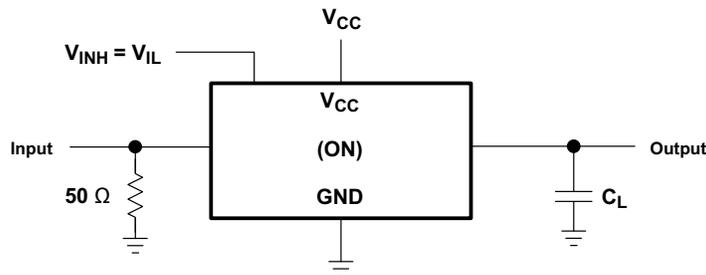
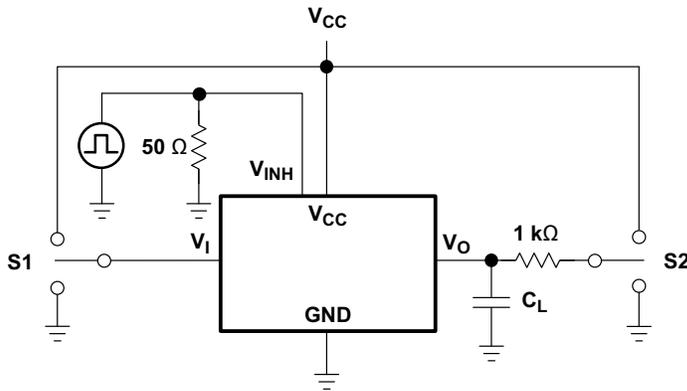
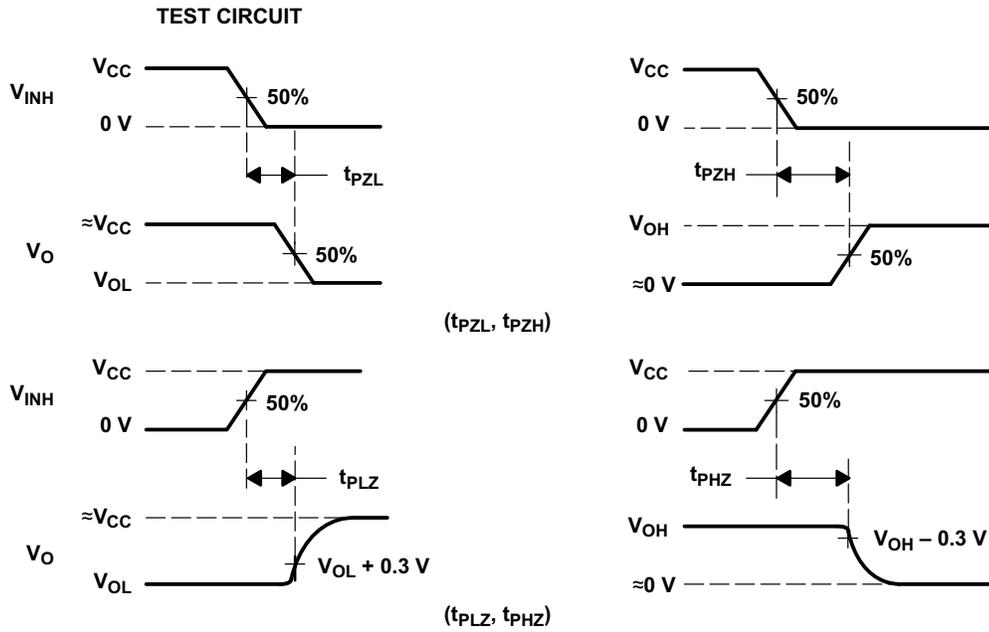


図 6-4. Propagation Delay Time, Signal Input to Signal Output

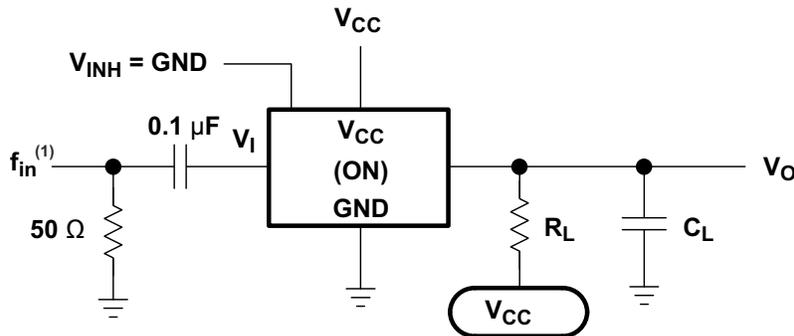


TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



A. f_{in} is a sine wave.

6-6. Frequency Response (Switch On)

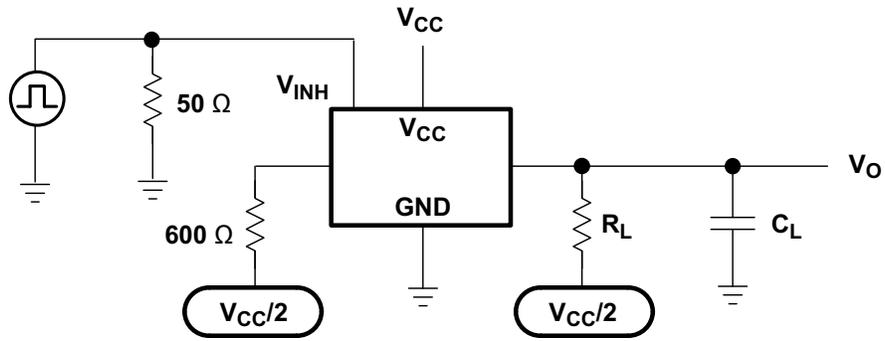


図 6-7. Crosstalk (Control Input, Switch Output)

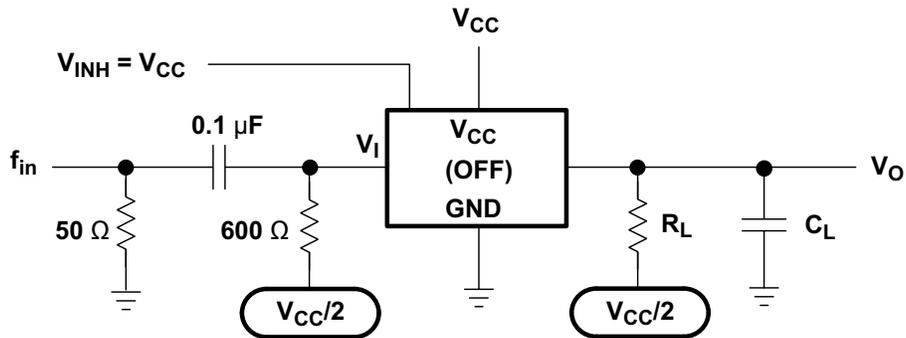


図 6-8. Feedthrough Attenuation (Switch Off)

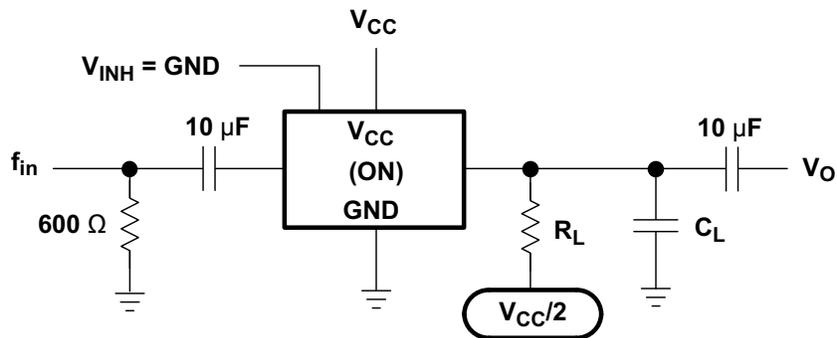


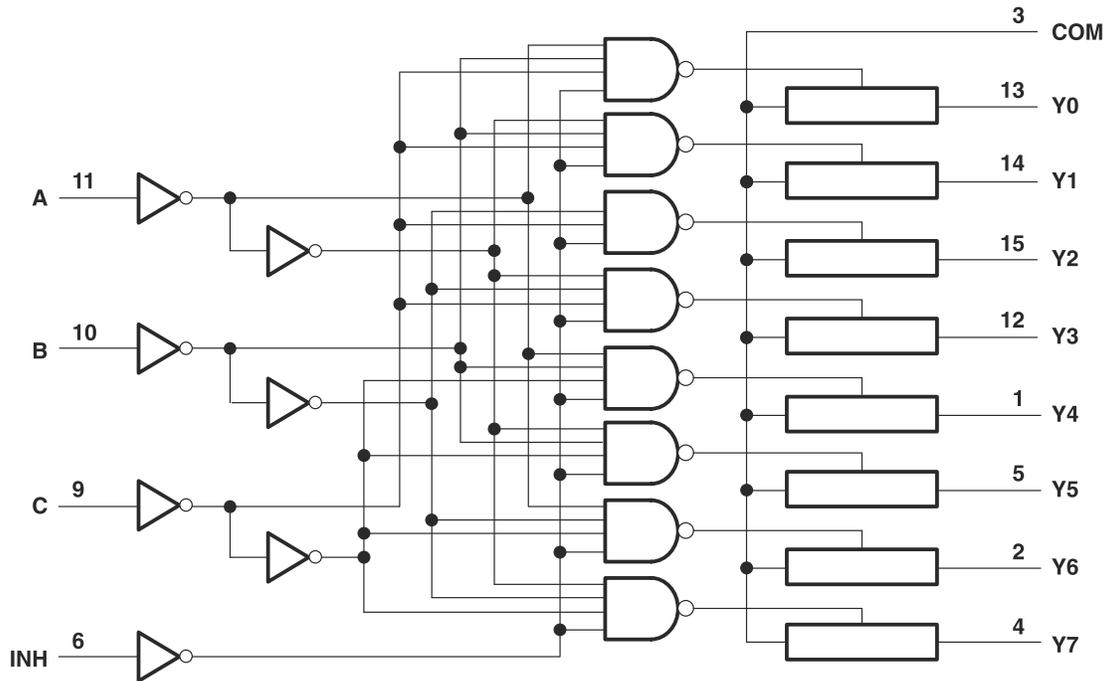
図 6-9. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SN74LV4051A device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows for the selection of one of these signals at a time for analysis or propagation.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74LV4051A device contains one 8-channel multiplexer for use in a variety of applications and can also be configured as demultiplexer by using the COM pin as an input and the Yn pins as outputs. This device is qualified to operate in the temperature range -40°C to $+85^{\circ}\text{C}$ (maximum depends on package type).

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (June 2024) to Revision K (September 2024)	Page
• DYY パッケージとサイズを追加.....	1
• Added DYY package.....	3
• Added DYY package.....	5

Changes from Revision I (September 2015) to Revision J (June 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Added new VIH and VIL Specifications at 1.65V Vcc.....	6
• Increased max ambient temperature max to 125C.....	6
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc.....	6
• Added Ron, Ron Peak, and Delta Ron Specifications at 125C.....	6
• Added Timing Specifications at 125C.....	8

Changes from Revision H (April 2005) to Revision I (September 2015)	Page
• 「製品情報」表、「ピン端子機能」表、「ESD 定格」表、「熱に関する情報」表、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• データシートから SN54LV4051A の部品番号を削除.....	1
• 「注文情報」表を削除。	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4051AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	LV4051A
SN74LV4051ADBR	NRND	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A
SN74LV4051ADBR.A	NRND	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW051A
SN74LV4051ADGVR	NRND	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A
SN74LV4051ADGVR.A	NRND	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW051A
SN74LV4051ADGVRG4	NRND	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A
SN74LV4051ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051A
SN74LV4051ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4051A
SN74LV4051ADYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051
SN74LV4051ADYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4051
SN74LV4051AN	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4051AN
SN74LV4051AN.A	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LV4051AN
SN74LV4051ANS	NRND	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A
SN74LV4051ANS.A	NRND	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV4051A
SN74LV4051ANSR	NRND	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A
SN74LV4051ANSR.A	NRND	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV4051A
SN74LV4051APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW051A
SN74LV4051APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LW051A
SN74LV4051APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW051A
SN74LV4051APWRG4	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW051A
SN74LV4051ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A
SN74LV4051ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW051A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

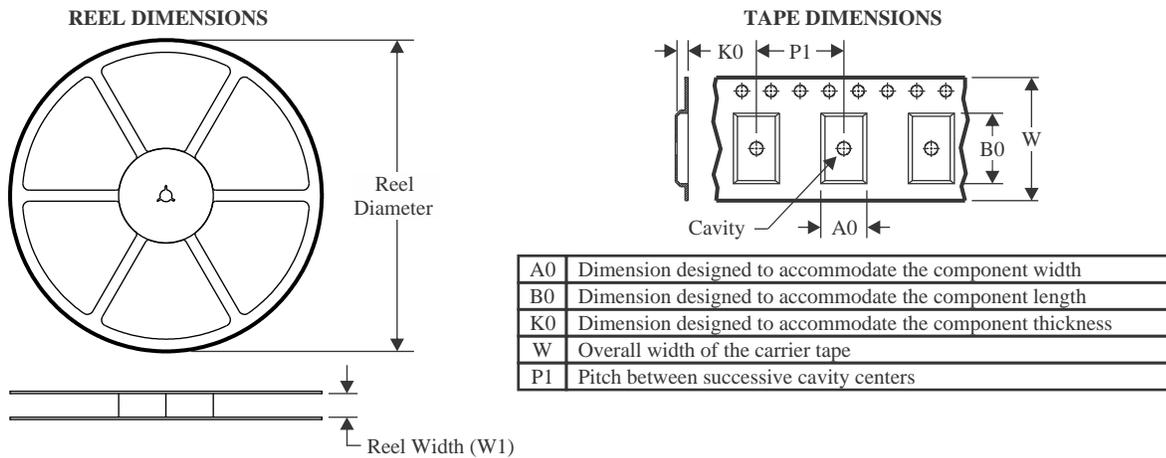
OTHER QUALIFIED VERSIONS OF SN74LV4051A :

● Automotive : [SN74LV4051A-Q1](#)

● Enhanced Product : [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4051ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4051ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4051ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4051ADYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74LV4051ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4051ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LV4051ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LV4051ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LV4051ADYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74LV4051ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LV4051APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4051APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV4051ARGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4051AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4051ANS	NS	SOP	16	50	530	10.5	4000	4.1
SN74LV4051ANS.A	NS	SOP	16	50	530	10.5	4000	4.1

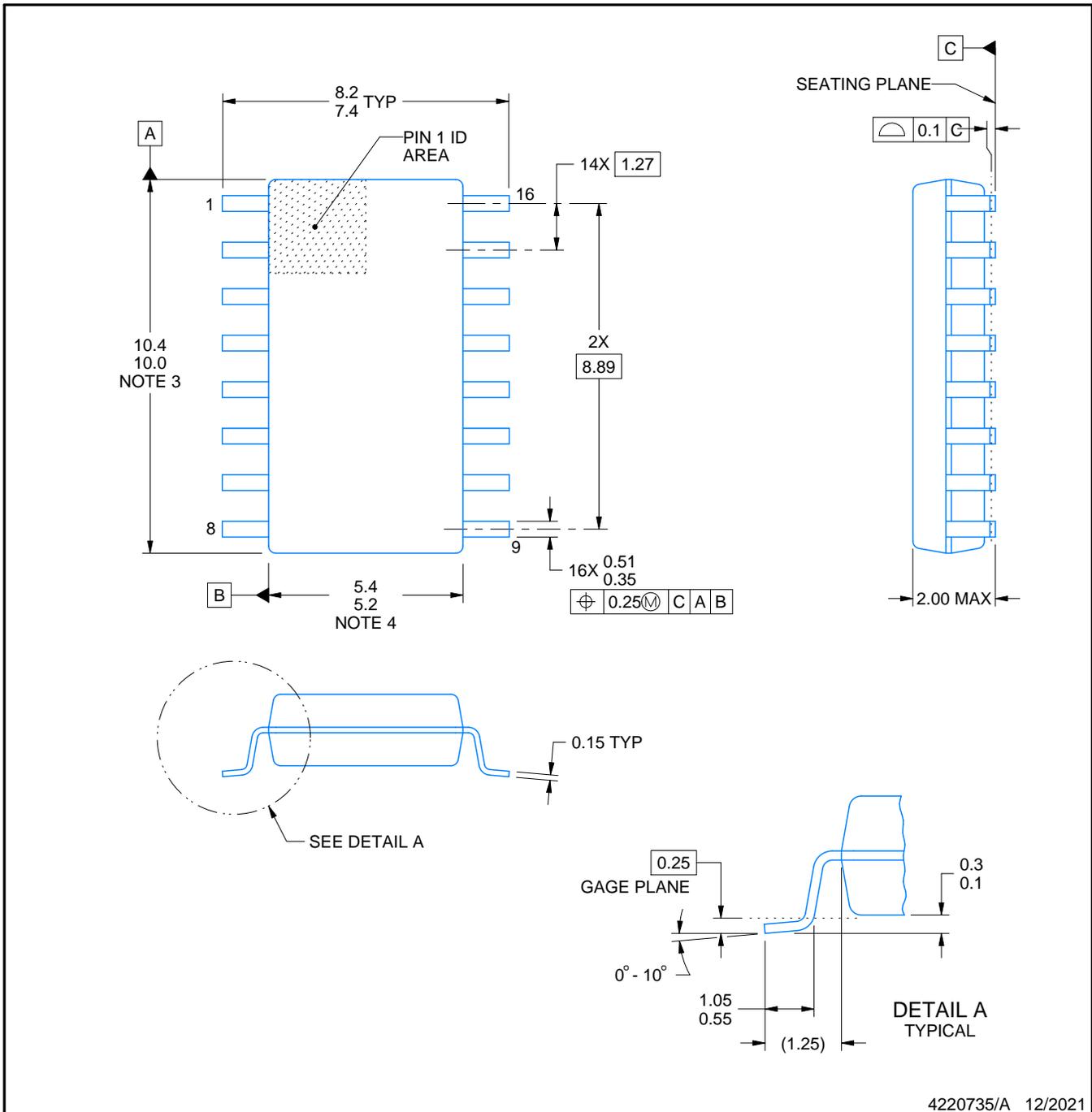


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

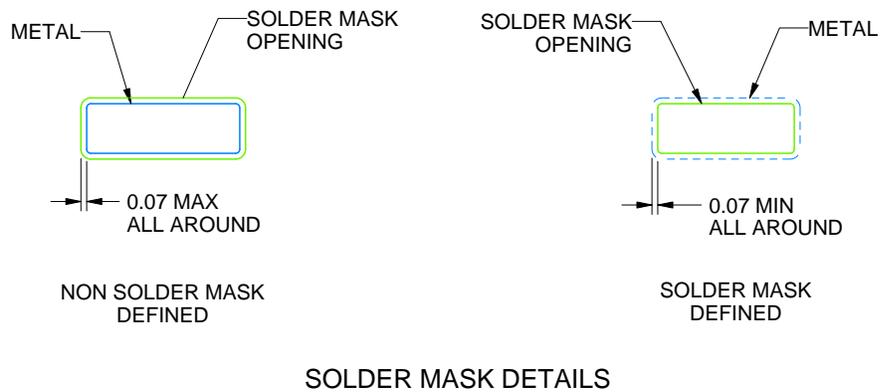
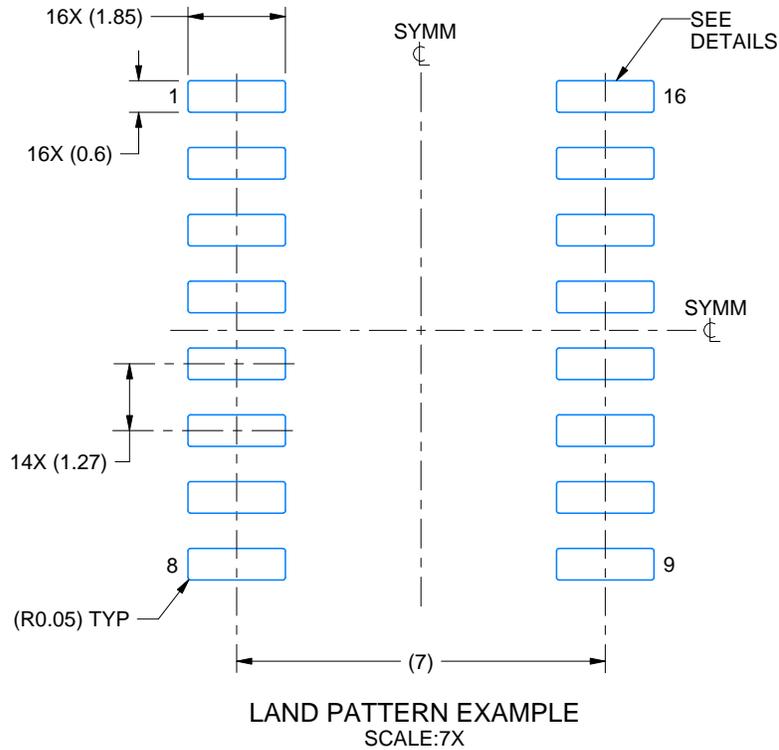
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

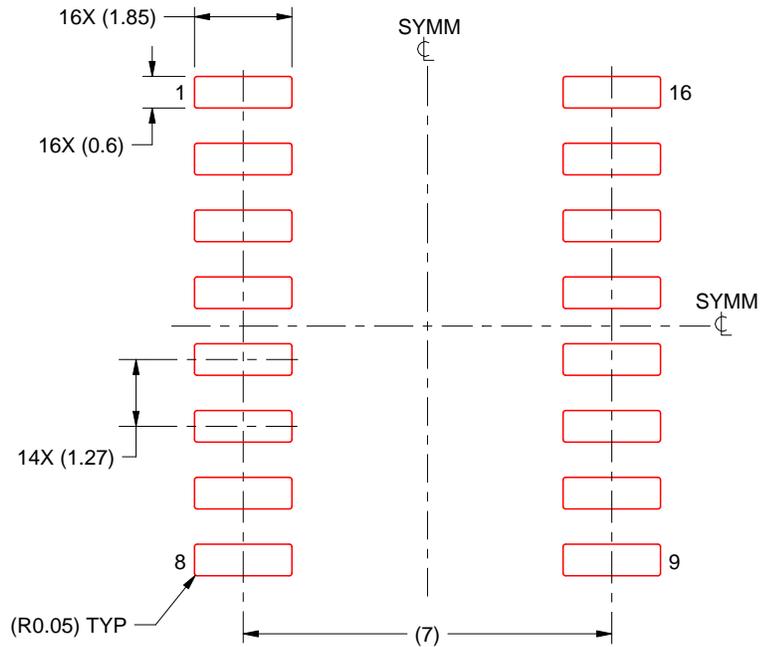
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

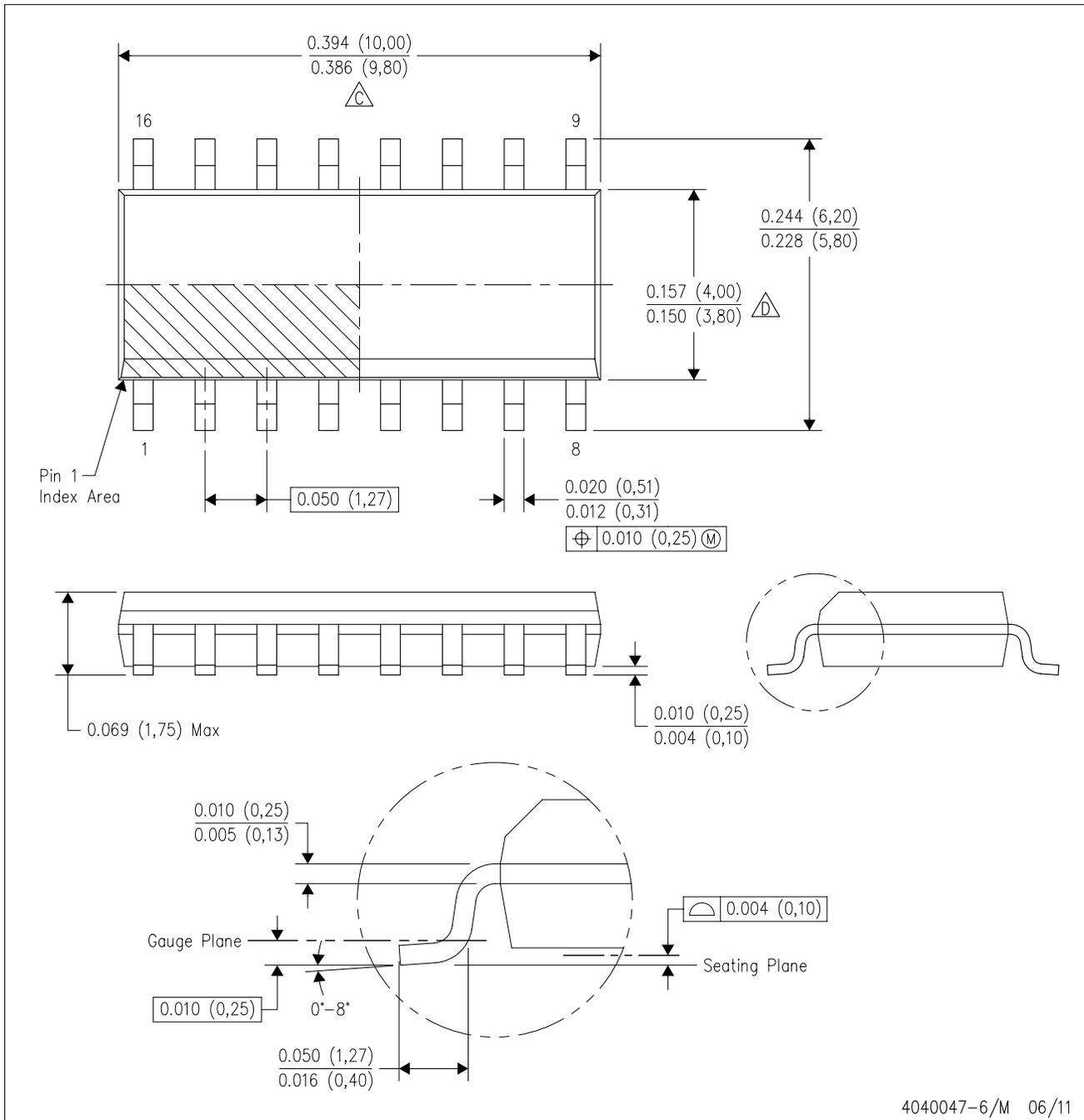
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

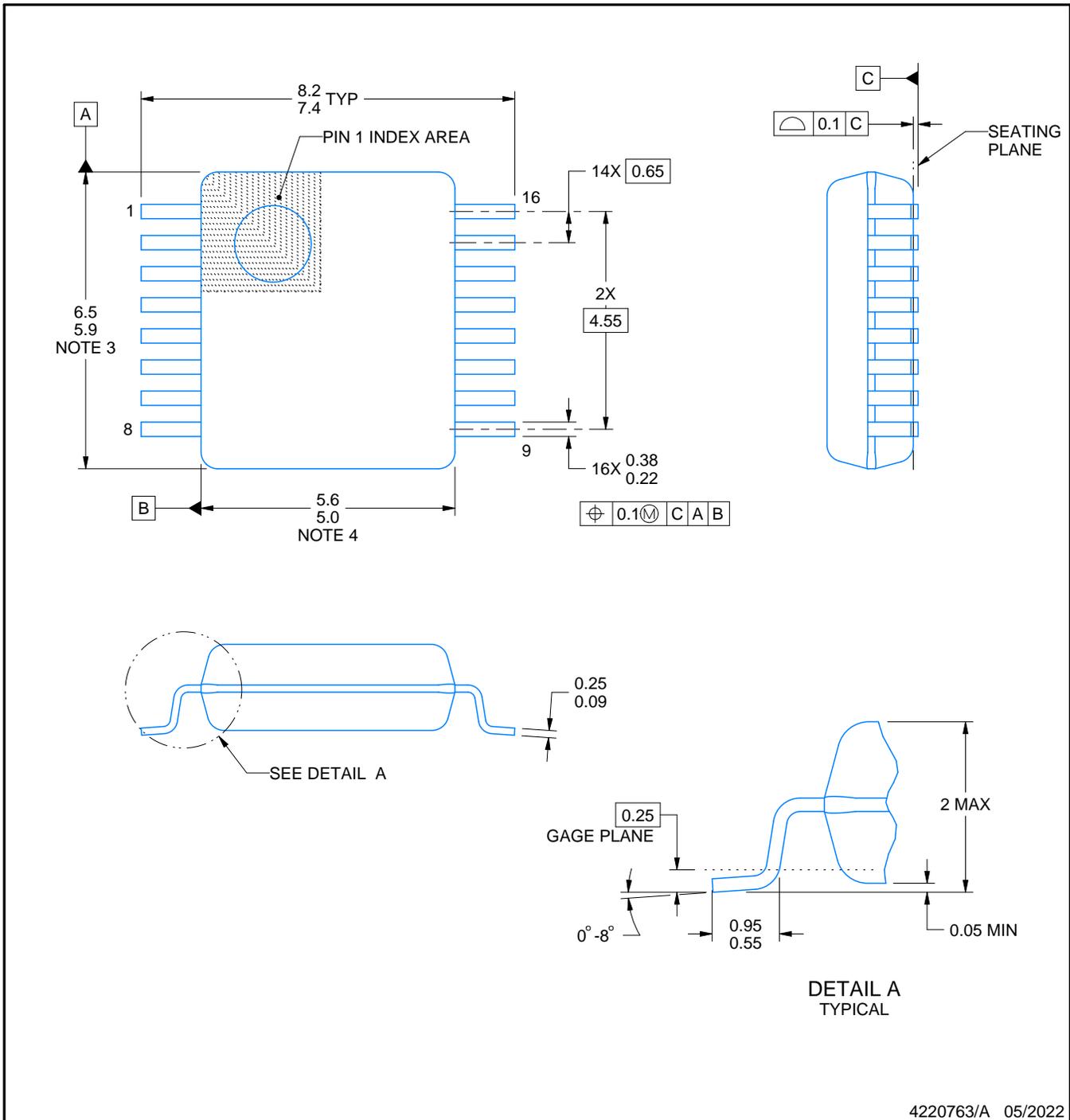
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

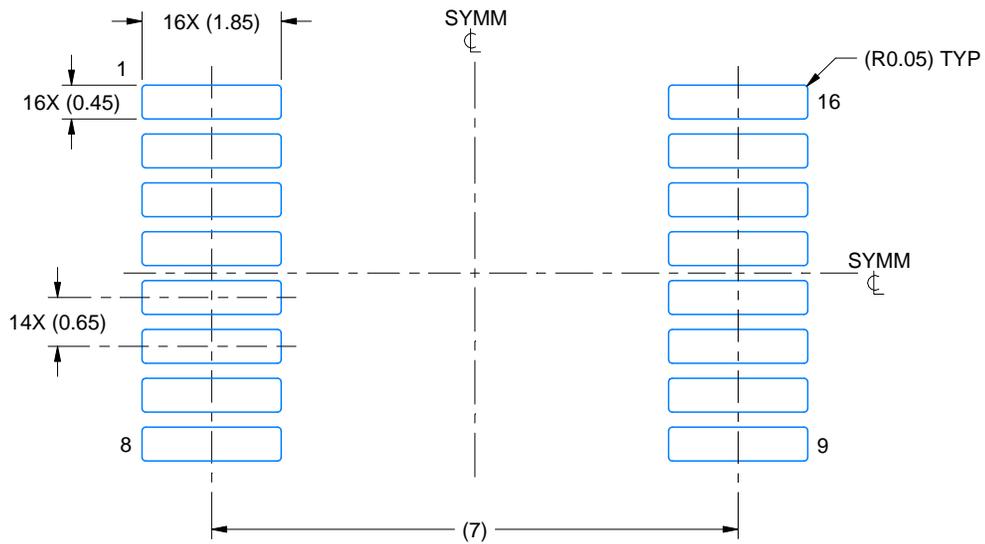
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

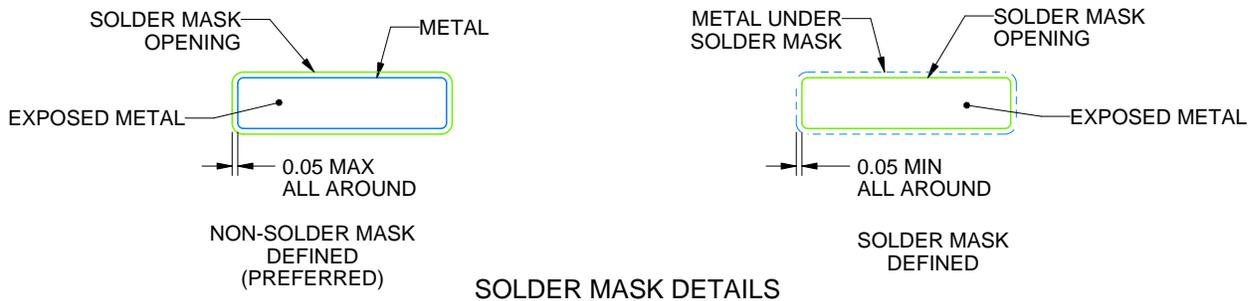
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

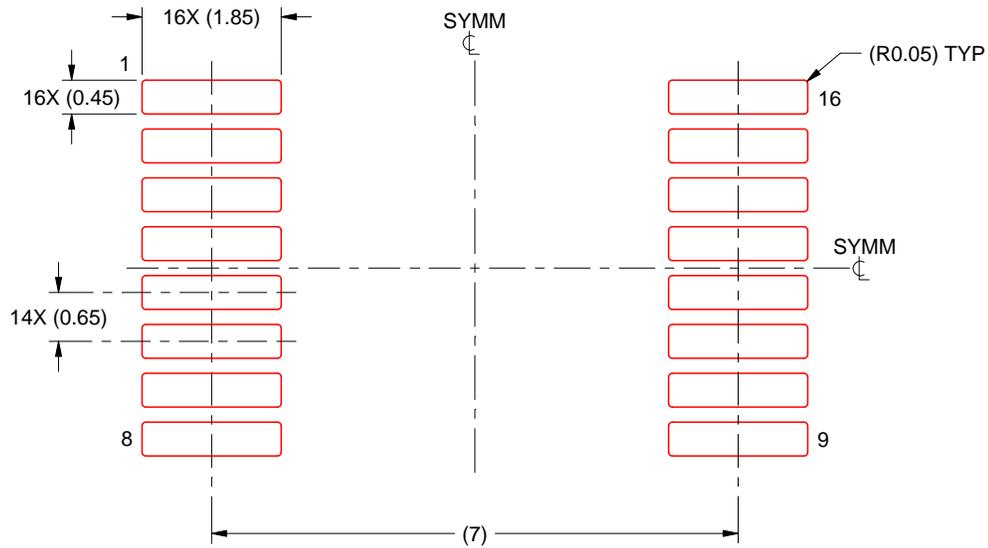
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

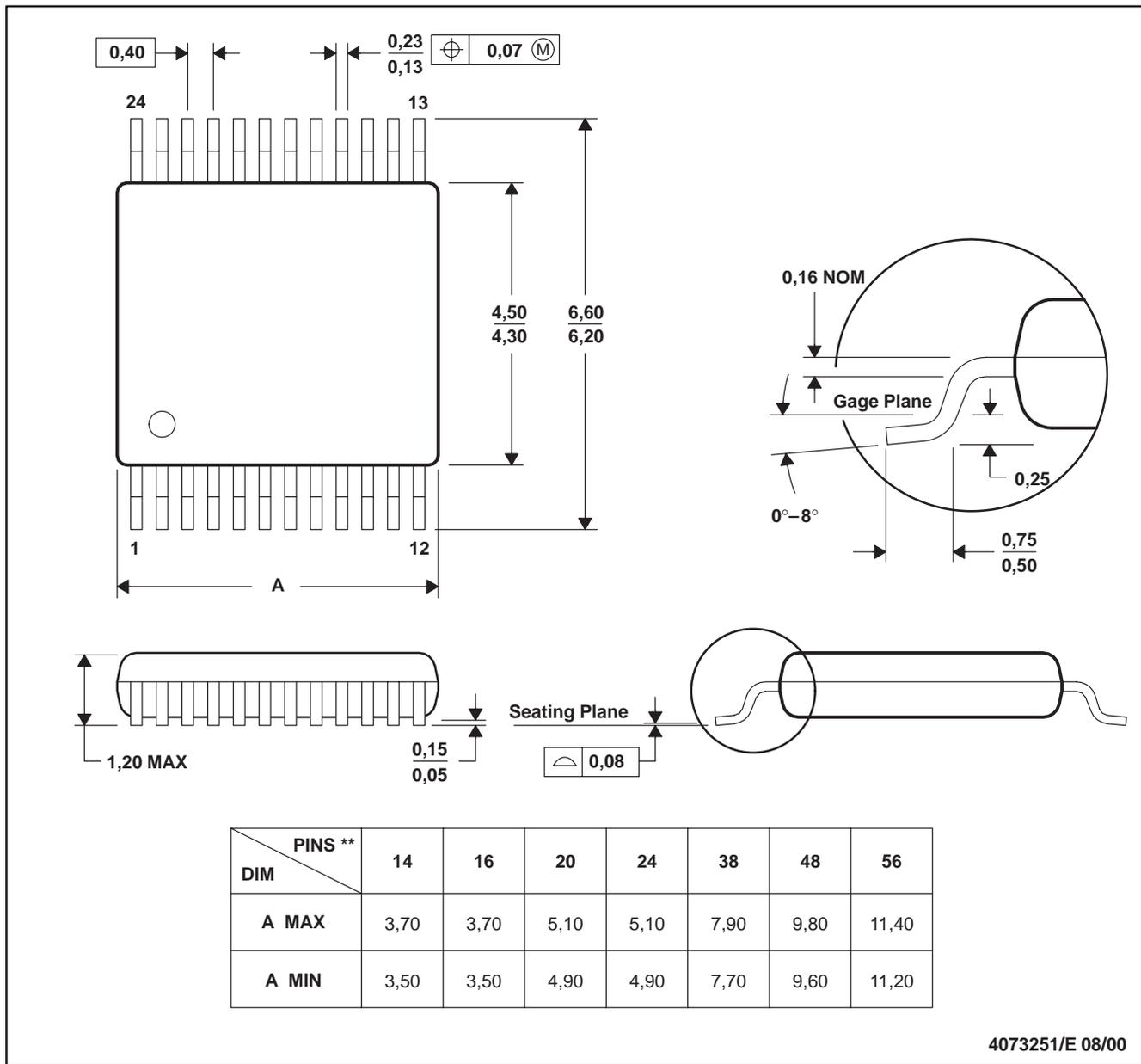
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

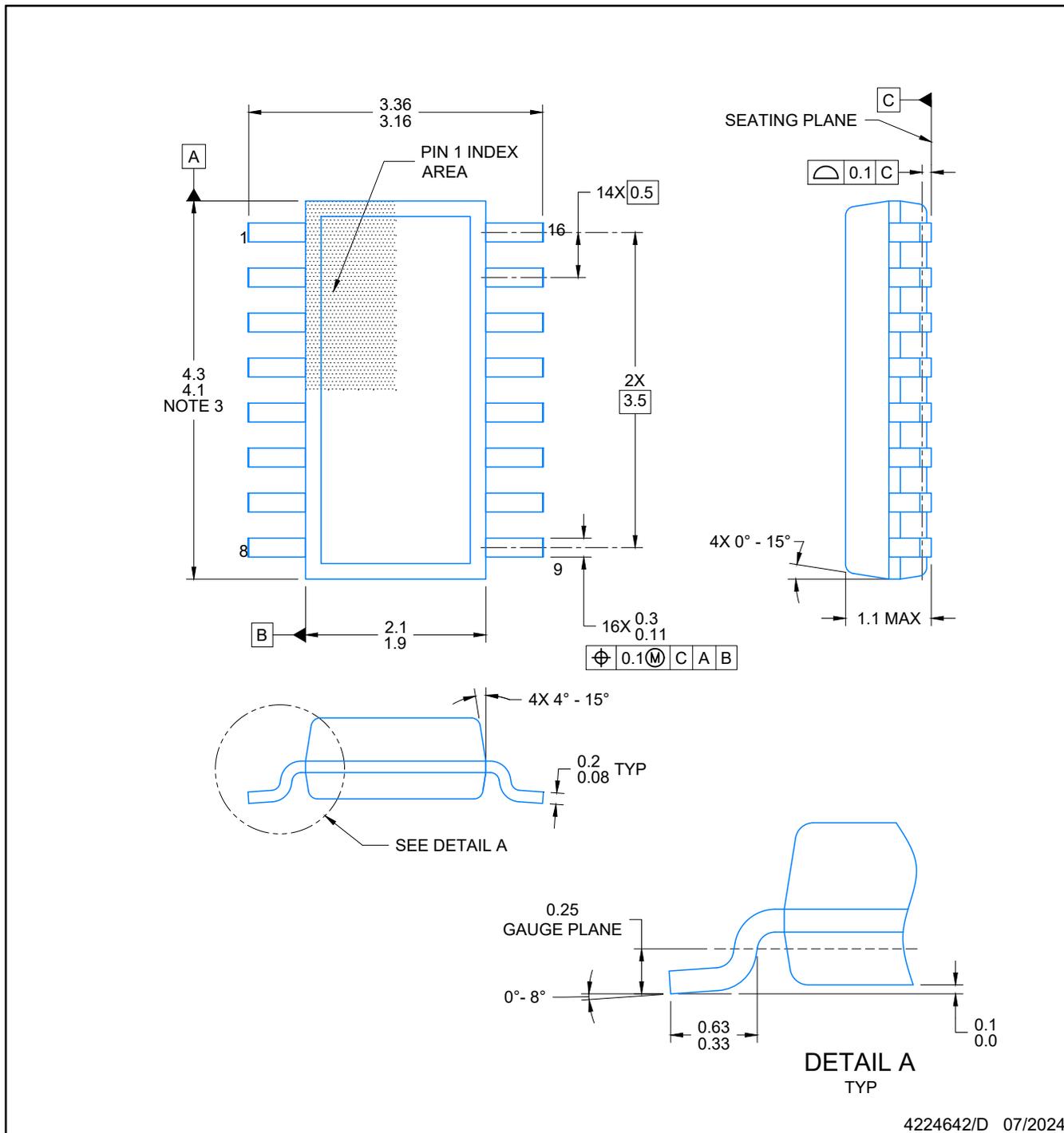
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



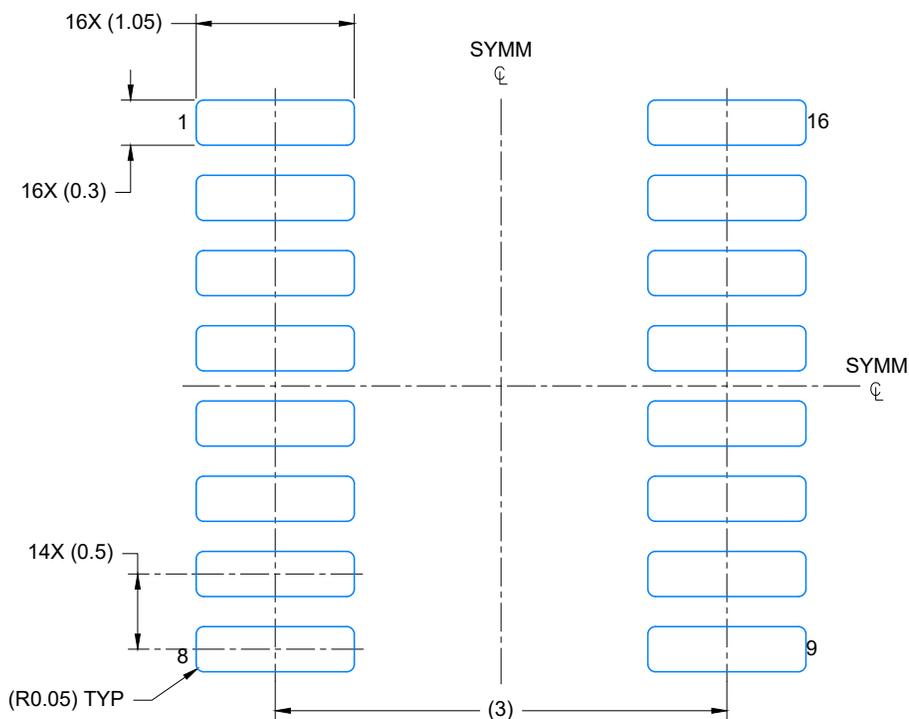
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



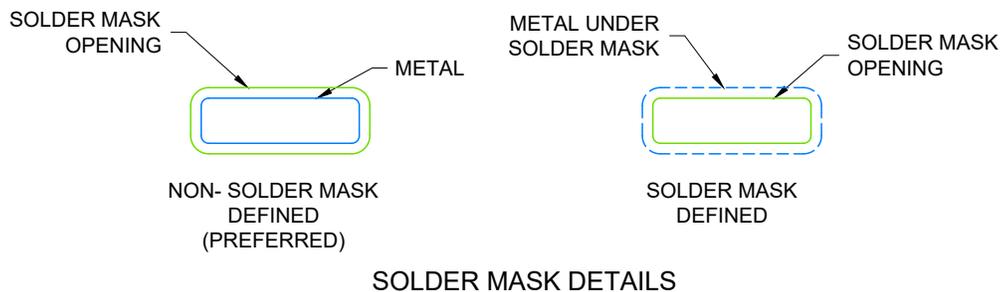
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



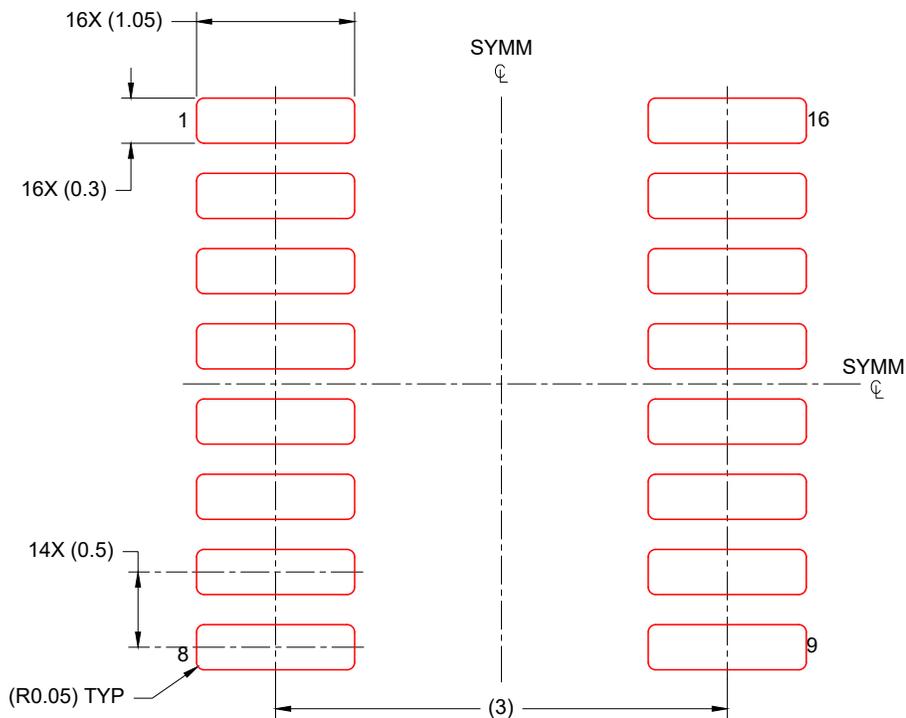
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

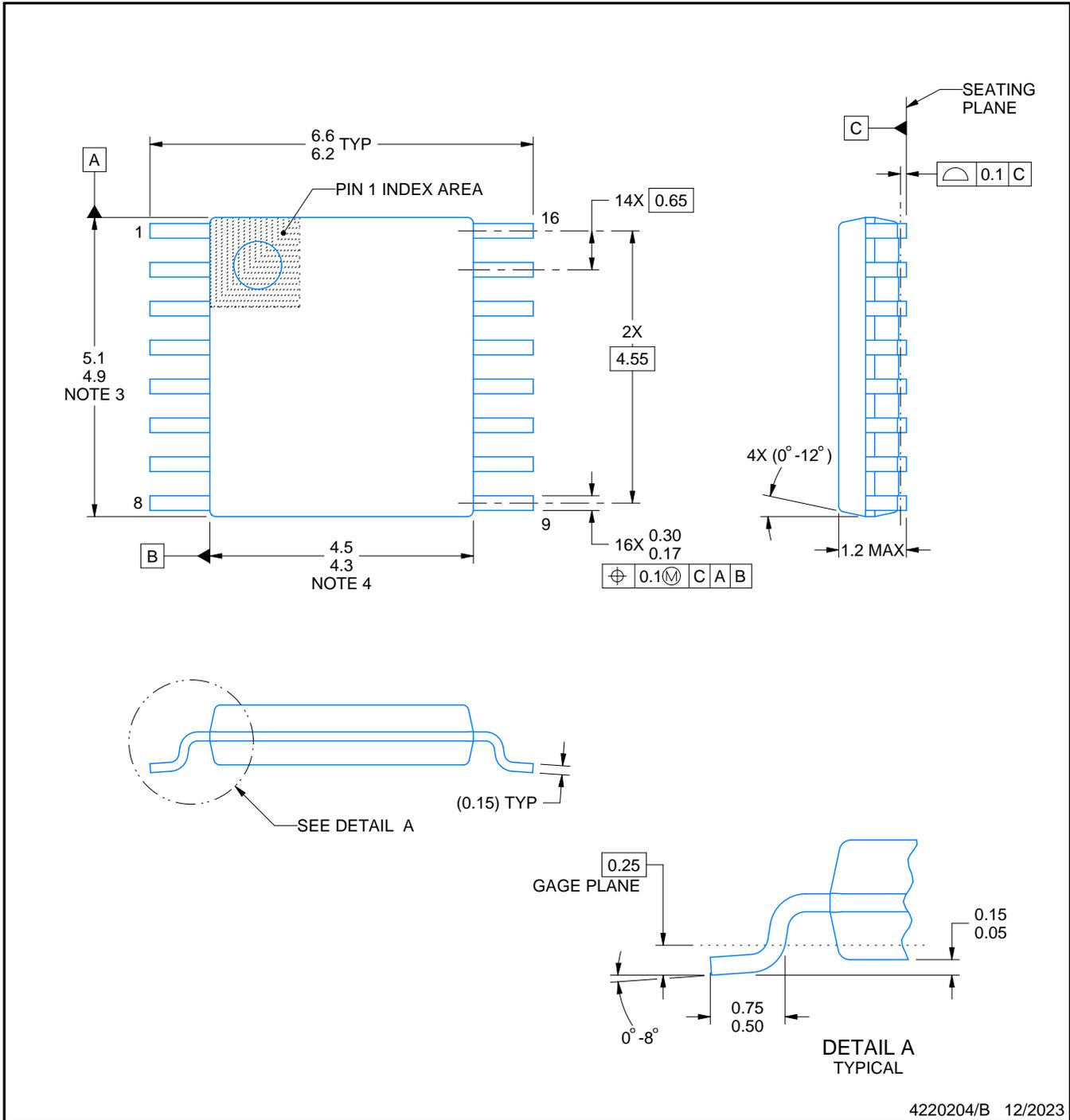


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

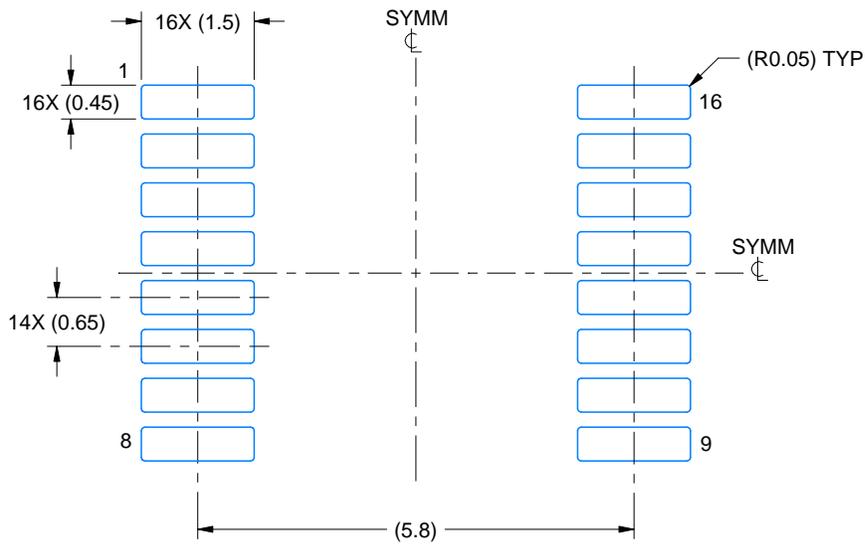
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

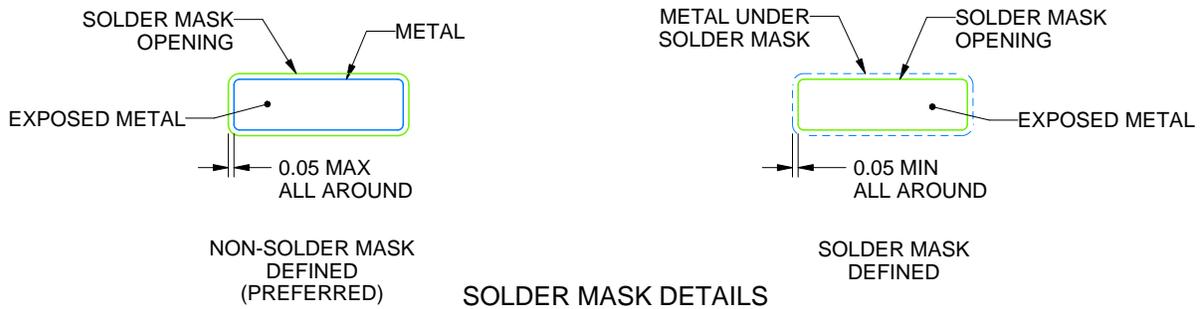
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

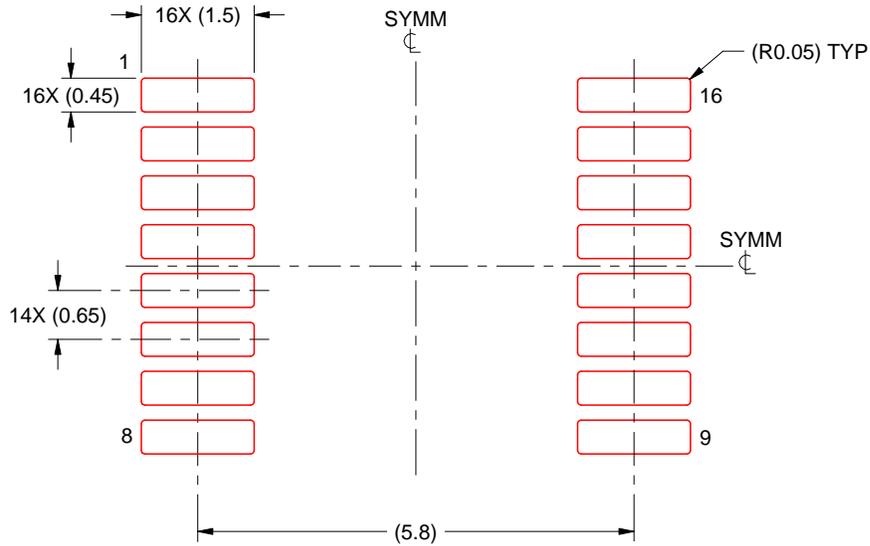
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

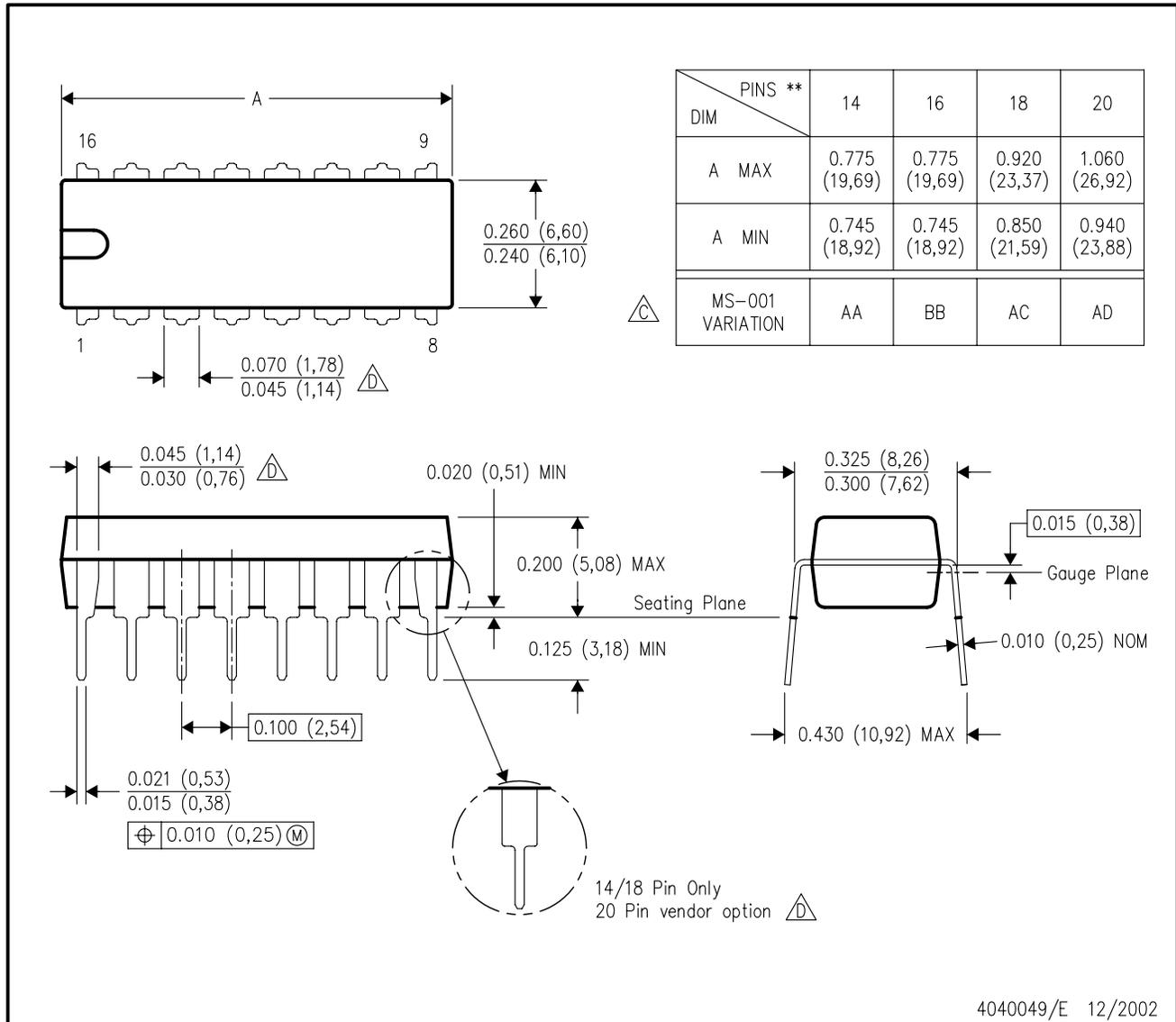
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

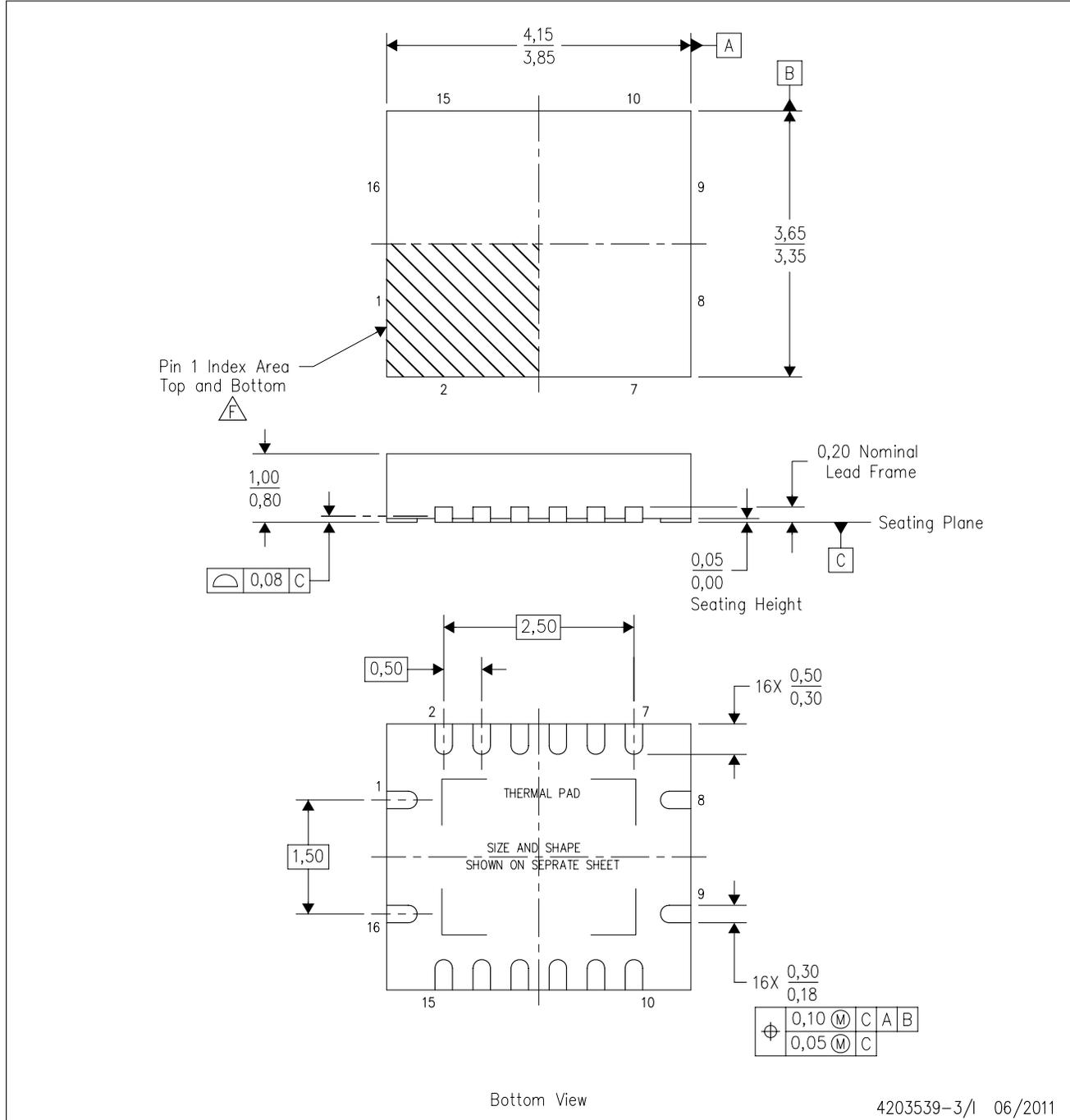
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月