SN74LV373A-Q1 3 ステート出力付きオクタル・トランスペアレント D タイプ・ラッチ

1 特長

- 車載アプリケーション用に認定済み
- 2V～5.5V の V_{CC} で動作
- 最大 tpd 8.5ns (5V 時)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2.3V (V_{CC} = 3.3V、TA = 25°C)
- すべてのポートで混合モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- デジタル信号のクロック同期
- 少ない入力による信号の監視
- スイッチからトグルへの変換

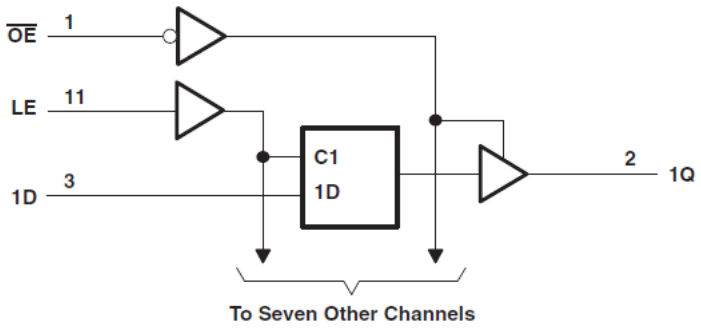
3 説明

SN74LV373A-Q1 デバイスは、2V～5.5V の V_{CC} で動作するように設計されたオクタル・トランスペアレント D タイプ・ラッチです。ラッチ・イネーブル (LE) 入力が HIGH の場合、Q 出力はデータ (D) 入力に追従します。LE を LOW にすると、D 入力で設定されたロジック・レベルで Q 出力がラッチされます。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
SN74LV373A-Q1	PW (TSSOP、20)	6.50mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2007) to Revision D (March 2023)	Page
• 「アプリケーション」、「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加	1
• Updated thermal values for PW package from RθJA = 83 to 128.2, all values in °C/W	5

5 Pin Configuration and Functions

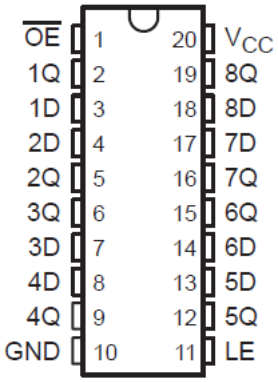


図 5-1. SN74LV373A-Q1 TSSOP -PW Package (Top View)

表 5-1. Pin Function

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	Input	Output enable, active low
1Q	2	Output	Output for channel 1
1D	3	Input	Input for channel 1
2D	4	Input	Input for channel 2
2Q	5	Output	Output for channel 2
3Q	6	Output	Output for channel 3
3D	7	Input	Input for channel 3
4D	8	Input	Input for channel 4
4Q	9	Output	Output for channel 4
GND	10	—	Ground
LE	11	Input	Latch enable
5Q	12	Output	Output for channel 5
5D	13	Input	Input for channel 5
6D	14	Input	Input for channel 6
6Q	15	Output	Output for channel 6
7Q	16	Output	Output for channel 7
7D	17	Input	Input for channel 7
8D	18	Input	Input for channel 8
8Q	19	Output	Output for channel 8
V_{CC}	20	—	Positive supply
Thermal Pad[1]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage (2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
θ_{JA}	Package thermal impedance			83	°C/W
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The package thermal impedance is calculated in accordance with JESD 51-7.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		VCC = 3 V to 3.6 V	V_{CC} × 0.7		
		VCC = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–8	
		V_{CC} = 4.5 V to 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV373A-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 mA	2.3 V	2			
	I_{OH} = –8 mA	3 V	2.48			
	I_{OH} = –16 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 8 mA	3 V			0.44	
	I_{OL} = 16 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5	µA
I_{cc}	V_I = V_{CC} or GND, I_O =0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.9		pF

6.6 Timing Requirements, 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			MIN	MAX	UNIT
t_w	Pulse duration, LE high		6.5		ns
t_{su}	Setup time, data before LE ↓	High or low	5		ns
t_h	Hold time, data after LE ↓	High or low	1.5		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			MIN	MAX	UNIT
t_w	Pulse duration, LE high		5		ns
t_{su}	Setup time, data before LE ↓	High or low	4		ns
t_h	Hold time, data after LE ↓	High or low	1		ns

6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			MIN	MAX	UNIT
t_w	Pulse duration, LE high		5		ns
t_{su}	Setup time, data before LE ↓	High or low	4		ns
t_h	Hold time, data after LE ↓	High or low	1		ns

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	2.5 V ± 0.2 V		3.3 V ± 0.3 V		5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF	1	17	1	13.5	1	8.5	ns
	LE	Q		1	19	1	13	1	8.5	
t_{en}	$\overline{OE}$	Q		1	19	1	13.5	1	9.5	ns
t_{dis}	$\overline{OE}$	Q		1	15	1	12	1	8.5	ns

over operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	2.5 V ± 0.2 V		3.3 V ± 0.3 V		5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 50 pF	1	21	1	17	1	10.5	ns
	LE	Q		1	22	1	16.5	1	10.5	
t_{en}	$\overline{OE}$	Q		1	22	1	17	1	11.5	ns
t_{dis}	$\overline{OE}$	Q		1	19	1	15	1	10.5	ns
$t_{sk(o)}$			C_L = 50 pF		2		1.5		1	ns

6.10 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[1]		SN74LV373A-Q1			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

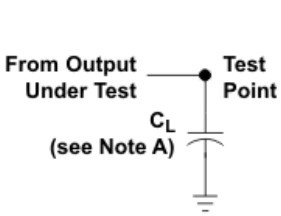
(1) Characteristics for surface-mount packages only.

6.11 Operating Characteristics

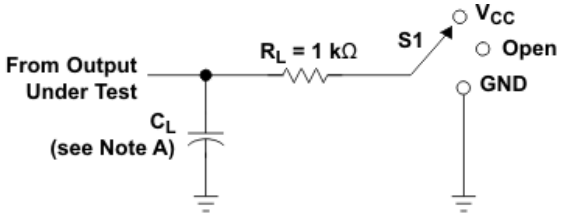
T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance (outputs enabled)	C_L = 50 pF, f = 10 MHz	3.3 V	17.4	pF
			5 V	19.5	

7 Parameter Measurement Information

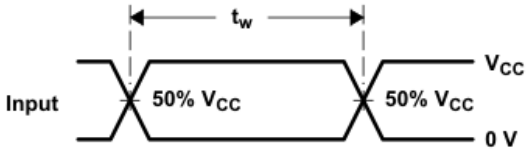


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

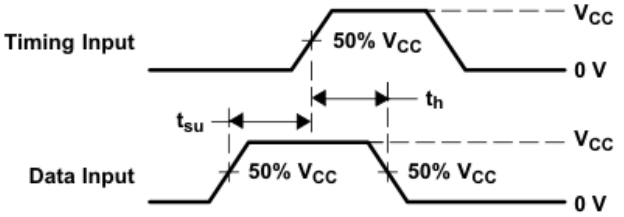


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

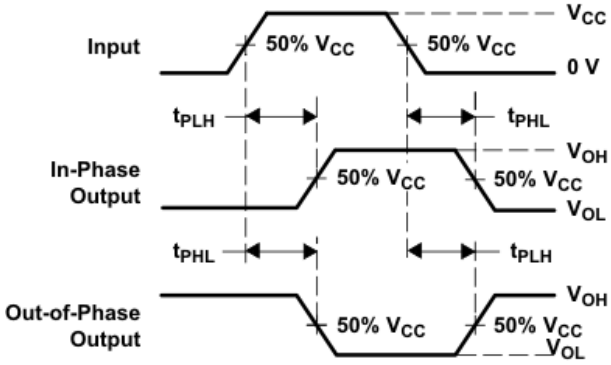
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



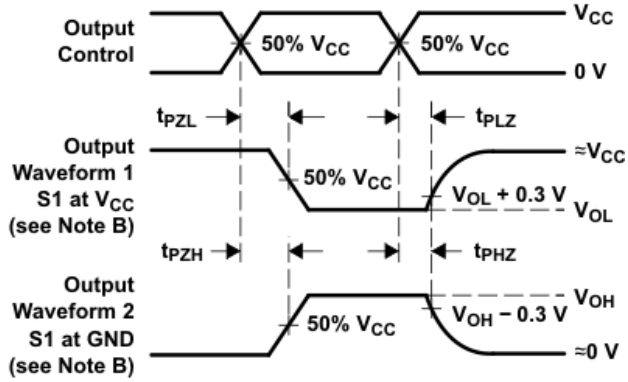
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

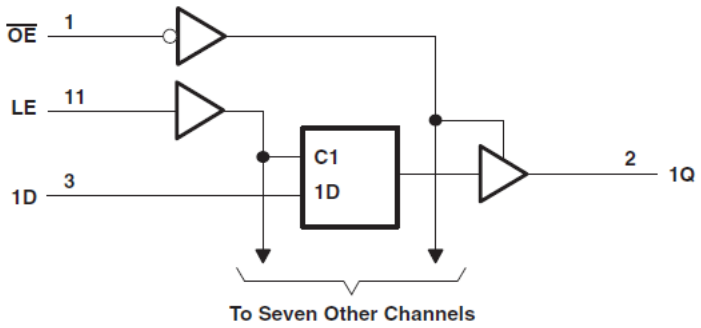


図 8-1. Logic Diagram (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	L, H, ↓	X	Q_0
H	↑	L	L
H	↑	H	H

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = do not care
(2) L = output low, H = output high, Q_0 = previous state

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.2.1.1 Layout Example

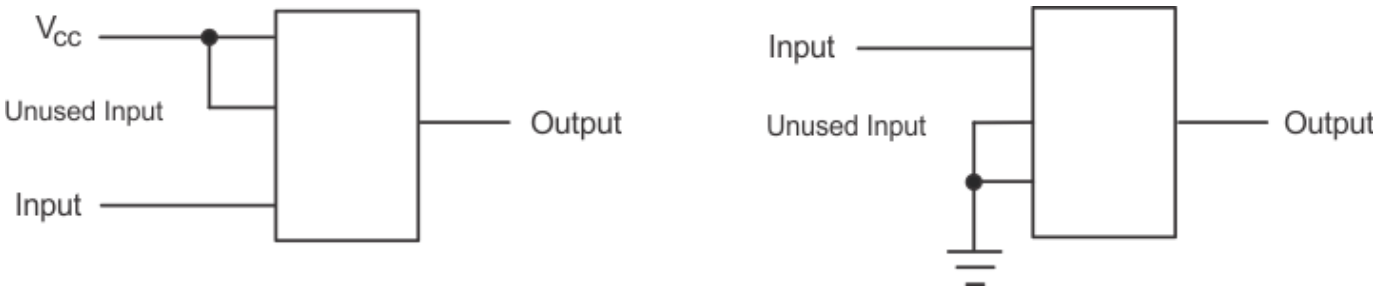


図 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV373A-Q1	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV373AIPWRG4Q1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV373AI
SN74LV373AIPWRG4Q1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV373AI
SN74LV373AIPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	LV373AI
SN74LV373AIPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LV373AI
SN74LV373AIPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 85	LV373AI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV373A-Q1 :

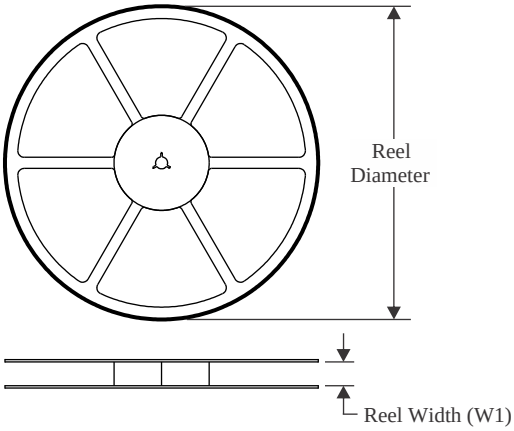
- Catalog : SN74LV373A

NOTE: Qualified Version Definitions:

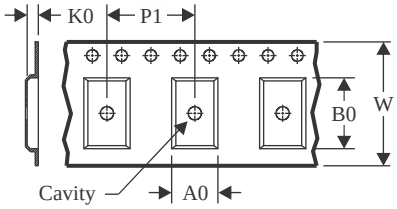
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

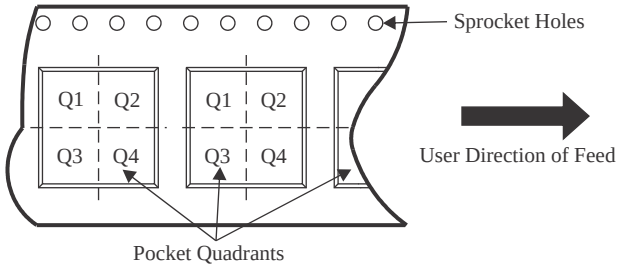


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

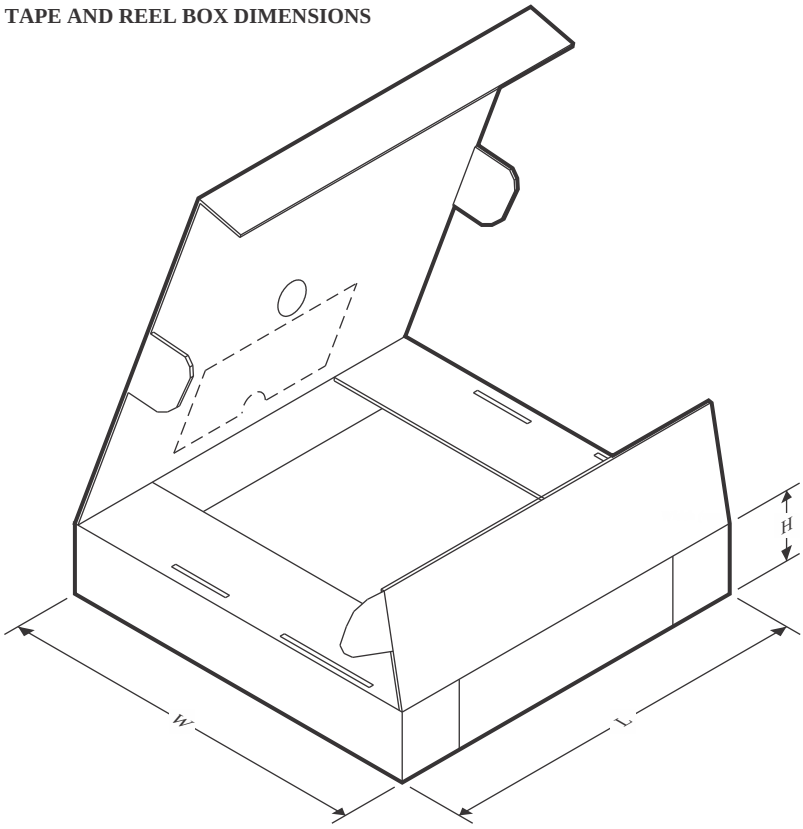
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV373AIPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

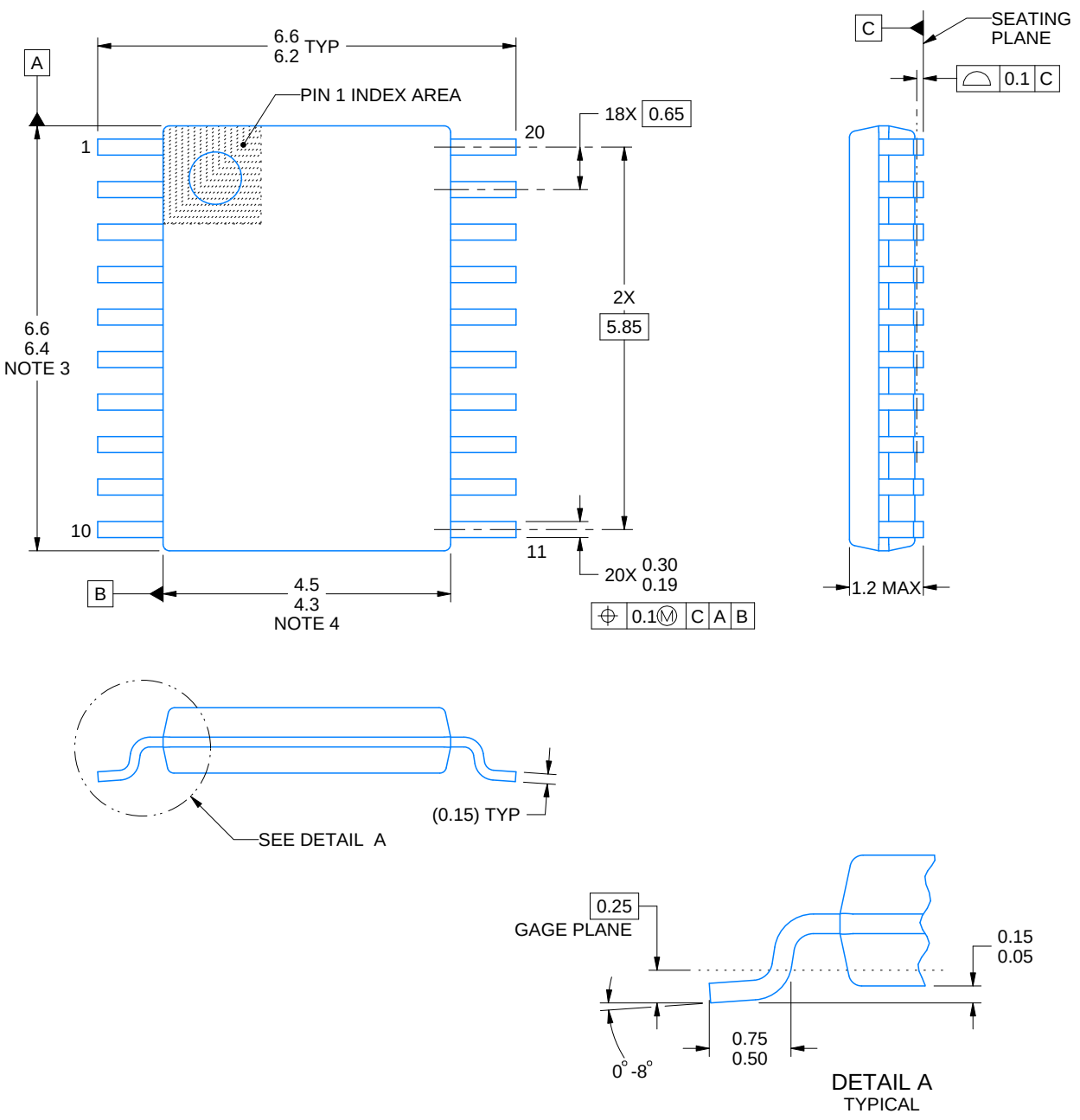
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373AIPWRG4Q1	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV373AIPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

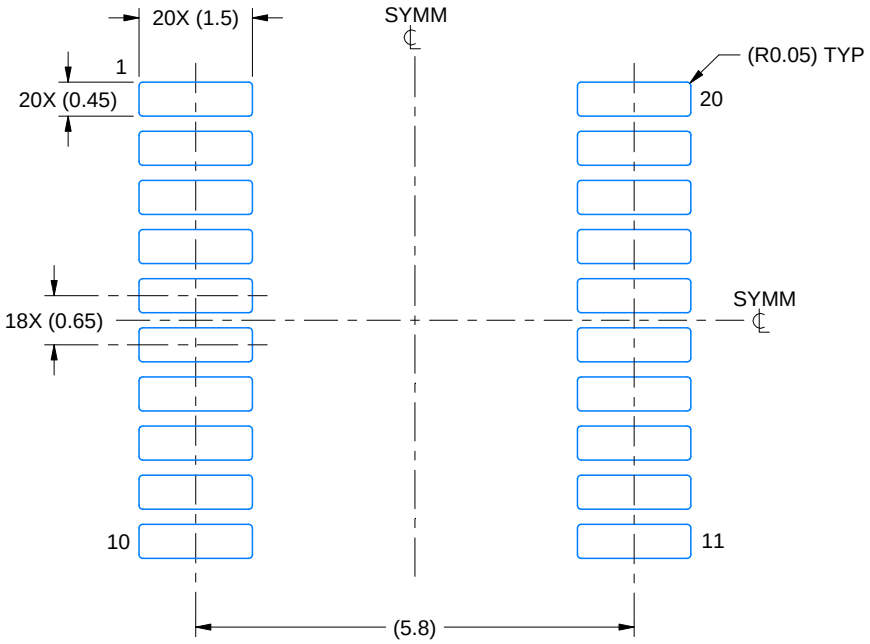
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



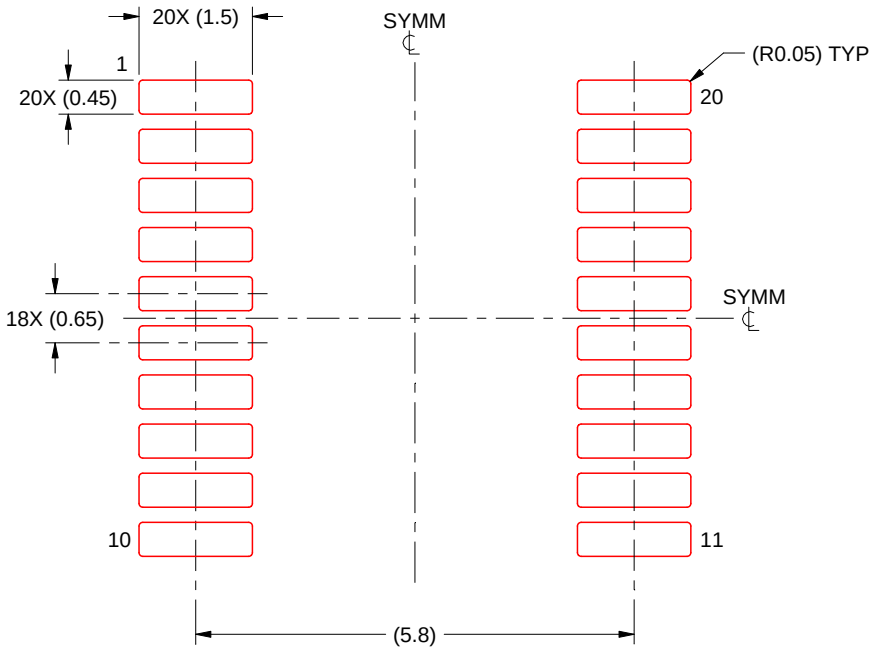
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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