

SN74LV2T74-Q1 車載用デュアル D タイプ・フリップ・フロップ、統合変換機能付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - デバイス温度グレード 1: -40°C ~ +125°C
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- ウェットابل・フランク QFN (WBQA) パッケージで供給されます
- 幅広い動作範囲: 1.8V ~ 5.5V
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」を参照):
 - 昇圧変換:
 - 1.2V から 1.8V
 - 1.5V から 2.5V
 - 1.8V から 3.3V
 - 3.3V から 5.0V
 - 降圧変換:
 - 5.0V、3.3V、2.5V から 1.8V
 - 5.0V、3.3V から 2.5V
 - 5.0V から 3.3V
- 5.5V 許容入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の V_{CC} で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- モメンタリ・スイッチからトグル・スイッチへの変換
- コントローラ・リセット時の信号保持
- 低速エッジレート信号の入力
- ノイズの多い環境での動作
- クロック信号の 2 分割

3 概要

SN74LV2T74-Q1 には、2 つの独立した D タイプ正エッジ・トリガのフリップ・フロップが含まれています。プリセット (PRE) 入力が Low レベルのとき、出力は High になります。クリア ($\overline{CLR}$) 入力が Low レベルのとき、出力は Low にリセットされます。プリセット機能とクリア機能は非同期であり、他方の入力レベルとは無関係です。PRE と CLR が非アクティブ (High) の場合、セットアップ時間の要件を満たすデータ (D) 入力のデータは、クロック (CLK) パルスの正方向エッジで出力 (Q、 $\overline{Q}$) に転送されます。クロックのトリガは電圧レベルで発生し、入力クロック (CLK) 信号の立ち上がり時間とは直接関係しません。ホールド時間が経過した後、データ (D) 入力のデータは、出力 (Q、 $\overline{Q}$) のレベルに影響を及ぼさずに変化させることができます。出力レベルは電源電圧 (V_{CC}) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

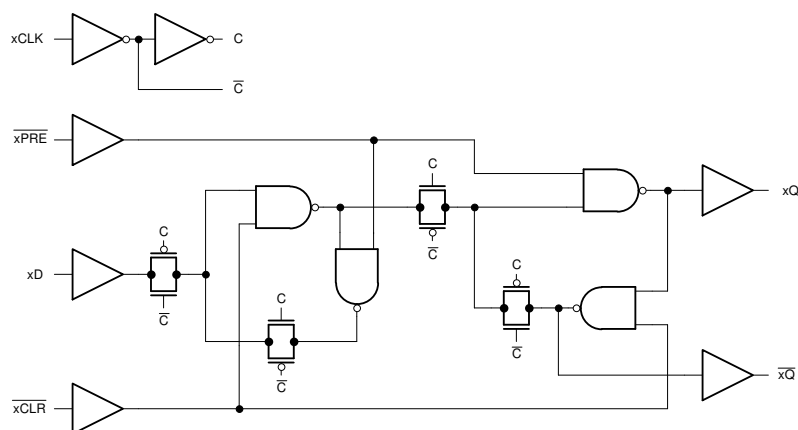
入力は低スレッシュホルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例: 1.2V 入力から 1.8V 出力、1.8V 入力から 3.3V 出力) をサポートします。また、5V 許容の入力ピンにより、降圧変換 (例: 3.3V から 2.5V 出力) が可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)	本体サイズ (公称) (3)
SN74LV2T74-Q1	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれていません。





概略論理図 (正論理)

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4 Revision History

DATE	REVISION	NOTES
May 2023	*	Initial Release

5 Pin Configuration and Functions

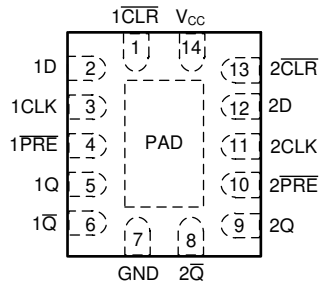


图 5-1. BQA Package, 14-Pin WQFN (Top View)

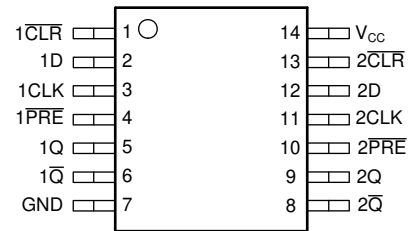


图 5-2. PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1CLR	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1CLK	3	Input	Clock for channel 1, rising edge triggered
1PRE	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1Q	6	Output	Inverted output for channel 1
GND	7	—	Ground
2Q	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2PRE	10	Input	Preset for channel 2, active low
2CLK	11	Input	Clock for channel 2, rising edge triggered
2D	12	Input	Data for channel 2
2CLR	13	Input	Clear for channel 2, active low
V _{CC}	14	—	Positive supply
Thermal Pad ⁽¹⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) BQA package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range ⁽²⁾		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	7	V
V_O	Output voltage range ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < -0.5$ V		-20	mA
I_{OK}	Output clamp current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.6	5.5	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 2 V	1.1	V	
		V _{CC} = 2.25 V to 2.75 V	1.28		
		V _{CC} = 3 V to 3.6 V	1.45		
		V _{CC} = 4.5 V to 5.5 V	2		
V _{IL}	Low-Level input voltage	V _{CC} = 1.65 V to 2 V	0.5	V	
		V _{CC} = 2.25 V to 2.75 V	0.65		
		V _{CC} = 3 V to 3.6 V	0.75		
		V _{CC} = 4.5 V to 5.5 V	0.85		
I _O	Output current	V _{CC} = 1.6 V to 2 V	±3	mA	
		V _{CC} = 2.25 V to 2.75 V	±7		
		V _{CC} = 3.3 V to 5.0 V	±15		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.6 V to 5.0 V	20	ns/V	
T _A	Operating free-air temperature		-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV2T74-Q1		UNIT
		WBQA (WQFN)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	88.3	151.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.9	80.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.8	94.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	9.9	28.0	°C/W
Y _{JB}	Junction-to-board characterization parameter	56.7	93.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	33.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	1.65 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	1.65 V to 2 V	1.28	1.7 ⁽¹⁾		1.21			
	I _{OH} = -3 mA	2.25 V to 2.75 V	2	2.4 ⁽¹⁾		1.93			
	I _{OH} = -5.5 mA	3 V to 3.6 V	2.6	3.08 ⁽¹⁾		2.49			
	I _{OH} = -8 mA	4.5 V to 5.5 V	4.1	4.65 ⁽¹⁾		3.95			
V _{OL}	I _{OL} = 50 μA	1.65 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	1.65 V to 2 V		0.1 ⁽¹⁾	0.2			0.25	
	I _{OL} = 3 mA	2.25 V to 2.75 V		0.1 ⁽¹⁾	0.15			0.2	
	I _{OL} = 5.5 mA	3 V to 3.6 V		0.2 ⁽¹⁾	0.2			0.25	
	I _{OL} = 8 mA	4.5 V to 5.5 V		0.3 ⁽¹⁾	0.3			0.35	
I _I	V _I = 0 V or V _{CC}	0 V to 5.5 V			±0.1			±1	μA
I _{CC}	V _I = 0 V or V _{CC} , I _O = 0; open on loading	1.65 V to 5.5 V			2			20	μA
ΔI _{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V _{CC} , I _O = 0	5.5 V			1.35			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V _{CC} , I _O = 0	1.8 V			10			20	μA
C _I	V _I = V _{CC} or GND	5 V		4	10			10	pF
C _O	V _O = V _{CC} or GND	5 V		3					pF
C _{PD} ^{(2) (3)}	No load, F = 1 MHz	5 V		14					pF

- (1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) P_D = V_{CC}² × F_I × (C_{PD} + C_L) where F_I = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6.6 Timing Characteristics 1.8-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	8		9		nS
t_W	Pulse duration	CLK	8		9		nS
t_{SU}	Setup time before CLK $\uparrow$	Data	8		9		nS
t_{SU}	Setup time before CLK $\uparrow$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	7		7		nS
t_H	Hold time, data after CLK $\uparrow$		0.5		0.5		nS

6.7 Timing Characteristics 2.5-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	7		8		nS
t_W	Pulse duration	CLK	7		8		nS
t_{SU}	Setup time before CLK $\uparrow$	Data	7		8		nS
t_{SU}	Setup time before CLK $\uparrow$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	6		6		nS
t_H	Hold time, data after CLK $\uparrow$		0.5		0.5		nS

6.8 Timing Characteristics 3.3-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	6		7		nS
t_W	Pulse duration	CLK	6		7		nS
t_{SU}	Setup time before CLK $\uparrow$	Data	6		7		nS
t_{SU}	Setup time before CLK $\uparrow$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	5		5		nS
t_H	Hold time, data after CLK $\uparrow$		0.5		0.5		nS

6.9 Timing Characteristics 5-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	5		5		nS
t_W	Pulse duration	CLK	5		5		nS
t_{SU}	Setup time before CLK $\uparrow$	Data	5		5		nS
t_{SU}	Setup time before CLK $\uparrow$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	3		3		nS
t_H	Hold time, data after CLK $\uparrow$		0.5		0.5		nS

6.10 Switching Characteristics 1.8-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	34	53		30			MHz
			C _L = 50 pF	21	32		19			MHz
t _{PLH}	PRE or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 15 pF	14.8	24.0		1	28.3		nS
t _{PHL}				14.8	24.0		1	28.3		nS
t _{PLH}	CLK	Q or $\overline{\text{Q}}$		13.1	23.2		1	27.3		nS
t _{PHL}				13.1	23.2		1	27.3		nS
t _{PLH}	PRE or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	C _L = 50 pF	19.7	30.8		1	35.1		nS
t _{PHL}				19.7	30.8		1	35.1		nS
t _{PLH}	CLK	Q or $\overline{\text{Q}}$		17.9	30.0		1	34.1		nS
t _{PHL}				17.9	30.0		1	34.1		nS

6.11 Switching Characteristics 2.5-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	52	81		46			MHz
			C _L = 50 pF	33	49		29			MHz
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 15 pF	9.9	16.0		1	18.9		nS
t _{PHL}				9.9	16.0		1	18.9		nS
t _{PLH}	CLK	Q or Q̄		8.7	15.5		1	18.2		nS
t _{PHL}				8.7	15.5		1	18.2		nS
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 50 pF	13.1	20.5		1	23.4		nS
t _{PHL}				13.1	20.5		1	23.4		nS
t _{PLH}	CLK	Q or Q̄		12.0	20.0		1	22.8		nS
t _{PHL}				12.0	20.0		1	22.8		nS

6.12 Switching Characteristics 3.3-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	80	125		70			MHz
			C _L = 50 pF	50	75		45			MHz
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 15 pF		7.6	12.3	1		14.5	nS
t _{PHL}					7.6	12.3	1		14.5	nS
t _{PLH}	CLK	Q or Q̄			6.7	11.9	1		14	nS
t _{PHL}					6.7	11.9	1		14	nS
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 50 pF		10.1	15.8	1		18	nS
t _{PHL}					10.1	15.8	1		18	nS
t _{PLH}	CLK	Q or Q̄			9.2	15.4	1		17.5	nS
t _{PHL}					9.2	15.4	1		17.5	nS

6.13 Switching Characteristics 5-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	130	170		110			MHz
			C _L = 50 pF	90	140		75			MHz
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 15 pF	4.8	7.7		1		9	nS
t _{PHL}				4.8	7.7		1		9	nS
t _{PLH}	CLK	Q or Q̄		4.6	7.3		1		8.5	nS
t _{PHL}				4.6	7.3		1		8.5	nS
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 50 pF	6.3	9.7		1		11	nS
t _{PHL}				6.3	9.7		1		11	nS
t _{PLH}	CLK	Q or Q̄		6.1	9.3		1		10	nS
t _{PHL}				6.1	9.3		1		10	nS

6.14 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	5		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

6.15 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

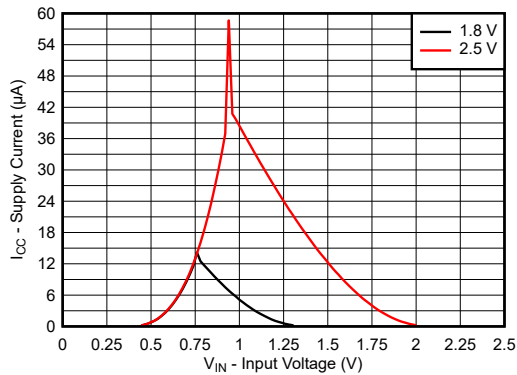


FIG 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

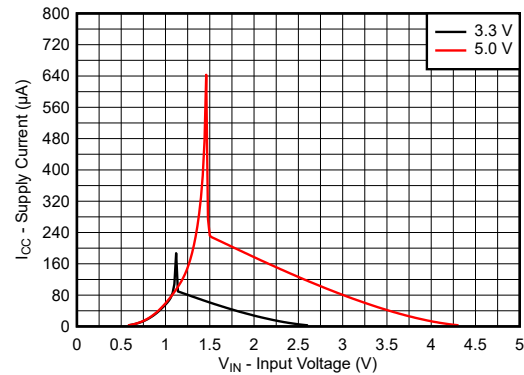


FIG 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

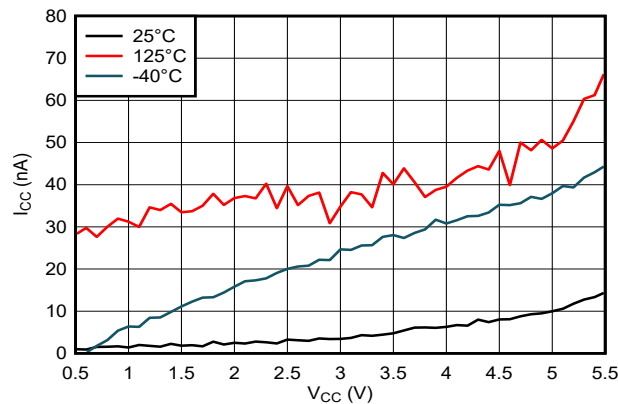


FIG 6-3. Supply Current Across Supply Voltage

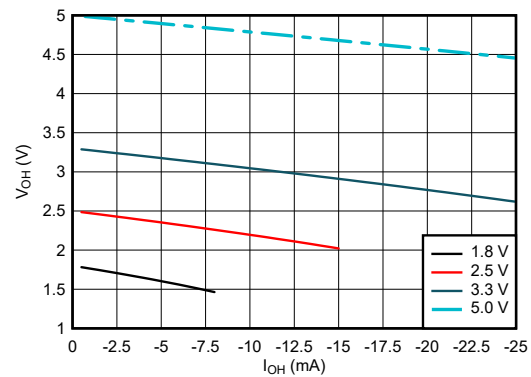


FIG 6-4. Output Voltage vs Current in HIGH State

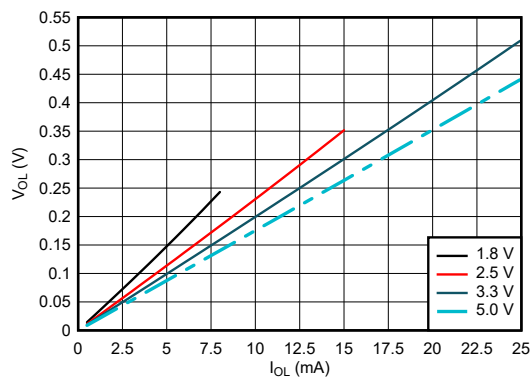


FIG 6-5. Output Voltage vs Current in LOW State

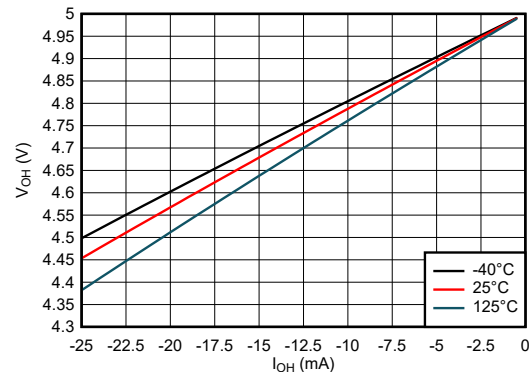


FIG 6-6. Output Voltage vs Current in HIGH State; 5-V Supply

6.15 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

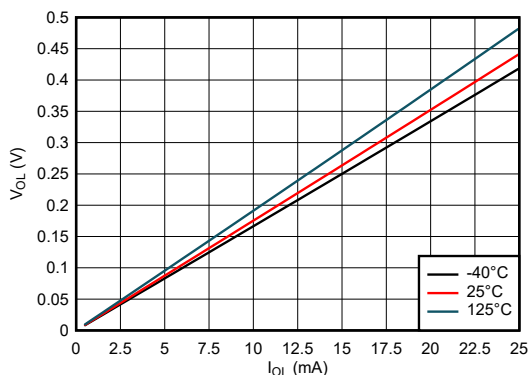


图 6-7. Output Voltage vs Current in LOW State; 5-V Supply

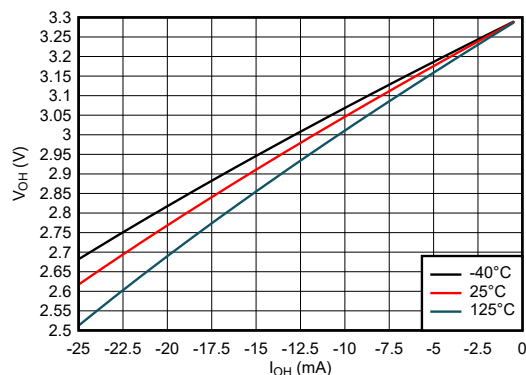


图 6-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

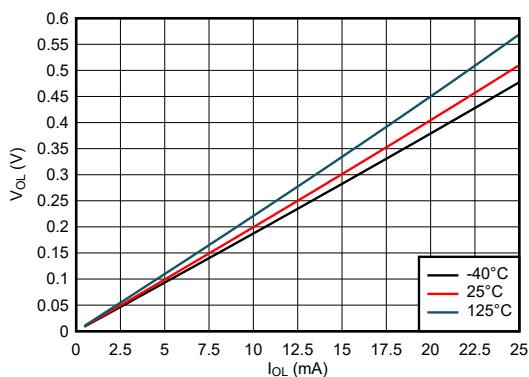


图 6-9. Output Voltage vs Current in LOW State; 3.3-V Supply

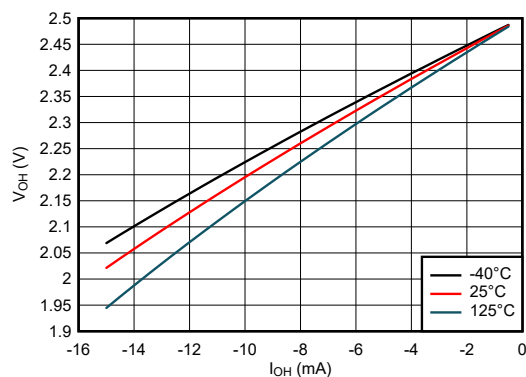


图 6-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

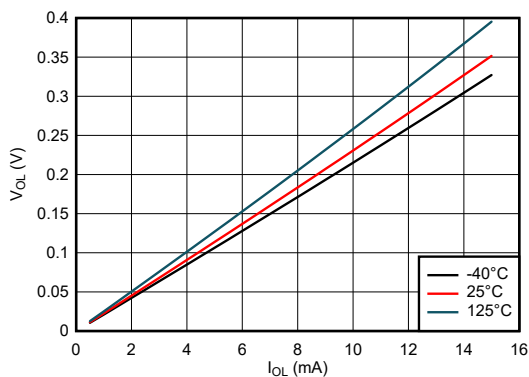


图 6-11. Output Voltage vs Current in LOW State; 2.5-V Supply

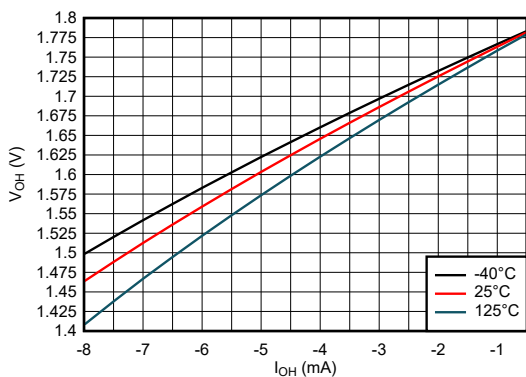
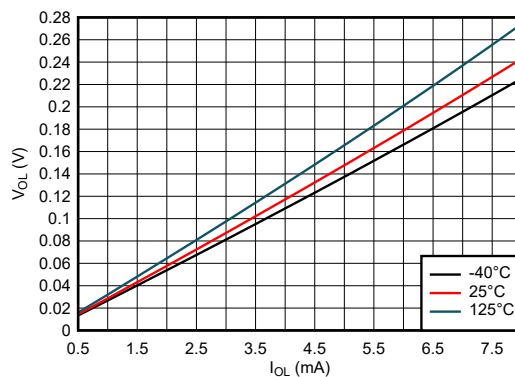


图 6-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

6.15 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)



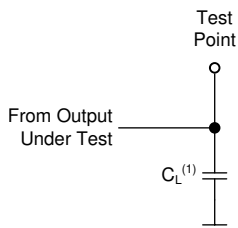
6-13. Output Voltage vs Current in LOW State; 1.8-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$.

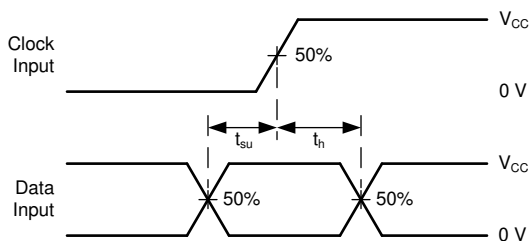
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

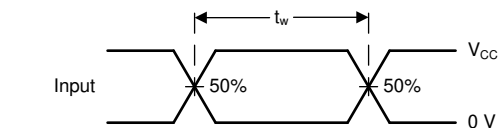


(1) C_L includes probe and test-fixture capacitance.

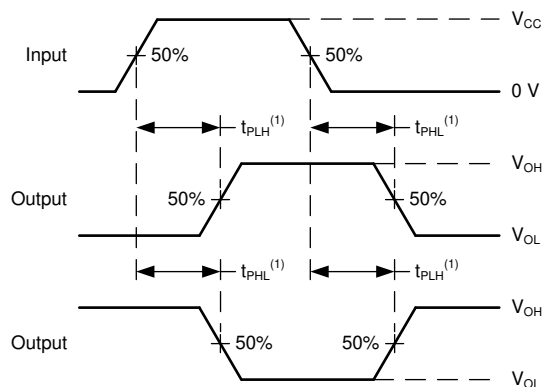
7-1. Load Circuit for Push-Pull Outputs



7-3. Voltage Waveforms, Setup and Hold Times

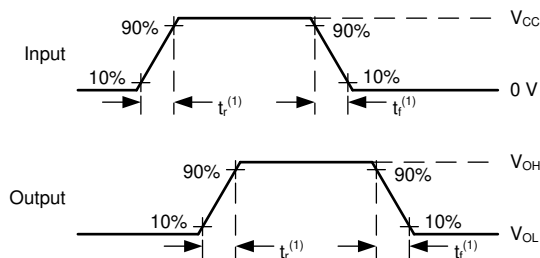


7-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

7-5. Voltage Waveforms, Input and Output Transition Times

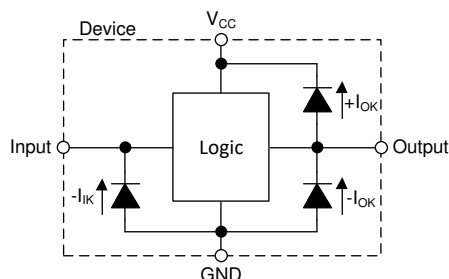


FIG 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.3 LVxT Enhanced Input Voltage

The SN74LV2T74-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. To ensure proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. FIG 8-3 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k Ω resistor is recommended and will typically meet all requirements.

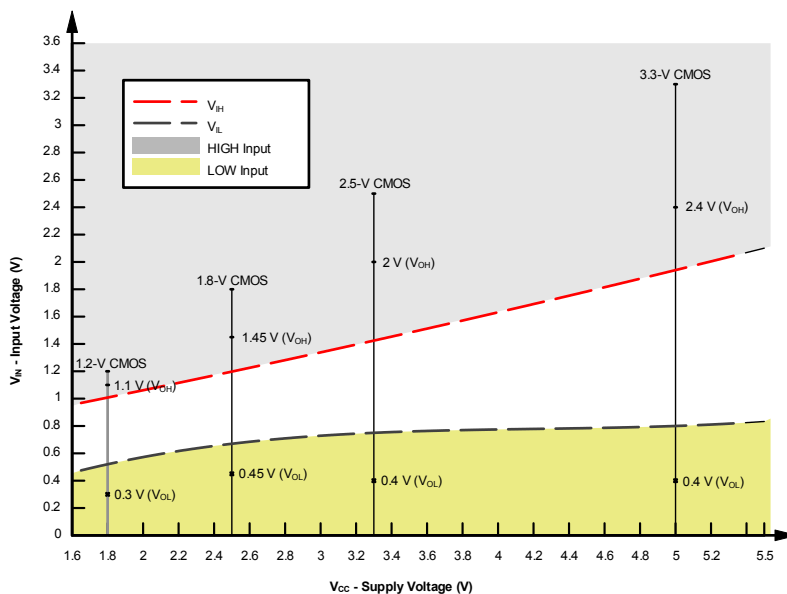


FIG 8-3. LVxT Input Voltage Levels

8.3.3.1 Down Translation

Signals can be translated down using the SN74LV2T74-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. As shown in [Figure 8-3](#), ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in [Figure 8-4](#) for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC} .

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V V_{CC} – Inputs from 3.3 V and 5.0 V
- 3.3-V V_{CC} – Inputs from 5.0 V

8.3.3.2 Up Translation

Input signals can be up translated using the SN74LV2T74-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV2T74-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in [Figure 8-4](#), ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2 V
- 2.5-V V_{CC} – Inputs from 1.8 V
- 3.3-V V_{CC} – Inputs from 1.8 V and 2.5 V
- 5.0-V V_{CC} – Inputs from 2.5 V and 3.3 V

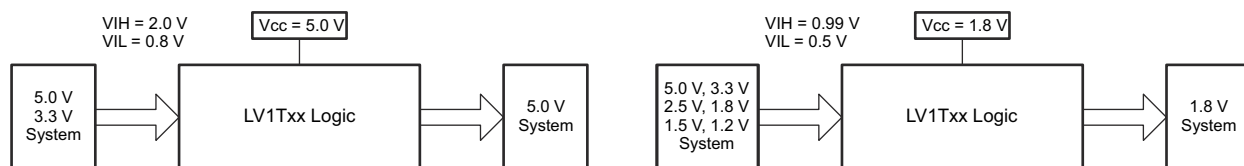


Figure 8-4. LVxT Up and Down Translation Example

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

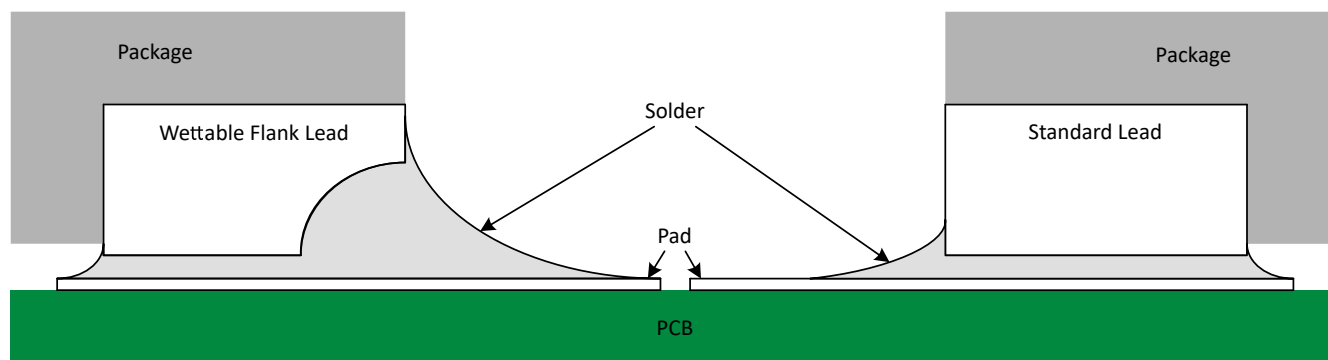


图 8-5. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 8-5, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV2T74-Q1.

表 8-1. Function Table

INPUTS				OUTPUTS ⁽¹⁾	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\bar{Q}_0$

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. External Schmitt-trigger buffers are used to remove noisy inputs into the (CLK) and (D) inputs.

If the data input (D) of the SN74LV2T74-Q1 is tied to the inverted output ($\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

9.2 Typical Application

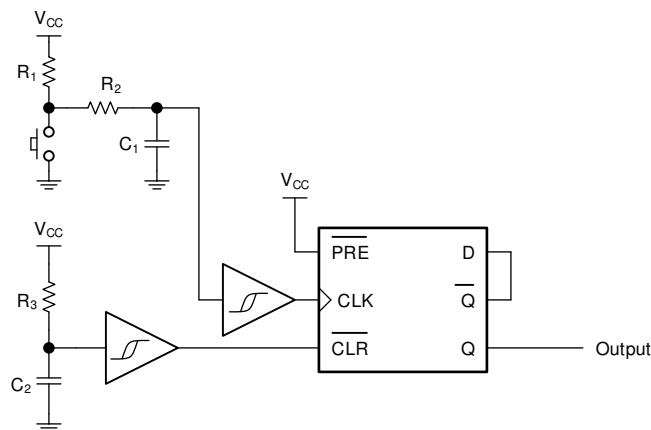


图 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV2T74-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV2T74-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.2 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

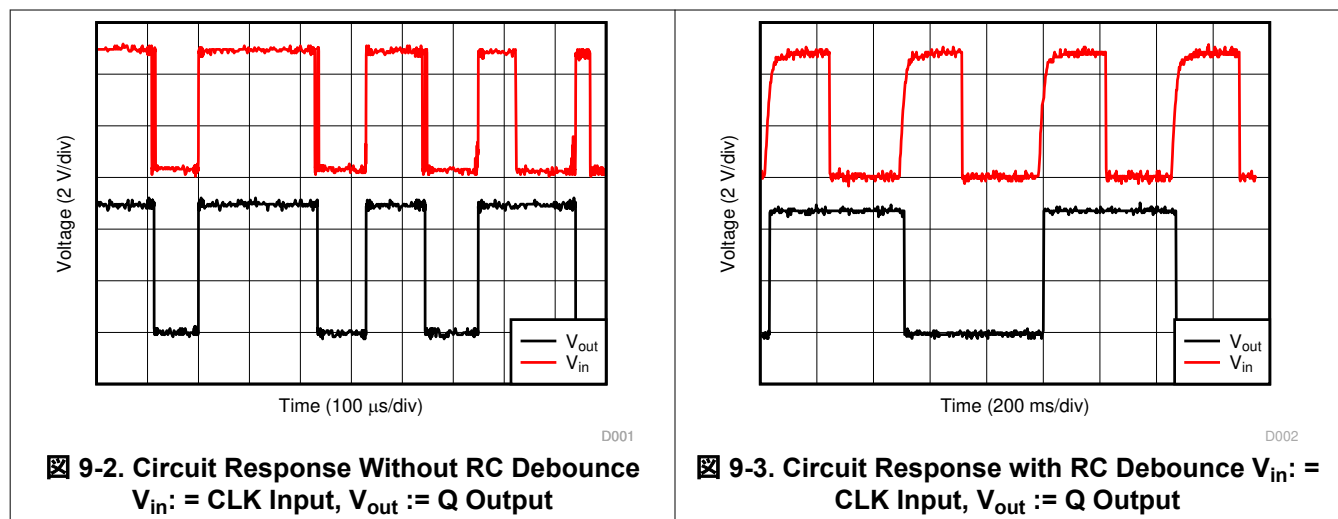
Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV2T74-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curves

Figure 9-2 shows an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Figure 9-3 shows 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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11.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV2T74QPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT74Q
SN74LV2T74QPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT74Q
SN74LV2T74QWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT74Q
SN74LV2T74QWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT74Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV2T74-Q1 :

- Catalog : [SN74LV2T74](#)
- Enhanced Product : [SN74LV2T74-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV2T74QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV2T74QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV2T74QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74LV2T74QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



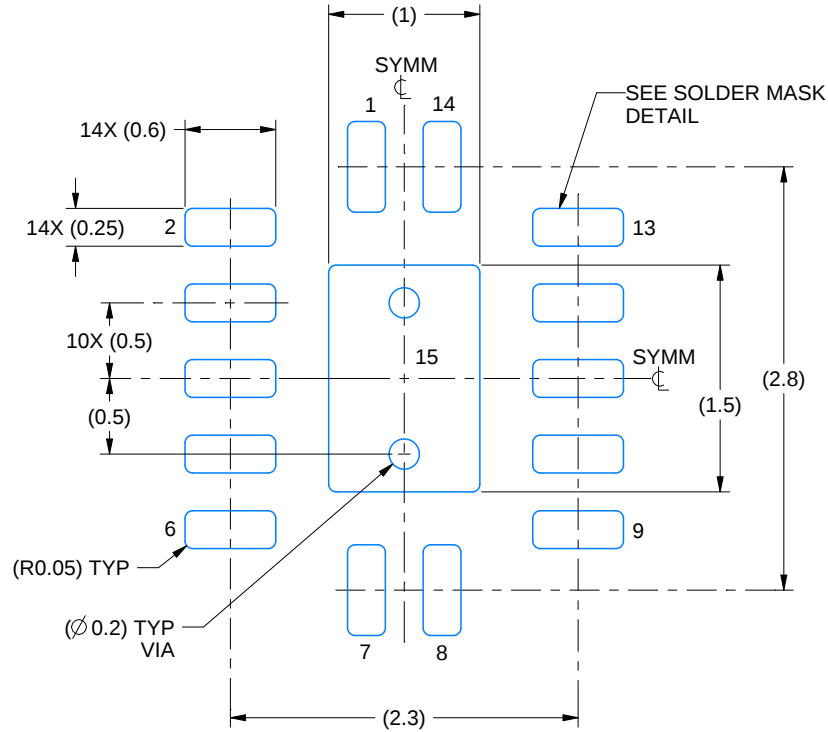
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

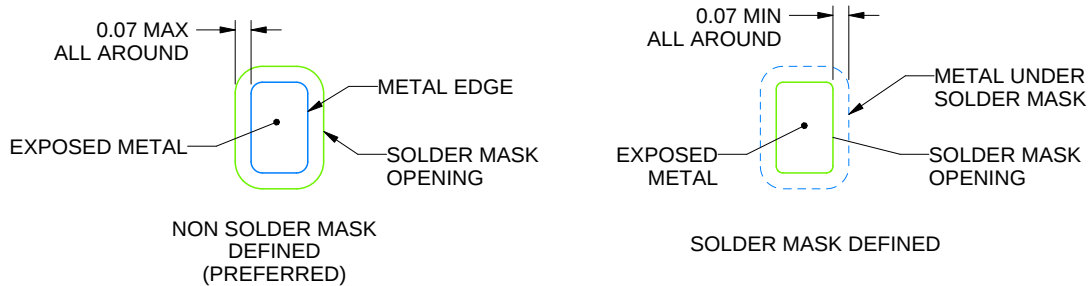
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

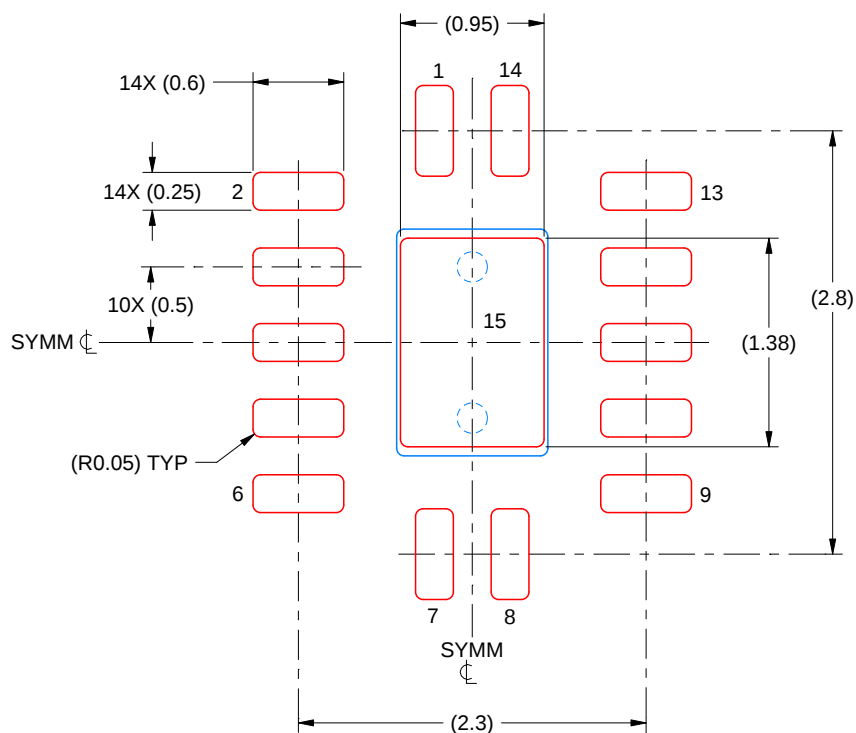
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

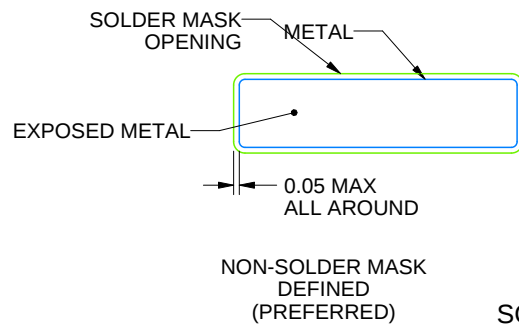
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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