

SN74LV245A 3 ステート出力、オクタル・バス・トランシーバ

1 特長

- 2V~5.5V の V_{CC} で動作
- 最大 t_{pd} 6.5ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス)
 $< 0.8V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート)
 $> 2.3V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- すべてのポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン・モデル (A115-A)
 - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- サーバー
- LED ディスプレイ
- ネットワーク・スイッチ
- 通信インフラ
- モーター・ドライバ
- I/O エクスパンダ

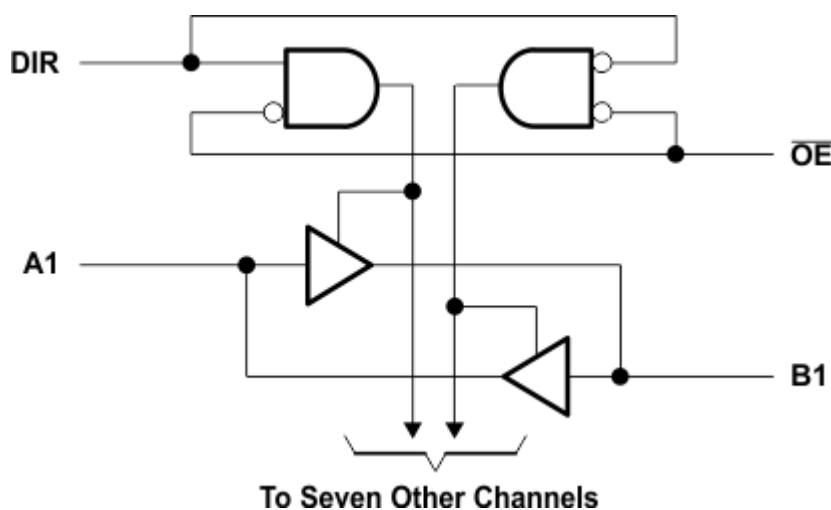
3 概要

これらのオクタル・バス・トランシーバは、2V~5.5V の V_{CC} で動作するように設計されています。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74LV245A	DB (SSOP, 20)	7.20mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 4.40mm
	PW (TSSOP, 20)	6.50mm × 4.40mm
	RGY (VQFN, 20)	4.50mm × 3.50mm
	DW (SOIC, 20)	12.80mm × 7.50mm
	RKS (VQFN, 20)	4.50mm × 2.50mm
	DGS (VSSOP, 20)	5.10mm × 3.00mm
	DW (SOIC, 20)	12.80mm × 7.50mm
	N (PDIP, 20)	24.33mm × 6.35mm
	NS (SO, 20)	12.60mm × 5.30mm

- (1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



概略回路図



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Changes from Revision Q (April 2023) to Revision R (July 2023) Page

- Updated R0JA values: DB = 94.6 to 113.1, DW = 77.5 to 96.2, NS = 76.6 to 101.1; Updated DB, DW, and PW packages for R0JC(top), R0JB, Ψ JT, Ψ JB, and R0JC(bot), all values in °C/W5

Changes from Revision P (December 2022) to Revision Q (April 2023) Page

- DGS パッケージ情報を追加。1
- 「パッケージ情報」表を更新。1

Changes from Revision O (September 2014) to Revision P (December 2022) Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....1
- RKS パッケージ情報を追加。1

5 Pin Configuration and Functions

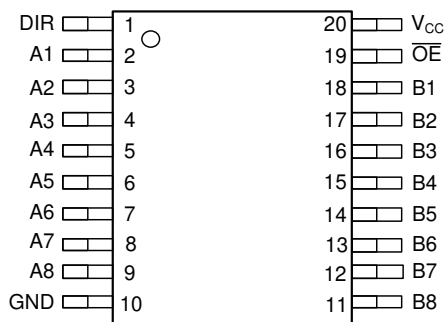


図 5-1. SN74LV245A: DB, DGV, DW, N, NS, PW or DGS, 20-Pin SSOP, TVSOP, SOIC, PDIP, SO, TSSOP, or VSSOP (Top View)

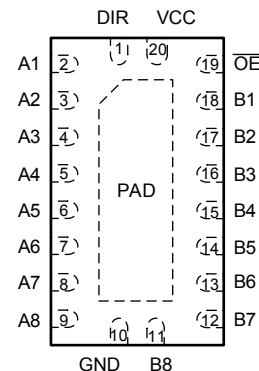


図 5-2. SN74LV245A: RGY or RKS Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction Pin
A1	2	I/O	A1 I/O
A2	3	I/O	A2 I/O
A3	4	I/O	A3 I/O
A4	5	I/O	A4 I/O
A5	6	I/O	A5 I/O
A6	7	I/O	A6 I/O
A7	8	I/O	A7 I/O
A8	9	I/O	A8 I/O
GND	10	—	Ground Pin
B8	11	I/O	B8 I/O
B7	12	I/O	B7 I/O
B6	13	I/O	B6 I/O
B5	14	I/O	B5 I/O
B4	15	I/O	B4 I/O
B3	16	I/O	B3 I/O
B2	17	I/O	B2 I/O
B1	18	I/O	B1 I/O
OE	19	I	Output Enable
V _{CC}	20	—	Power Pin

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range	Except I/O ports ⁽²⁾	–0.5	7	V
		I/O ports ⁽²⁾ (3)	–0.5	7	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	7	V
V_O	Output voltage range applied in the high or low state ⁽²⁾ (3)		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LV245A		UNIT
			MIN	MAX	
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2	mA
		V _{CC} = 3 V to 3.6 V		–8	
		V _{CC} = 4.5 V to 5.5 V		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 V to 2.7 V		2	mA
		V _{CC} = 3 V to 3.6 V		8	
		V _{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	ns/V
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV245A								UNIT
		DB	DGV	DW	NS	PW	RGY	RKS	DGS	
		20 PINS								
R _{θJA}	Junction-to-ambient thermal resistance	113.1	114.8	96.2	101.1	101.5	34.1	67.7	118.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.9	30.1	63.6	67	35.6	38.4	72.4	57.7	
R _{θJB}	Junction-to-board thermal resistance	67.9	56.3	64.7	66.1	52.5	12.0	40.4	73.1	
Ψ _{JT}	Junction-to-top characterization parameter	39.3	0.9	40.5	37.6	2.2	0.8	10.3	5.7	
Ψ _{JB}	Junction-to-board characterization parameter	67.5	55.6	64.3	65.8	52.0	12.0	40.4	72.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	7.1	24.1	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	–40°C to 85°C SN74LV245A			–40°C to 125°C SN74LV245A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
		I _{OH} = –2 mA	2.3 V	2			2			
		I _{OH} = –8 mA	3 V	2.48			2.48			
		I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
		I _{OL} = 2 mA	2.3 V	0.4			0.4			
		I _{OL} = 8 mA	3 V	0.44			0.44			
		I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	Control inputs	V _I = 5.5 V or GND	0 to 5.5 V	±1			±1			μA
I _{OZ}	A or B port	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}		V _I or V _O = 0 to 5.5 V	0	5			5			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3						pF
			5 V	3						
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V	5.5						pF
			5 V	5.5						

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	C _L = 15 pF		8.3	13	1	15	1	17	ns
t _{en}	$\overline{\text{OE}}$	A or B			11.8	19.9	1	22	1	24	
t _{dis}	$\overline{\text{OE}}$	A or B			11.8	18.1	1	20	1	22	
t _{pd}	A or B	B or A	C _L = 50 pF		11.2	15.9	1	18	1	21	ns
t _{en}	$\overline{\text{OE}}$	A or B			14.1	22.7	1	26	1	28	
t _{dis}	$\overline{\text{OE}}$	A or B			17.6	23.1	1	25	1	27	
t _{sk(o)}						2		2			

6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	$C_L = 15\text{ pF}$		5.9	8.4	1	10	1	11	ns
t_{en}	$\overline{OE}$	A or B			8.2	13.2	1	15.5	1	16.5	
t_{dis}	$\overline{OE}$	A or B			9.6	16.5	1	19.5	1	20.5	
t_{pd}	A or B	B or A	$C_L = 50\text{ pF}$		7.9	11.9	1	13.5	1	14.5	ns
t_{en}	$\overline{OE}$	A or B			9.9	16.7	1	19	1	20	
t_{dis}	$\overline{OE}$	A or B			13.9	19.8	1	22	1	23	
$t_{sk(o)}$						1.5		1.5			

6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	$C_L = 15\text{ pF}$		4.3	5.5	1	6.5	1	7	ns
t_{en}	$\overline{OE}$	A or B			5.7	8.5	1	10	1	10.5	
t_{dis}	$\overline{OE}$	A or B			7.8	12.8	1	14.2	1	14.7	
t_{pd}	A or B	B or A	$C_L = 50\text{ pF}$		5.6	7.5	1	8.5	1	9	ns
t_{en}	$\overline{OE}$	A or B			7	10.6	1	12	1	12.5	
t_{dis}	$\overline{OE}$	A or B			10.9	14.7	1	16	1	16.5	
$t_{sk(o)}$						1		1			

6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	20	pF
				5 V	25	

6.11 Typical Characteristics

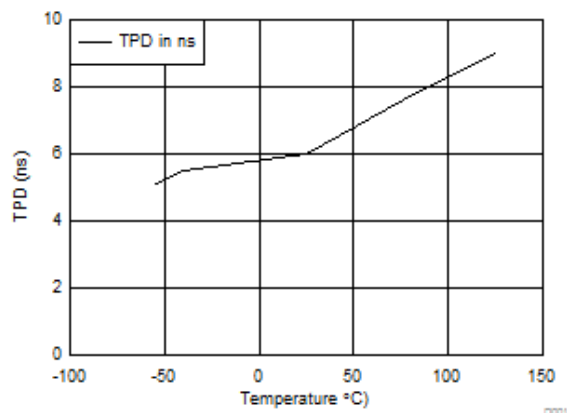


图 6-1. TPD vs Temperature at 3.3 V

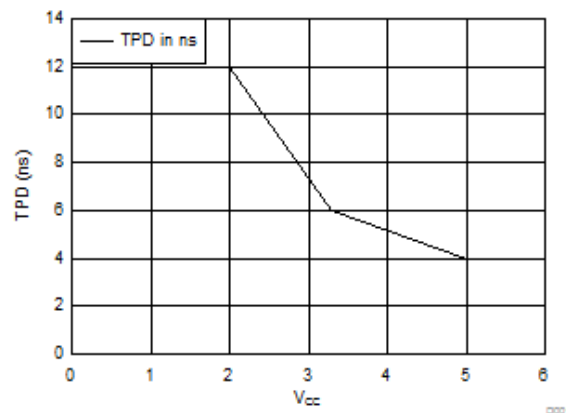
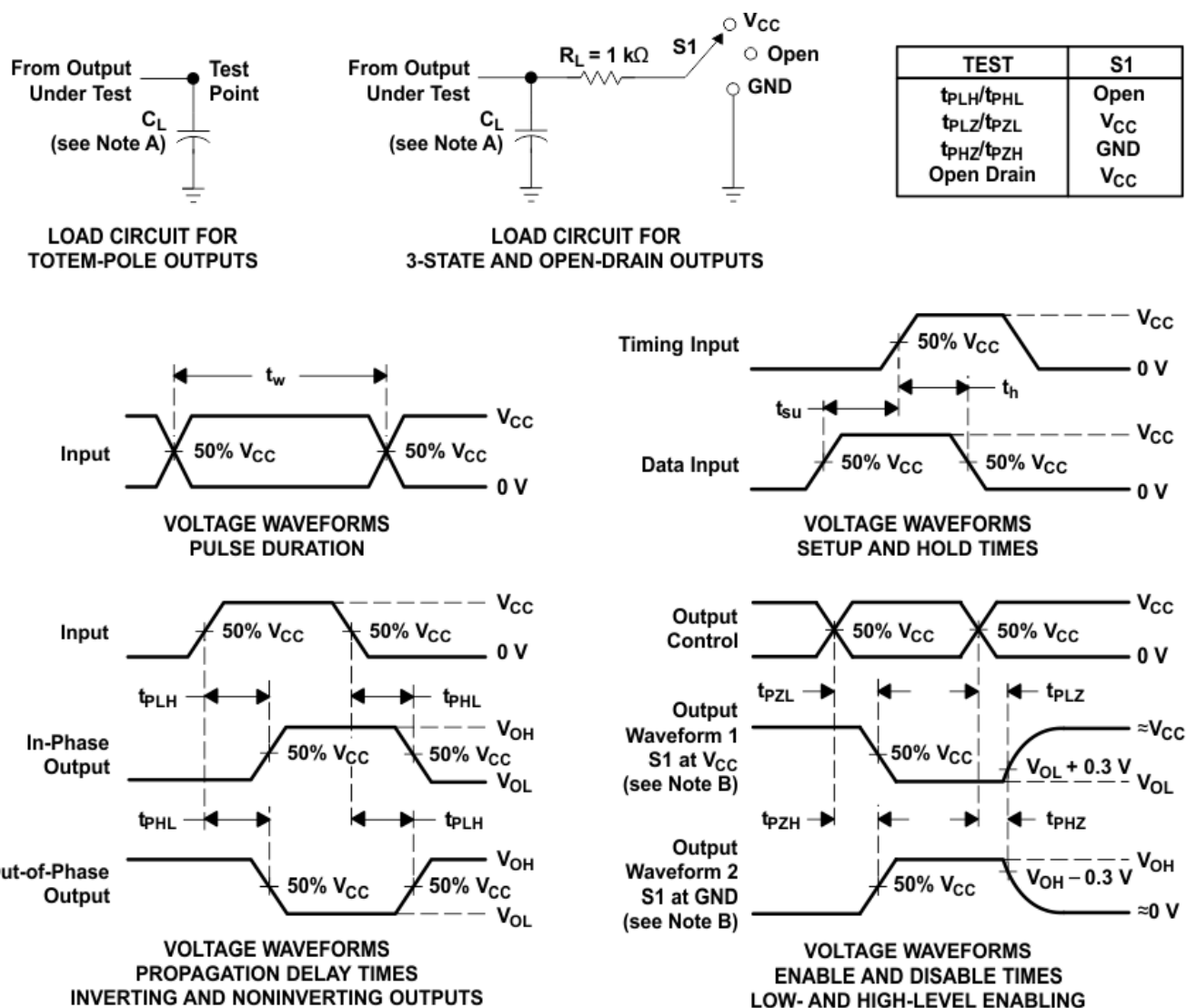


图 6-2. TPD vs V_{CC}

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

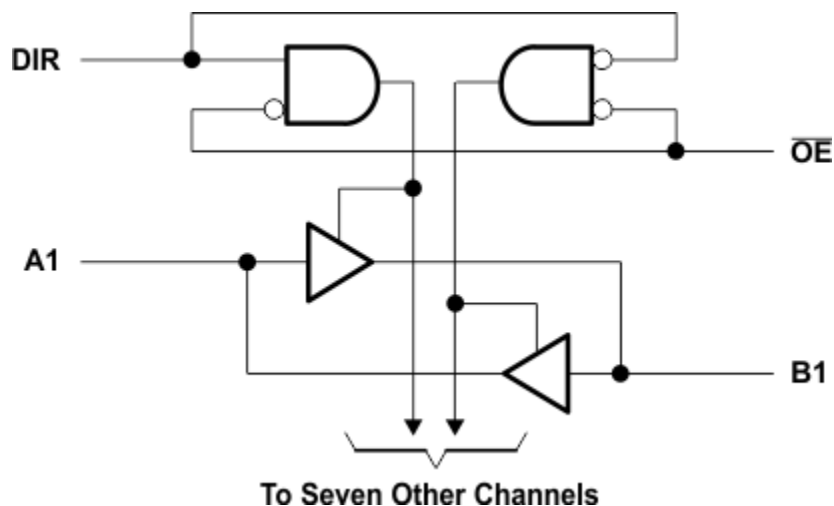


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- Allows down voltage translation from 5 V to 3.3 V
 - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74LV245A is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making the device ideal for down translation.

9.2 Typical Application

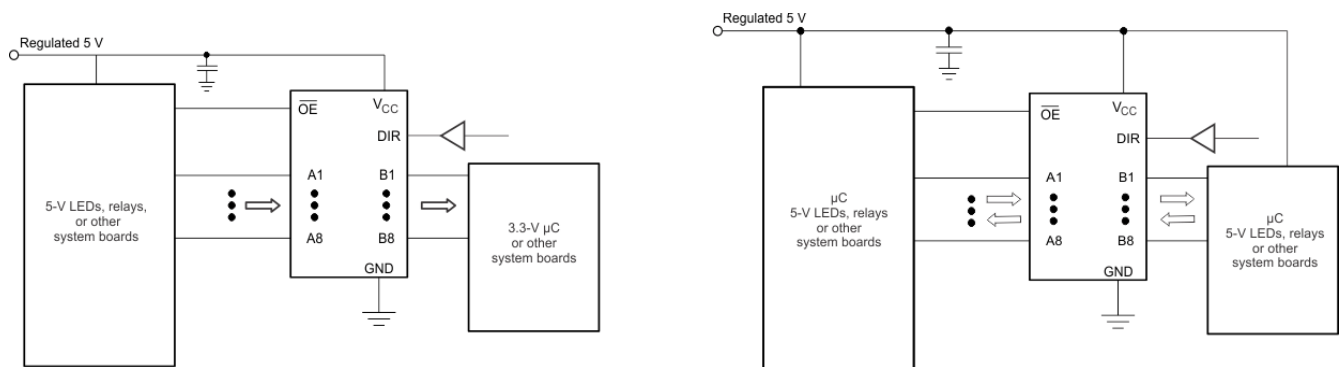


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive will also create faster edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Rise time and fall time specifications, see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#) table.
 - Specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend output conditions:
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

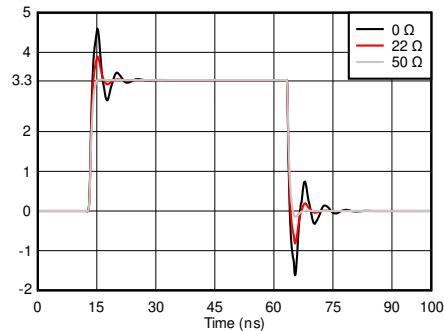


図 9-2. Application Timing Curve

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 図 9-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they cannot float when disabled.

9.4.2 Layout Example

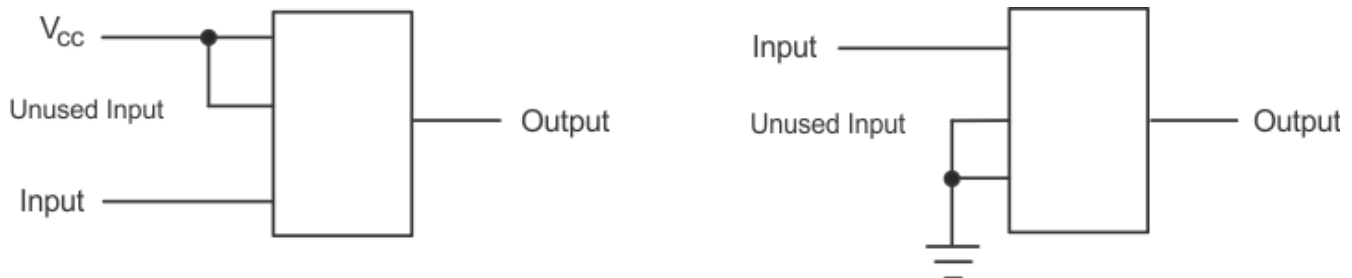


図 9-3. Layout Diagram

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://www.ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV245ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ADGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L245A
SN74LV245ADGSR.A	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L245A
SN74LV245ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ADGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV245A
SN74LV245ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV245A
SN74LV245ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV245A
SN74LV245APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV245A
SN74LV245APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWRG3	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWRG3.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245APWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV245A
SN74LV245ARGYR.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV245A
SN74LV245ARKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV245A
SN74LV245ARKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV245A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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