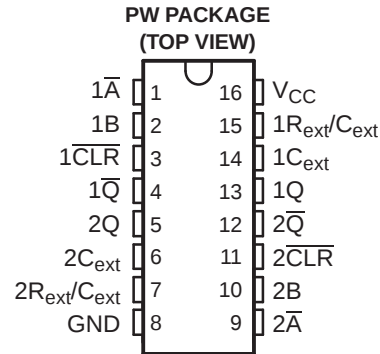


DUAL MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

Check for Samples: [SN74LV221A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 2-V to 5.5-V V_{CC} Operation
- Supports Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Transition Rates
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- I_{off} Supports Partial-Power-Down Mode Operation



DESCRIPTION/ORDERING INFORMATION

The SN74LV221A is a dual multivibrator designed for 2-V to 5.5-V V_{CC} operation. Each multivibrator has a negative-transition-triggered ($\overline{A}$) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the A input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear (CLR) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistor between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking CLR low.

Pulse triggering occurs at a particular voltage level and is not related directly to the transition time of the input pulse. The $\overline{A}$, B, and CLR inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the SN74LV221A-Q1 is shown in Figure 8. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 5.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



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Table 1. ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	SN74LV221AQPWRQ1	LV221AQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

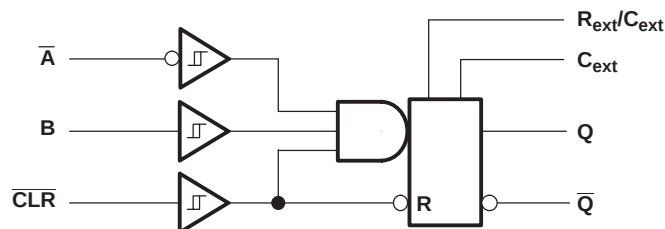
Pin assignments are identical to those of the SN74AHC123A and SN74AHCT123A devices, so the SN74LV221A-Q1 can be substituted for those devices not using the retrigger feature.

For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

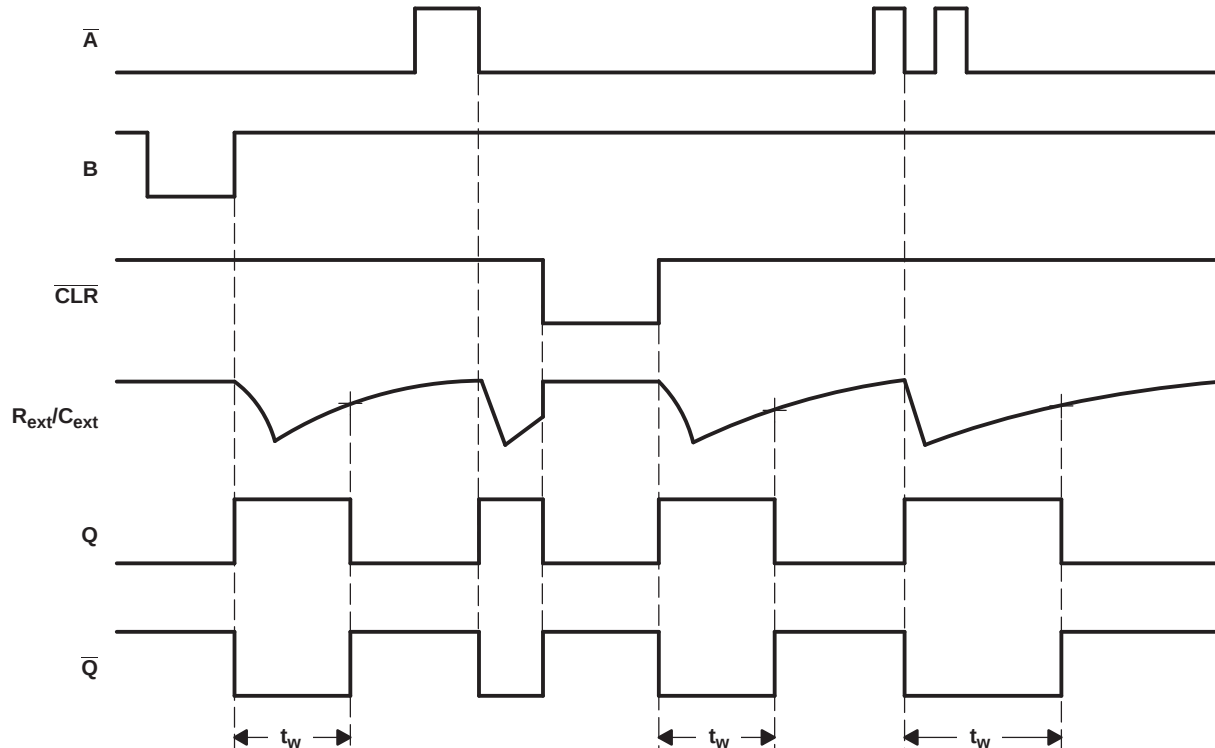
**FUNCTION TABLE
(EACH MULTIVIBRATOR)**

INPUTS			OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{A}}$	B	Q	$\overline{\text{Q}}$	
L	X	X	L	H	Reset
H	H	X	L	H	Inhibit
H	X	L	L	H	Inhibit
H	L	↑	⌋	⌋	Outputs enabled
H	↓	H	⌋	⌋	Outputs enabled
↑ ⁽¹⁾	L	H	⌋	⌋	Outputs enabled

- (1) This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to $\overline{\text{CLR}}$ going high. This latch is conditioned by taking either $\overline{\text{A}}$ high or B low while $\overline{\text{CLR}}$ is inactive (high).

LOGIC DIAGRAM (POSITIVE LOGIC)

INPUT/OUTPUT TIMING DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
V _I	Input voltage range ⁽²⁾		−0.5	7	V
V _O	Output voltage range in high or low state ⁽²⁾ ⁽³⁾		−0.5	V _{CC} + 0.5	V
V _O	Output voltage range in power-off state ⁽²⁾		−0.5	7	V
I _{IK}	Input clamp current	V _I < 0		−20	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾			108	°C/W
ESD rating ⁽⁵⁾	Human-Body Model			2 (H2)	kV
	Charged-Device Model			1 (C5)	
		Machine Model			200 (M3)
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) ESD protection level per AEC Q100 classification

Recommended Operating Conditions⁽¹⁾

			–40°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
R _{ext}	External timing resistance	V _{CC} = 2 V	5k		5k		Ω
		V _{CC} ≥ 3 V	1k		1k		
C _{ext}	External timing capacitance		No restriction		No restriction		pF
Δt/ΔV _{CC}	Power-up ramp rate		1		1		ms/V
T _A	Operating free-air temperature		–40	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	–40°C to 125°C			–40°C to 85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = –50 µA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
		I _{OH} = –2 mA	2.3 V	2			2			
		I _{OH} = –6 mA	3 V	2.48			2.48			
		I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}		I _{OL} = 50 µA	2 V to 5.5 V	0.1			0.1			V
		I _{OL} = 2 mA	2.3 V	0.4			0.4			
		I _{OL} = 6 mA	3 V	0.44			0.44			
		I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	$\overline{A}$, B _I , and $\overline{CLR}$	V _I = 5.5 V or GND	0	±1			±1			µA
			0 to 5.5 V	±1			±1			
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			µA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	3 V	280			280			µA
			4.5 V	650			650			
			5.5 V	975			975			
I _{off}		V _I or V _O = 0 to 5.5 V	0	10			5			µA
C _i		V _I = V _{CC} or GND	3.3 V	1.9			1.9			pF
			5 V	1.9			1.9			

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		–40°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{CLR}$	5		7		5		ns
		$\overline{A}$ or B trigger	5		7		5		

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		–40°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{CLR}$	5		7		5		ns
		$\overline{A}$ or B trigger	5		7		5		

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	$C_L = 50 \text{ pF}$		11.8	24.1	1	30.5	1	27.5	ns
	$\overline{CLR}$				10.6	19.3	1	25	1	22	
	$\overline{CLR}$ trigger				12.3	25.9	1	32.5	1	29.5	
$t_w^{(1)}$		Q or $\overline{Q}$	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$		186	240		340		300	ns
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \text{ }\mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	90	100	110	85	115	90	110	μs
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.85	1.15	0.9	1.1	ms
$\Delta t_w^{(2)}$			$C_L = 50 \text{ pF}$	± 1							%

(1) t_w = Pulse duration at Q and $\overline{Q}$ outputs

(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	$C_L = 50 \text{ pF}$		8.2	14	1	19	1	16	ns
	$\overline{CLR}$				7.4	11.4	1	16	1	13	
	$\overline{CLR}$ trigger				8.6	14.9	1	20	1	17	
$t_w^{(1)}$		Q or $\overline{Q}$	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$		171	200		280		240	ns
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \text{ }\mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	90	100	110	85	115	90	110	μs
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.85	1.15	0.9	1.1	ms
$\Delta t_w^{(2)}$			$C_L = 50 \text{ pF}$	± 1							%

(1) t_w = Pulse duration at Q and $\overline{Q}$ outputs

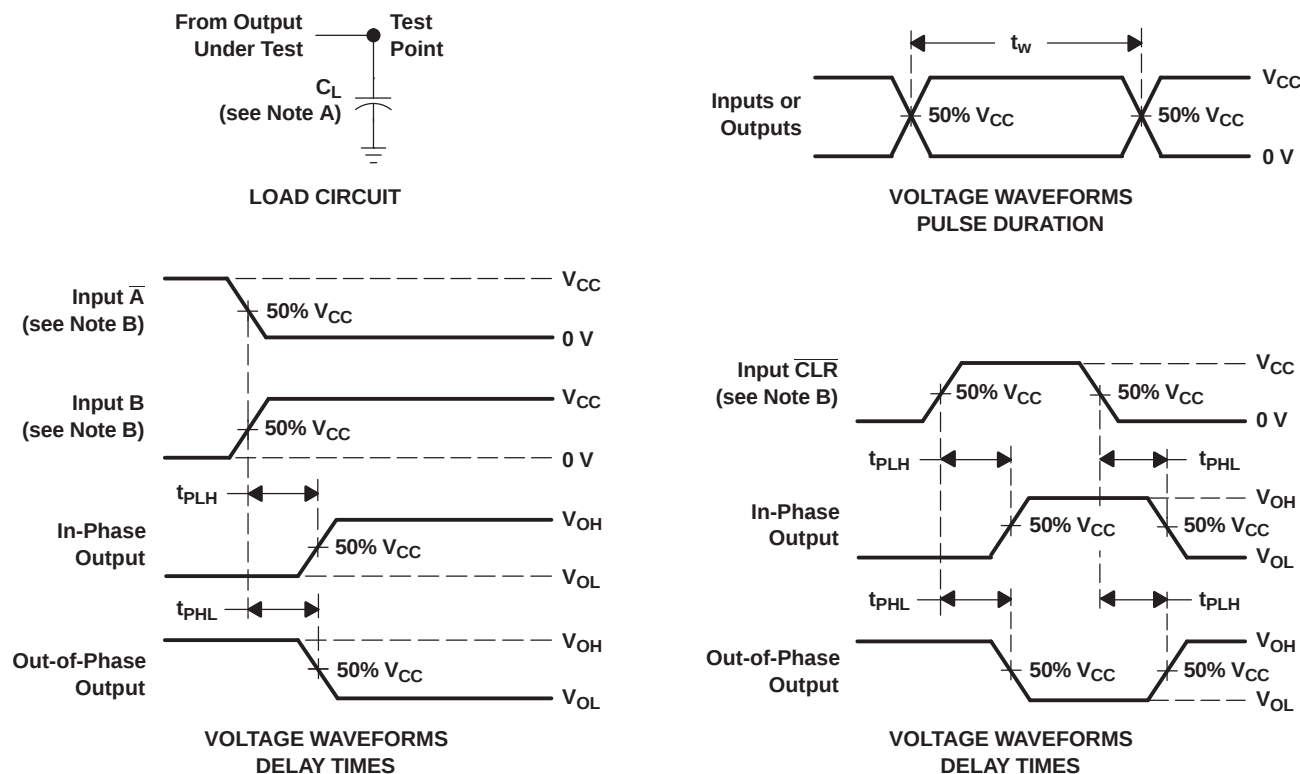
(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	50	pF
			5 V	51	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Caution in Use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

Power-Down Considerations

Large values of C_{ext} can cause problems when powering down the SN74LV221A-Q1 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30 \text{ mA}$. For example, if $V_{CC} = 5 \text{ V}$ and $C_{ext} = 15 \text{ pF}$, the V_{CC} supply must turn off no faster than $t = (5 \text{ V}) \times (15 \text{ pF})/30 \text{ mA} = 2.5 \text{ ns}$. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the SN74LV221A-Q1 can sustain damage. To avoid this possibility, use external clamping diodes.

Output Pulse Duration

The output pulse duration, t_w , is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in [Figure 2](#).

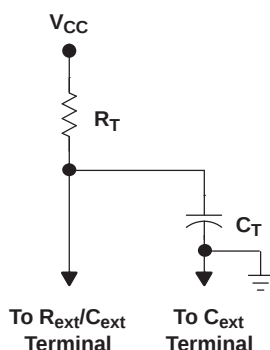


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T$$

if $C_T \geq 1000 \text{ pF}$, $K = 1.0$

or

if C_T is $< 1000 \text{ pF}$, K can be determined from [Figure 7](#)

where:

t_w = pulse duration in ns

R_T = external timing resistance in $k\Omega$

C_T = external capacitance in pF

K = multiplier factor

(1)

[Equation 1](#) and [Figure 3](#) or [Figure 4](#) can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

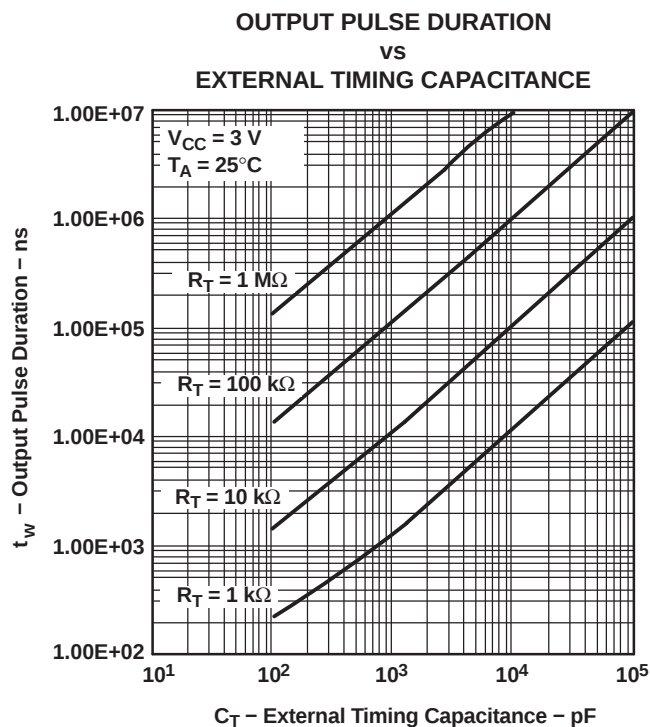


Figure 3.

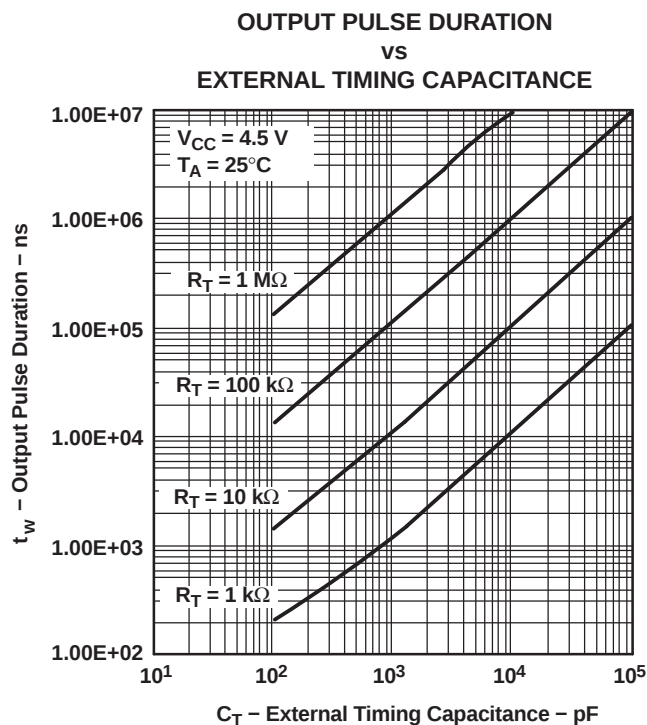


Figure 4.

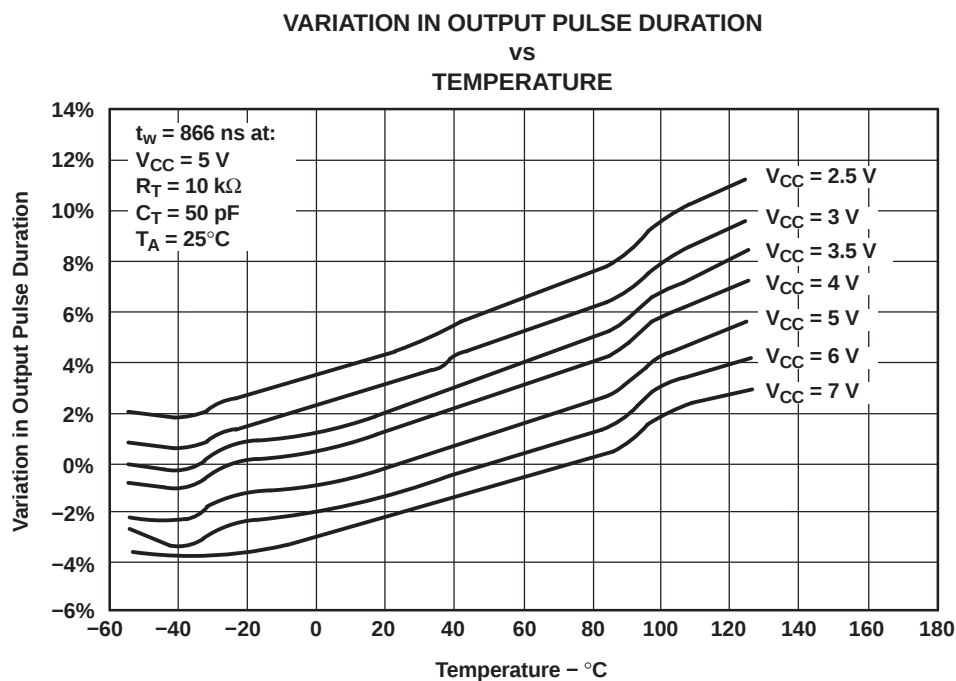


Figure 5.

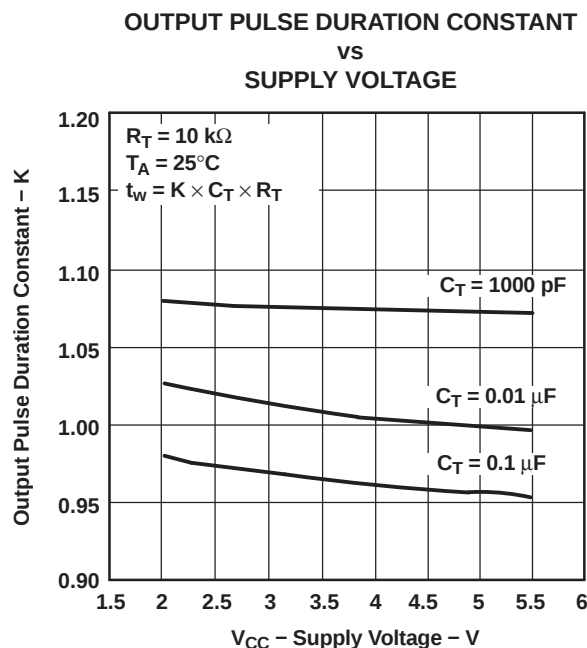


Figure 6.

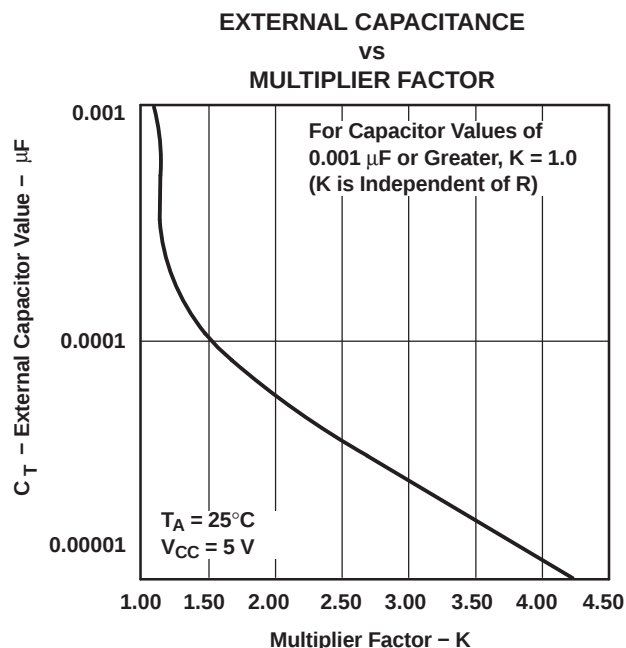


Figure 7.

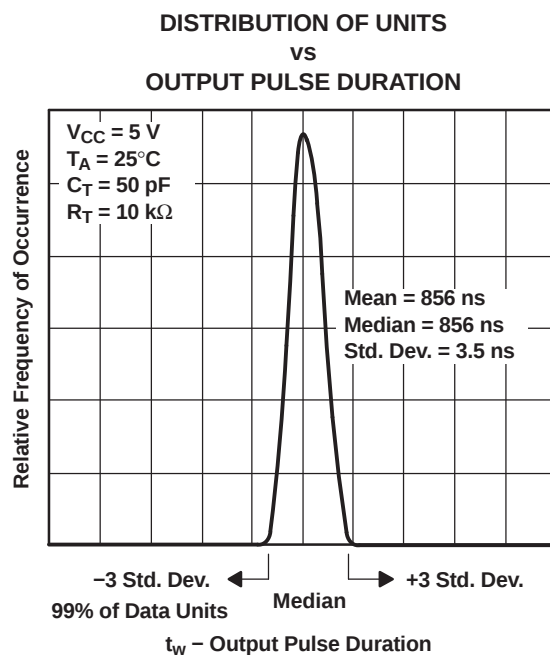


Figure 8.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV221AQPWRG4Q1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV221AQ
SN74LV221AQPWRG4Q1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV221AQ
SN74LV221AQPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV221AQ
SN74LV221AQPWRQ1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV221AQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV221A-Q1 :

- Catalog : [SN74LV221A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV221AQPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV221AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV221AQPWRG4Q1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV221AQPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0



PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



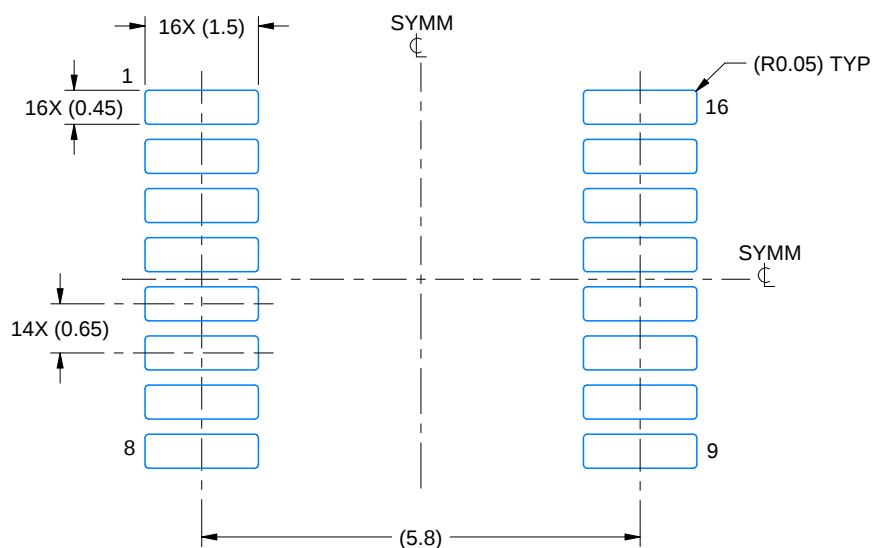
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

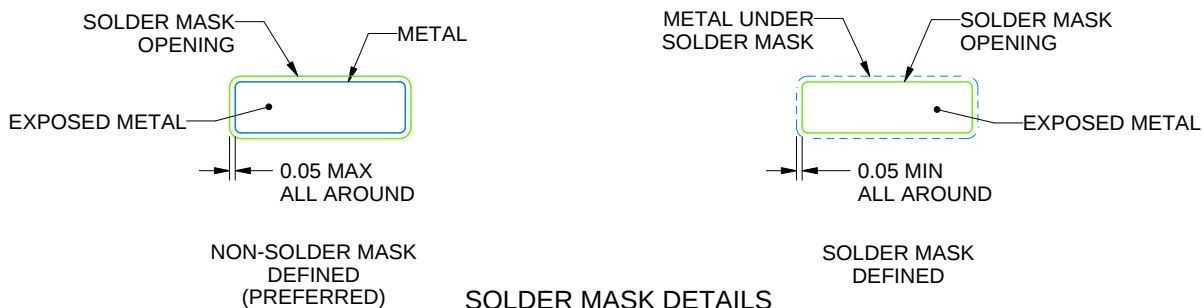
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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