

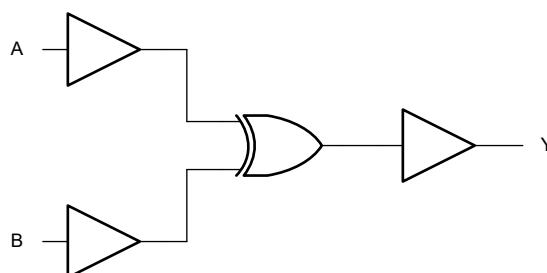
SN74LV1T86-Q1 車載用単一電源 2 入力排他 OR ゲート CMOS ロジック・レベル・シフタ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - デバイス温度グレード 1: -40°C ~ +125°C
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- 幅広い動作範囲: 1.8V ~ 5.5V
- 単一電源電圧トランスレータ (「LVxT 拡張入力電圧」を参照):
 - 昇圧変換:
 - 1.2V ~ 1.8V
 - 1.5V ~ 2.5V
 - 1.8V ~ 3.3V
 - 3.3V ~ 5.0V
 - 降圧変換:
 - 5.0V、3.3V、2.5V から 1.8V
 - 5.0V、3.3V から 2.5V
 - 5.0V ~ 3.3V
- 5.5V 耐圧入力ピン
- 標準ピン配置をサポート
- 5V または 3.3V の V_{CC} で最大 150Mbps
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- 複数の入力信号の位相差を検出
- 選択可能なインバータまたはバッファの作成



概略論理図 (正論理)

3 概要

SN74LV1T86-Q1 は 2 入力 XOR ゲートです。本デバイスはブール関数 $Y = A \oplus B$ を正論理で実行します。出力レベルは電源電圧 (V_{CC}) を基準としており、1.8V、2.5V、3.3V、5V の CMOS レベルをサポートしています。

入力は低スレッショルド回路を使用して設計され、低電圧 CMOS 入力の昇圧変換 (例: 1.2V 入力から 1.8V 出力、1.8V 入力から 3.3V 出力) をサポートします。また、5V 許容の入力ピンにより、降圧変換 (例: 3.3V から 2.5V 出力) が可能です。

パッケージ情報

| 部品番号 | パッケージ (1) | パッケージ サイズ (2) | 本体サイズ (3) |
|---------------|----------------|---------------|---------------|
| SN74LV1T86-Q1 | DCK (SC-70、5) | 2mm × 2.1mm | 2mm × 1.25mm |
| | DBV (SOT-23、5) | 2.9mm × 2.8mm | 2.9mm × 1.6mm |

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ×幅) は公称値で、該当する場合はピンも含まれます。
- 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 特長 | 1 | 7.4 Device Functional Modes..... | 13 |
| 2 アプリケーション | 1 | 8 Application and Implementation | 14 |
| 3 概要 | 1 | 8.1 Application Information..... | 14 |
| 4 Pin Configuration and Functions | 3 | 8.2 Typical Application..... | 14 |
| 5 Specifications | 4 | 8.3 Power Supply Recommendations..... | 16 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.4 Layout..... | 16 |
| 5.2 ESD Ratings..... | 4 | 9 Device and Documentation Support | 17 |
| 5.3 Recommended Operating Conditions..... | 4 | 9.1 Documentation Support..... | 17 |
| 5.4 Thermal Information..... | 5 | 9.2 ドキュメントの更新通知を受け取る方法..... | 17 |
| 5.5 Electrical Characteristics..... | 5 | 9.3 サポート・リソース..... | 17 |
| 5.6 Switching Characteristics..... | 6 | 9.4 Trademarks..... | 17 |
| 5.7 Typical Characteristics..... | 7 | 9.5 静電気放電に関する注意事項..... | 17 |
| 6 Parameter Measurement Information | 10 | 9.6 用語集..... | 17 |
| 7 Detailed Description | 11 | 10 Revision History | 17 |
| 7.1 Overview..... | 11 | 11 Mechanical, Packaging, and Orderable Information | 18 |
| 7.2 Functional Block Diagram..... | 11 | | |
| 7.3 Feature Description..... | 11 | | |

4 Pin Configuration and Functions

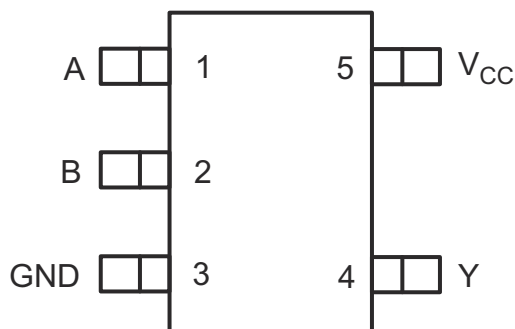


図 4-1. SN74LV1T86-Q1 DBV Package, 5-Pin SOT-23; DCK Package, 5-Pin SC-70 (Top View)

表 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-----|---------------------|-----------------|
| NAME | NO. | | |
| A | 1 | I | Input A |
| B | 2 | I | Input B |
| GND | 3 | G | Ground |
| Y | 4 | O | Output Y |
| V _{CC} | 5 | P | Positive Supply |

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------|--|-----------------------------|------|----------------|------|
| V_{CC} | Supply voltage | | -0.5 | 7 | V |
| V_I | Input voltage range | | -0.5 | 7 | V |
| V_O | Output voltage range | | -0.5 | $V_{CC} + 0.5$ | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state | | -0.5 | 4.6 | V |
| I_{IK} | Input clamp current ⁽²⁾ | $V_I < 0$ | -20 | | mA |
| I_{OK} | Output clamp current ⁽²⁾ | $V_O < 0$ or $V_O > V_{CC}$ | -20 | 20 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | -25 | 25 | mA |
| I_O | Continuous output current through V_{CC} or GND | | -50 | 50 | mA |
| T_J | Junction temperature | | | 150 | °C |
| T_{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|--|-----------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2 | ±200 0 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±100 0 | |

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|--------------------------|---|------|----------|------|
| V_{CC} | Supply voltage | | 1.6 | 5.5 | V |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65\text{ V to }2\text{ V}$ | 1.1 | | V |
| | | $V_{CC} = 2.25\text{ V to }2.75\text{ V}$ | 1.28 | | V |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 1.45 | | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 2.00 | | V |
| V_{IL} | Low-Level input voltage | $V_{CC} = 1.65\text{ V to }2\text{ V}$ | | 0.50 | V |
| | | $V_{CC} = 2.25\text{ V to }2.75\text{ V}$ | | 0.65 | V |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 0.75 | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 0.85 | V |
| I_O | Output current | $V_{CC} = 1.6\text{ V to }2\text{ V}$ | | ±3 | mA |
| | | $V_{CC} = 2.25\text{ V to }2.75\text{ V}$ | | ±7 | mA |
| | | $V_{CC} = 3.3\text{ V to }5.0\text{ V}$ | | ±15 | mA |

5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|-----|-----|------|
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 1.6 \text{ V to } 5.0 \text{ V}$ | | 20 | ns/V |
| T_A | Operating free-air temperature | | -40 | 125 | C |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LV1T86-Q1 | | UNIT |
|-------------------------------|--|---------------|------------|------|
| | | DBV (SOT-23) | DCK (SC70) | |
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278.0 | 293.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 180.5 | 208.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 184.4 | 180.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 115.4 | 120.6 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 183.4 | 179.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 125^\circ\text{C}$ | | | UNIT |
|-----------------|--|-----------------|--------------------------|---------------------|------|---|-----|---------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{OH} | $I_{OH} = -50 \mu\text{A}$ | 1.65 V to 5.5 V | $V_{CC}-0.1$ | | | $V_{CC}-0.1$ | | | V |
| | $I_{OH} = -2 \text{ mA}$ | 1.65 V | 1.28 | 1.7 ⁽¹⁾ | | 1.21 | | | |
| | $I_{OH} = -3 \text{ mA}$ | 2.25 V | 2 | 2.4 ⁽¹⁾ | | 1.93 | | | |
| | $I_{OH} = -5.5 \text{ mA}$ | 3.0 V | 2.6 | 3.08 ⁽¹⁾ | | 2.49 | | | |
| | $I_{OH} = -8 \text{ mA}$ | 4.5 V | 4.1 | 4.65 ⁽¹⁾ | | 3.95 | | | |
| V_{OL} | $I_{OH} = 50 \mu\text{A}$ | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OH} = 2 \text{ mA}$ | 1.65 V | | 0.1 ⁽¹⁾ | 0.2 | | | 0.25 | |
| | $I_{OH} = 3 \text{ mA}$ | 2.25 V | | 0.1 ⁽¹⁾ | 0.15 | | | 0.2 | |
| | $I_{OH} = 5.5 \text{ mA}$ | 3.0 V | | 0.2 ⁽¹⁾ | 0.2 | | | 0.25 | |
| | $I_{OH} = 8 \text{ mA}$ | 4.5 V | | 0.3 ⁽¹⁾ | 0.3 | | | 0.35 | |
| I_{CC} | $V_I = V_{CC} \text{ or GND, } I_O = 0$ | 5 V | | | 1 | | | 10 | μA |
| | | 3.3 V | | | 1 | | | 10 | |
| | | 2.5 V | | | 1 | | | 10 | |
| | | 1.8 V | | | 1 | | | 10 | |
| ΔI_{CC} | One input at 0.3 V or 3.4 V, other inputs at V_{CC} or GND | 5.5 V | | | 1.35 | | | 1.5 | mA |
| | One input at 0.3 V or 1.1 V, other inputs at V_{CC} or GND | 1.8 V | | | 10 | | | 10 | μA |
| I_I | $V_I = 0 \text{ V to } V_{CC}$ | | | | 0.12 | | | ± 1 | μA |
| C_i | $V_I = V_{CC} \text{ or GND}$ | 3.3 V | | 2 | 10 | | 2 | 10 | pF |
| C_O | $V_O = V_{CC} \text{ or GND}$ | 3.3 V | | 2.5 | | | 2.5 | | pF |

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | -40°C to 125°C | | | UNIT |
|------------------------------------|----------------------|-----------------|-----------------------|-----|-----|----------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| C _{PD} ^{(2) (3)} | F = 1 MHz and 10 MHz | 1.8 V | | 14 | | | | | pF |
| | | 2.5 V | | 14 | | | | | |
| | | 3.3 V | | 14 | | | | | |
| | | 5.5 V | | 14 | | | | | |

(1) Typical value at nearest nominal voltage (1.8 V; 2.5 V; 3.3 V; 5 V)

(2) C_{PD} is used to determine the dynamic power consumption, per channel.

(3) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where F_I = input frequency, C_L = output load capacitance, V_{CC} = supply voltage

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | V _{CC} | T _A = 25°C | | | -40°C to 125°C | | | UNIT |
|------------------|-----------------|----------------|---------------------|-----------------|-----------------------|------|------|----------------|------|------|------|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| T _{PLH} | A or B | Y | CL = 15 pF | 5 V | | 3.4 | 4.1 | 1 | 4.1 | 4.7 | ns |
| T _{PHL} | A or B | Y | CL = 15 pF | 5 V | | 3.4 | 4.1 | 1 | 4.1 | 4.7 | ns |
| T _{PLH} | A or B | Y | CL = 50 pF | 5 V | | 3.9 | 5.3 | 1 | 4.9 | 6.3 | ns |
| T _{PHL} | A or B | Y | CL = 50 pF | 5 V | | 3.9 | 5.3 | 1 | 4.9 | 6.3 | ns |
| T _{PLH} | A or B | Y | CL = 15 pF | 3.3 V | | 4.9 | 5.9 | 1 | 6 | 7.3 | ns |
| T _{PHL} | A or B | Y | CL = 15 pF | 3.3 V | | 4.9 | 5.9 | 1 | 6 | 7.3 | ns |
| T _{PLH} | A or B | Y | CL = 50 pF | 3.3 V | | 5.9 | 7.2 | 1 | 7.1 | 8.8 | ns |
| T _{PHL} | A or B | Y | CL = 50 pF | 3.3 V | | 5.9 | 7.2 | 1 | 7.1 | 8.8 | ns |
| T _{PLH} | A or B | Y | CL = 15 pF | 2.5 V | | 6.3 | 7.9 | 1 | 7.4 | 9.5 | ns |
| T _{PHL} | A or B | Y | CL = 15 pF | 2.5 V | | 6.3 | 7.9 | 1 | 7.4 | 9.5 | ns |
| T _{PLH} | A or B | Y | CL = 50 pF | 2.5 V | | 7.4 | 9.6 | 1 | 8.9 | 11.5 | ns |
| T _{PHL} | A or B | Y | CL = 50 pF | 2.5 V | | 7.4 | 9.6 | 1 | 8.9 | 11.5 | ns |
| T _{PLH} | A or B | Y | CL = 15 pF | 1.8 V | | 8.8 | 12.7 | 1 | 10.4 | 14.9 | ns |
| T _{PHL} | A or B | Y | CL = 15 pF | 1.8 V | | 8.8 | 12.7 | 1 | 10.4 | 14.9 | ns |
| T _{PLH} | A or B | Y | CL = 50 pF | 1.8 V | | 10.8 | 15.7 | 1 | 12.7 | 18.3 | ns |
| T _{PHL} | A or B | Y | CL = 50 pF | 1.8 V | | 10.8 | 15.7 | 1 | 12.7 | 18.3 | ns |

5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

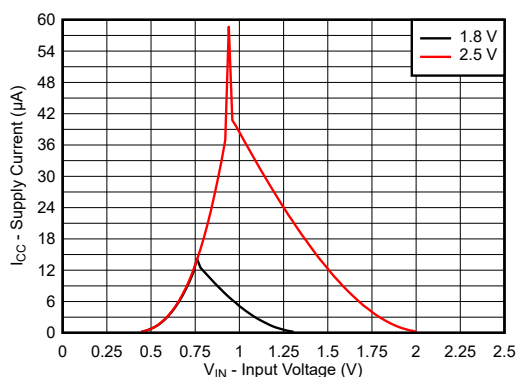


図 5-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

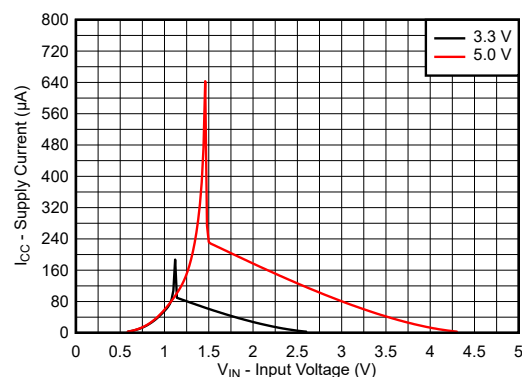


図 5-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

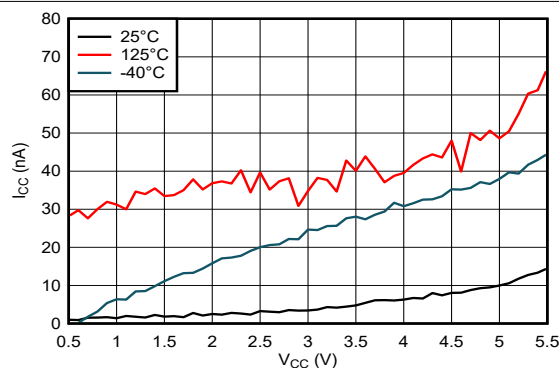


図 5-3. Supply Current Across Supply Voltage

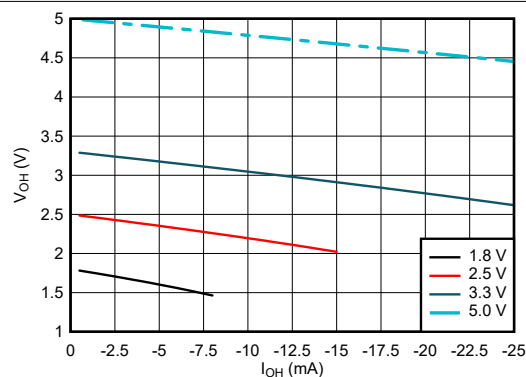


図 5-4. Output Voltage vs Current in HIGH State

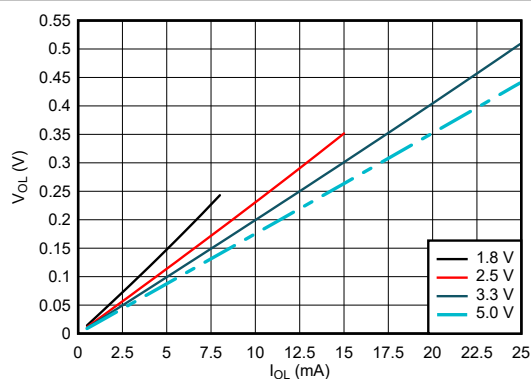


図 5-5. Output Voltage vs Current in LOW State

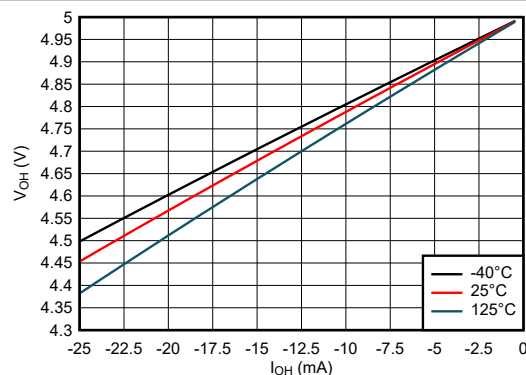


図 5-6. Output Voltage vs Current in HIGH State; 5-V Supply

5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

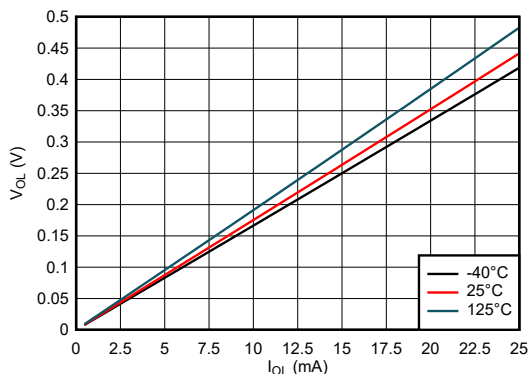


図 5-7. Output Voltage vs Current in LOW State; 5-V Supply

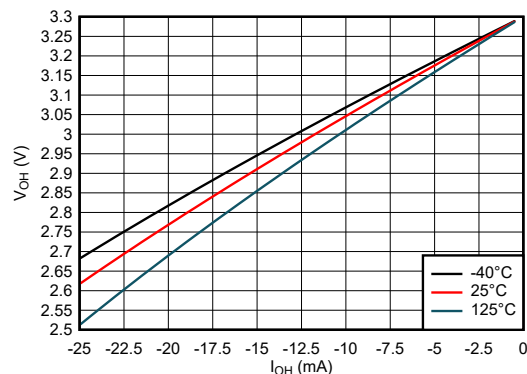


図 5-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

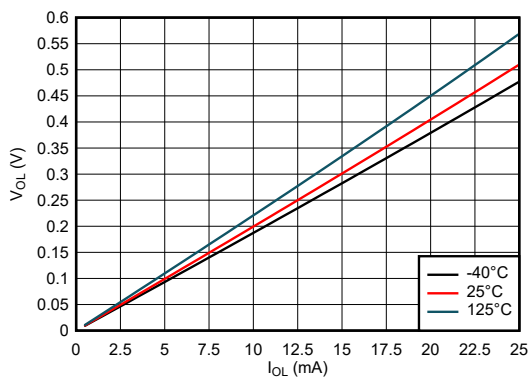


図 5-9. Output Voltage vs Current in LOW State; 3.3-V Supply

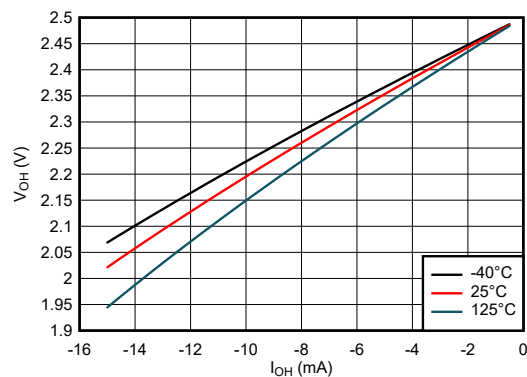


図 5-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

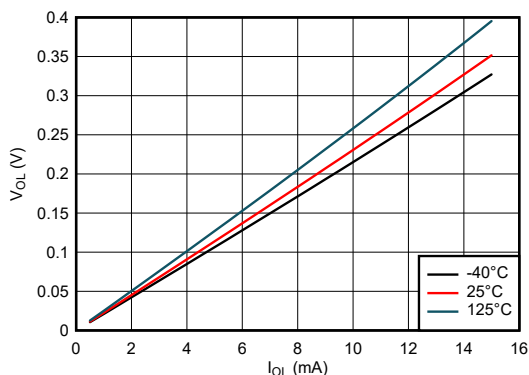


図 5-11. Output Voltage vs Current in LOW State; 2.5-V Supply

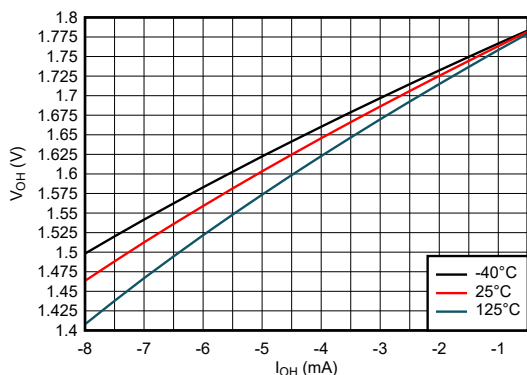


図 5-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

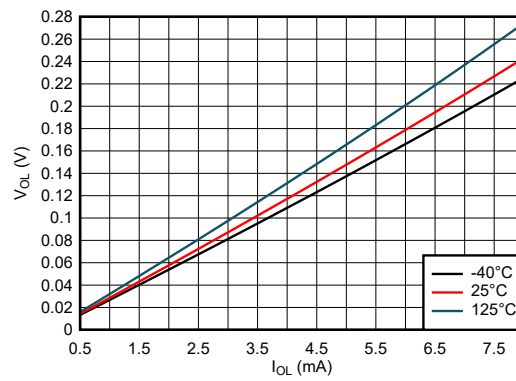


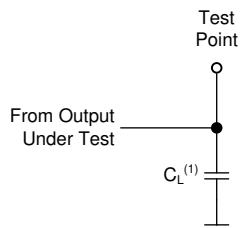
FIG 5-13. Output Voltage vs Current in LOW State; 1.8-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 3 \text{ ns}$.

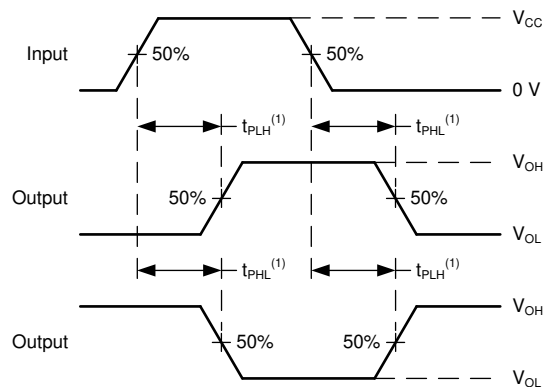
For clock inputs, f_{\max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



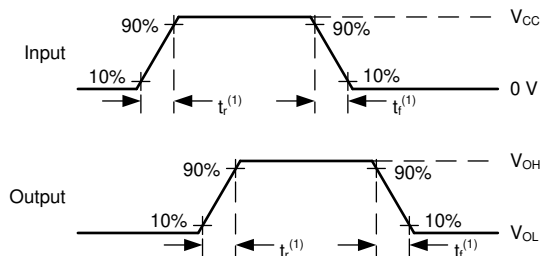
(1) C_L includes probe and test-fixture capacitance.

FIG 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

FIG 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

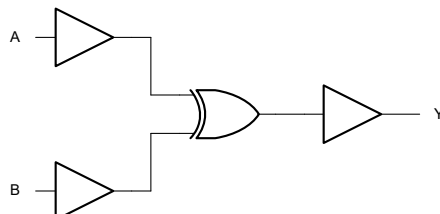
FIG 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LV1T86-Q1 is a 2-input XOR Gates which performs the Boolean function $Y = A \oplus B$ in positive logic. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

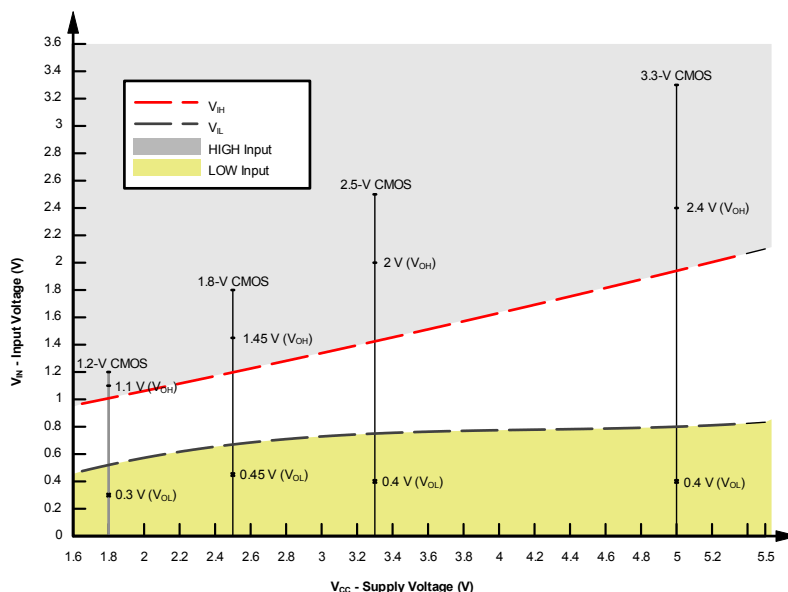
7.3.2 LVxT Enhanced Input Voltage

The SN74LV1T86-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. [Figure 7-1](#) shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k Ω resistor is recommended and will typically meet all requirements.



7-1. LVxT Input Voltage Levels

7.3.2.1 Down Translation

Signals can be translated down using the SN74LV1T86-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. As shown in 7-1, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in 7-2 for example, the standard CMOS inputs for devices operating at 5.0-V, 3.3-V or 2.5-V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC} .

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5-V, 3.3-V, and 5.0-V
- 2.5-V V_{CC} – Inputs from 3.3-V and 5.0-V
- 3.3-V V_{CC} – Inputs from 5.0-V

7.3.2.2 Up Translation

Input signals can be up translated using the SN74LV1T86-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV1T86-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in 7-2, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2-V
- 2.5-V V_{CC} – Inputs from 1.8-V

- 3.3-V V_{CC} – Inputs from 1.8-V and 2.5-V
- 5.0-V V_{CC} – Inputs from 2.5-V and 3.3-V

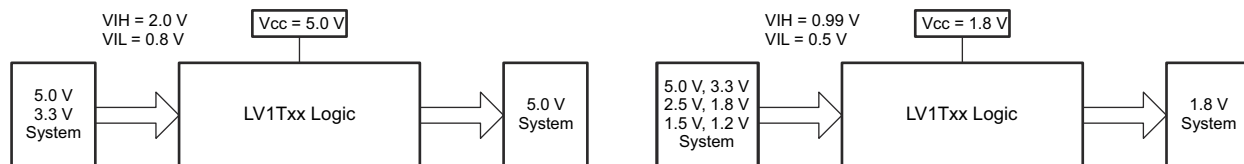


図 7-2. LVxT Up and Down Translation Example

7.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in 図 7-3.

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

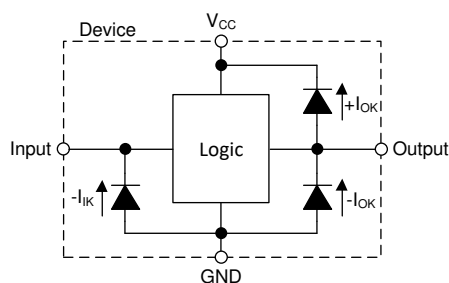


図 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74LV1T86-Q1.

表 7-1. Function Table

| INPUTS ⁽¹⁾ | | OUTPUT Y |
|-----------------------|---|-------------|
| A | B | |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in 図 8-1.

The SN74LV1T86-Q1 is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

Typically, clock signals have fast transition rates, but additional filtering can be added to the clock signals which can lead to slower transitions rates. This makes the SN74LV1T86-Q1 an excellent choice for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

8.2 Typical Application

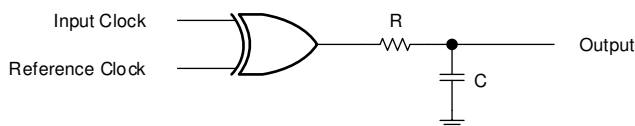


図 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV1T86-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV1T86-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV1T86-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV1T86-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

注意

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV1T86-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV1T86-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

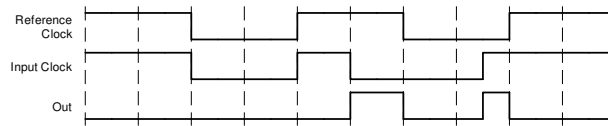
Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV1T86-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. Doing this will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.2.3 Application Curves



8-2. Application Timing Diagram

8.3 Power Supply Recommendations

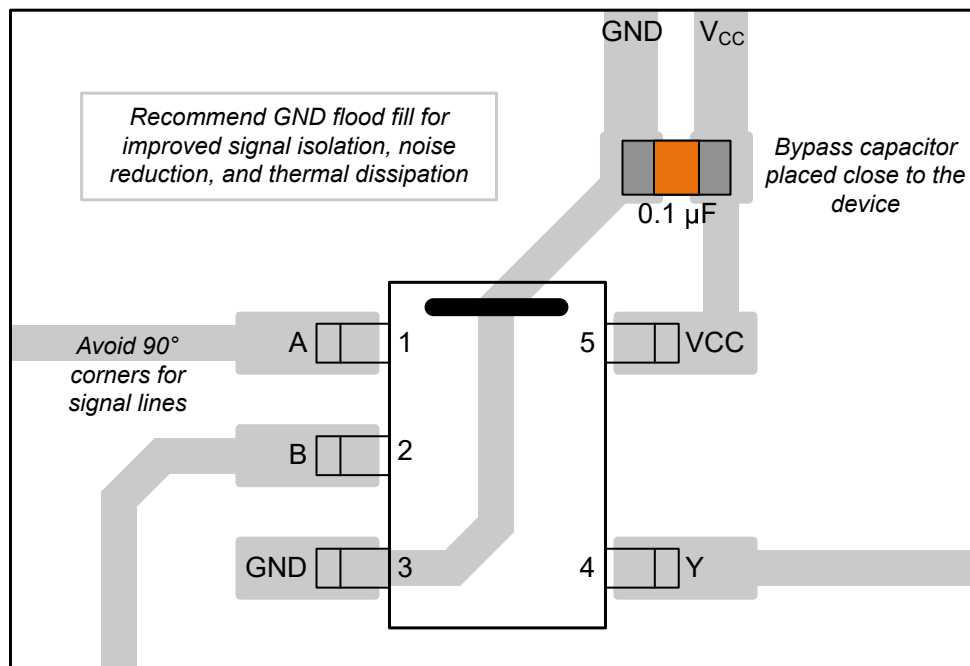
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example



8-3. Example Layout for the SN74LV1T86-Q1

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

| Changes from Revision * (August 2023) to Revision A (January 2024) | Page |
|---|------|
| • 「パッケージ情報」表に DBV パッケージを追加 | 1 |
| • Added DBV package to <i>Pin Configuration and Functions</i> section..... | 3 |
| • Added thermal values for DBV package: RθJA = 278.0, RθJC(top) = 180.5, RθJB = 184.4, ΨJT = 115.4, ΨJB = 183.4, RθJC(bot) = N/A, all values in °C/W..... | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74LV1T86QDBVRQ1 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 3BAH |
| SN74LV1T86QDBVRQ1.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 3BAH |
| SN74LV1T86QDCKRQ1 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1PO |
| SN74LV1T86QDCKRQ1.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1PO |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV1T86-Q1 :

- Catalog : [SN74LV1T86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV1T86QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LV1T86QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV1T86QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LV1T86QDCKRQ1 | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとしします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated