SN74LV08A Quadruple 2-Input Positive-AND Gates

1 Features

- 2V to 5.5V V_{CC} operation
- Max t_{pd} of 7ns at 5V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2.3V at V_{CC} = 3.3V, T_A = 25°C
- Support mixed-mode voltage operation on all ports
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Servers
- Telecom Infrastructure
- PCs and Notebooks
- Combining Power Good Signals

3 Description

This quadruple 2-input positive-AND gate is designed for 2V to 5.5V V_{CC} operation. The SN74LV08A device performs the Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV08A	DGV (TVSOP, 14)	3.60mm × 4.40mm
	D (SOIC, 14)	8.65mm × 3.91mm
	RGY (VQFN, 14)	3.50mm × 3.50mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

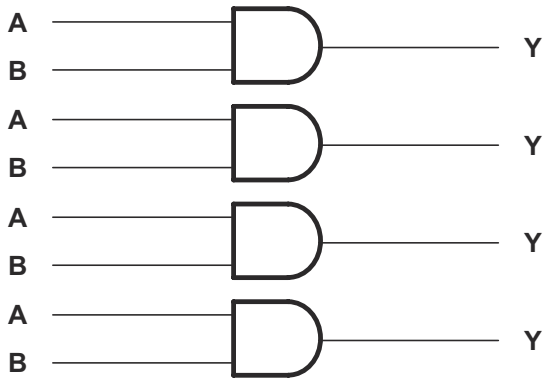

Figure 3-1. Simplified Schematic

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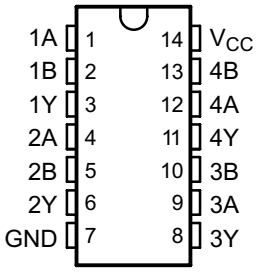
4 Pin Configuration and Functions

SN74LV08A . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



SN74LV08A . . . RGY PACKAGE (TOP VIEW)

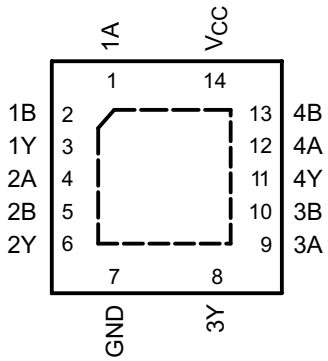


Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	SN74LV08A D, DB, DGV, NS, PW, RGY		
1A	1	I	1A Input
1B	2	I	1B Input
1Y	3	O	1Y Output
2A	4	I	2A Input
2B	5	I	2B Input
2Y	6	O	2Y Output
3Y	8	O	3Y Output
3A	9	I	3A Input
3B	10	I	3B Input
4Y	11	O	4Y Output
4A	12	I	4A Input
4B	13	I	4B Input
GND	7	—	Ground Pin
V_{CC}	14	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2) (3)		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV08A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 2.3V to 2.7V	V_{CC} × 0.7		
		V_{CC} = 3V to 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5V to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2V		0.5	V
		V_{CC} = 2.3V to 2.7V		V_{CC} × 0.3	
		V_{CC} = 3V to 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5V to 5.5V		V_{CC} × 0.3 5	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2V		–50	µA
		V_{CC} = 2.3V to 2.7V		–2	mA
		V_{CC} = 3V to 3.6V		–6	
		V_{CC} = 4.5V to 5.5V		–12	
I_{OL}	Low-level output current	V_{CC} = 2V		50	µA
		V_{CC} = 2.3V to 2.7V		2	mA
		V_{CC} = 3V to 3.6V		6	
		V_{CC} = 4.5V to 5.5V		12	
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2.3V to 2.7V		200	ns/V
		V_{CC} = 3V to 3.6V		100	
		V_{CC} = 4.5V to 5.5V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC(1)		SN74LV08A							UNIT
		D	DB	DGV	N	NS	PW	RGY	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.6	107.1	129.0	57.4	90.7	122.6	57.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	59.6	52.1	44.9	48.3	51.4	70.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	54.4	62.0	37.2	49.4	64.4	33.6	
ψ_{JT}	Junction-to-top characterization parameter	14.7	20.5	6.5	30.1	14.6	6.7	3.4	
ψ_{JB}	Junction-to-board characterization parameter	44.5	53.8	61.3	37.1	49.1	63.8	33.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	–	13.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN74LV08A –40°C to 85°C			SN74LV08A –40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –50µA	2V to 5.5V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –2mA	2.3V	2			2			
		I_{OH} = –6mA	3V	2.48			2.48			
		I_{OH} = –12mA	4.5V	3.8			3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50µA	2V to 5.5V			0.1			0.1	V
		I_{OL} = 2mA	2.3V			0.4			0.4	
		I_{OL} = 6mA	3V			0.44			0.44	
		I_{OL} = 12mA	4.5V			0.55			0.55	
I_I	Input leakage current VI	V_I = 5.5V or GND	0 to 5.5V			±1			±1	µA
I_{CC}	Static supply current	V_I = V_{CC} or GND, I_O = 0	5.5V			20			20	µA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5V	0			5			5	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3V		3.3			3.3		pF
			5V		3.3			3.3		

5.6 Switching Characteristics, V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV08A –40°C to 85°C		SN74LV08A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		7.9[1]	13.8[1]	1	16	1	17	ns
			C_L = 50pF		10.5	17.3	1	20	1	21	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Switching Characteristics, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV08A –40°C to 85°C		SN74LV08A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		5.6[1]	8.8[1]	1	10.5	1	11.5	ns
			C_L = 50pF		7.5	12.3	1	14	1	15	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.8 Switching Characteristics, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV08A –40°C to 85°C		SN74LV08A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	C_L = 15pF		4.1[1]	5.9[1]	1	7	1	8	ns
			C_L = 50pF		5.5	7.9	1	9	1	10	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.9 Noise Characteristics

V_{CC} = 3.3V, C_L = 50pF, T_A = 25°C

PARAMETER		SN74LV08A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50pF,	f = 10MHz	3.3V	8	pF
				5V	10	

5.11 Typical Characteristics

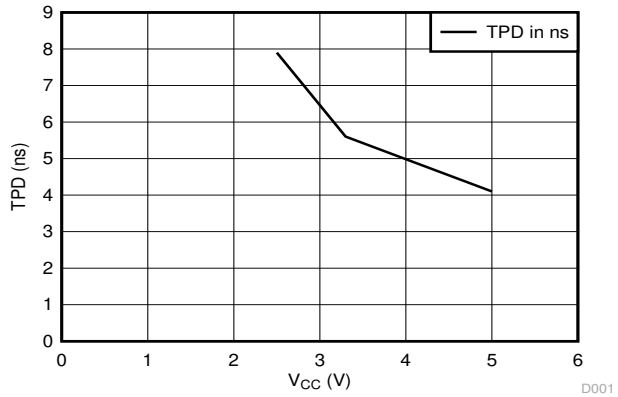


Figure 5-1. TPD vs V_{CC}

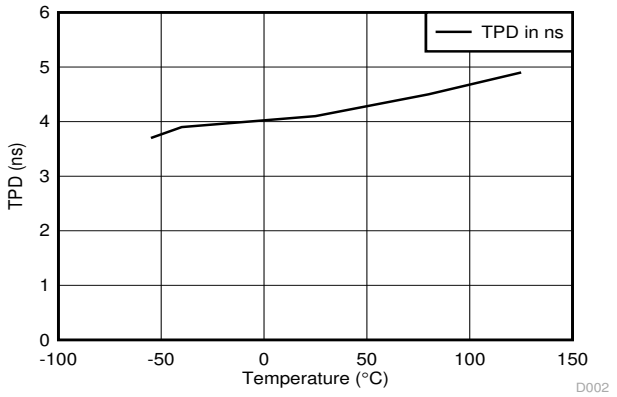
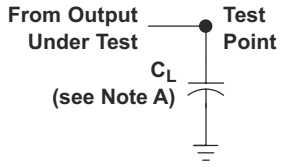
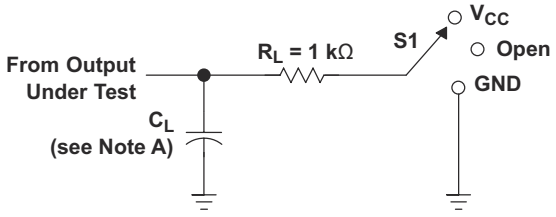


Figure 5-2. TPD vs Temperature

6 Parameter Measurement Information

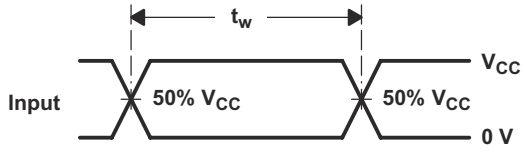


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

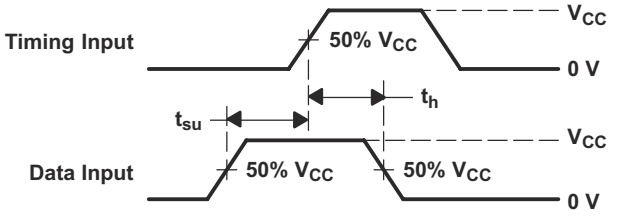


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

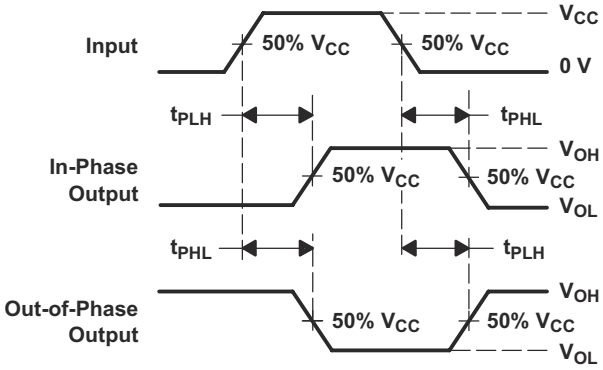
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



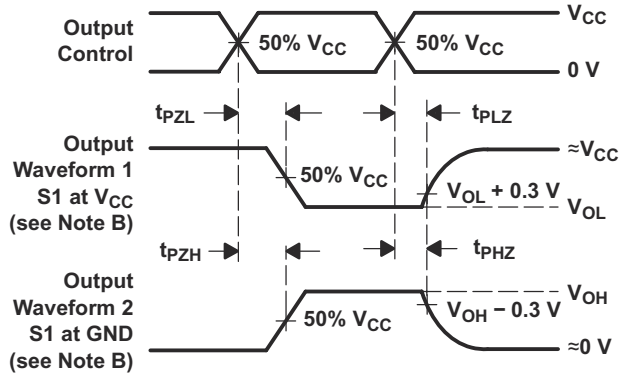
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50 Ω, t_r ≤ 3ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This quadruple 2-input positive-AND gate is designed for 2V to 5.5V V_{CC} operation. The SN74LA08A device performs the Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

This device is fully specified for partial-power-down application using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

7.2 Functional Block Diagram

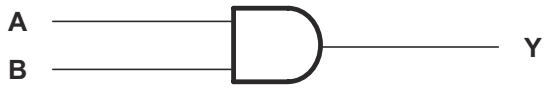


Figure 7-1. Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

- Wide operating voltage range
  - Operates From 2V to 5.5V
- Allows down voltage translation
  - Inputs accept voltages to 5.5V
- I_{off} feature
  - Allows voltages on the input or output when V_{CC} is 0V

7.4 Device Functional Modes

Table 7-1. Function Table (Each Gate)

INPUTS(1)		OUTPUT (2)
A	B	Y
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LV08A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages up to 5.5V at any valid V_{CC}, thus making it ideal for down translation.

8.2 Typical Application

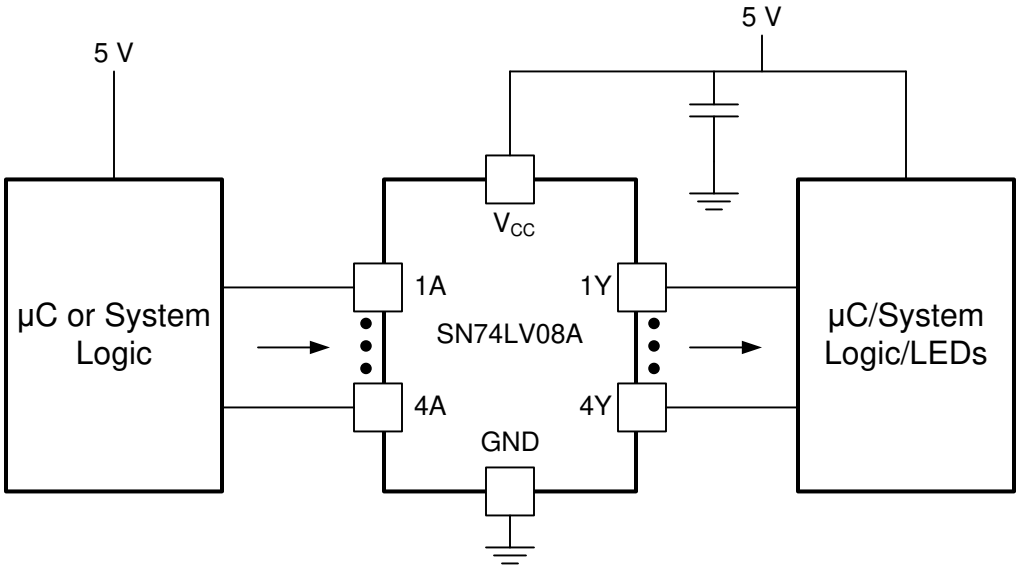


Figure 8-1. Application Diagram

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents should not exceed 25mA per output and 50mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

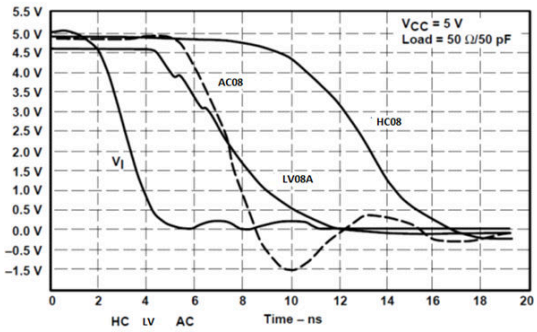


Figure 8-2. Application Curves

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01µF or 0.022µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1.0µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

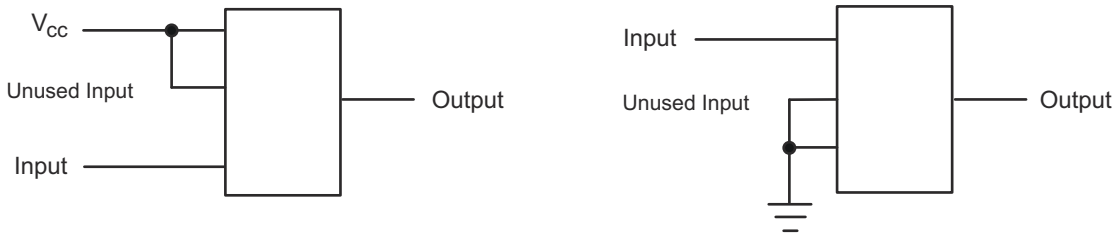


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision M (October 2014) to Revision N (September 2025)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1
• Added –40°C to 85°C temperature range	4

Changes from Revision L (October 2010) to Revision M (October 2014)	Page
• Updated document to new TI data sheet format	1
• Deleted Ordering Information table	1
• Deleted SN54LV08A device from data sheet	1
• Added Applications	1
• Added Pin Functions table	3
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	5
• Added Thermal Information table	5
• Added Typical Characteristics	7
• Added Application and Implementation section	10
• Added Power Supply Recommendations and Layout sections	12

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV08AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LV08A
SN74LV08ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADBR.B	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV08A
SN74LV08ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV08A
SN74LV08APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	LV08A
SN74LV08APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV08A
SN74LV08APWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	LV08A
SN74LV08ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV08A
SN74LV08ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV08A
SN74LV08ARGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV08A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV08A :

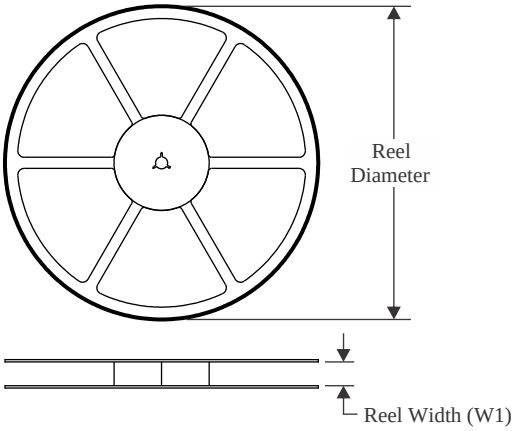
- Automotive : SN74LV08A-Q1
- Enhanced Product : SN74LV08A-EP

NOTE: Qualified Version Definitions:

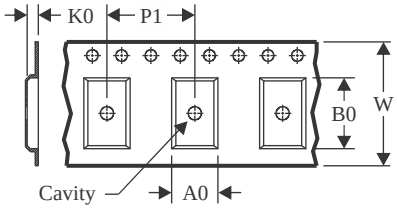
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

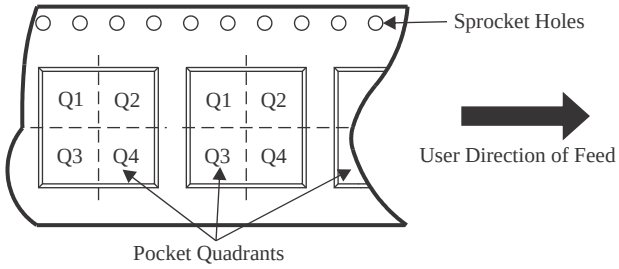


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

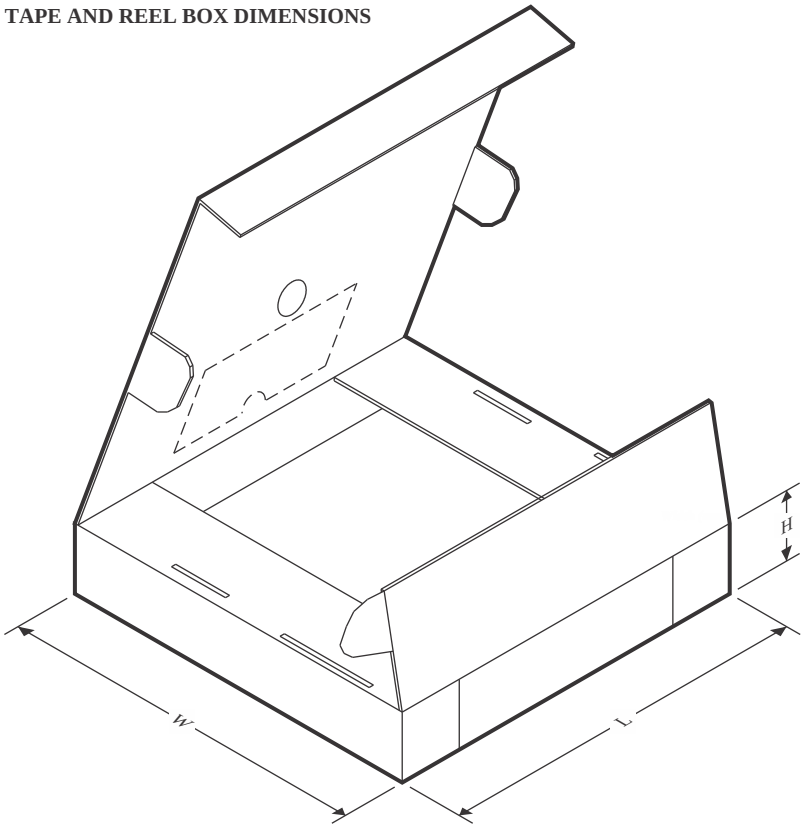
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

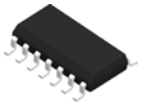
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV08ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV08ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV08ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV08ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV08APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV08APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV08APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74LV08APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV08ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV08ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV08ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV08ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV08ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV08APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV08APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV08APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV08APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV08ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

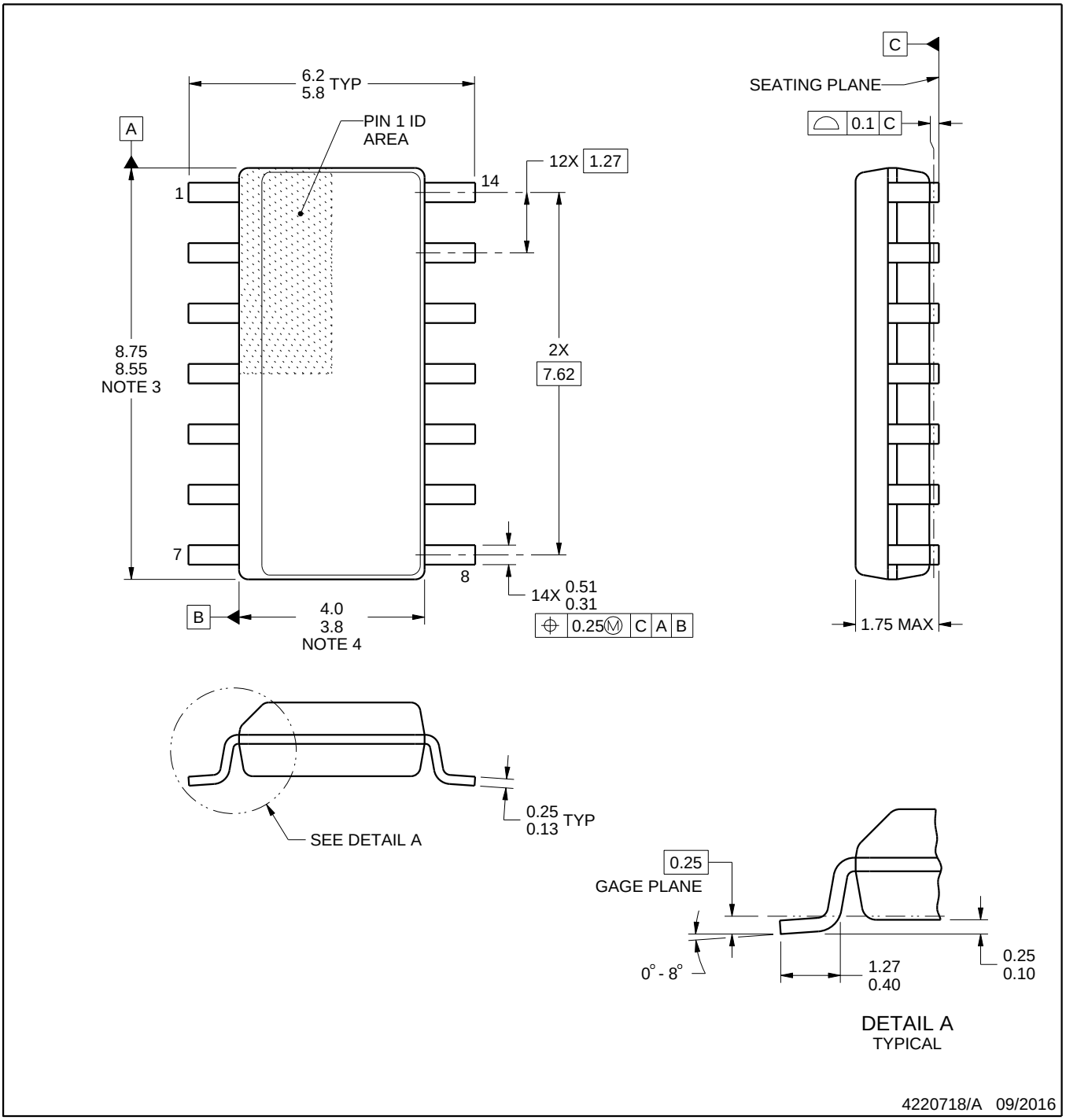


PACKAGE OUTLINE

D0014A

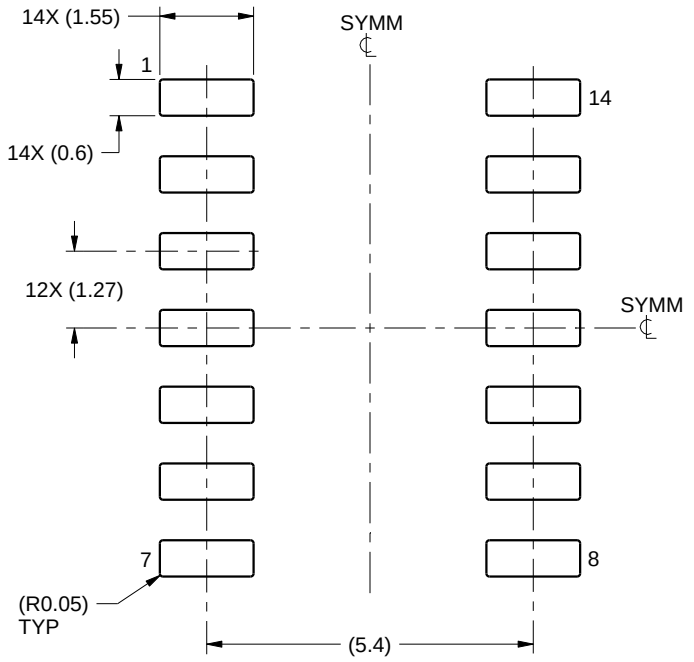
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

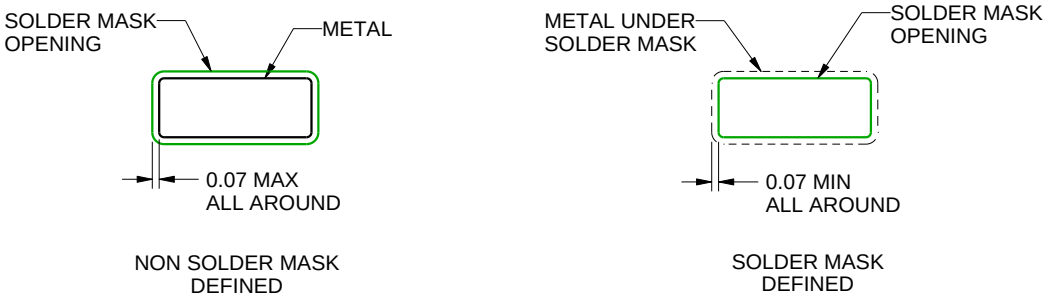


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

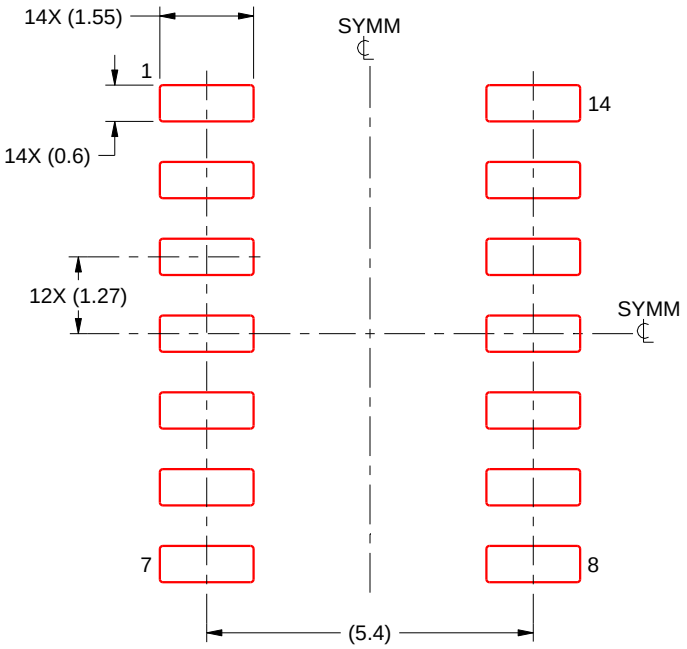
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

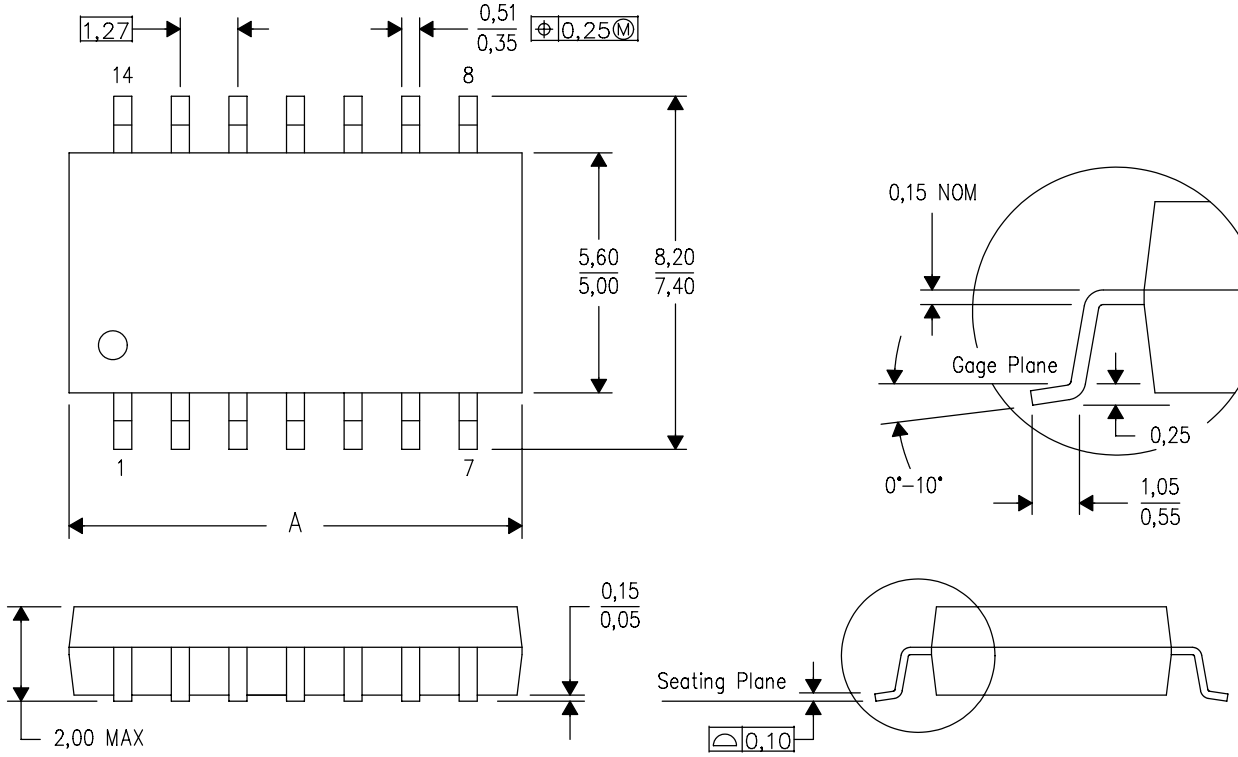
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



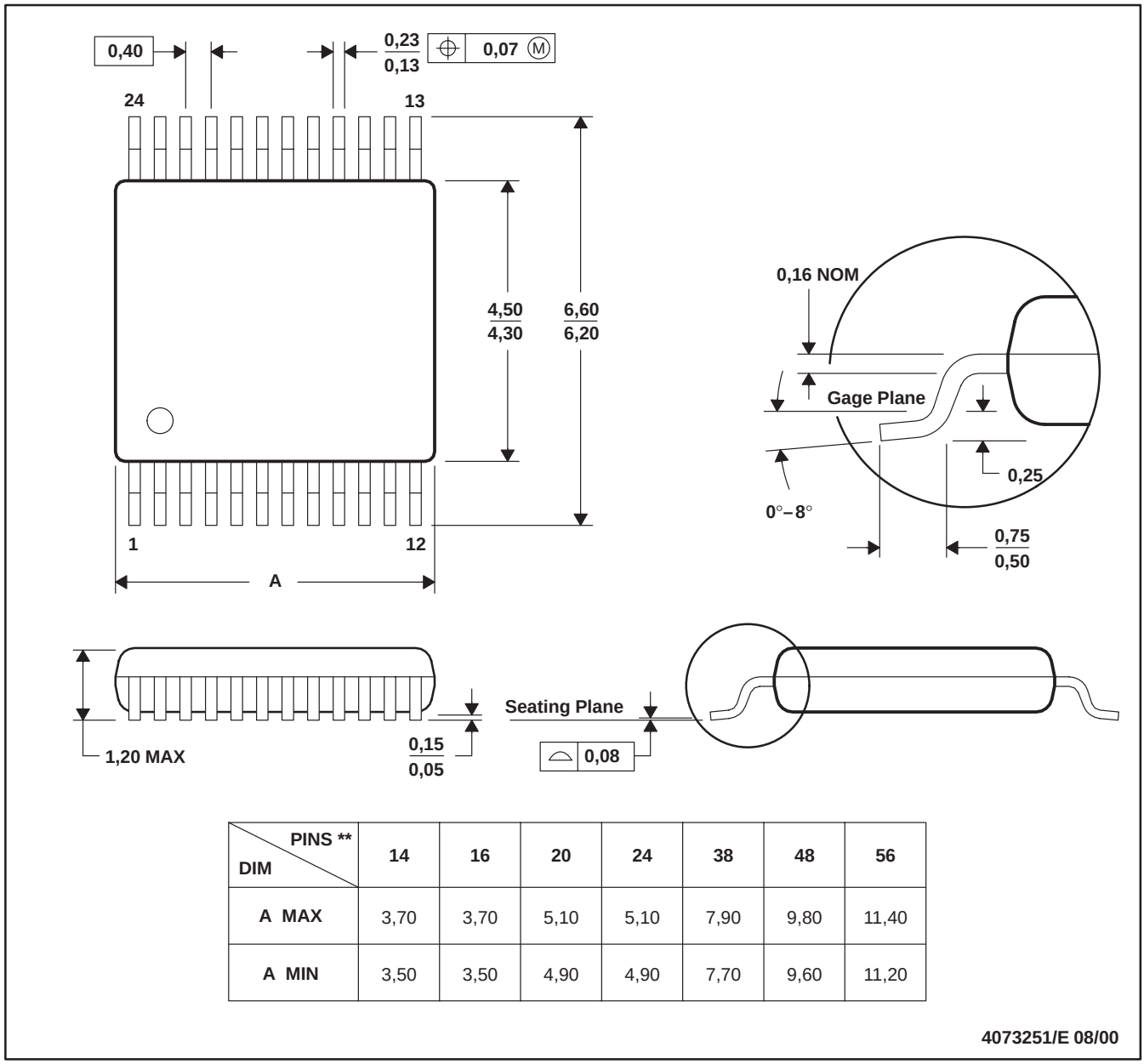
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

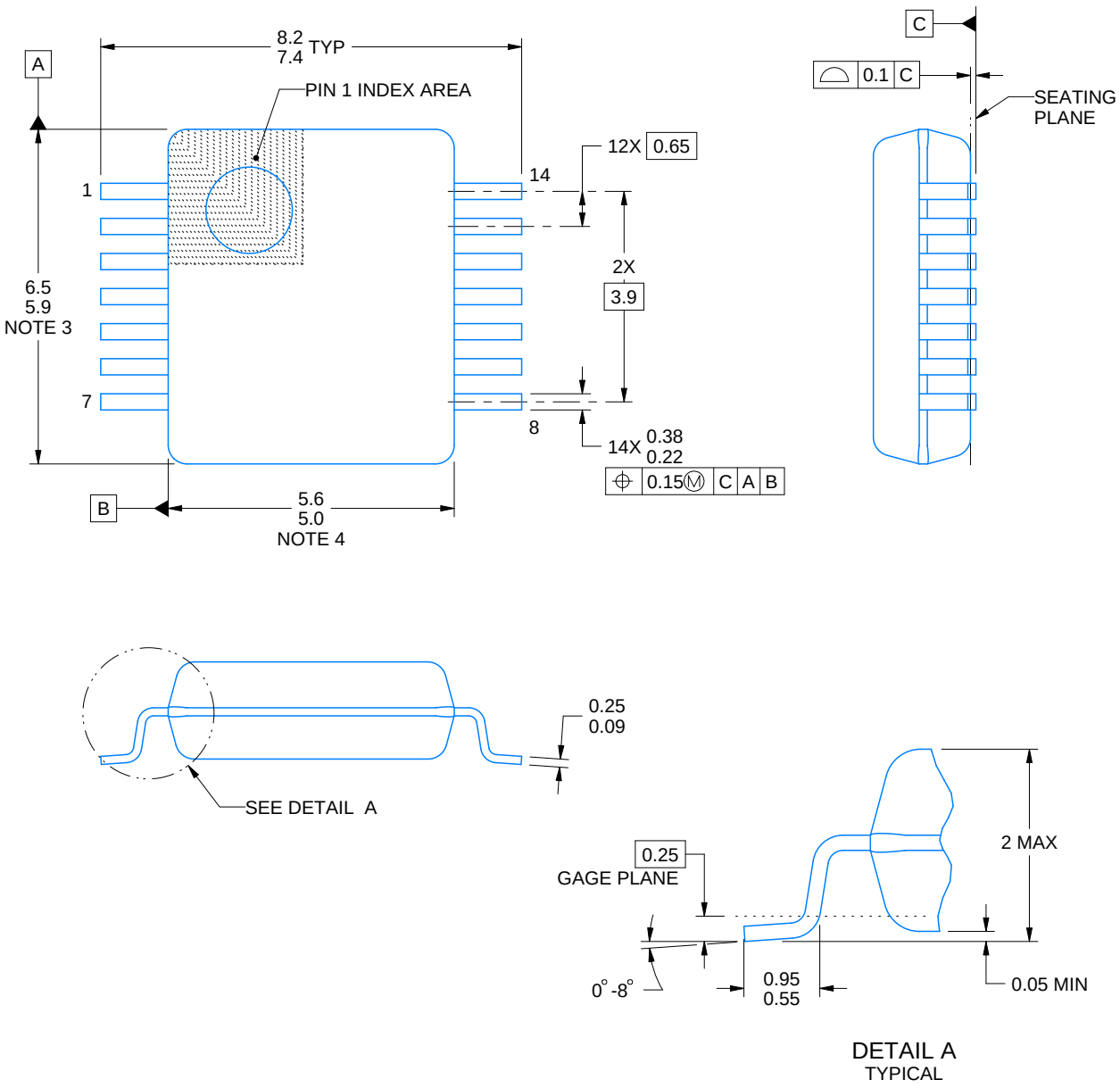
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

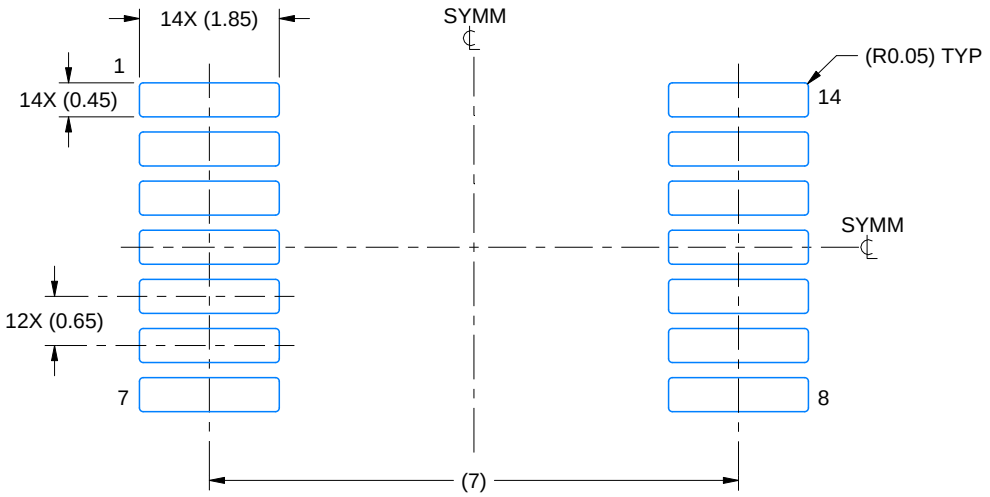
SMALL OUTLINE PACKAGE



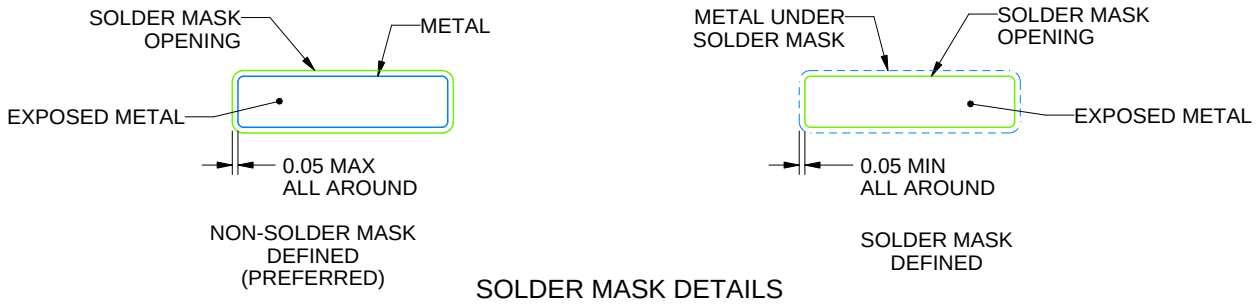
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

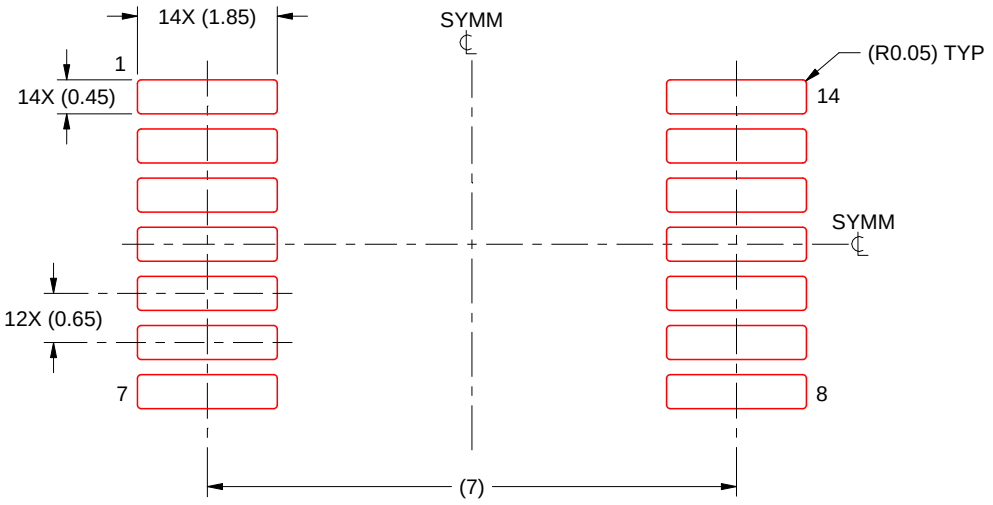


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

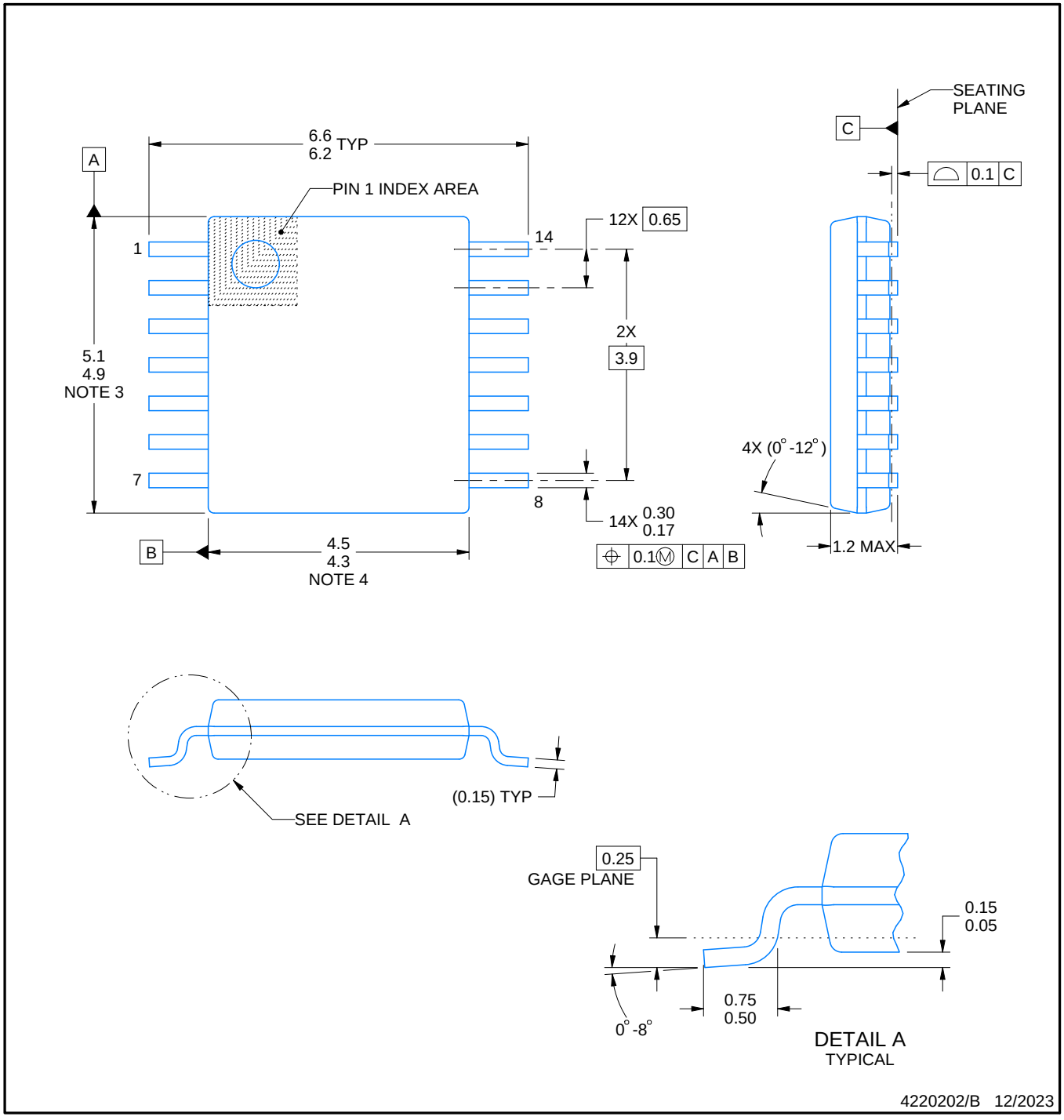
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

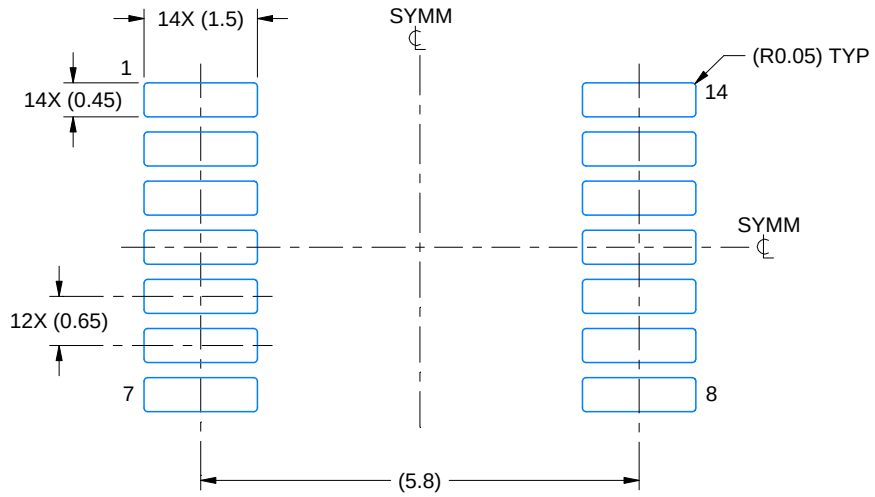
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

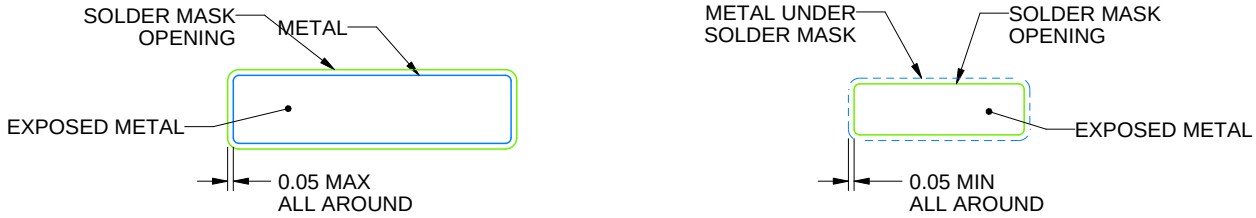


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

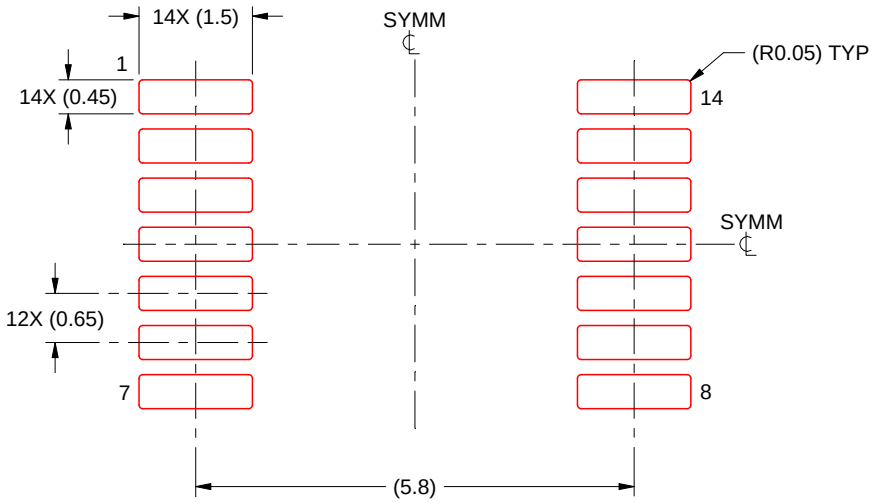


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

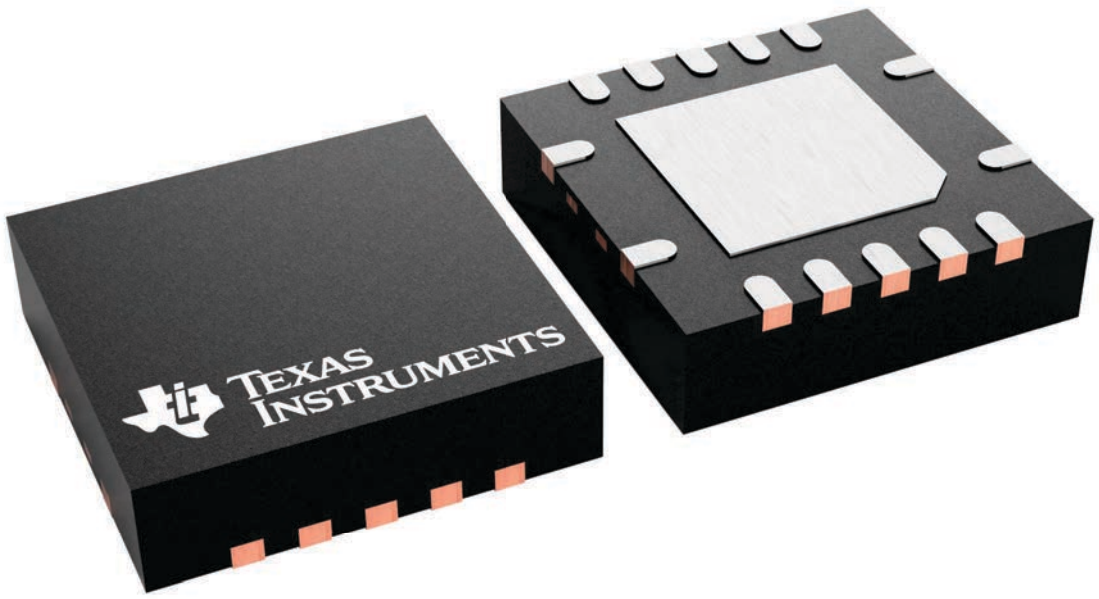
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



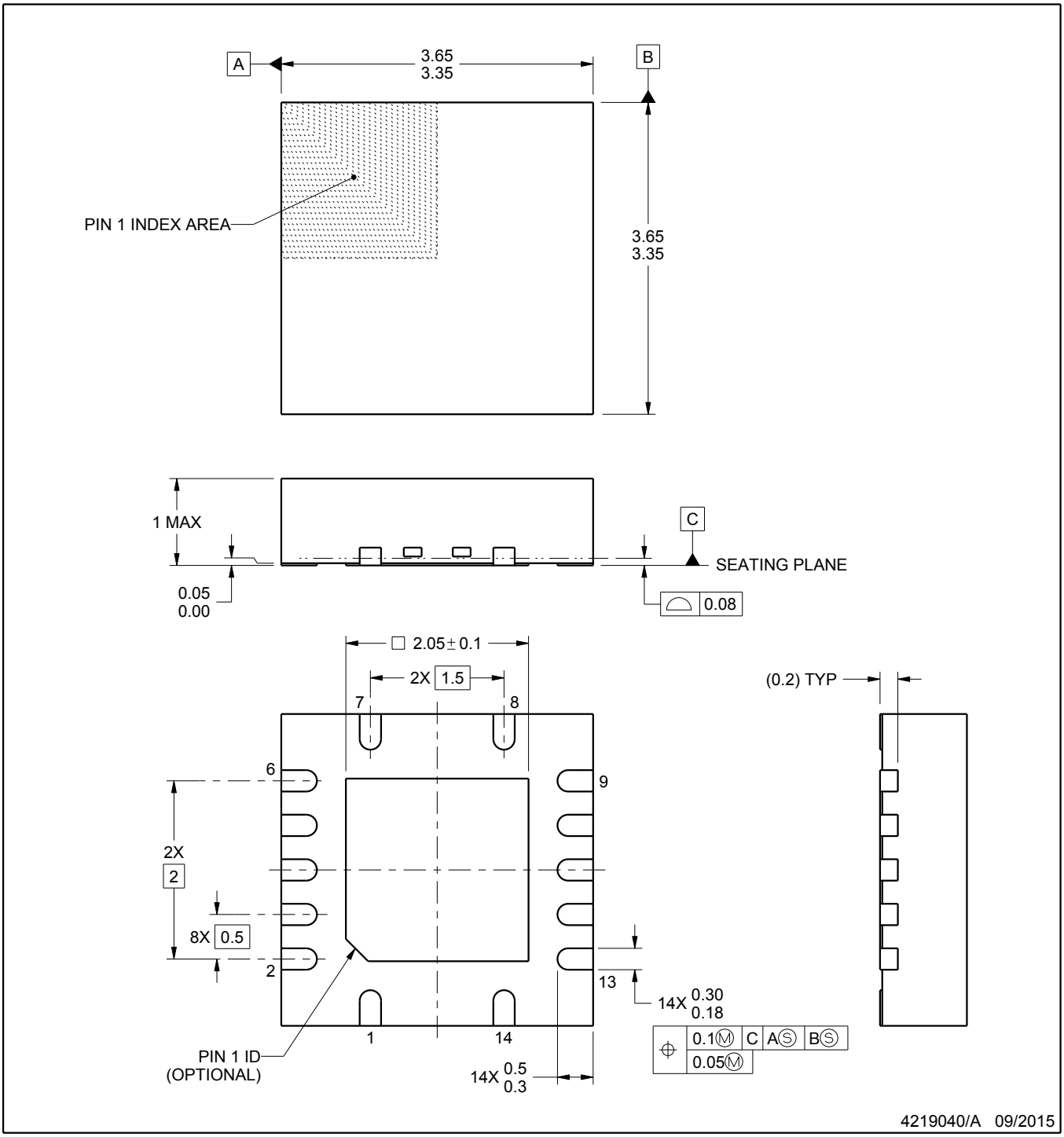
4231541/A

PACKAGE OUTLINE

RGY0014A

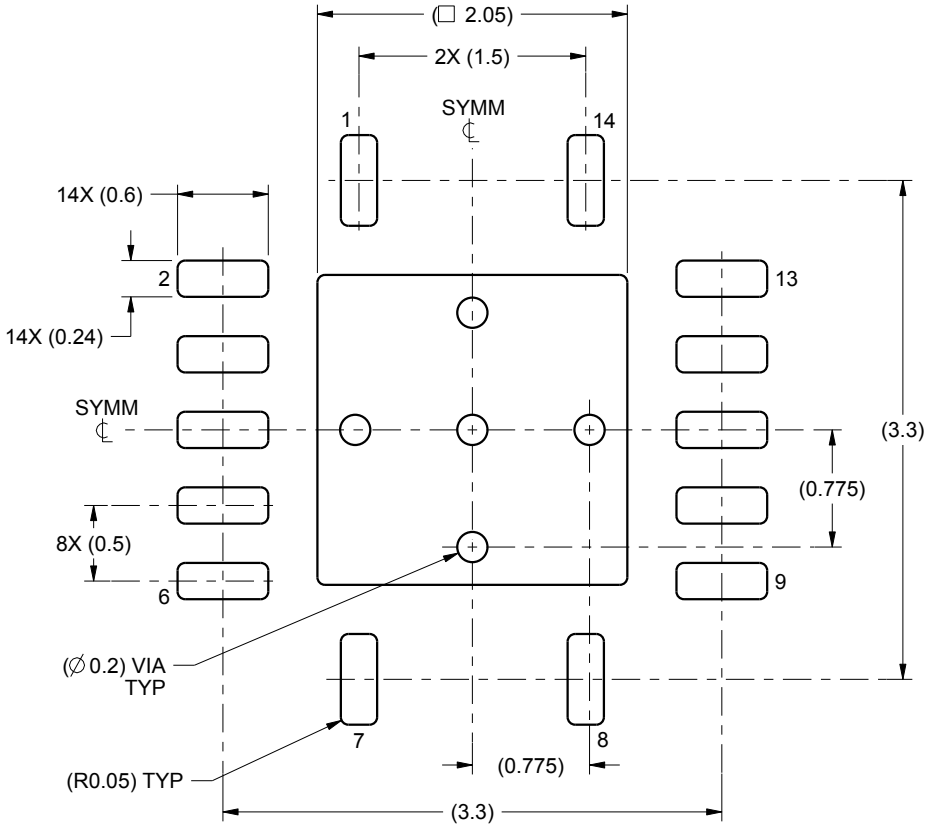
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

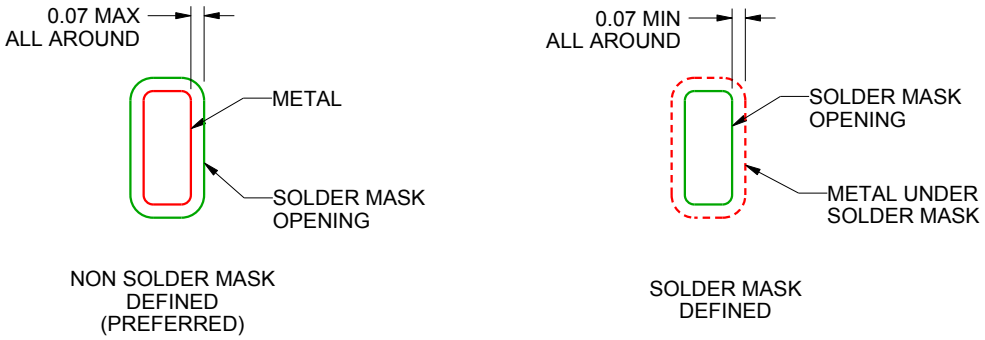


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

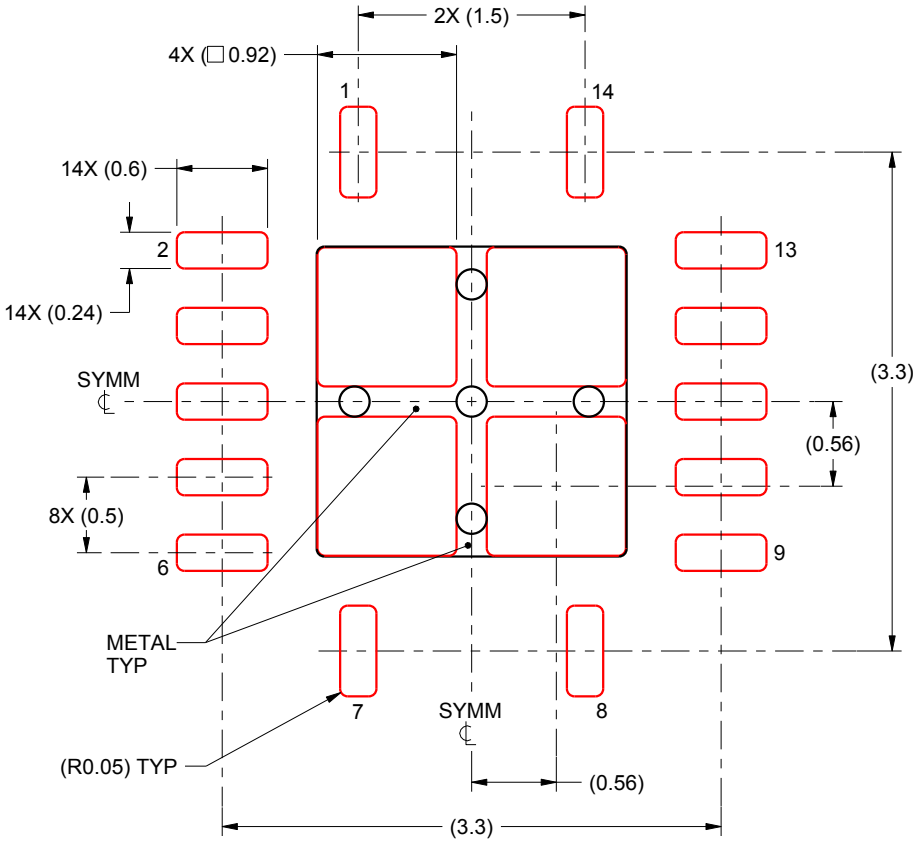


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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