

# SN54LS399, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

SDLS174 – OCTOBER 1976 – REVISED MARCH 1988

- **Single-Rail Outputs on 'LS399**
- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
  - Universal Type Register for Implementing Various Shift Patterns: Even Has Compound Left-Right Capabilities

## description

This monolithic quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54LS157/SN74LS157 and SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the positive-going edge of the clock pulse.

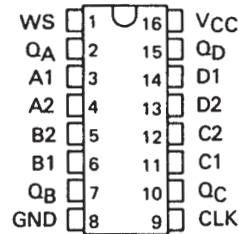
Typical power dissipation is 37 milliwatts. The SN54LS399 is characterized for operation over the full military range of -55°C to 125°C. The SN74LS399 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

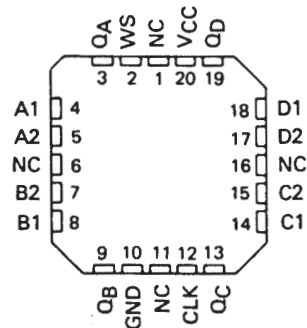
SN54LS399 . . . J OR W PACKAGE  
SN74LS399 . . . D OR N PACKAGE

(TOP VIEW)



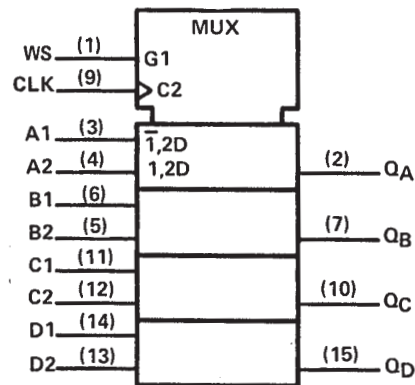
SN54LS399 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

## logic symbol†



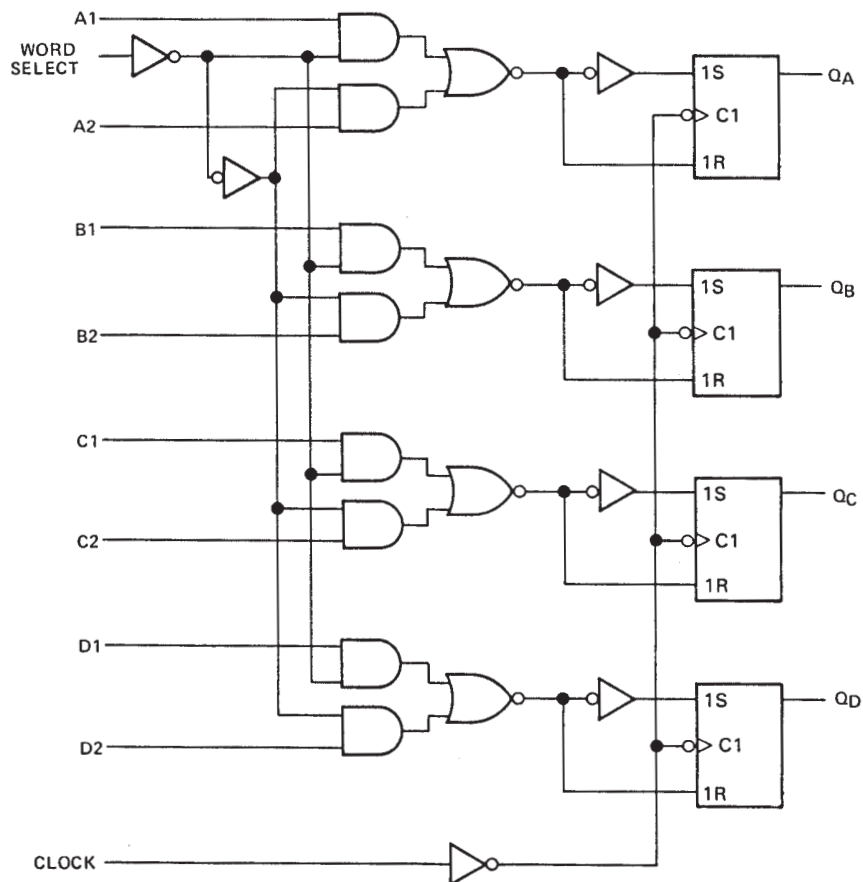
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

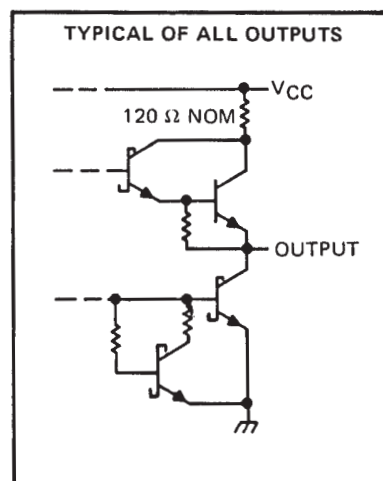
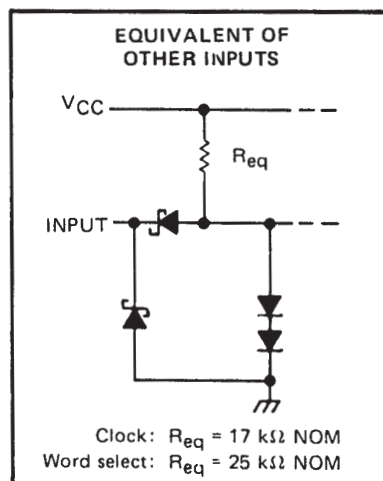
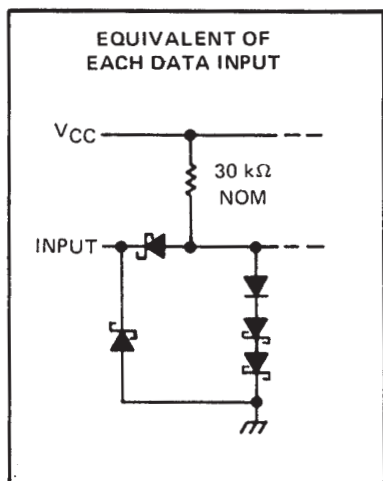
# SN54LS399, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

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## logic diagram (positive logic)



## schematics of inputs and outputs



# SN54LS399, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS399	–55°C to 125°C
SN74LS399	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

## recommended operating conditions

		SN54LS399			SN74LS399			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$				–400			–400	$\mu$ A
Low-level output current, $I_{OL}$				4			8	mA
Width of clock pulse, high or low level, $t_W$		20			20			ns
Setup time, $t_{su}$	Data	25			25			ns
	Word select	45			45			
Hold time, $t_h$	Data	0			0			ns
	Word select	0			0			
Operating free-air temperature, $T_A$		–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS399			SN74LS399			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage			2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8			V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = −18 mA		−1.5			−1.5			V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> I <sub>OH</sub> = −400 μA		2.5	3.4		2.7	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
		I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1			mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20			μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		−0.4			−0.4			mA
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX		−20	−100		−20	−100		mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 2		7.3	13		7.3	13		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and all inputs except clock low,  $I_{CC}$  is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ ,		18	27	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output	See Note 3		21	32	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">8415401EA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415401EA SNJ54LS399J
<a href="#">SN54LS399J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS399J
<a href="#">SN54LS399J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS399J
SN54LS399J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS399J
SN54LS399J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS399J
<a href="#">SN74LS399N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU   NIPDAU	N/A for Pkg Type	0 to 70	SN74LS399N
<a href="#">SN74LS399N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU   NIPDAU	N/A for Pkg Type	0 to 70	SN74LS399N
SN74LS399N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS399N
SN74LS399N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS399N
<a href="#">SNJ54LS399J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415401EA SNJ54LS399J
<a href="#">SNJ54LS399J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415401EA SNJ54LS399J
SNJ54LS399J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415401EA SNJ54LS399J
SNJ54LS399J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415401EA SNJ54LS399J

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54LS399, SN74LS399 :**

- Catalog : [SN74LS399](#)
- Military : [SN54LS399](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS399N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS399N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS399N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS399N.A	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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