

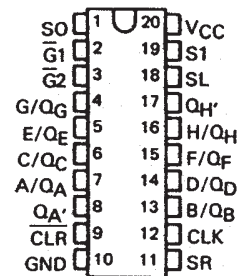
# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:  
Hold (Store)      Shift Left  
Shift Right      Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

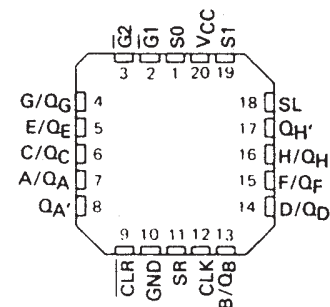
SN54LS299, SN54S299 . . . J OR W PACKAGE  
SN74LS299, SN74S299 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS299, SN54S299 . . . FK PACKAGE

(TOP VIEW)



- Applications:  
Stacked or Push-Down Registers  
Buffer Storage, and Accumulator Registers

| TYPE   | GUARANTEED<br>SHIFT (CLOCK)<br>FREQUENCY | TYPICAL<br>POWER<br>DISSIPATION |
|--------|------------------------------------------|---------------------------------|
| 'LS299 | 25 MHz                                   | 175 mW                          |
| 'S299  | 50 MHz                                   | 700 mW                          |

## description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

| MODE        | INPUTS |          |         |        |   |     | INPUTS/OUTPUTS |   |                                         |     |     |     |     |     | OUTPUTS |     |     |     |
|-------------|--------|----------|---------|--------|---|-----|----------------|---|-----------------------------------------|-----|-----|-----|-----|-----|---------|-----|-----|-----|
|             | CLR    | FUNCTION |         | OUTPUT |   | CLK | SERIAL         |   | A/QA B/QB C/QC D/QD E/QE F/QF G/QG H/QH |     |     |     |     |     |         |     | QA' | QH' |
|             |        | SELECT   | CONTROL |        |   |     |                |   |                                         |     |     |     |     |     |         |     |     |     |
|             |        | S1 S0    | G1† G2† |        |   |     |                |   |                                         |     |     |     |     |     |         |     |     |     |
| Clear       | L      | X        | L       | L      | L | X   | X              | X | L                                       | L   | L   | L   | L   | L   | L       | L   | L   | L   |
|             | L      | L        | X       | L      | L | X   | X              | X | L                                       | L   | L   | L   | L   | L   | L       | L   | L   | L   |
|             | L      | H        | H       | X      | X | X   | X              | X | X                                       | X   | X   | X   | X   | X   | X       | X   | L   | L   |
| Hold        | H      | L        | L       | L      | L | X   | X              | X | QA0                                     | QB0 | QC0 | QD0 | QE0 | QF0 | QG0     | QH0 | QA0 | QH0 |
|             | H      | X        | X       | L      | L | L   | X              | X | QA0                                     | QB0 | QC0 | QD0 | QE0 | QF0 | QG0     | QH0 | QA0 | QH0 |
| Shift Right | H      | L        | H       | L      | L | †   | X              | H | H                                       | QAn | QBn | QCn | QDn | QEn | QFn     | QGn | H   | QGn |
|             | H      | L        | H       | L      | L | †   | X              | L | L                                       | QAn | QBn | QCn | QDn | QEn | QFn     | QGn | L   | QGn |
| Shift Left  | H      | H        | L       | L      | L | †   | H              | X | QBn                                     | QCn | QDn | QEn | QFn | QGn | QHn     | H   | QBn | H   |
|             | H      | H        | L       | L      | L | †   | L              | X | QBn                                     | QCn | QDn | QEn | QFn | QGn | QHn     | L   | QBn | L   |
| Load        | H      | H        | H       | X      | X | †   | X              | X | a                                       | b   | c   | d   | e   | f   | g       | h   | a   | h   |

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

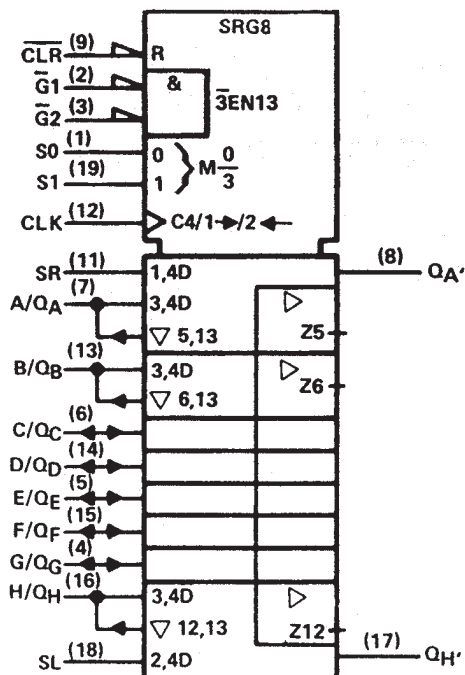
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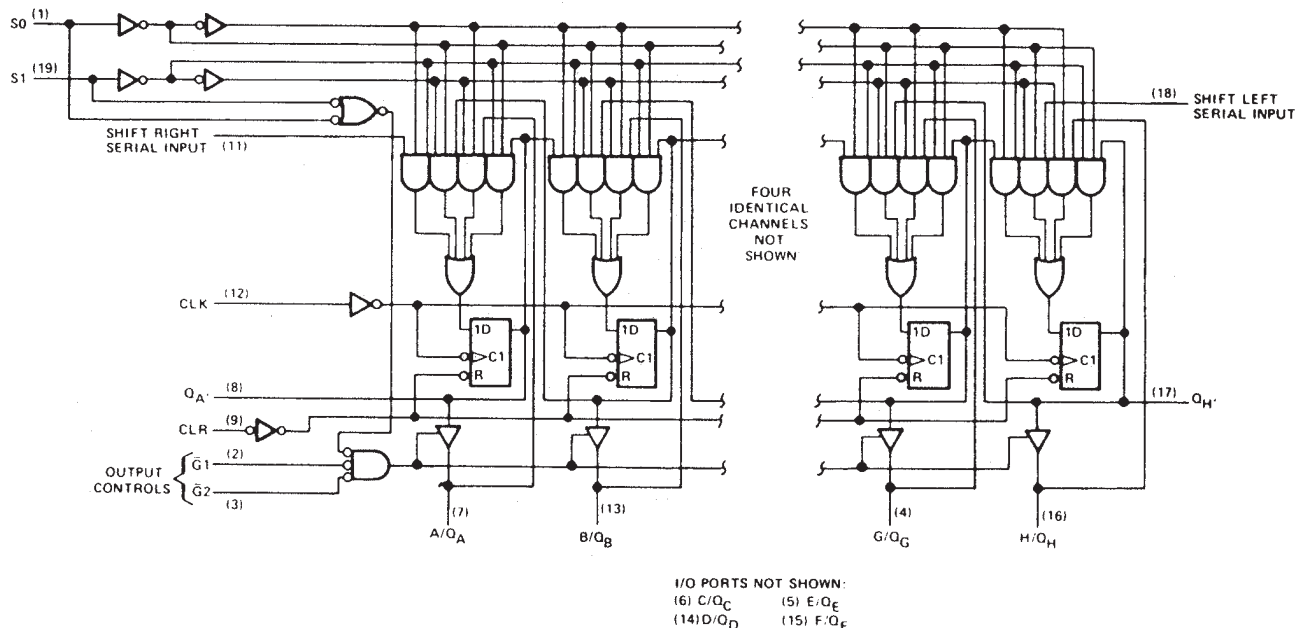
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

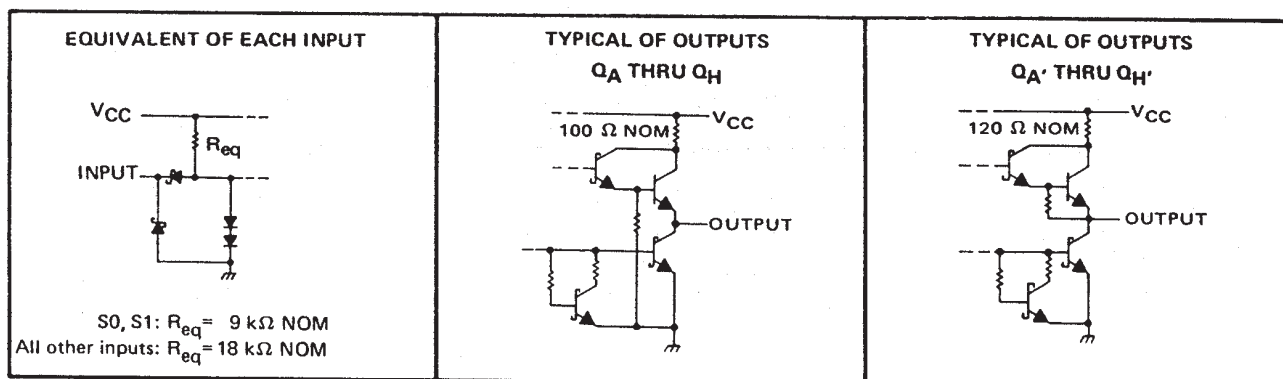


Pin numbers shown are for DW, J, N, and W packages.

# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                 |                                                |
|-------------------------------------------------|------------------------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V                                            |
| Input voltage                                   | 7 V                                            |
| Off-state output voltage                        | 5.5 V                                          |
| Operating free-air temperature range: SN54LS299 | $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ |
| SN74LS299                                       | $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$    |
| Storage temperature                             | $-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$ |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

|                                                |                                      | SN54LS299 |     |     | SN74LS299 |     |      | UNIT |
|------------------------------------------------|--------------------------------------|-----------|-----|-----|-----------|-----|------|------|
|                                                |                                      | MIN       | NOM | MAX | MIN       | NOM | MAX  |      |
| Supply voltage, V <sub>CC</sub>                |                                      | 4.5       | 5   | 5.5 | 4.75      | 5   | 5.25 | V    |
| High-level output current, I <sub>OH</sub>     | Q <sub>A</sub> thru Q <sub>H</sub>   | -1        |     |     | -2.6      |     |      | mA   |
|                                                | Q <sub>A</sub> ' or Q <sub>H</sub> ' | -0.4      |     |     | -0.4      |     |      |      |
| Low-level output current, I <sub>OL</sub>      | Q <sub>A</sub> thru Q <sub>H</sub>   | 12        |     |     | 24        |     |      | mA   |
|                                                | Q <sub>A</sub> ' or Q <sub>H</sub> ' | 4         |     |     | 8         |     |      |      |
| Clock frequency, f <sub>clock</sub>            |                                      | 0         | 20  |     | 0         | 20  |      | MHz  |
| Width of clock pulse, t <sub>w</sub> (clock)   | Clock high                           | 30        |     |     | 30        |     |      | ns   |
|                                                | Clock low                            | 18        |     |     | 10        |     |      |      |
| Width of clear pulse, t <sub>w</sub> (clear)   |                                      | Clear low |     | 25  | 20        |     | ns   |      |
| Setup time, t <sub>su</sub>                    | Select                               | 35†       |     |     | 35†       |     |      | ns   |
|                                                | High-level data†                     | 20†       |     |     | 20†       |     |      |      |
|                                                | Low-level data†                      | 20†       |     |     | 20†       |     |      |      |
|                                                | Clear inactive-state                 | 24†       |     |     | 20†       |     |      |      |
| Hold time, t <sub>h</sub>                      | Select                               | 10†       |     |     | 10†       |     |      | ns   |
|                                                | Data†                                | 3†        |     |     | 0†        |     |      |      |
| Operating free-air temperature, T <sub>A</sub> |                                      | -55       | 125 |     | 0         | 70  |      | °C   |

† Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                                      | TEST CONDITIONS†                               | SN54LS299 |      |      | SN74LS299 |      |      | UNIT |
|------------------|------------------------------------------------------|------------------------------------------------|-----------|------|------|-----------|------|------|------|
|                  |                                                      |                                                | MIN       | TYP‡ | MAX  | MIN       | TYP‡ | MAX  |      |
| V <sub>IH</sub>  | High-level input voltage                             |                                                | 2         |      |      | 2         |      |      | V    |
| V <sub>IL</sub>  | Low-level input voltage                              |                                                |           |      | 0.7  |           |      | 0.8  | V    |
| V <sub>IK</sub>  | Input clamp voltage                                  | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA |           |      | -1.5 |           |      | -1.5 | V    |
| V <sub>OH</sub>  | High-level output voltage                            | Q <sub>A</sub> thru Q <sub>H</sub>             |           |      | 2.4  |           |      | 2.4  | V    |
|                  |                                                      | Q <sub>A</sub> ' or Q <sub>H</sub> '           |           |      | 2.5  |           |      | 2.7  |      |
| V <sub>OL</sub>  | Low-level output voltage                             | Q <sub>A</sub> thru Q <sub>H</sub>             |           |      | 0.25 |           |      | 0.25 | V    |
|                  |                                                      |                                                |           |      |      |           |      | 0.35 |      |
|                  |                                                      | Q <sub>A</sub> ' or Q <sub>H</sub> '           |           |      | 0.25 |           |      | 0.25 |      |
|                  |                                                      |                                                |           |      |      |           |      | 0.35 |      |
| I <sub>OZH</sub> | Off-state output current, high-level voltage applied | Q <sub>A</sub> thru Q <sub>H</sub>             |           |      | 40   |           |      | 40   | μA   |
| I <sub>OZL</sub> | Off-state output current, low-level voltage applied  | Q <sub>A</sub> thru Q <sub>H</sub>             |           |      | -400 |           |      | -400 | μA   |
| I <sub>I</sub>   | Input current at maximum input voltage               | S0, S1                                         |           |      | 200  |           |      | 200  | μA   |
|                  |                                                      | A thru H                                       |           |      | 100  |           |      | 100  |      |
|                  |                                                      | Any other                                      |           |      | 100  |           |      | 100  |      |
| I <sub>IH</sub>  | High-level input current                             | A thru H, S0, S1                               |           |      | 40   |           |      | 40   | μA   |
|                  |                                                      | Any other                                      |           |      | 20   |           |      | 20   |      |
| I <sub>IL</sub>  | Low-level input current                              | S0, S1                                         |           |      | -0.8 |           |      | -0.8 | mA   |
|                  |                                                      | Any other                                      |           |      | -0.4 |           |      | -0.4 |      |
| I <sub>OS</sub>  | Short-circuit output current§                        | Q <sub>A</sub> thru Q <sub>H</sub>             |           |      | -30  |           |      | -30  | mA   |
|                  |                                                      | Q <sub>A</sub> ' or Q <sub>H</sub> '           |           |      | -20  |           |      | -20  |      |
| I <sub>CC</sub>  | Supply current                                       | V <sub>CC</sub> = MAX                          |           |      | 33   |           |      | 33   | mA   |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER¶       | FROM (INPUT) | TO (OUTPUT)                          | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|------------------|--------------|--------------------------------------|------------------------------------------------|-----|-----|-----|------|
| f <sub>max</sub> |              |                                      | See Note 2                                     | 20  | 35  |     | MHz  |
| t <sub>PLH</sub> | CLK          | Q <sub>A</sub> ' or Q <sub>H</sub> ' | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF  |     | 22  | 33  | ns   |
| t <sub>PHL</sub> |              | Q <sub>A</sub> ' or Q <sub>H</sub> ' |                                                |     | 26  | 39  |      |
| t <sub>PHL</sub> | CLR          | Q <sub>A</sub> ' or Q <sub>H</sub> ' |                                                |     | 27  | 40  | ns   |
| t <sub>PLH</sub> | CLK          | Q <sub>A</sub> thru Q <sub>H</sub>   | R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 45 pF |     | 17  | 25  | ns   |
| t <sub>PHL</sub> |              | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 26  | 39  |      |
| t <sub>PHL</sub> | CLR          | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 26  | 40  | ns   |
| t <sub>PZH</sub> | G1, G2       | Q <sub>A</sub> thru Q <sub>H</sub>   | R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 5 pF  |     | 13  | 21  | ns   |
| t <sub>PZL</sub> |              | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 19  | 30  |      |
| t <sub>PHZ</sub> | G1, G2       | Q <sub>A</sub> thru Q <sub>H</sub>   | R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 5 pF  |     | 10  | 20  | ns   |
| t <sub>PLZ</sub> |              | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 10  | 15  |      |

¶f<sub>max</sub> ≡ maximum clock frequency

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output

t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output

t<sub>PZH</sub> ≡ output enable time to high level

t<sub>PZL</sub> ≡ output enable time to low level

t<sub>PHZ</sub> ≡ output disable time from high level

t<sub>PLZ</sub> ≡ output disable time from low level

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.

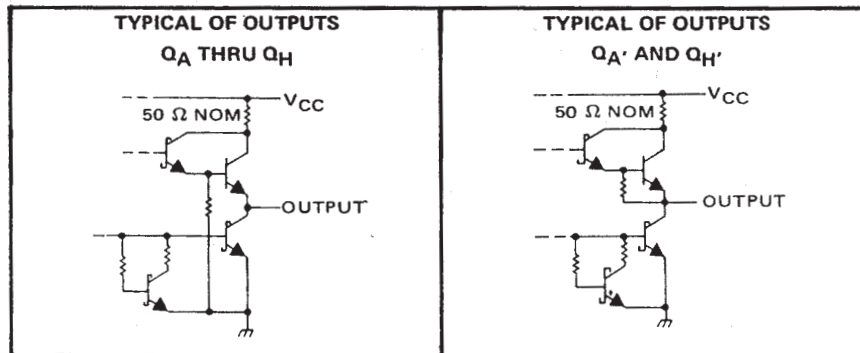
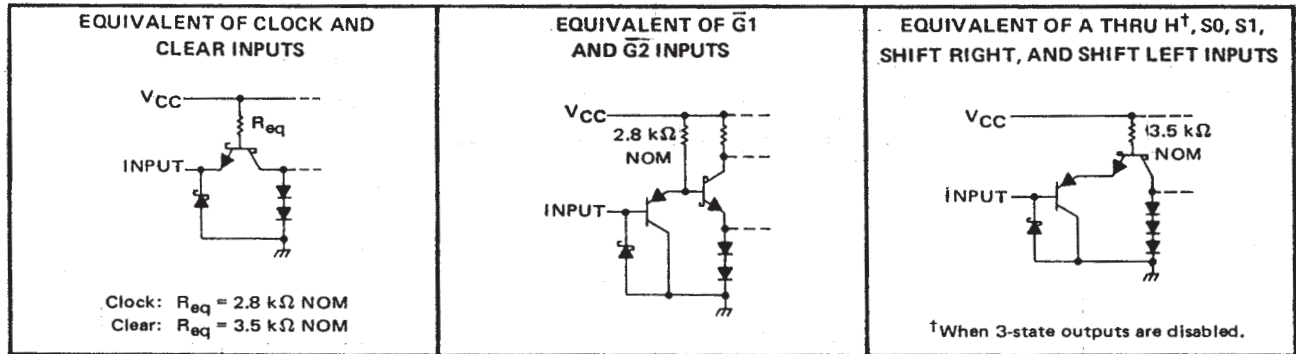


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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                             |                                            |
|-------------------------------------------------------------|--------------------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                       | 7 V                                        |
| Input voltage                                               | 5.5 V                                      |
| Off-state output voltage                                    | 5.5 V                                      |
| Operating free-air temperature range: SN54S299 (See Note 1) | $-55^\circ\text{C}$ to $125^\circ\text{C}$ |
| SN74S299                                                    | $0^\circ\text{C}$ to $70^\circ\text{C}$    |
| Storage temperature range                                   | $-65^\circ\text{C}$ to $150^\circ\text{C}$ |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

|                                       |                              | SN54S299        |     |      | SN74S299        |     |      | UNIT             |
|---------------------------------------|------------------------------|-----------------|-----|------|-----------------|-----|------|------------------|
|                                       |                              | MIN             | NOM | MAX  | MIN             | NOM | MAX  |                  |
| Supply voltage, $V_{CC}$              |                              | 4.5             | 5   | 5.5  | 4.75            | 5   | 5.25 | V                |
| High-level output current, $I_{OH}$   | $Q_A$ thru $Q_H$             |                 |     | -2   |                 |     | -6.5 | mA               |
|                                       | $Q_A'$ or $Q_H'$             |                 |     | -0.5 |                 |     | -0.5 |                  |
| Low-level output current, $I_{OL}$    | $Q_A$ thru $Q_H$             |                 |     | 20   |                 |     | 20   | mA               |
|                                       | $Q_A'$ or $Q_H'$             |                 |     | 6    |                 |     | 6    |                  |
| Clock frequency, $f_{clock}$          |                              | 0               |     | 50   | 0               |     | 50   | MHz              |
| Width of clock pulse, $t_{w(clock)}$  | Clock high                   | 10              |     |      | 10              |     |      | ns               |
|                                       | Clock low                    | 10              |     |      | 10              |     |      |                  |
| Width of clear pulse, $t_{w(clear)}$  |                              | 10              |     |      | 10              |     |      | ns               |
| Setup time, $t_{su}$                  | Select                       | 15 <sup>†</sup> |     |      | 15 <sup>†</sup> |     |      | ns               |
|                                       | High-level data <sup>†</sup> | 7 <sup>†</sup>  |     |      | 7 <sup>†</sup>  |     |      |                  |
|                                       | Low-level data <sup>†</sup>  | 5 <sup>†</sup>  |     |      | 5 <sup>†</sup>  |     |      |                  |
|                                       | Clear inactive-state         | 10 <sup>†</sup> |     |      | 10 <sup>†</sup> |     |      |                  |
| Hold time, $t_h$                      | Select                       | 5 <sup>†</sup>  |     |      | 5 <sup>†</sup>  |     |      | ns               |
|                                       | Data <sup>†</sup>            | 5 <sup>†</sup>  |     |      | 5 <sup>†</sup>  |     |      |                  |
| Operating free-air temperature, $T_A$ |                              | -55             |     | 125  | 0               |     | 70   | $^\circ\text{C}$ |

<sup>†</sup> Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                                      | TEST CONDITIONS†                                                                             | MIN                                                                  | TYP‡ | MAX  | UNIT |
|------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------|------|------|------|
| V <sub>IH</sub>  | High-level input voltage                             |                                                                                              | 2                                                                    |      |      | V    |
| V <sub>IL</sub>  | Low-level input voltage                              |                                                                                              |                                                                      |      | 0.8  | V    |
| V <sub>IK</sub>  | Input clamp voltage                                  | V <sub>CC</sub> = MIN, I <sub>I</sub> = –18 mA                                               |                                                                      |      | –1.2 | V    |
| V <sub>OH</sub>  | High-level output voltage                            | Q <sub>A</sub> thru Q <sub>H</sub>                                                           | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,                        | 2.4  | 3.2  | V    |
|                  |                                                      | Q <sub>A</sub> ' or Q <sub>H</sub> '                                                         | V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX                       | 2.7  | 3.4  |      |
| V <sub>OL</sub>  | Low-level output voltage                             | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX |                                                                      |      | 0.5  | V    |
| I <sub>OZH</sub> | Off-state output current, high-level voltage applied | Q <sub>A</sub> thru Q <sub>H</sub>                                                           | V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.4 V |      | 100  | μA   |
| I <sub>OZL</sub> | Off-state output current, low-level voltage applied  | Q <sub>A</sub> thru Q <sub>H</sub>                                                           | V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.5 V |      | –250 | μA   |
| I <sub>I</sub>   | Input current at maximum input voltage               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                                                |                                                                      | 1    |      | mA   |
| I <sub>IH</sub>  | High-level input current                             | A thru H, S0, S1                                                                             | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                        |      | 100  | μA   |
|                  |                                                      | Any other                                                                                    |                                                                      |      | 50   |      |
| I <sub>IL</sub>  | Low-level input current                              | CLK or CLR                                                                                   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V                        |      | –2   | mA   |
|                  |                                                      | S0, S1                                                                                       |                                                                      |      | –500 | μA   |
|                  |                                                      | Any other                                                                                    |                                                                      |      | –250 | μA   |
|                  |                                                      |                                                                                              |                                                                      |      |      |      |
| I <sub>OS</sub>  | Short-circuit output current§                        | Q <sub>A</sub> thru Q <sub>H</sub>                                                           | V <sub>CC</sub> = MAX                                                | –40  | –100 | mA   |
|                  |                                                      | Q <sub>A</sub> ' or Q <sub>H</sub> '                                                         |                                                                      | –20  | –100 |      |
| I <sub>CC</sub>  | Supply current                                       | V <sub>CC</sub> = MAX                                                                        |                                                                      | 140  | 225  | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER¶       | FROM<br>(INPUT) | TO<br>(OUTPUT)                       | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|------------------|-----------------|--------------------------------------|------------------------------------------------|-----|-----|-----|------|
| f <sub>max</sub> |                 |                                      | See Note 2                                     | 50  | 70  |     | MHz  |
| t <sub>PLH</sub> | CLK             | Q <sub>A</sub> ' or Q <sub>H</sub> ' | R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF  |     | 12  | 20  | ns   |
| t <sub>PHL</sub> |                 |                                      |                                                |     | 13  | 20  |      |
| t <sub>PHL</sub> | CLR             | Q <sub>A</sub> ' or Q <sub>H</sub> ' |                                                |     | 14  | 21  | ns   |
| t <sub>PLH</sub> | CLK             | Q <sub>A</sub> thru Q <sub>H</sub>   | R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 45 pF |     | 15  | 21  | ns   |
| t <sub>PHL</sub> |                 |                                      |                                                |     | 15  | 21  |      |
| t <sub>PHL</sub> | CLR             | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 16  | 24  | ns   |
| t <sub>PZH</sub> | G1, G2          | Q <sub>A</sub> thru Q <sub>H</sub>   |                                                |     | 10  | 18  | ns   |
| t <sub>PZL</sub> |                 |                                      |                                                |     | 12  | 18  |      |
| t <sub>PHZ</sub> | G1, G2          | Q <sub>A</sub> thru Q <sub>H</sub>   | R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 5 pF  |     | 7   | 12  | ns   |
| t <sub>PLZ</sub> |                 |                                      |                                                |     |     |     |      |

¶ f<sub>max</sub> = maximum clock frequency

t<sub>PLH</sub> = Propagation delay time, low-to-high-level output

t<sub>PHL</sub> = Propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">78024012A</a>    | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 78024012A<br>SNJ54LS<br>299FK |
| <a href="#">7802401RA</a>    | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| <a href="#">7802401RA</a>    | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| <a href="#">7802401SA</a>    | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |
| <a href="#">7802401SA</a>    | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |
| <a href="#">SN54LS299J</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS299J                    |
| <a href="#">SN54LS299J</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS299J                    |
| SN54LS299J.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS299J                    |
| SN54LS299J.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS299J                    |
| <a href="#">SN74LS299DW</a>  | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS299                         |
| <a href="#">SN74LS299DW</a>  | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS299                         |
| SN74LS299DW.A                | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS299                         |
| SN74LS299DW.A                | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS299                         |
| <a href="#">SN74LS299N</a>   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS299N                    |
| <a href="#">SN74LS299N</a>   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS299N                    |
| SN74LS299N.A                 | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS299N                    |
| SN74LS299N.A                 | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS299N                    |
| <a href="#">SNJ54LS299FK</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 78024012A<br>SNJ54LS<br>299FK |
| <a href="#">SNJ54LS299FK</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 78024012A<br>SNJ54LS<br>299FK |
| SNJ54LS299FK.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 78024012A<br>SNJ54LS<br>299FK |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SNJ54LS299FK.A              | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 78024012A<br>SNJ54LS<br>299FK |
| <a href="#">SNJ54LS299J</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| <a href="#">SNJ54LS299J</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| SNJ54LS299J.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| SNJ54LS299J.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401RA<br>SNJ54LS299J      |
| <a href="#">SNJ54LS299W</a> | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |
| <a href="#">SNJ54LS299W</a> | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |
| SNJ54LS299W.A               | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |
| SNJ54LS299W.A               | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7802401SA<br>SNJ54LS299W      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54LS299, SN74LS299 :**

- Catalog : [SN74LS299](#)
- Military : [SN54LS299](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 78024012A      | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 7802401SA      | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74LS299DW    | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LS299DW.A  | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LS299N     | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74LS299N.A   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54LS299FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54LS299FK.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54LS299W    | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SNJ54LS299W.A  | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

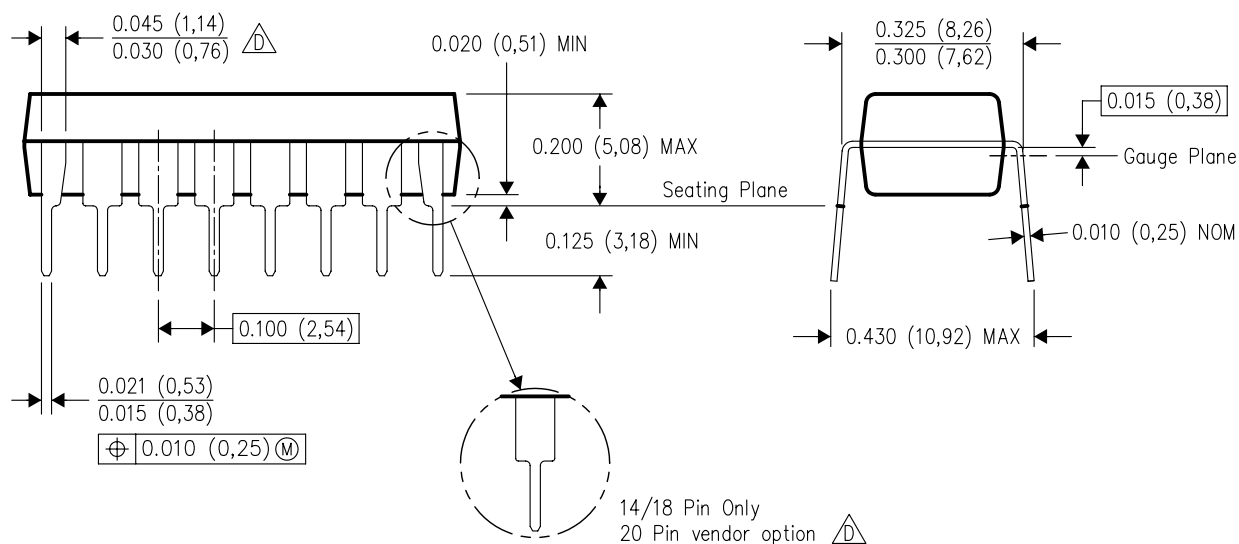
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



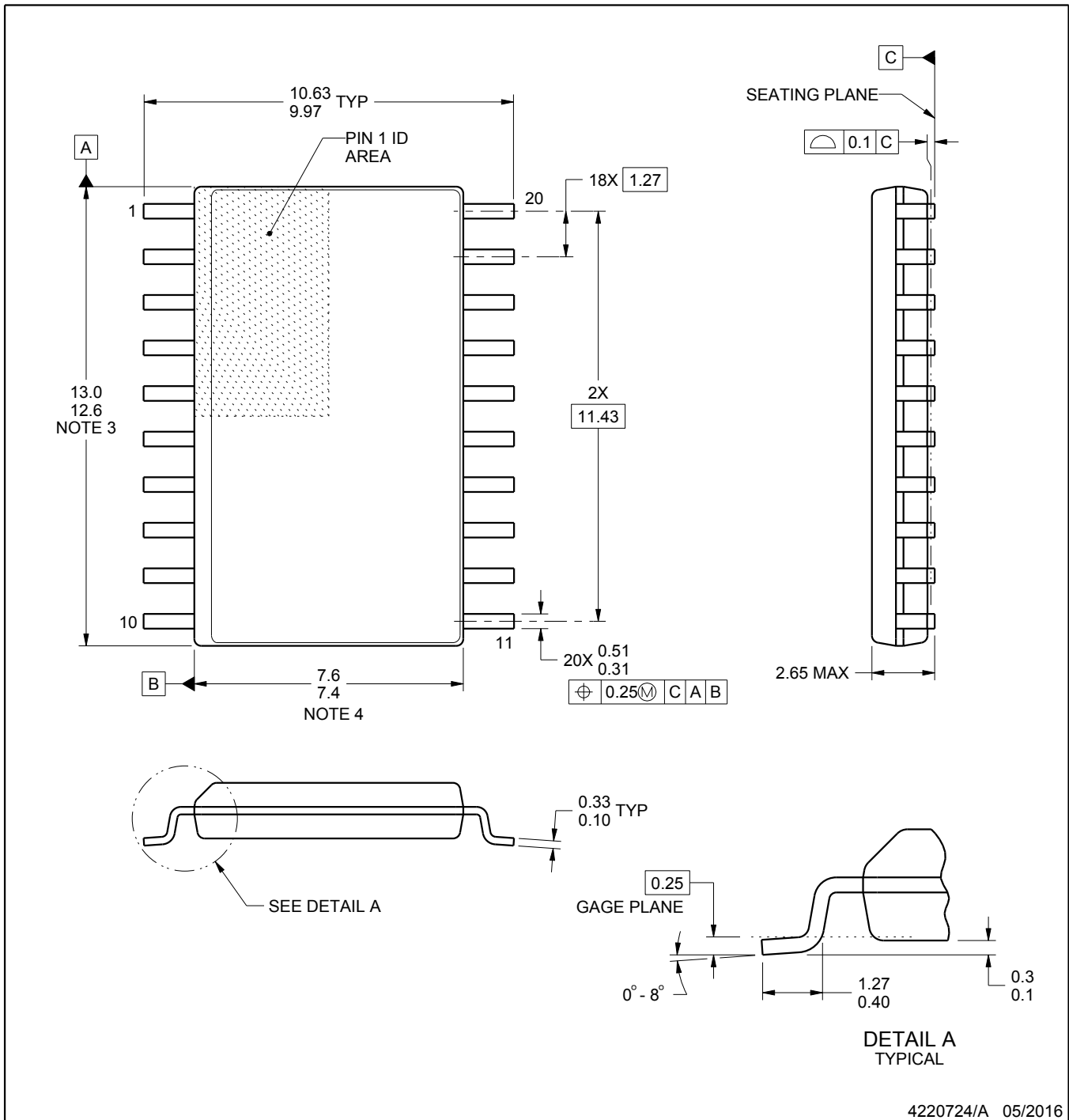
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

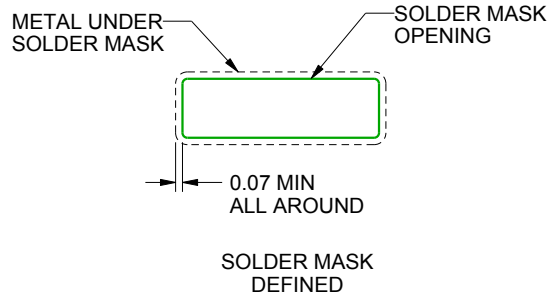
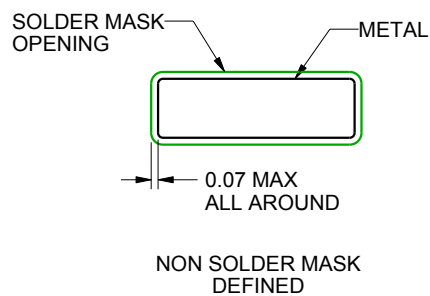
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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