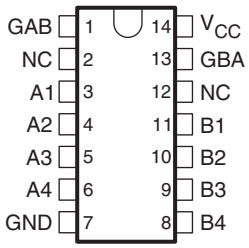
QUADRUPLE BUS TRANSCEIVERS

FEATURES

- **Two-Way Asynchronous Communication Between Data Buses**
- **PNP Inputs Reduce D-C Loading**
- **Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin**

SN54LS243 . . . J OR W PACKAGE
SN74LS243 . . . D, N, OR NS PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH TRANSCEIVER)

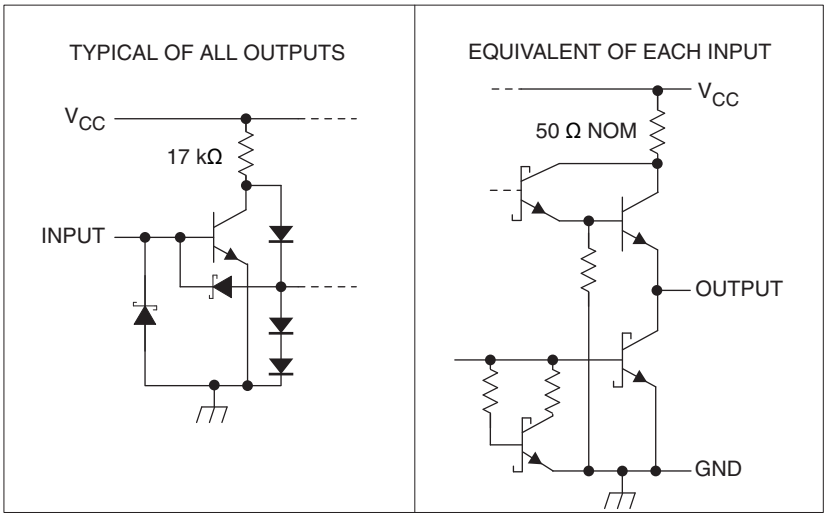
INPUTS		SNxxLS243
$\overline{G}$AB	GBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

DESCRIPTION

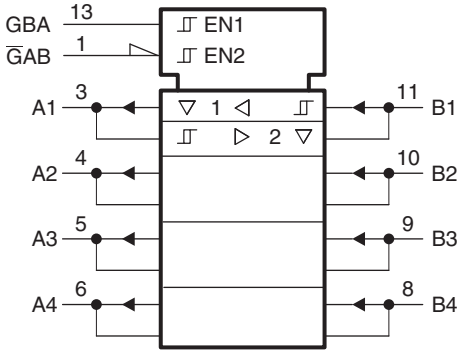
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. SN74LS243 can be used to drive terminated lines down to 133 Ω.

SN54LS243 is characterized for operation over the full military temperature range of –55°C to 125°C. SN74LS243 is characterized for operation from 0°C to 70°C.

SCHEMATICS OF INPUTS AND OUTPUTS

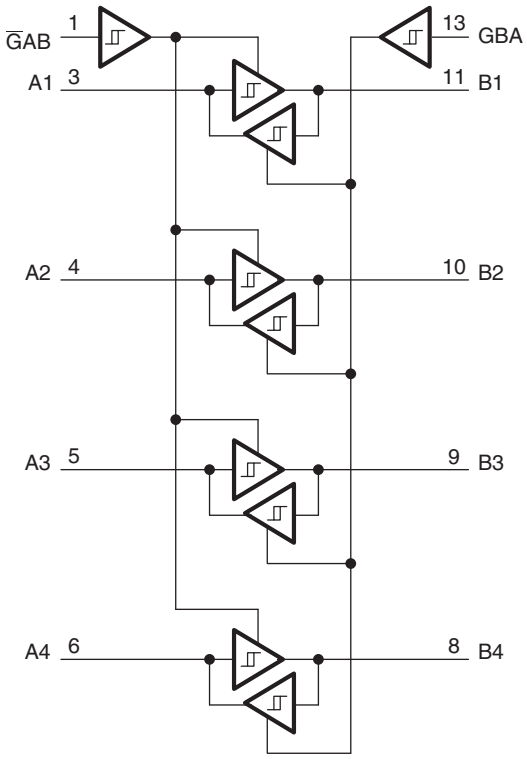


LOGIC SYMBOL



A. These symbols are in accordance with ANSI/EEE Std. 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_{IN}	Input voltage			7	V
	OFF-state output voltage			5.5	V
T_A	Operating free-air temperature range	SN54LS243	–55	125	°C
		SN74LS243	0	70	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		SN54LS243			SN74LS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage(1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output voltage			–12			–15	mA
I_{OL}	Low-level output voltage			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

(1) Voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		SN54LS243			SN74LS243			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IK}	A or B	V_{CC} = MIN, I_I = –18 mA				–1.5			–1.5	V
Hysteresis ($V_{T+} – V_{T–}$)		V_{CC} = MIN,		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OH} = –3 mA	2.4	3.1		2.4	3.1		V
			V_{IL} = 0.5 V, I_{OH} = MAX	2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	V_O = 2.7 V			40			40	µA
I_{OZL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	V_O = 0.4 V			–200			–200	µA
I_I	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
	$\overline{G}$AB or GBA		V_I = 7 V			0.1			0.1	
I_{IH}		V_{CC} = MAX,				20			20	µA
I_{IL}	A inputs	V_{CC} = MAX, V_I = 0.4 V, GAB and GBA at 0 V				–0.2			–0.2	mA
	B inputs	V_{CC} = MAX, V_I = 0.4 V, GAB and GBA at 4.5 V				–0.2			–0.2	
	$\overline{G}$AB or GBA	V_{CC} = MAX, V_I = 0.4 V,				–0.2			–0.2	
I_{OS}		V_{CC} = MAX		–40		–225	–40		–225	mA
I_{CC}	Outputs high	V_{CC} = MAX,[3]	Outputs open,		22	38		22	38	mA
	Outputs low				29	50		29	50	
	All outputs disabled				32	54		32	54	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under "recommended operating conditions."
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) I_{CC} is measured with transceivers eabled in one direction only, or with all transceivers disabled.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		SN54LS243			SN74LS243			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω,	C_L = 45 pF		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}				20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	R_L = 667 Ω,	C_L = 5 pF		10	20		10	20	ns
t_{PHZ}				15	25		15	25	ns

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8002002CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002CA SNJ54LS243J
8002002DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002DA SNJ54LS243W
SN54LS243J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS243J
SN54LS243J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS243J
SN74LS243D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LS243
SN74LS243DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS243
SN74LS243DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS243
SN74LS243N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS243N
SN74LS243N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS243N
SN74LS243NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS243N
SNJ54LS243J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002CA SNJ54LS243J
SNJ54LS243J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002CA SNJ54LS243J
SNJ54LS243W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002DA SNJ54LS243W
SNJ54LS243W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8002002DA SNJ54LS243W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS243, SN74LS243 :

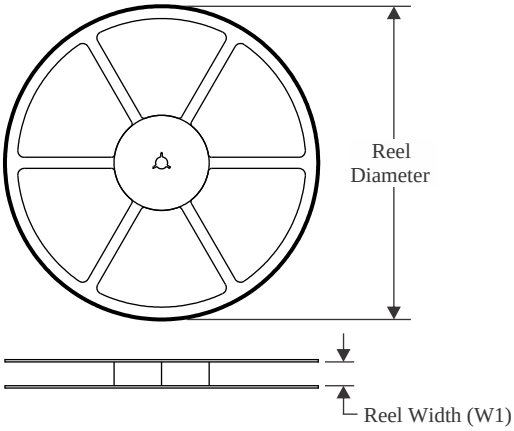
- Catalog : SN74LS243
- Military : SN54LS243

NOTE: Qualified Version Definitions:

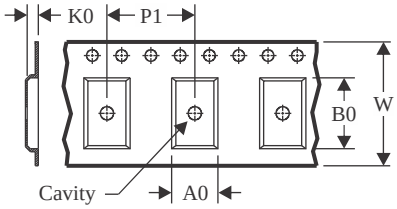
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

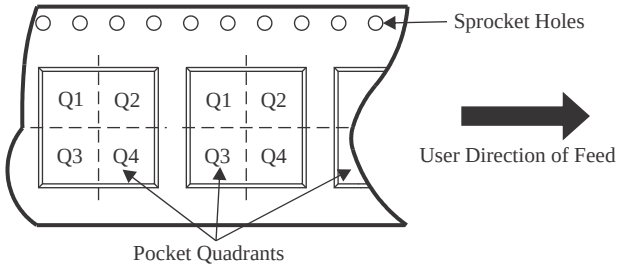


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

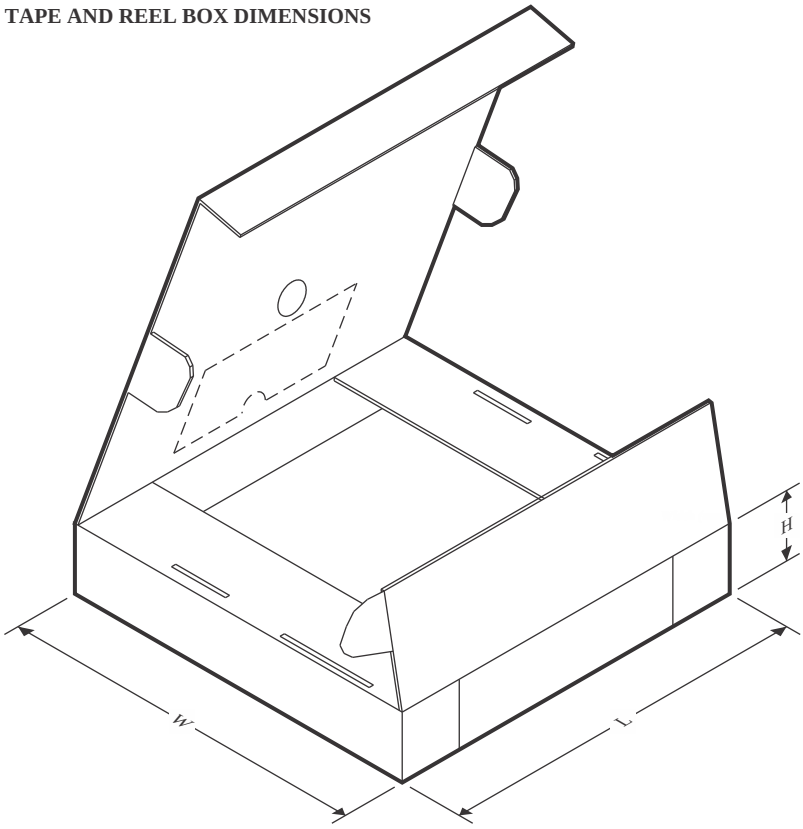
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS243DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

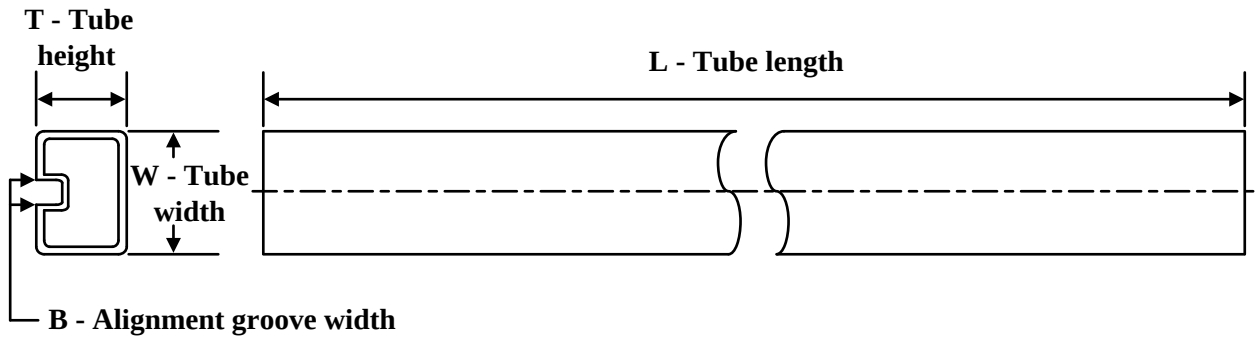
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS243DR	SOIC	D	14	2500	356.0	356.0	35.0

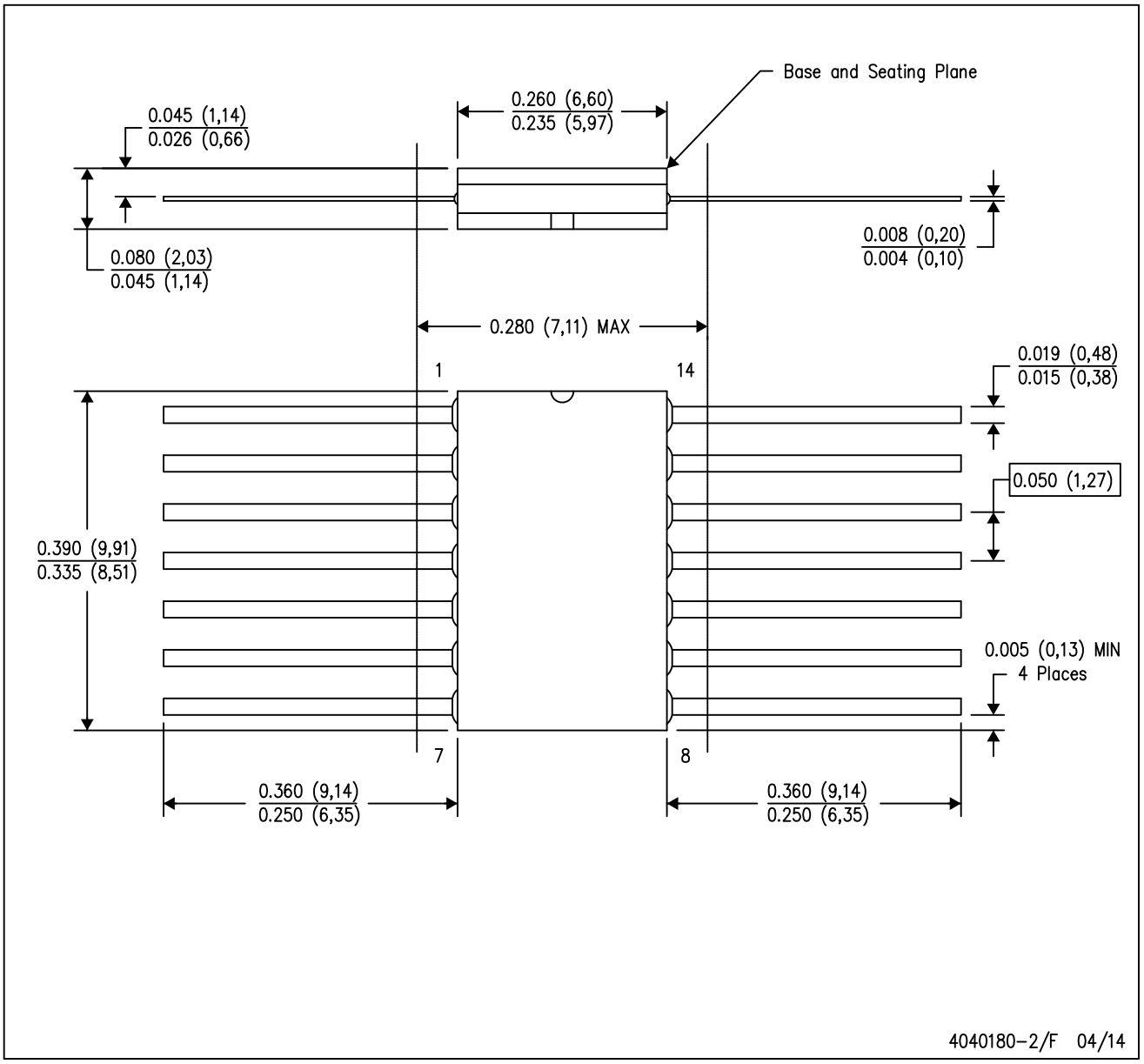
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
8002002DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS243N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS243N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS243N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS243N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS243NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS243NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS243W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS243W.A	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

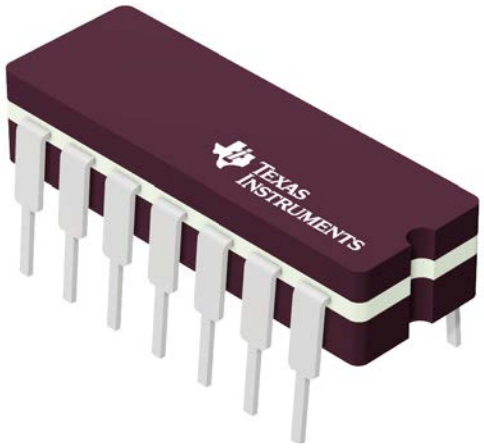


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

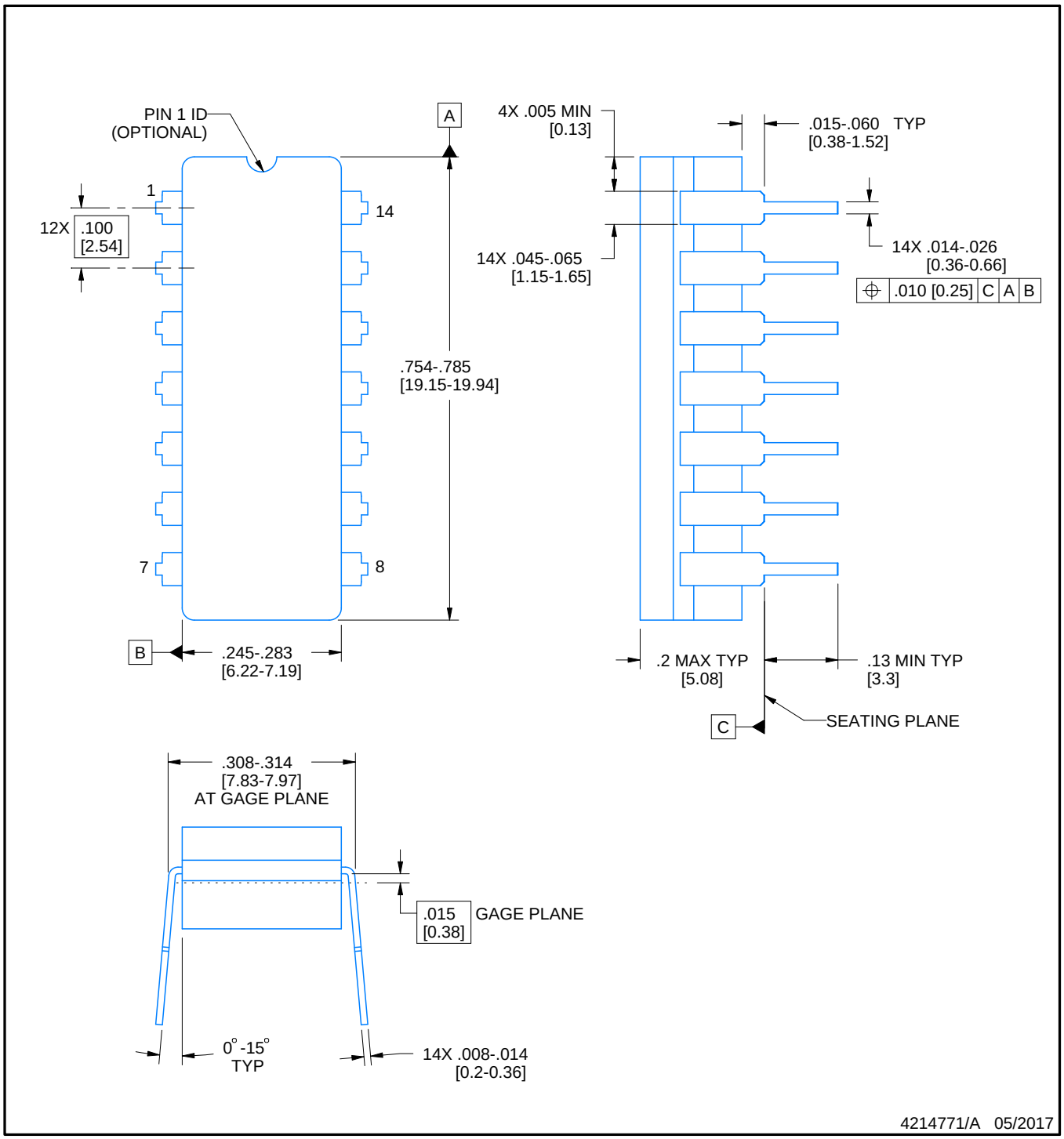
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

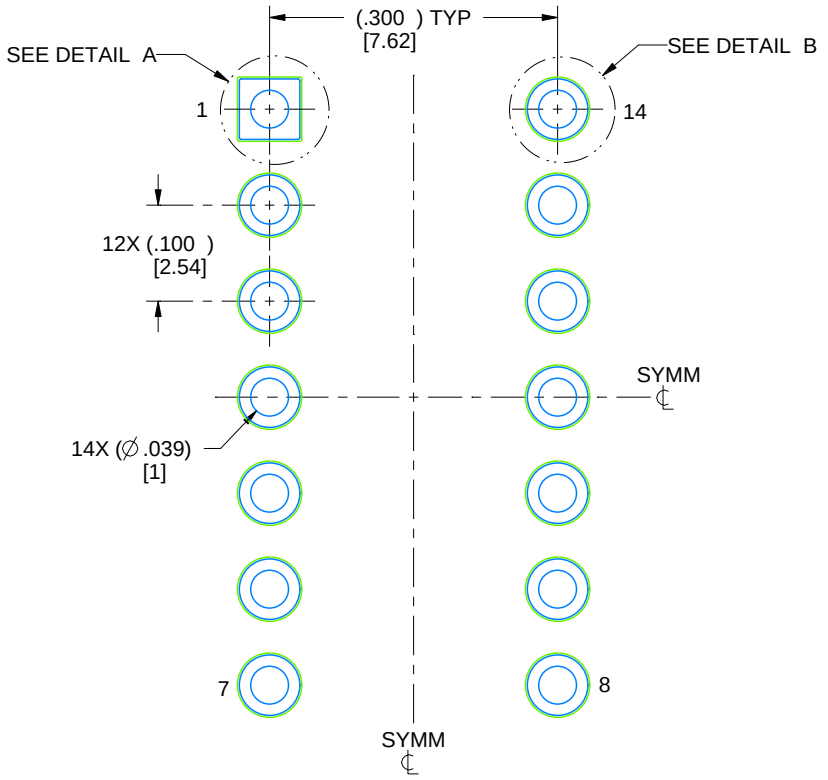
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

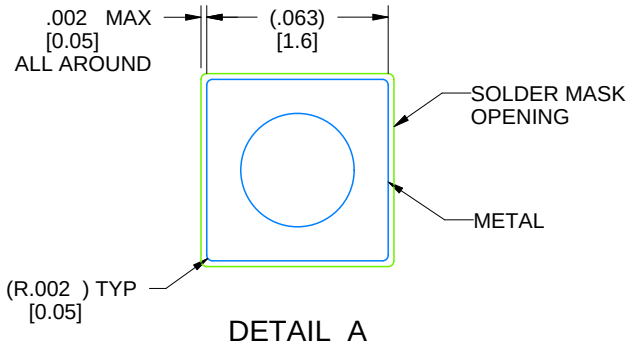
J0014A

CDIP - 5.08 mm max height

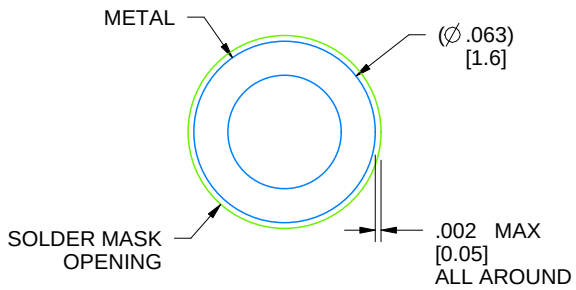
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



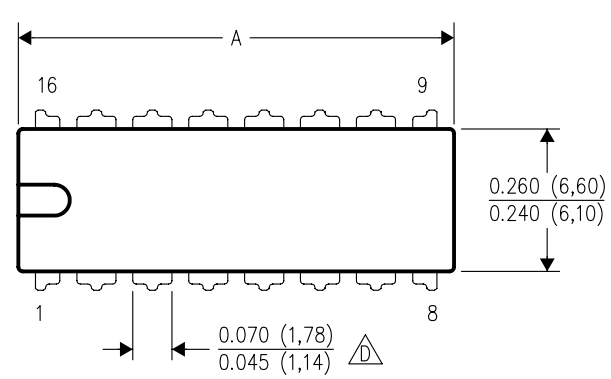
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

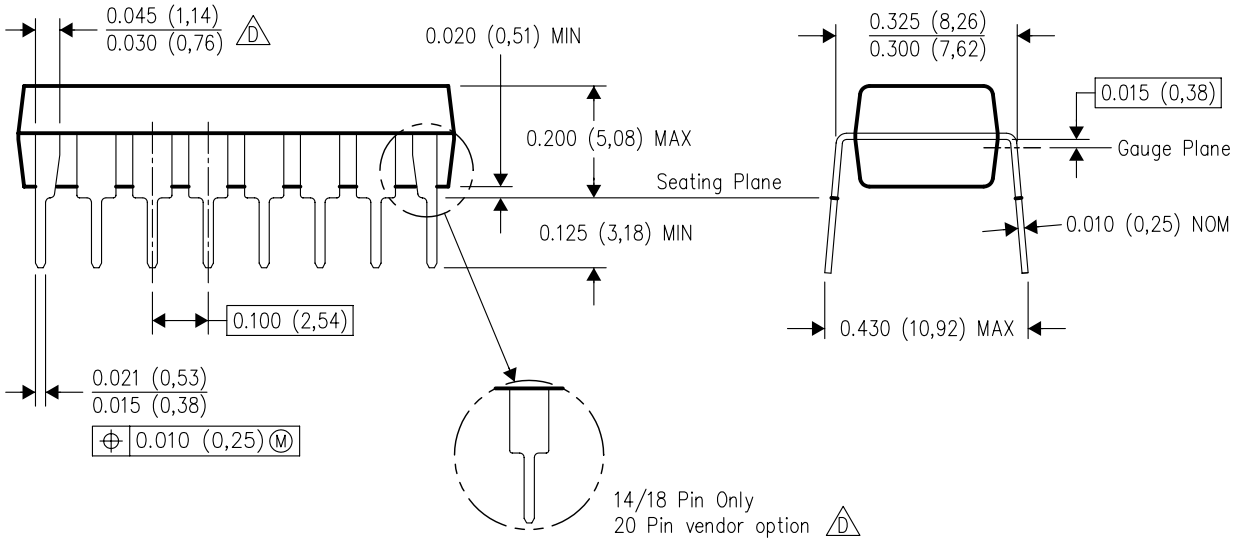
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

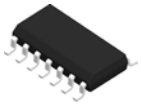


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

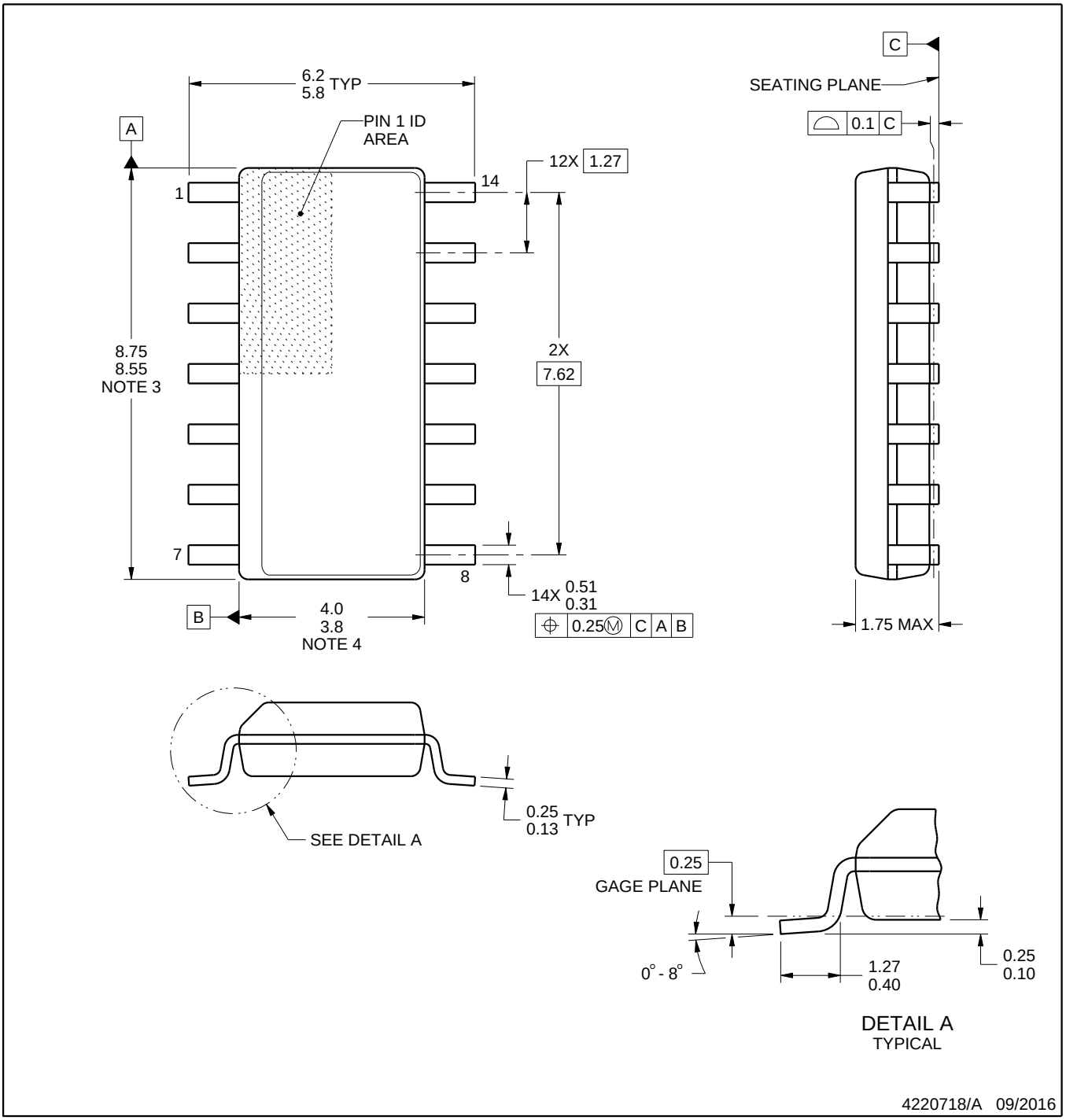


PACKAGE OUTLINE

D0014A

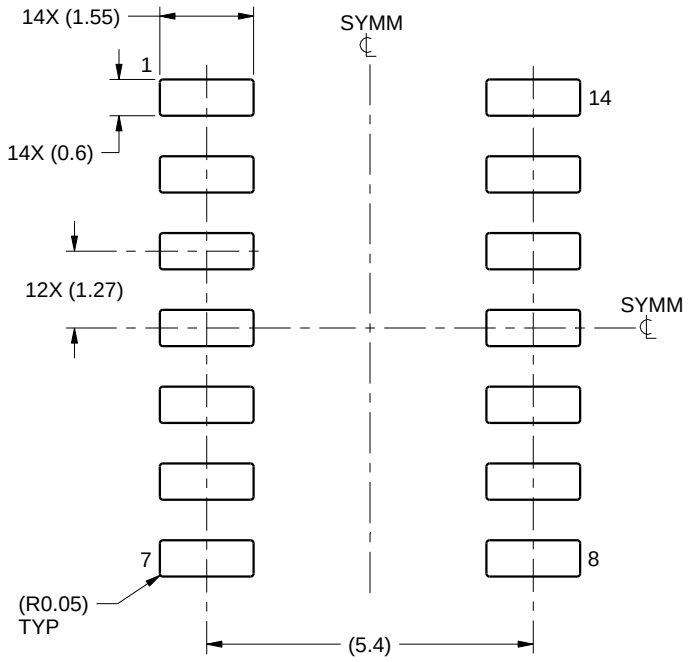
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

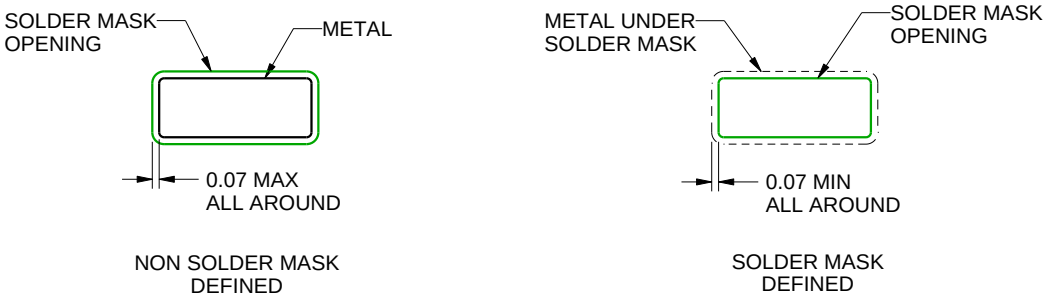


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

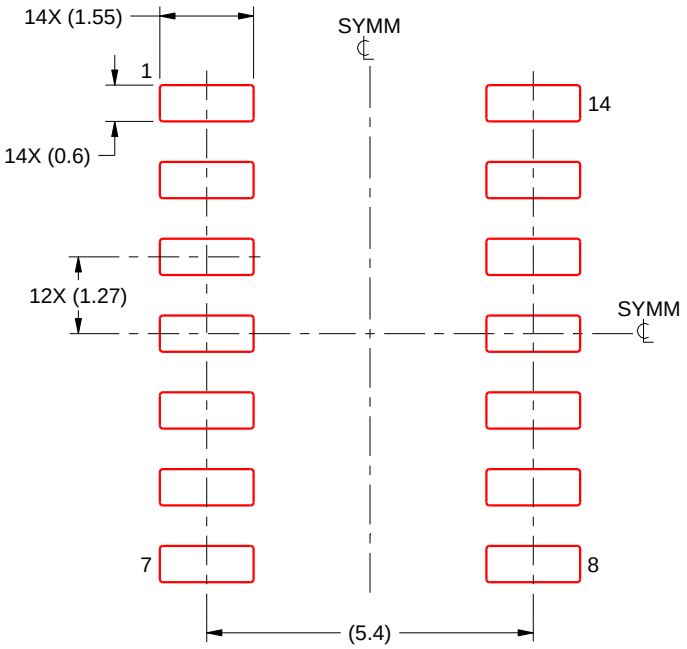
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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