

3 ステート出力、クワッド、2 ライン入力 1 ライン出力、データ選択 RS / マルチプレクサ

1 特長

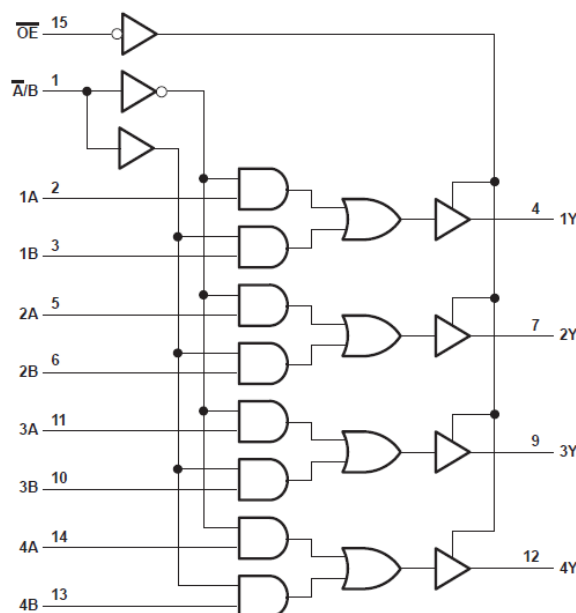
- 4.5V ~ 5.5V の動作電源電圧範囲
- 大電流 3 ステート出力は、システム・バスと直接インターフェイスする
- $t_{pd} = 17\text{ns}$ (標準値)
- 低消費電力、最大 $I_{CC} 80\mu\text{A}$
- 5V で $\pm 6\text{mA}$ の出力駆動能力
- 小さい入力電流、最大 $1\mu\text{A}$
- 入力は TTL 電圧互換
- 高性能システムの複数のソースからバス・インターフェイスを提供
- バッファ付き入力および出力

2 概要

HCT257 デバイスは、バス構成システムで 4 ビットのデータ・ソースからの信号を 4 つの出力データ・ラインへ多重化するように設計されています。

製品情報

発注型番	パッケージ	本体サイズ (公称)
SN74HCT257	N (PDIP, 16)	19.31mm × 6.35mm
	D (SOIC, 16)	9.90mm × 3.90mm
SNJ54HCT257	J (CDIP, 16)	24.38mm × 6.92mm



A. ここに示すピン番号は、D、J、N の各パッケージのものです。

論理図 (正論理)



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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2003) to Revision E (July 2022)

Page

- 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新..... 1

4 Pin Configuration and Functions

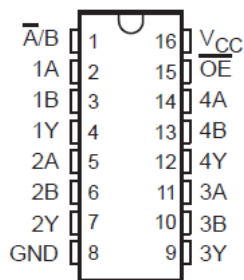


图 4-1. J, N and D Package
16-Pin CDIP, PDIP or SOIC
Top View

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	$\bar{A}/B$	I	Address select
2	1A	I	Channel 1, data input A
3	1B	I	Channel 1, data input B
4	1Y	I	Channel 1, data output
5	2A	O	Channel 2, data input A
6	2B	O	Channel 2, data input B
7	2Y	I	Channel 2, data output
8	GND	—	Ground
9	3Y	I	Channel 3, data output
10	3B	I	Channel 3, data input B
11	3A	I	Channel 3, data input A
12	4Y	I	Channel 4, data output
13	4B	I	Channel 4, data input B
14	4A	I	Channel 4, data input A
15	$\bar{G}$	I	Output strobe, active low
16	V _{CC}	—	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 35	mA
	Continuous current through V_{CC} or GND			± 70	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HCT257			SN74HCT257			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time				500			500	ns
T_A	Operating free-air temperature		-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

		D (SOIC)	N (PDIP)	UNIT
THERMAL METRIC		16 PINS	16 PINS	
$R_{\theta JA}$	Package thermal impedance	73	67	°C/W

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	$V_I = V_{IH}$ or V_{IL}	4.5 V	4.4	4.499		4.4		4.4		V
				3.98	4.3		3.7		3.84		
V_{OL}	L Low level output voltage	$V_I = V_{IH}$ or V_{IL}	4.5 V		0.001	0.1		0.1		0.1	V
					0.17	0.26		0.4		0.33	

5.4 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I _I	Input leakage current	V _I = V _{CC} or 0	5.5 V	±0.1	±100		±1000		±1000		nA
I _{oz}	Off-State (High-Impedance State) Output Current	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	5.5 V	±0.01	±0.5		±10		±5		μA
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0	5.5 V		8		160		80		μA
ΔI _{CC} ⁽²⁾	Supply-Current Change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V	1.4	2.4		3		2.9		mA
C _i	Input Capacitance		4.5 V to 5.5 V	3	10		10 ⁽¹⁾		10		pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
	A̅/B	Y	4.5 V		20	30		45		38	
			5.5 V		17	27		40		34	
t _{en}	OE̅	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t _{dis}	OE̅	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t _t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see [Figure 6-1](#))

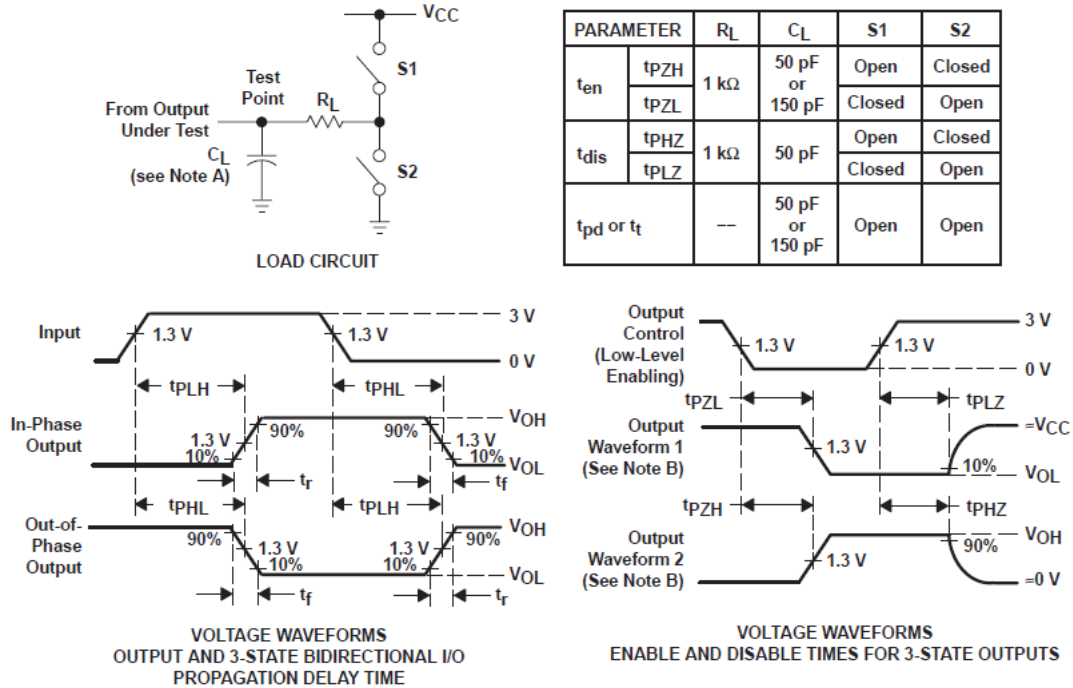
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C	T _A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		22	38		57		48	ns
			5.5 V		19	35		53		44	
	A̅/B	Y	4.5 V		22	38		57		48	
			5.5 V		19	35		53		44	
t _{en}	OE̅	Y	4.5 V		23	40		60		50	ns
			5.5 V		20	38		57		48	
t _t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

5.7 Operating Characteristics

 T_A 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	13	pF

6 Parameter Measurement Information



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The 'HCT257 devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

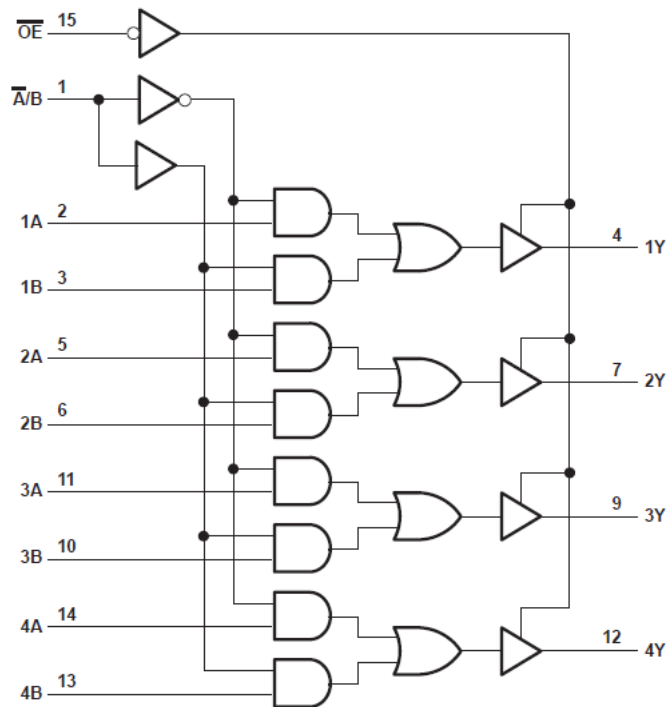


图 7-1. Function Diagram

8 Device Functional Modes

表 8-1. Function Table

INPUTS ⁽¹⁾				OUTPUT ⁽²⁾ Y
OE	SELECT A/B	DATA		
		A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

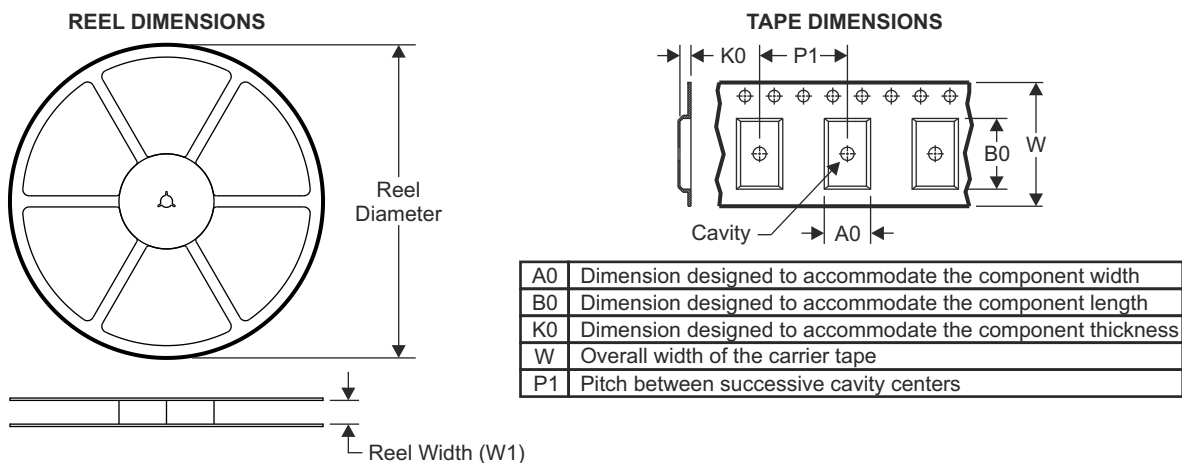
11.6 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

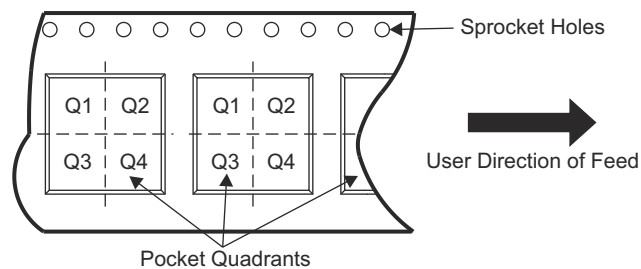
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

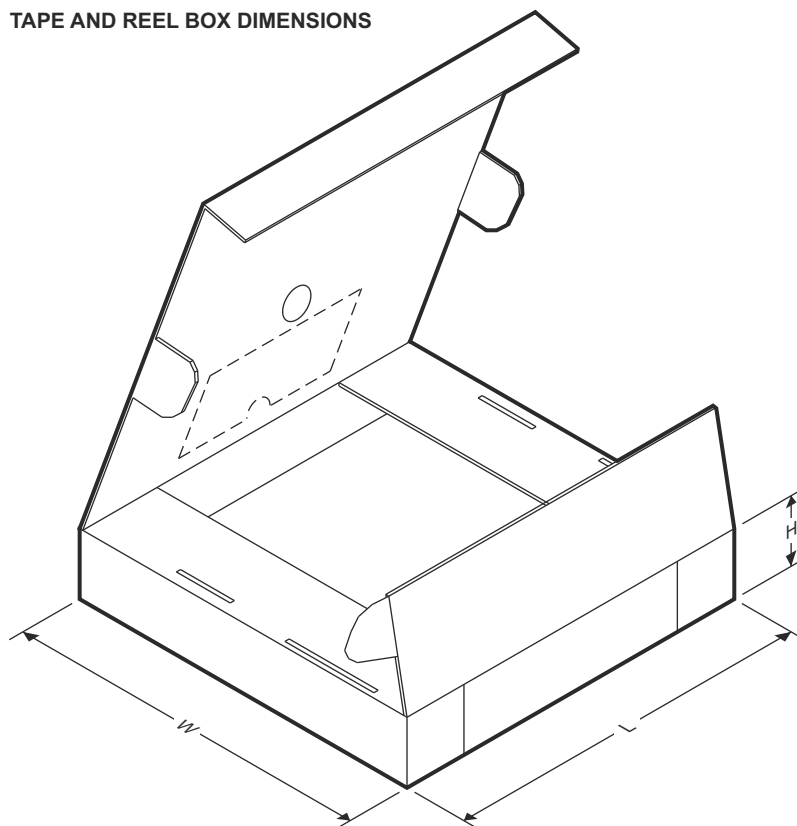


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)

12.2 Mechanical Data

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT257D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HCT257
SN74HCT257DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HCT257
SN74HCT257DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT257
SN74HCT257N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT257N
SN74HCT257N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT257N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

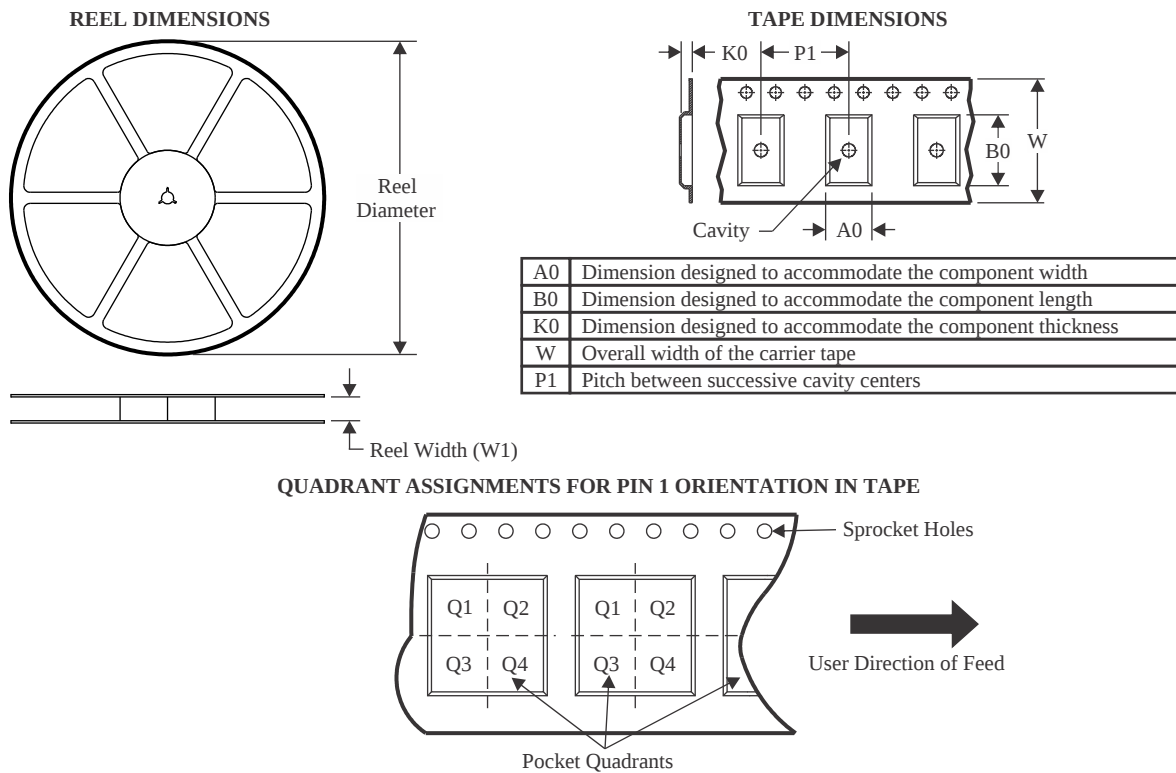
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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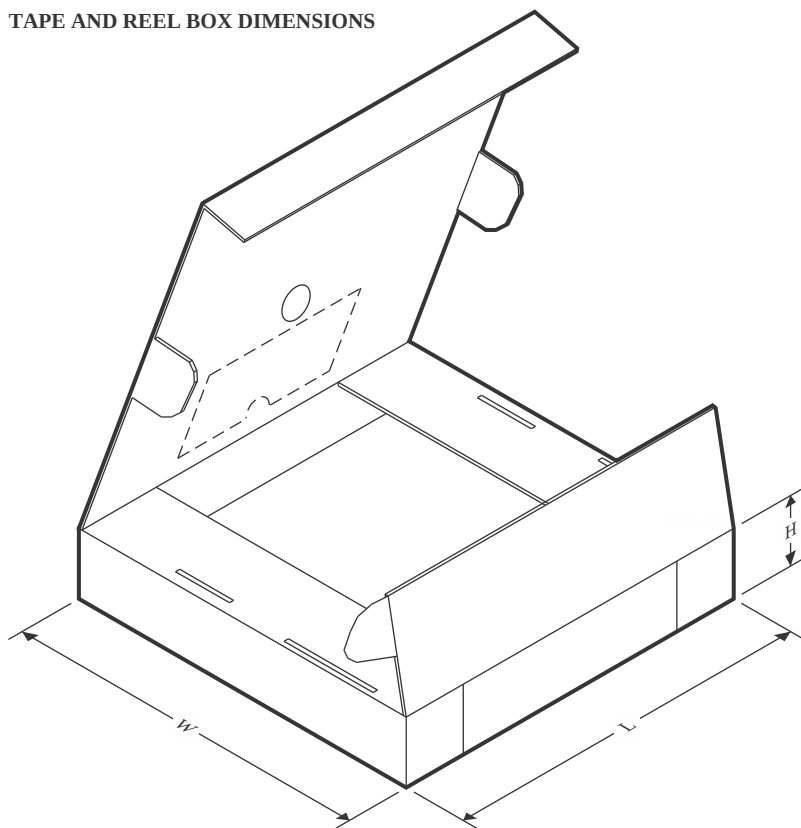
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

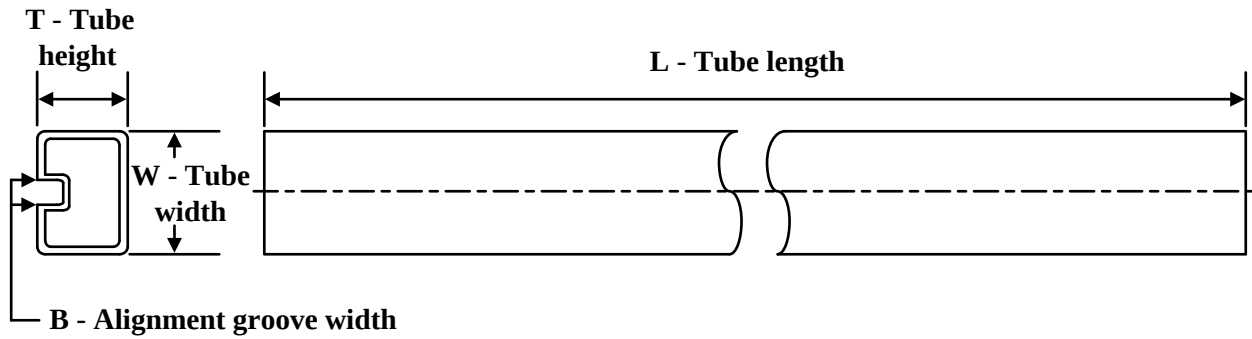
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT257DR	SOIC	D	16	2500	356.0	356.0	35.0

TUBE

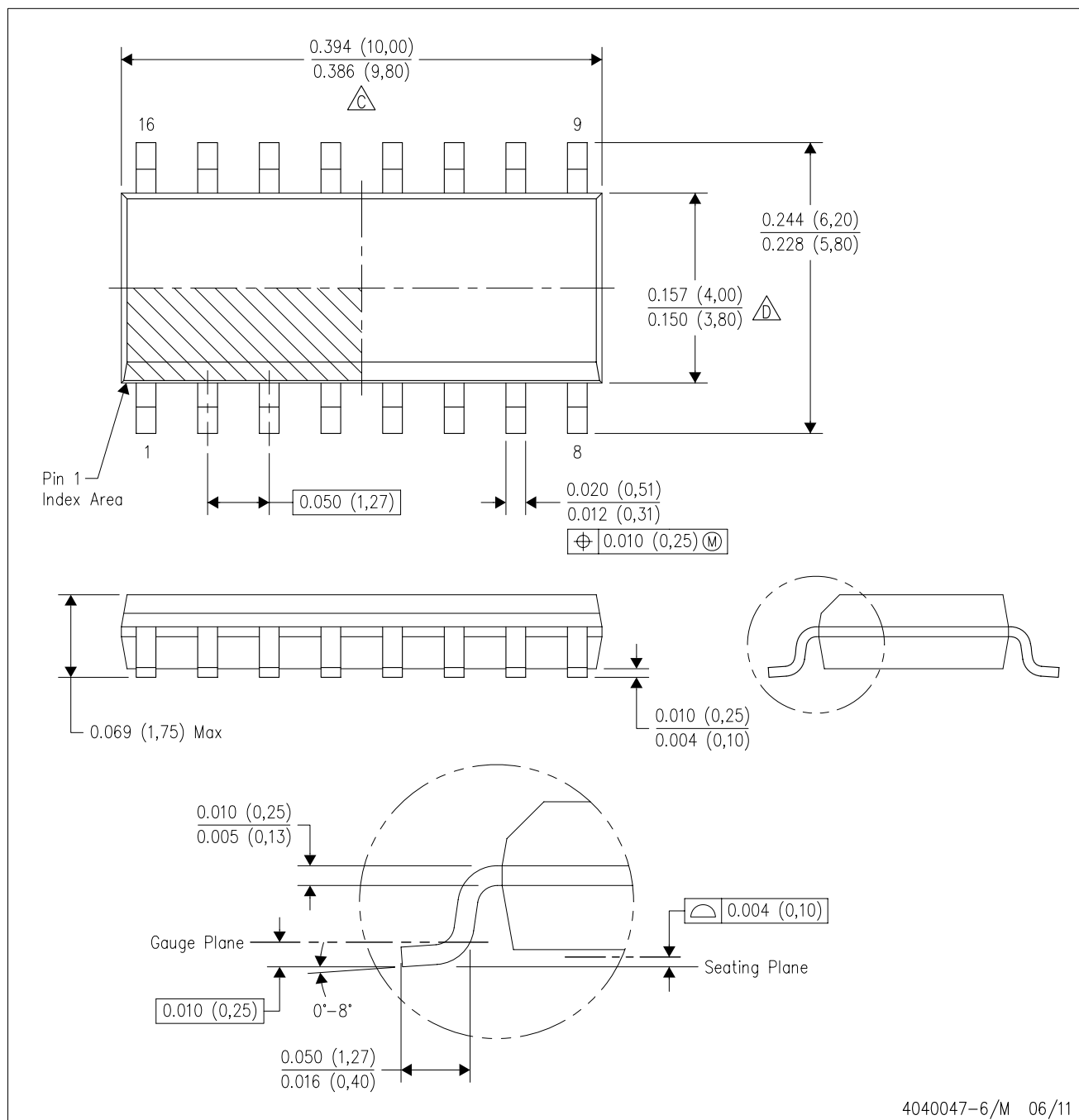


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT257N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT257N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



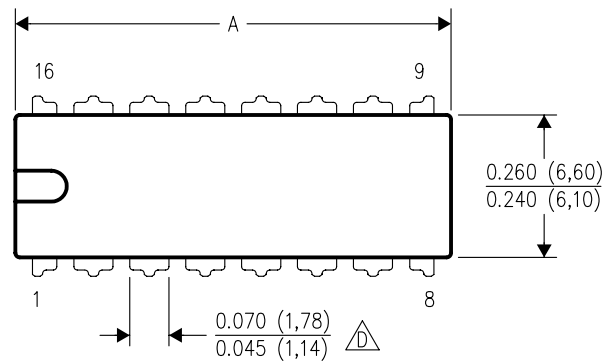
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

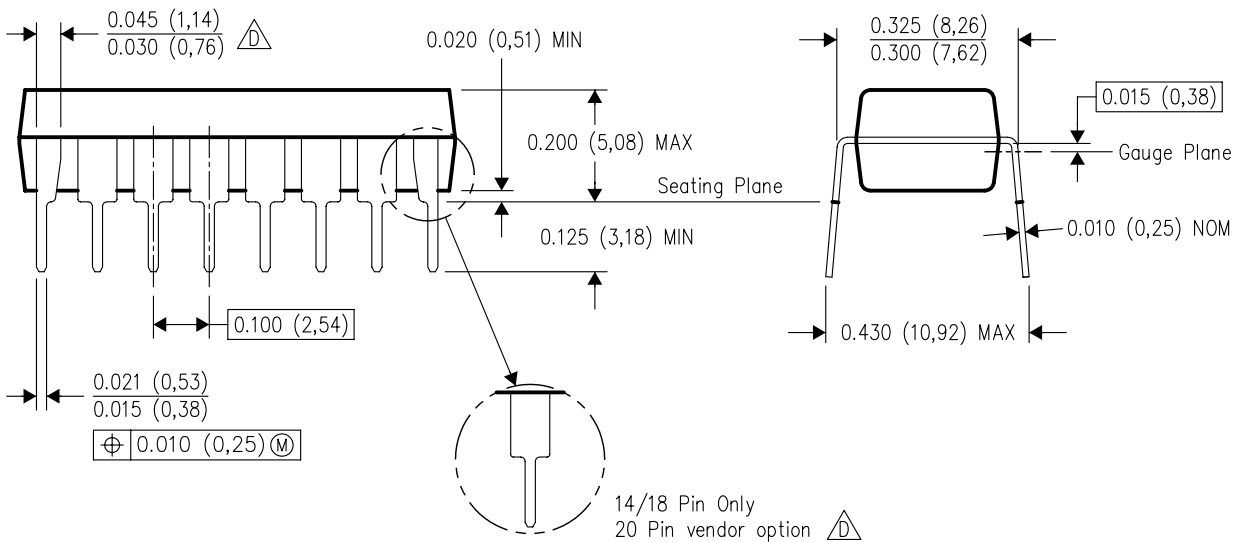
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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