TEXAS INSTRUMENTS

SN74HCS72-Q1
JAJSI39 – OCTOBER 2019

SN74HCS72-Q1 車載認定済み、クリア/プリセット機能搭載、シュミット・トリガ入力、デュアル D タイプ負エッジ・トリガ・フリップ・フロップ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - デバイス温度グレード 1: -40℃～+125℃、T_A
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 広い動作電圧範囲: 2V～6V
- シュミット・トリガ入力により低速またはノイズの多い入力信号に対応
- 低消費電力
  - I_{CC}：100nA (標準値)
  - 入力リーク電流：±100nA (標準値)
- 5V で ±7.8mA の出力駆動能力

2 アプリケーション

- モメンタリ・スイッチからトグル・スイッチへの変換
- 低速エッジレート信号の入力
- ノイズの多い環境での動作
- ウェイクアップ・パターンによる CAN コントローラ電源のイネーブル

3 概要
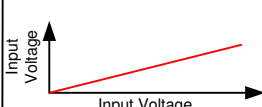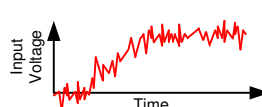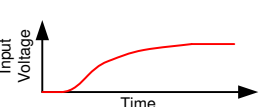
このデバイスには、2 つの独立した D タイプ負エッジ・トリガ・フリップ・フロップが含まれています。すべての入力はシュミット・トリガを備えているため、低速またはノイズの多い入力信号にも対応できます。プリセット ($\overline{PRE}$) 入力が Low レベルのとき、出力は High になります。クリア ($\overline{CLR}$) 入力が Low レベルのとき、出力は Low にリセットされます。プリセット機能とクリア機能は非同期であり、他方の入力レベルとは無関係です。$\overline{PRE}$ と $\overline{CLR}$ が非アクティブ (High) の場合、セットアップ時間の要件を満たすデータ (D) 入力のデータは、クロック ($\overline{CLK}$) パルスの負方向エッジで出力 (Q、$\overline{Q}$) に転送されます。ホールド時間が経過した後、データ (D) 入力のデータは、出力 (Q、$\overline{Q}$) のレベルに影響を及ぼさずに変化させることができます。

製品情報[1]
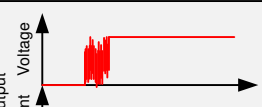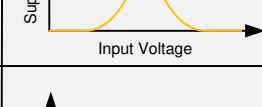
型番	パッケージ	本体サイズ（公称）
SN74HCS72QDRQ1	SOIC (14)	8.70mm x 3.90mm
SN74HCS72QPWRQ1	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

シュミットトリガ入力の利点

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			

目次

4 改訂履歴

日付	リビジョン	注
2019 年 10 月	*	初版

5 Pin Configuration and Functions

D and PW Package
14-Pin SOIC and TSSOP
Top View

```
1CLR    [   1  ○        14   ]  V_CC
1D      [   2            13   ]  2CLR
1CLK    [   3            12   ]  2D
1PRE    [   4            11   ]  2CLK
1Q      [   5            10   ]  2PRE
1Q̄      [   6             9   ]  2Q
GND     [   7             8   ]  2Q̄
```
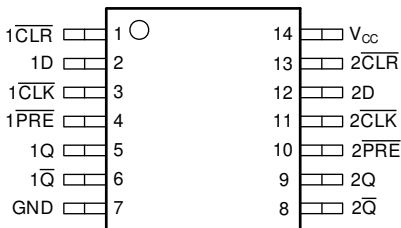
Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1$\overline{\text{CLR}}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1$\overline{\text{CLK}}$	3	Input	Clock for channel 1, falling edge triggered
1$\overline{\text{PRE}}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1$\overline{\text{Q}}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2$\overline{\text{Q}}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2$\overline{\text{PRE}}$	10	Input	Preset for channel 2, active low
2$\overline{\text{CLK}}$	11	Input	Clock for channel 2, falling edge triggered
2D	12	Input	Data for channel 2
2$\overline{\text{CLR}}$	13	Input	Clear for channel 2, active low
V$_{\text{CC}}$	14	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature[3]			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	−40		125	°C

6.4 Thermal Information

	THERMAL METRIC	SN74HCS72-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.1	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})[1]			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20 μA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0		6 V		0.1	2	μA
C_i	Input capacitance			2 V to 6 V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1)   Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	20	31		MHz
				4.5 V	64	95		
				6 V	74	105		
t_{pd}	Propagation delay	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		$\overline{CLK}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
t_t	Transition-time[1]		Q or $\overline{Q}$	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1) t_t = t_r or t_f, whichever is larger

6.7 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		2 V			20	MHz
			4.5 V			64	
			6 V			74	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	8	7		ns
			4.5 V	7	5		
			6 V	7	5		
		$\overline{CLK}$ high or low	2 V	10	5		ns
			4.5 V	9	3		
			6 V	8	2		
t_{su}	Setup time before $\overline{CLK}$ low	Data	2 V	16	11		ns
			4.5 V	6	1		
			6 V	3	1		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	7			ns
			4.5 V	0			
			6 V	0			
t_h	Hold time	Data after CLK ↓	2 V	5			ns
			4.5 V	3			
			6 V	2			

6.8 Typical Characteristics

$T_A = 25°C$
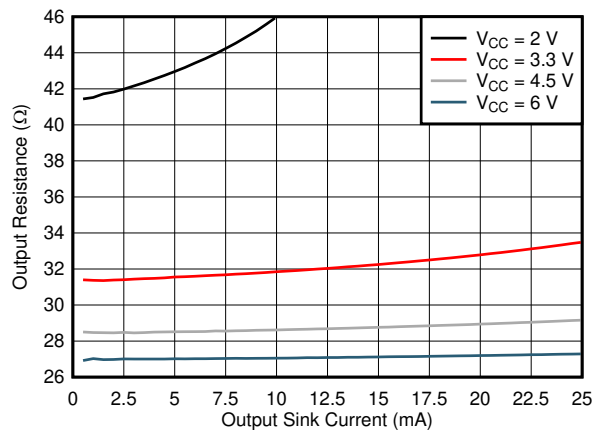
図 1. Output driver resistance in LOW state.

図 2. Output driver resistance in HIGH state.
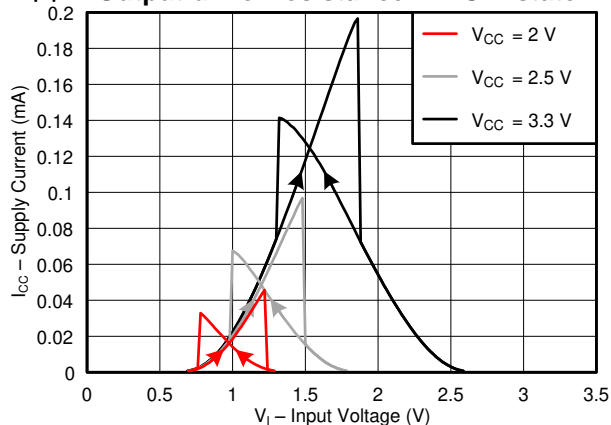
図 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

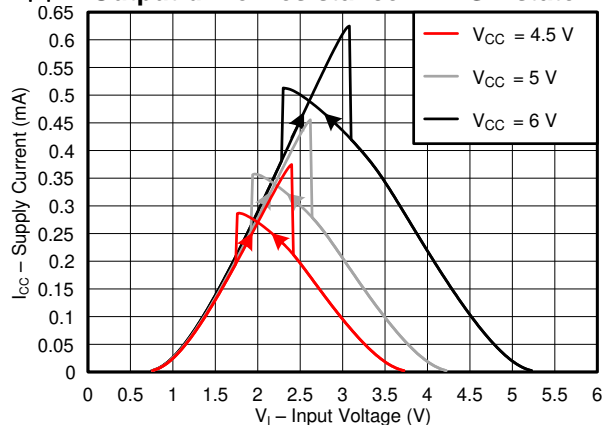図 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
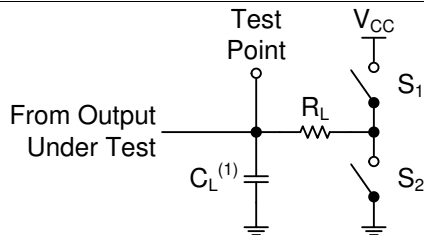
C_L includes probe and test-fixture capacitance.
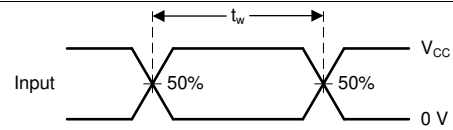
図 5. **Load Circuit**
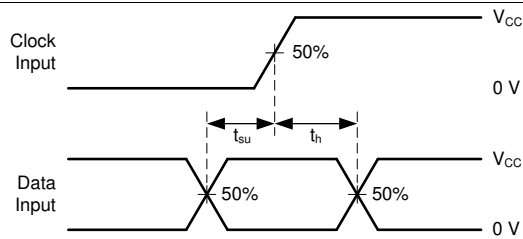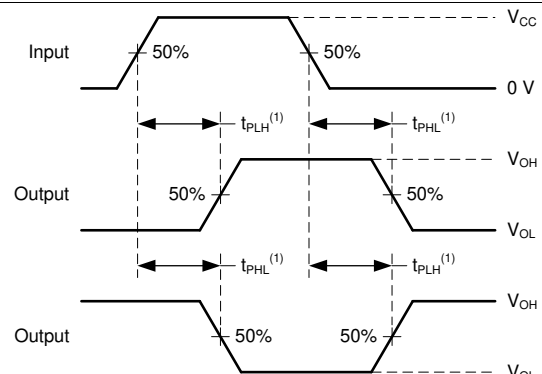
図 6. **Voltage Waveforms, Pulse Duration**

図 7. **Voltage Waveforms, Setup and Hold Times**

Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.
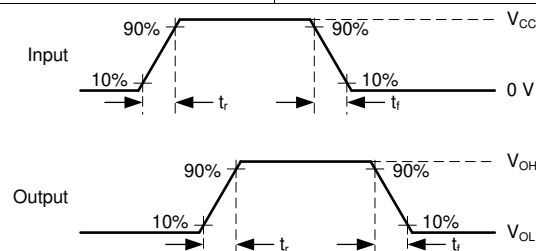
図 8. **Voltage Waveforms Propagation Delays**

図 9. **Voltage Waveforms, Input and Output Transition Times**

8 Detailed Description

8.1 Overview

図 10 describes the SN74HCS72-Q1. As the SN74HCS72-Q1 is a dual D-Type negative-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.
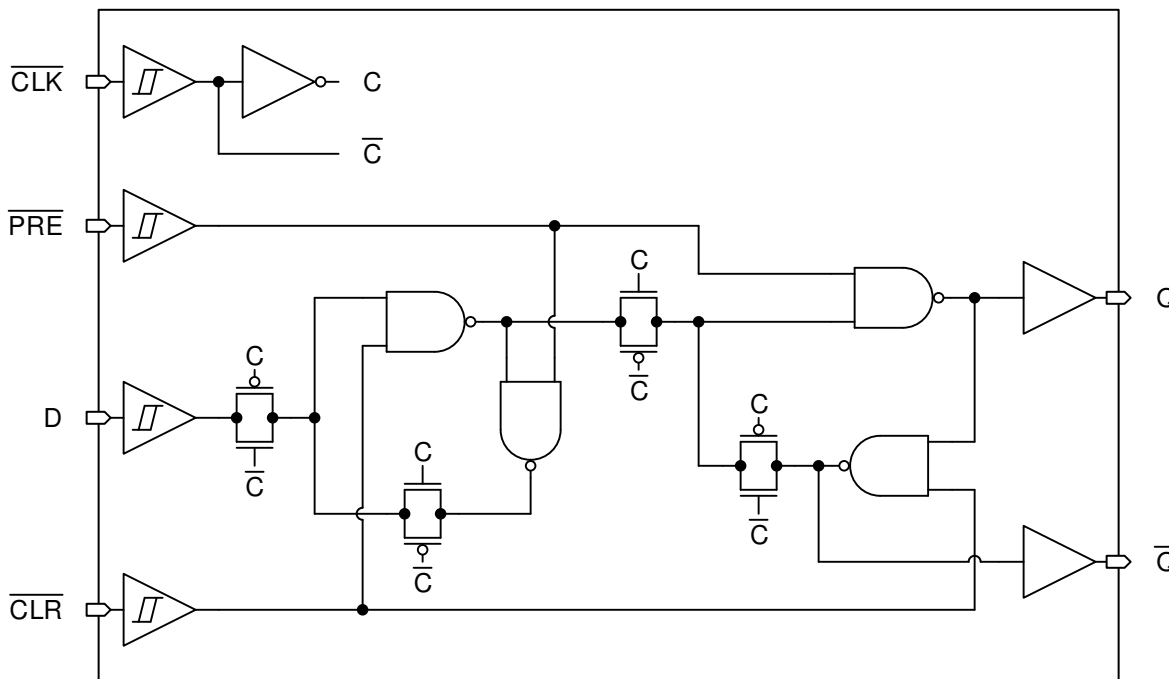
8.2 Functional Block Diagram

図 10. Logic Diagram (Positive Logic) for one channel of SN74HCS72-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Feature Description (continued)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 図 11.

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
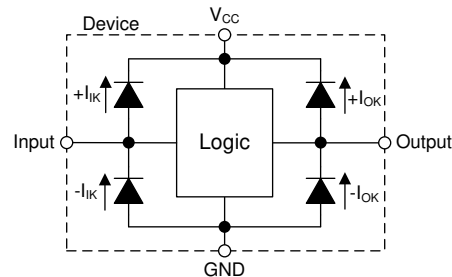
図 11. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 1 lists the functional modes of the SN74HCS72-Q1.

表 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	$\overline{CLK}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[1]	H[1]
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

9 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS72-Q1 is an ideal device for taking a CAN wake-up request and converting it to a power supply enable due to its low power consumption and noise rejecting inputs, which eliminate false triggers. CAN communication can occur when the vehicle ignition is off. Therefore, many circuits are designed to work in a standby or low power mode. Because a CAN wake-up request causes the RX pin to pulse LOW, the SN74HCS72-Q1 will trigger off the falling edge enabling the power for the CAN controller. Then the CAN controller powers on for the incoming communication. When communications are finished, the controller sends a reset pulse to the SN74HCS72-Q1 and CAN transceiver putting the circuit back into a standby mode.

9.2 Typical Application
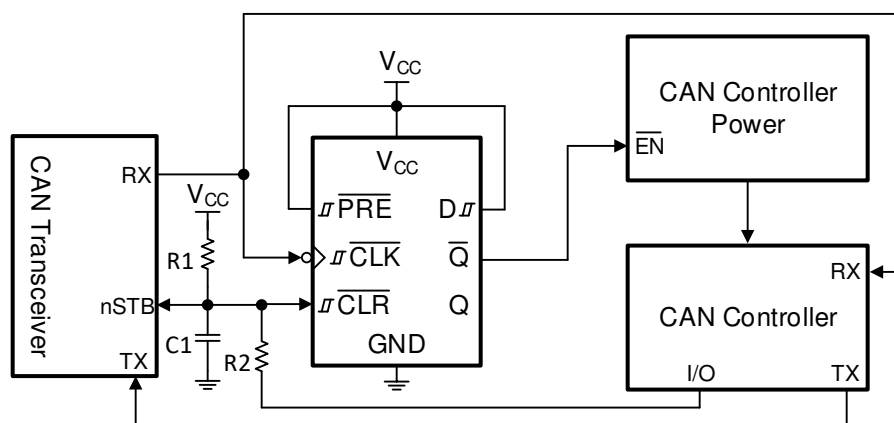
図 12. Power Enable Using CAN Wake-up Request

9.2.1 Design Requirements

The SN74HCS72-Q1 device allows flexibility by having complementary outputs for active-high or active-low enables. The supply should be selected such that the device is always powered along with the CAN transceiver. The same supply for both devices is recommended.

With the SN74HCS72-Q1, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately 2.2×RC. In this application, it is desired to have the output ($\overline{Q}$) in the HIGH state at startup, so R1 and C1 are connected directly to the $\overline{CLR}$ pin, as shown in 図 12. A second resistor is needed to limit the current into the CAN controller when it sets the circuit back into standby mode. It is required for the R1 resistor to be at least ten times larger than R2 to avoid a divider circuit (R2 ≤ 10R1).

The D input can be tied either to V_{CC} or ground depending on the desired implementation. In this example, it is tied to V_{CC} to obtain a HIGH signal from $\overline{Q}$ when a wake-up request occurs.

Typical Application (continued)

9.2.1.1 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the flip-flop output is transmitting over a relatively short trace (under 10 cm) to a CMOS input.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
    - See the *Switching Characteristics* section for the capacitive loads tested with this device.
    - Increasing capacitance will proportionally increase output transition times.
    - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 µA
    - Leakage current into connected devices.
    - Parasitic current from other components.
    - Resistive load current.
- Output Voltage: see *Electrical Characteristics* for output voltage ratings at a given current.
    - Output HIGH (V_{OH}) and output LOW (V_{OL}) voltage levels affect the input voltage, V_{IH} and V_{IL}, respectively, to subsequent devices.

9.2.1.2 Input Considerations

The SN74HCS72-Q1 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than $V_{T+(max)}$ to be guaranteed to be read as a logic high, and below $V_{T-(min)}$ to be guaranteed to be read as a logic low, as defined in the *Electrical Characteristics*. Do not exceed the values specified in the *Absolute Maximum Ratings* or the device could be damaged.

9.2.1.3 Timing Considerations

The SN74HCS72-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Characteristics* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Characteristics*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Characteristics*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Characteristics*.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
    - Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
    - Input thresholds are listed in the *Electrical Characteristics*.
    - Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the *Absolute Maximum Ratings*. Do not exceed the absolute maximum voltage rating of the device or it could be damaged.
2. Recommended Output Conditions:
    - Load currents should not exceed the value listed in the *Absolute Maximum Ratings*.
    - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the

Typical Application (continued)

output current.

9.2.3 Application Curve

RX

$\overline{Q}$

I/O

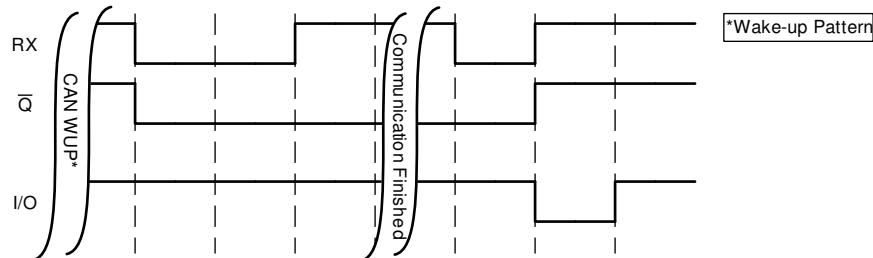CAN WUP*

Communication Finished

*Wake-up Pattern

図 13. **Application timing diagram**

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-µF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in 図 14 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.
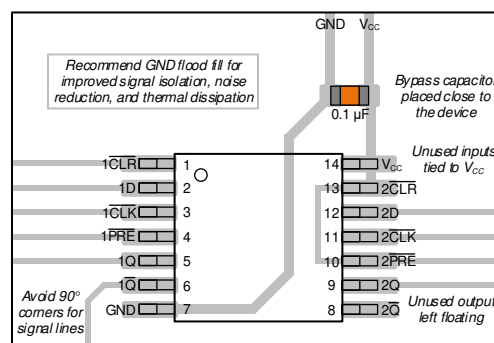
11.2 Layout Example

GND V_{CC}

Recommend GND flood fill for improved signal isolation, noise reduction, and thermal dissipation

0.1 µF

Bypass capacitor placed close to the device

1CLR	1	14	V_{CC}	*Unused inputs tied to V_{CC}*
1D	2	13	2CLR	
1CLK	3	12	2D	
1PRE	4	11	2CLK	
1Q	5	10	2PRE	
1Q̅	6	9	2Q	
GND	7	8	2Q̅	*Unused output left floating*

Avoid 90° corners for signal lines

図 14. **Layout Example**

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『*Implications of Slow or Floating CMOS Inputs*』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『*Reduce Noise and Save Power with the New HCS Logic Family*』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『*Understanding Schmitt Triggers*』アプリケーション・レポート (英語)

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商標

E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS72QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1
SN74HCS72QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1
SN74HCS72QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q
SN74HCS72QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS72-Q1 :

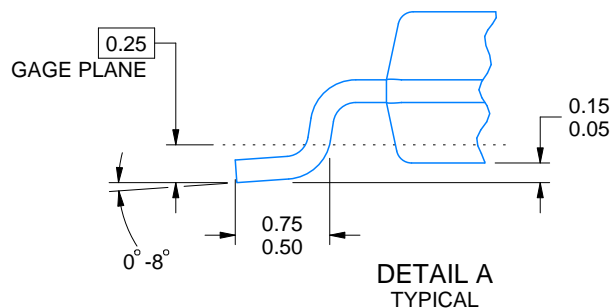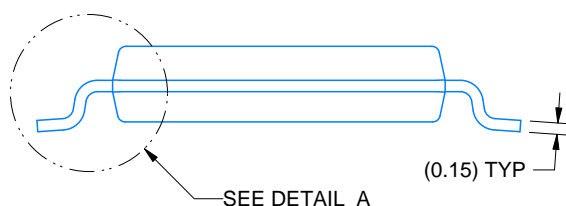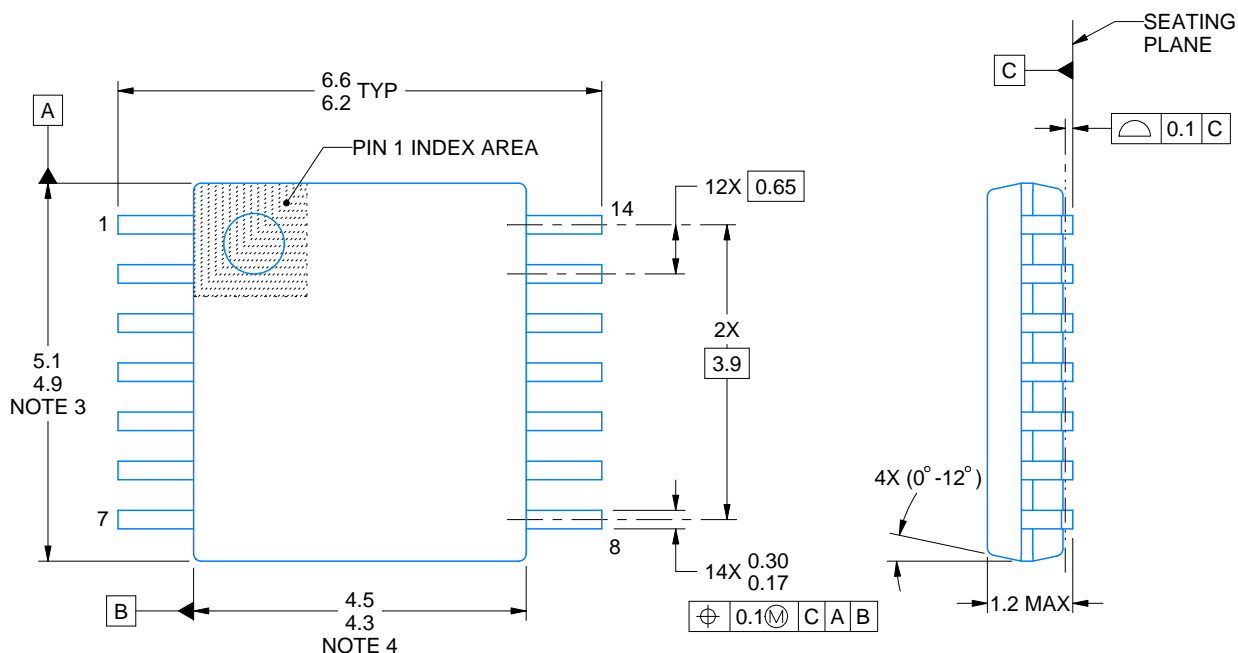● Catalog : SN74HCS72

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

SEATING PLANE

PIN 1 INDEX AREA

6.6 / 6.2 TYP

A

1

14

12X 0.65

2X 3.9

5.1 / 4.9 NOTE 3

7

8

14X 0.30 / 0.17

4X (0°-12°)

1.2 MAX

B

4.5 / 4.3 NOTE 4

⌖ 0.1 Ⓜ C A B

C

⌓ 0.1 C

SEE DETAIL A

(0.15) TYP

GAGE PLANE 0.25

0°-8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

4220718/A   09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

SYMM

14

8

7

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

14X (1.55)

1

14X (0.6)

12X (1.27)

7

8

14

(5.4)

SYMM

SYMM

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.