SN74HCS594-Q1 車載用　8 ビット・シフト・レジスタ、シュミット・トリガ入力 / 出力レジスタ付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃、T_A
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- ウェッタブル・フランク QFN (WBQB) パッケージで供給
- 広い動作電圧範囲:2V～6V
- シュミット・トリガ入力により低速の入力信号またはノイズの多い入力信号に対応
- 低消費電力:
  - I_{CC}:100nA (標準値)
  - 入力リーク電流:±100nA (標準値)
- 6V で ±7.8mA の出力駆動能力

2 アプリケーション

- 出力拡張
- LED マトリクス制御
- 7 セグメント・ディスプレイ制御
- 8 ビット・データ・ストレージ

3 概要

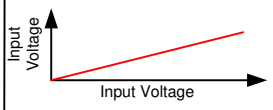
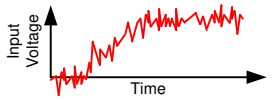
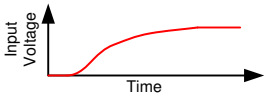
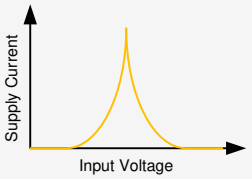
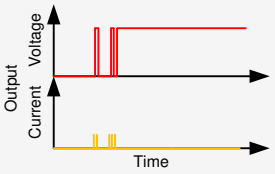
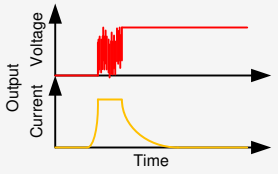
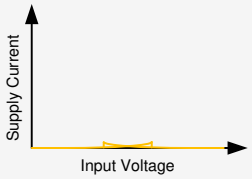
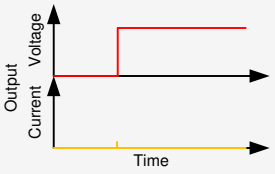
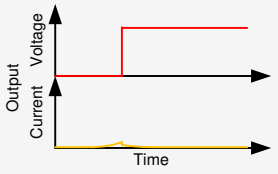
SN74HCS594-Q1 デバイスには、8 ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが内蔵されており、8 ビットの D タイプ・ストレージ・レジスタへデータを供給します。すべての入力はシュミット・トリガを備えているため、低速エッジまたはノイズの多い入力信号によるデータ出力エラーを解消できます。ストレージ・レジスタはパラレル出力を備えています。シフト・レジスタとストレージ・レジスタの両方に対して、独立したクロックとダイレクト・オーバーライディング・クリア ($\overline{SRCLR}$、$\overline{RCLR}$) 入力が提供されます。カスケード接続用にシリアル出力 ($Q_{H'}$) が用意されています。

シフト・レジスタ (SRCLK) とストレージ・レジスタ (RCLK) クロックの両方がポジティブ・エッジ・トリガです。両方のクロックが一緒に接続されている場合、シフト・レジスタはストレージ・レジスタより 1 カウント・パルス前になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)	本体サイズ (公称) (3)
SN74HCS594-Q1	PW (TSSOP、16)	5mm × 6.4mm	5mm × 4.4mm
	D (SOIC、16)	9.9mm × 6mm	9.9mm × 3.9mm
	BQB (WQFN、16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	DYY (SOT-23-THN、16)	4.2mm × 2mm	4.2mm × 2mm
	WBQB (WQFN、16)	3.6mm × 2.6mm	3.6mm × 2.6mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれていません。

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			

シュミット・トリガ入力の利点

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (December 2021) to Revision E (July 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- パッケージ・サイズを含めるよう「パッケージ情報」表を更新 ... 1
- Updated the *Function Table* ... 13

Changes from Revision C (June 2021) to Revision D (December 2021) — **Page**

- 「製品情報」表に WBQB パッケージの情報を追加 ... 1
- Added WBQB Package, pinout diagram and information to *Pin Configuration and Functions* ... 4
- Added WBQB package to Thermal Information table ... 6
- Added Wettable Flanks section to *Feature Description* ... 11

Changes from Revision B (March 2021) to Revision C (June 2021) — **Page**

- DYY パッケージを製品プレビューから量産データへ変更 ... 1

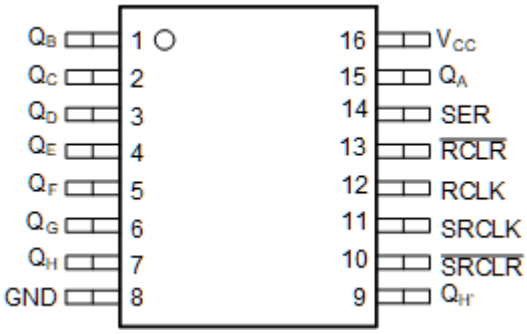
Changes from Revision A (February 2021) to Revision B (March 2021) — **Page**

- 「製品情報」表に DYY パッケージの情報を追加 ... 1
- Added DYY Package, pinout diagram and information to *Pin Configuration and Functions* ... 4
- Added DYY Package to *Thermal Information* table ... 6

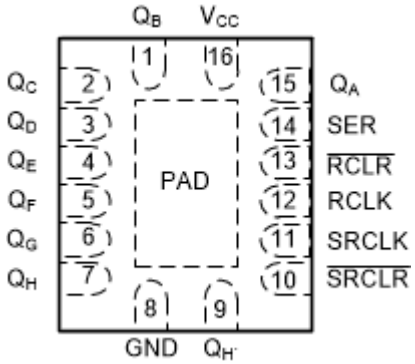
Changes from Revision * (June 2020) to Revision A (February 2021) — **Page**

- 「製品情報」に BQB パッケージの情報を追加 ... 1
- Added BQB Package, information to *Pin Configuration and Functions* ... 4
- Added BQB Package to *Thermal Information* table ... 6

5 Pin Configuration and Functions



D, PW, or DYY Package,
16-Pin SOIC, TSSOP, or SOT
(Top View)



BQB or WBQB Package,
16-Pin WQFN
(Top View)

Pin Functions

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
Q_B	1	O	Q_B output
Q_C	2	O	Q_C output
Q_D	3	O	Q_D output
Q_E	4	O	Q_E output
Q_F	5	O	Q_F output
Q_G	6	O	Q_G output
Q_H	7	O	Q_H output
GND	8	—	Ground
$Q_{H'}$	9	O	Serial output, can be used for cascading
$\overline{SRCLR}$	10	I	Shift register clear, active low
SRCLK	11	I	Shift register clock, rising edge triggered
RCLK	12	I	Output register clock, rising edge triggered
$\overline{RCLR}$	13	I	Storage register clear, active low
SER	14	I	Serial input
Q_A	15	O	Q_A output
V_{CC}	16	—	Positive supply
Thermal Pad[1]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQB and WBQB Package, only.
(2) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Specified by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74HCS594-Q1					UNIT
		PW (TSSOP)	D (SOIC)	BQB (WQFN)	DYY (SOT)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	108.4	186.2	97.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	80.9	77.3	109.1	93.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	80.6	74.4	111.0	66.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	40.4	12.6	18.0	14.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	80.3	74.5	110.9	66.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	54.3	N/A	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})[1]			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF

(1) Specified by design.

6.6 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER			V_{CC}	Operating free-air temperature (T_A)				UNIT
				25°C		–40°C to 125°C		
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		32		17	
			4.5 V		100		54	
			6 V		115		68	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	8		12		ns
			4.5 V	6		7		
			6 V	6		7		
		$\overline{SRCLR}$ or $\overline{RCLR}$ low	2 V	7		12		
			4.5 V	6		7		
			6 V	6		7		
t_{su}	Setup time	SER before SRCLK ↑	2 V	11		16		ns
			4.5 V	4		7		
			6 V	4		5		
		SRCLK ↑ before RCLK ↑	2 V	15		24		
			4.5 V	5		9		
			6 V	5		7		
		$\overline{SRCLR}$ low before RCLK ↑	2 V	16		27		
			4.5 V	7		10		
			6 V	5		8		
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑	2 V	5		9		
			4.5 V	3		5		
			6 V	3		4		
		$\overline{RCLR}$ high (inactive) before RCLK ↑	2 V	8		12		
			4.5 V	4		5		
			6 V	3		4		
t_h	Hold time	SER after SRCLK ↑	2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

6.7 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Max switching frequency			2 V	32			17			MHz
				4.5 V	100			54			
				6 V	115			68			
t_{pd}	Propagation delay	SRCLK	$Q_{H'}$	2 V		19	30			45	ns
				4.5 V		7	11			17	
				6 V		6	9			12	
		RCLK	Q_A - Q_H	2 V		19	30			45	
				4.5 V		7	11			17	
				6 V		6	9			12	
t_{PHL}	Propagation delay	$\overline{SRCLR}$	$Q_{H'}$	2 V		18	27			55	ns
				4.5 V		7	11			17	
				6 V		6	9			15	
		$\overline{RCLR}$	Q_A - Q_H	2 V		18	27			55	
				4.5 V		7	11			17	
				6 V		6	9			15	
t_t	Transition-time		Any output	2 V			9			16	ns
				4.5 V			5			9	
				6 V			4			8	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF

6.9 Typical Characteristics

T_A = 25°C

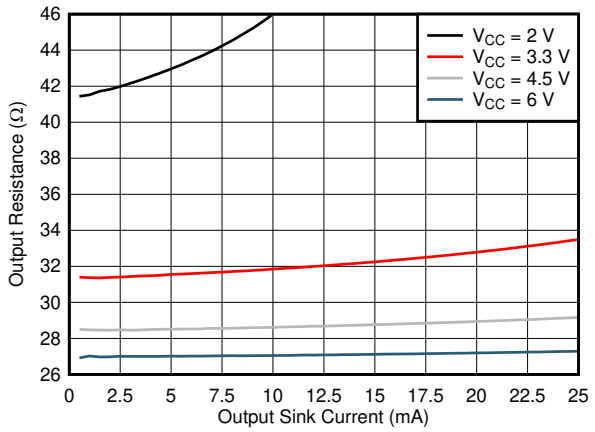


図 6-1. Output Driver Resistance in LOW State

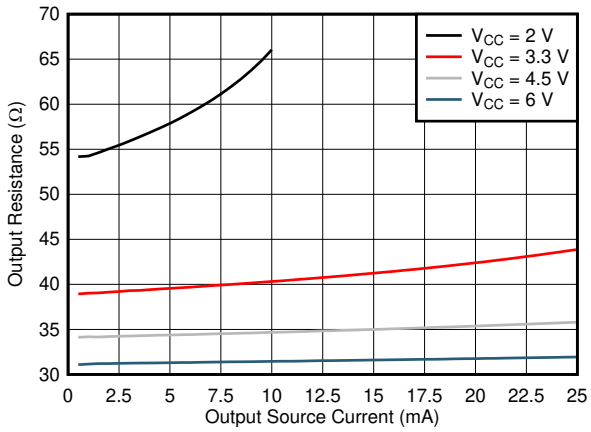


図 6-2. Output Driver Resistance in HIGH State

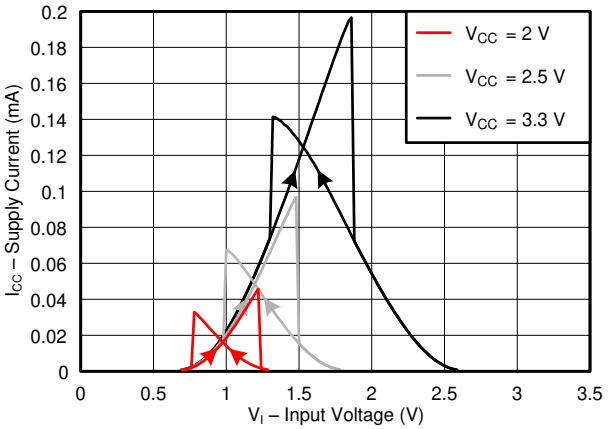


図 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

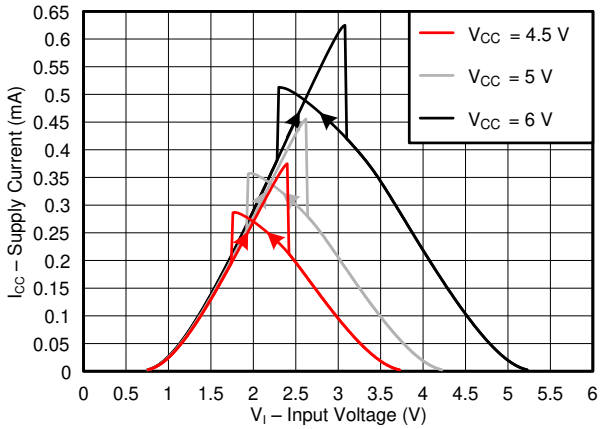


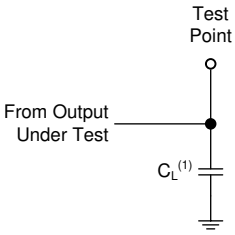
図 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 7-1. Load Circuit for Push-Pull Outputs

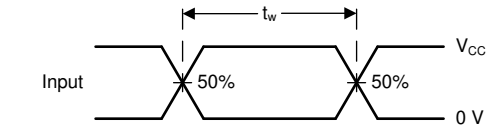


図 7-2. Voltage Waveforms, Pulse Duration

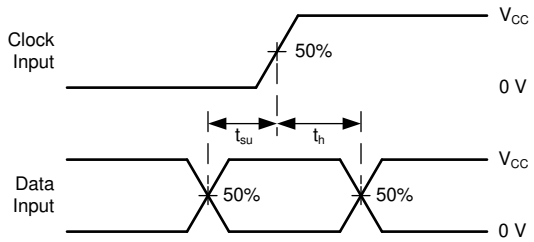
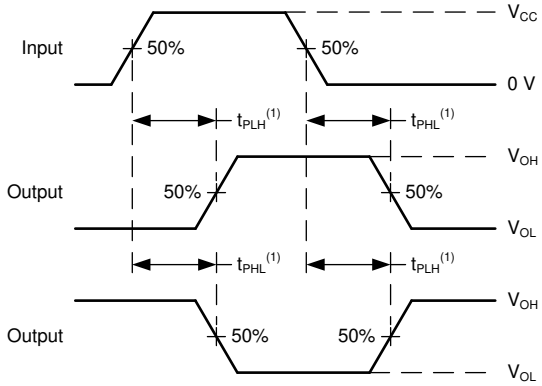
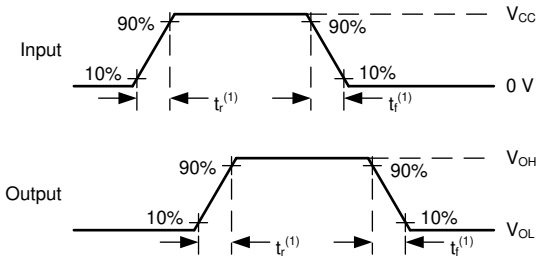


図 7-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

図 7-5. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

The SN74HCS594-Q1 is an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. All inputs include Schmitt-triggers allowing for slow input transitions and providing more noise margin.

8.2 Functional Block Diagram

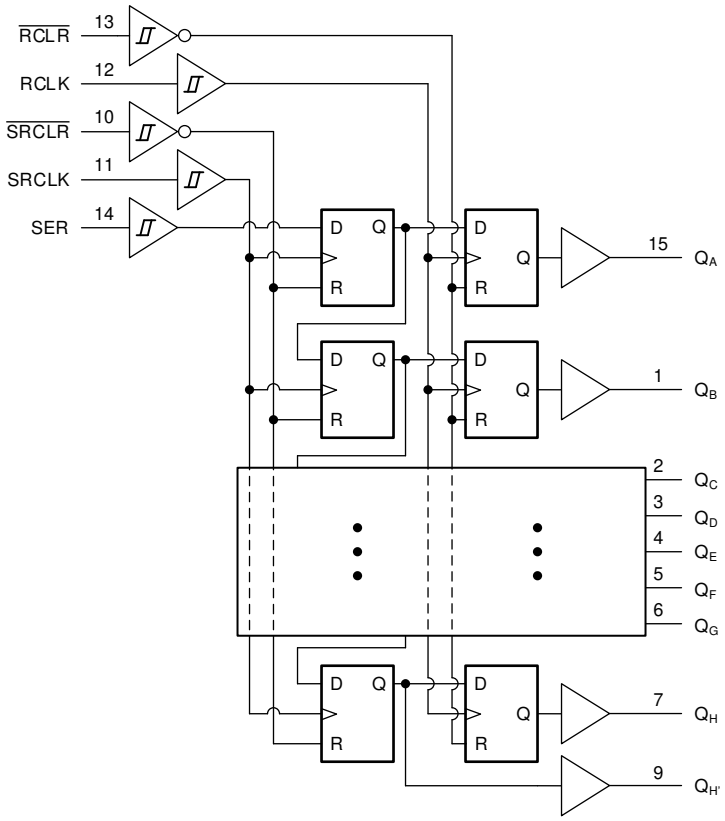


図 8-1. Logic Diagram (Positive Logic) for SN74HCS594-Q1

8.3 Feature Description

8.3.1 平衡な CMOS プッシュプル出力

このデバイスには、平衡な CMOS プッシュプル出力が内蔵されています。「平衡な」という用語 は、デバイスが同様の電流をシンクおよびソースできることを示します。このデバイスは駆動能力を備えており、軽負荷に高速エッジが生成されるため、リンギングを防ぐために配線と負荷の条件を考慮する必要があります。さらに、このデバイスの出力は、デバイスを損傷することなく維持できる以上に大きな電流を駆動できます。過電流による損傷を防止するため、デバイスの出力電力を制限することが重要です。「絶対最大定格」で定義されている電気的および熱的制限を常に順守してください。

未使用のプッシュプル CMOS 出力は、未接続のままにする必要があります。

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

8.3.3 Clamp Diode Structure

As shown in 図 8-2, the inputs and outputs to this device have both positive and negative clamping diodes.

> **注意**
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

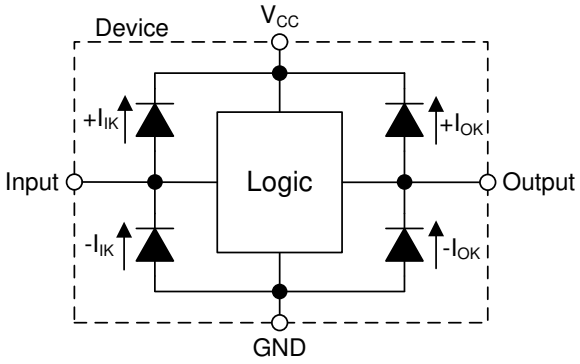


図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

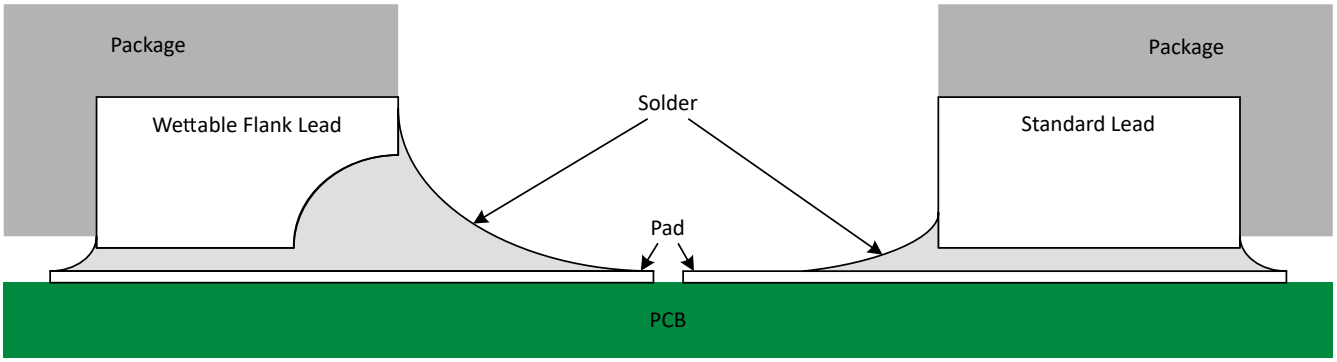


図 8-3. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 図 8-3, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74HCS594-Q1.

表 8-1. Function Table

INPUTS(1)					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	X	X	L	Output register is cleared
X	X	L	X	X	Internal shift register is cleared
H/L	↑	H	X	X	SER Data is loaded into first shift bit as H/L, data shifts from bit to bit within the internal shift register
X	X	H	↑	H	Data is transferred from internal shift register to output register
H/L	↑	H	↑	H	When SRCLK and RCLK are synchronous, Data is transferred from internal shift register to output register, internal shift register first bit is loaded with SER data H/L and data shifts from bit to bit within internal shift register
X	↓, L, H	H	X	X	Internal shift register remains in previous state
X	X	H	↓, L, H	H	Output register remains in previous state

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

In this application, the SN74HCS594-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCS594-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

There is no practical limitation to how many SN74HCS594-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, both registers need to be cleared. An RC can be connected to the $\overline{\text{SRCLR}}$ and $\overline{\text{RCLR}}$ pins as shown in the 図 9-1 to initialize the shift and output registers to all zeros.

9.2 Typical Application

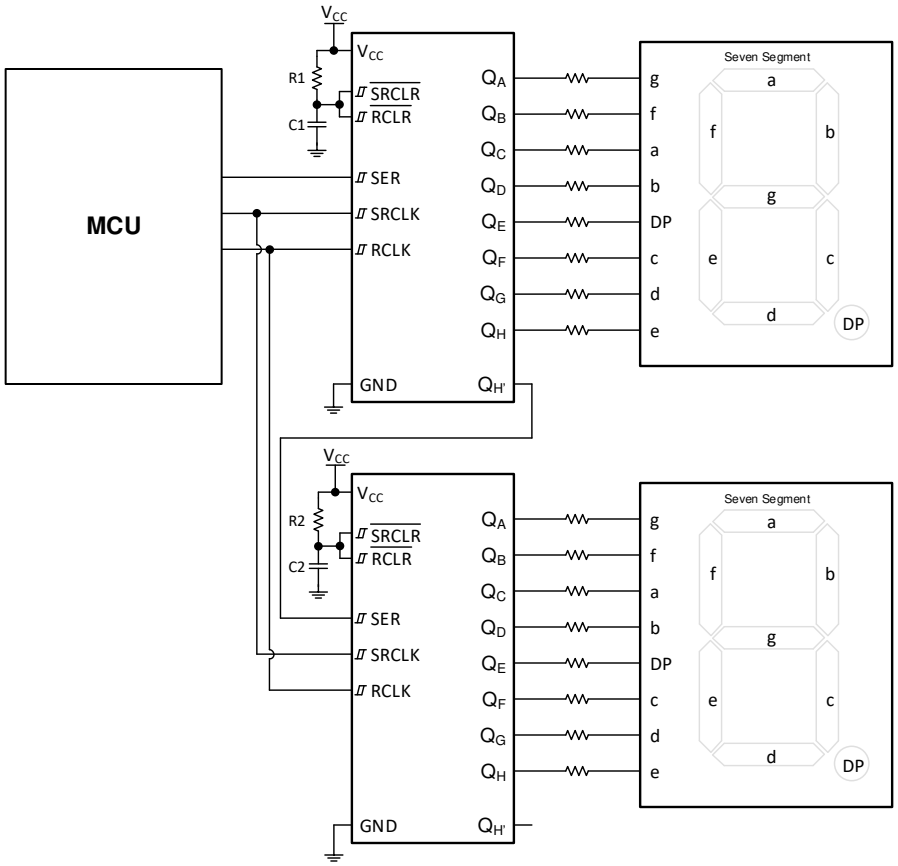


図 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS594-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS594-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS594-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCS594-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> 注意
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HCS594-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS594-Q1 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 詳細な設計手順

1. V_{CC} と GND の間にデカップリング・コンデンサを追加します。このコンデンサは物理的にデバイスの近く、かつ V_{CC} ピンと GND ピンの両方に電気的に近づけて配置する必要があります。レイアウト例を「レイアウト」セクションに示します。
2. 出力の容量性負荷が 50pF 以下であることを確認します。これは厳密な制限ではありませんが、設計上、性能が最適化されます。これは、SN74HCS594-Q1 から 1 つまたは複数の受信デバイスまでの短い適切なサイズのトレースを提供することで実現できます。
3. 出力の抵抗性負荷が $(V_{CC} / I_{O(max)})$ Ω より大きいことを確認します。これを行うと、「絶対最大定格」の最大出力電流に違反するのを防ぐことができます。ほとんどの CMOS 入力には、MΩ で測定される抵抗性負荷があります。これは、前に計算した最小値よりもはるかに大きくなります。
4. 熱の問題がロジック・ゲートにとって問題となることはほとんどありません。ただし、消費電力と熱の上昇は、アプリケーション・レポート『CMOS 消費電力と CPD の計算』に記載されている手順を使用して計算できます。

9.2.3 Application Curves

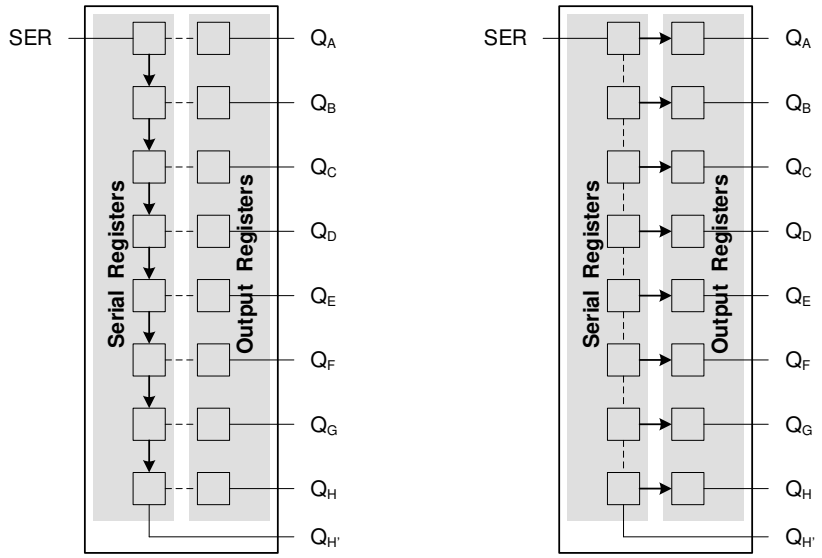


図 9-2. Simplified Functional Diagram Showing Clock Operation

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

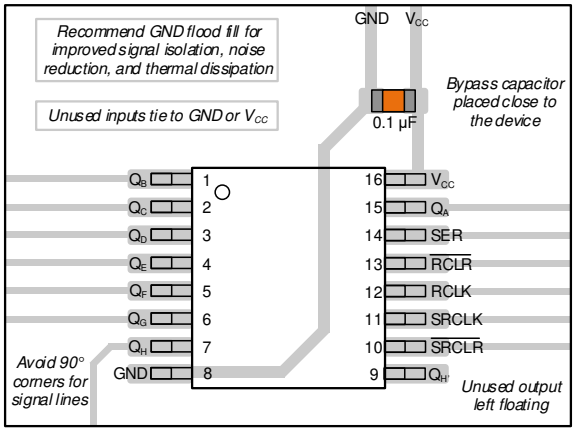


図 11-1. Example Layout for the SN74HCS594-Q1 in the PW Package

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *HCMOS Design Considerations* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS594QBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS594Q
SN74HCS594QWBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q
SN74HCS594QWBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS594Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74HCS594-Q1 :

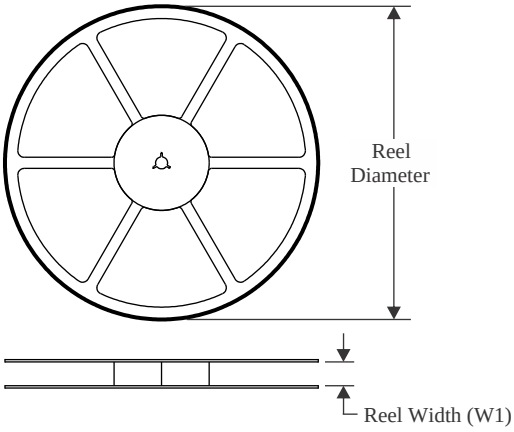
- Catalog : SN74HCS594

NOTE: Qualified Version Definitions:

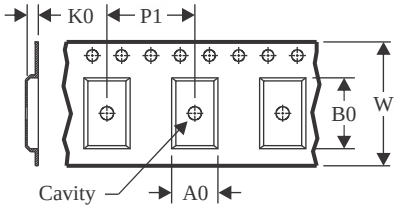
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

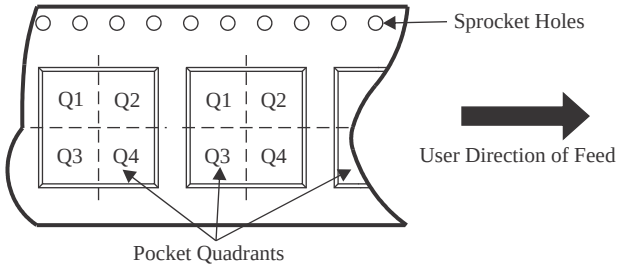


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

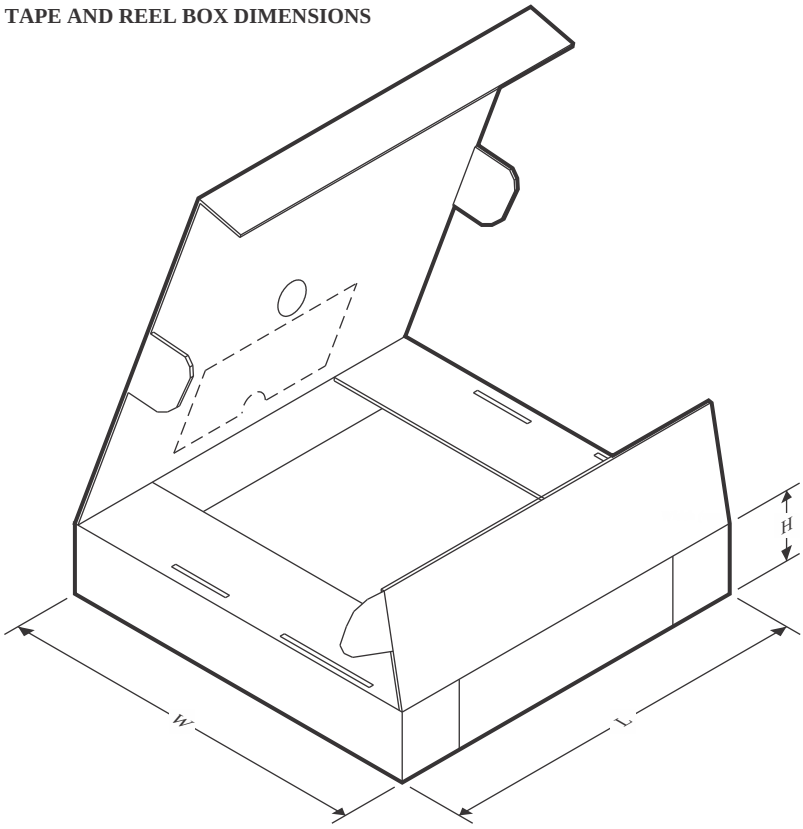
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS594QBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74HCS594QDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS594QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS594QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

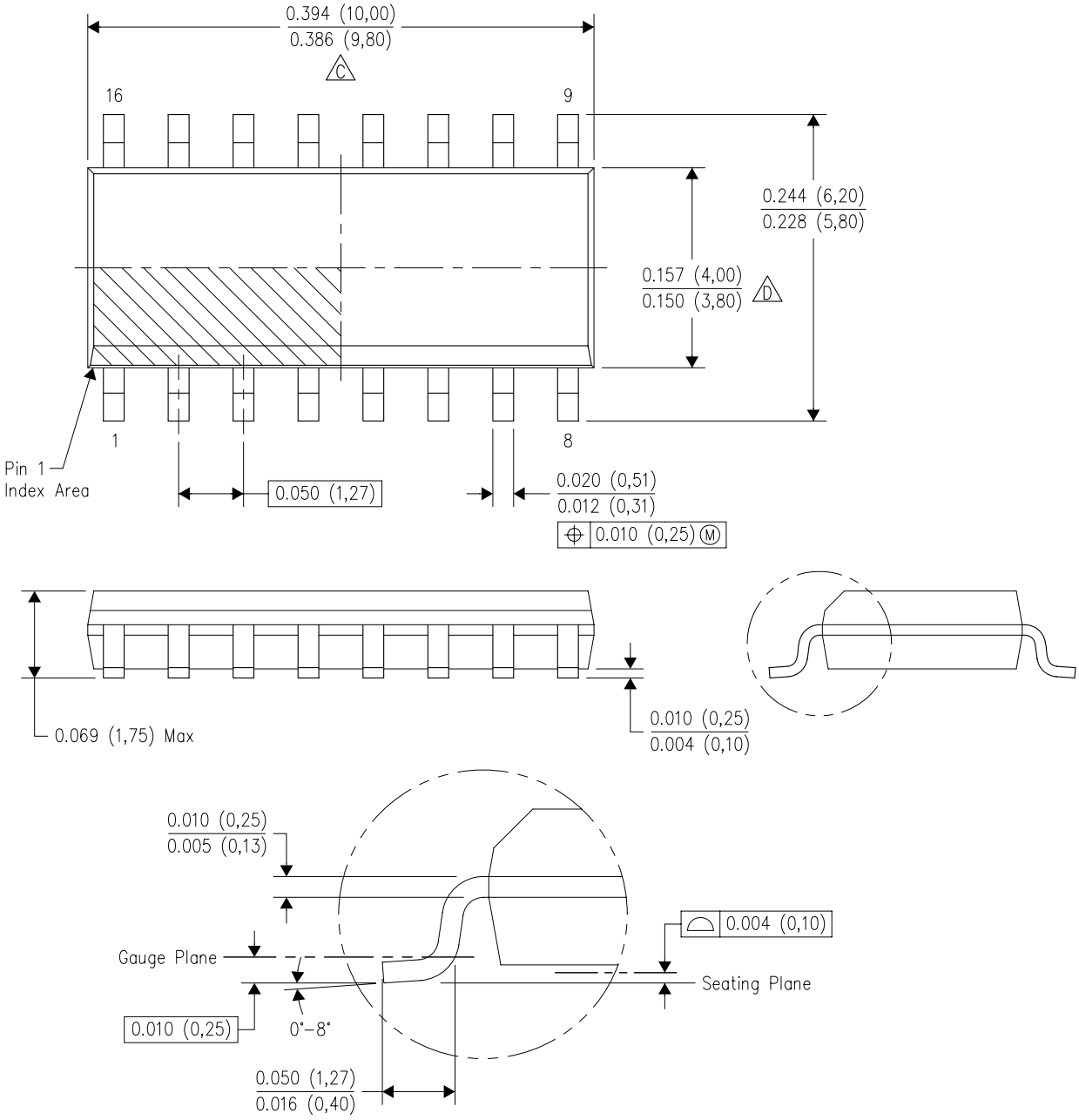
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS594QBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74HCS594QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74HCS594QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HCS594QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

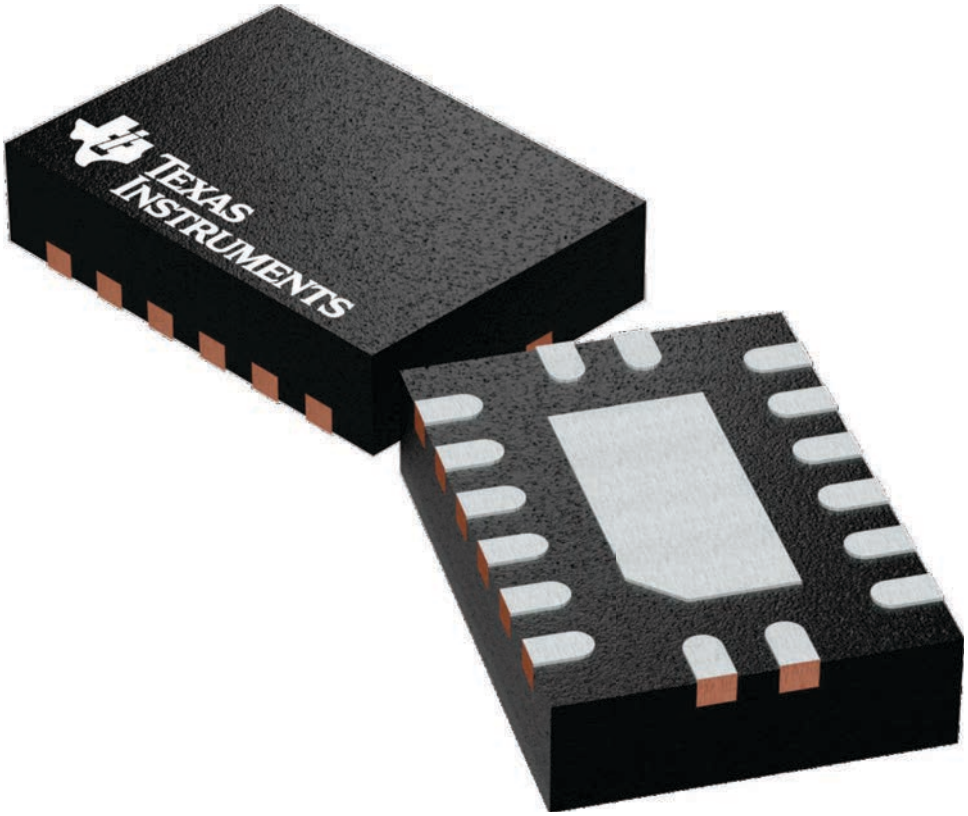
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



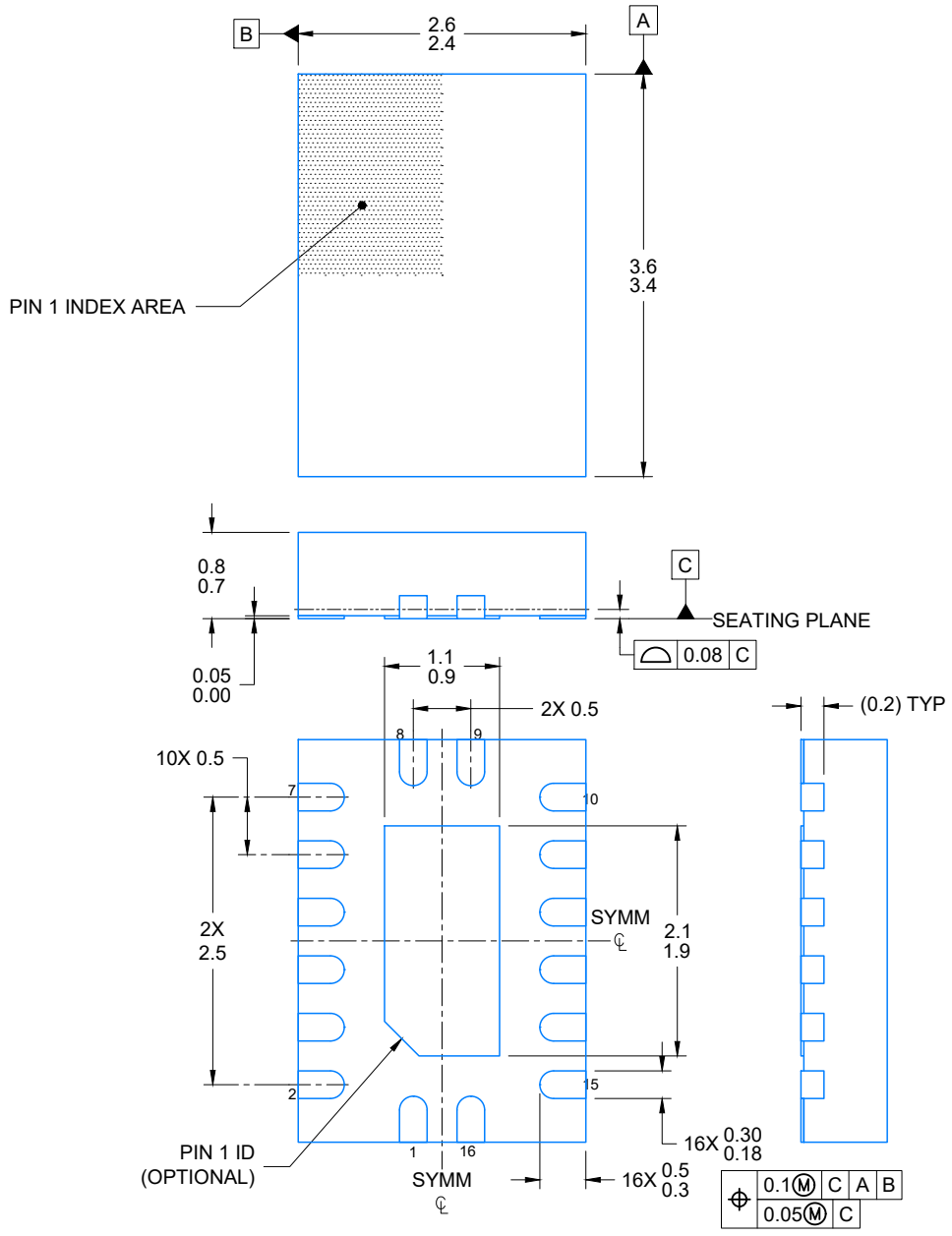
4226161/A

PACKAGE OUTLINE

BQB0016A

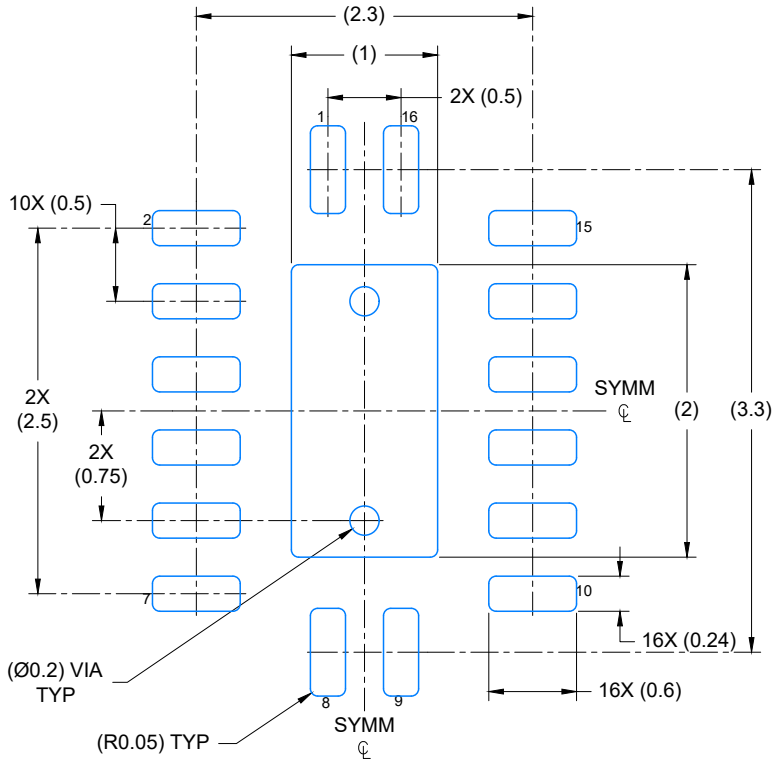
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

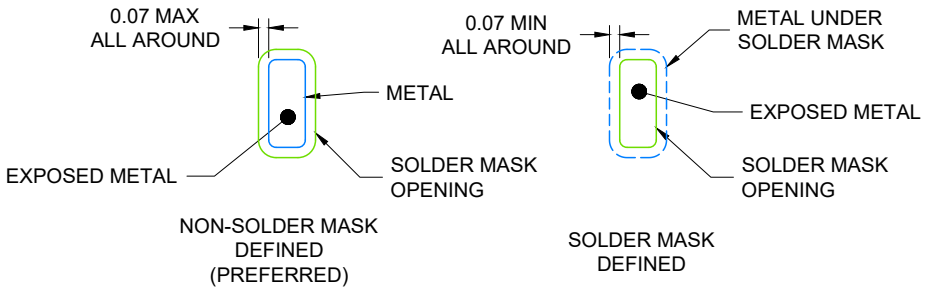


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



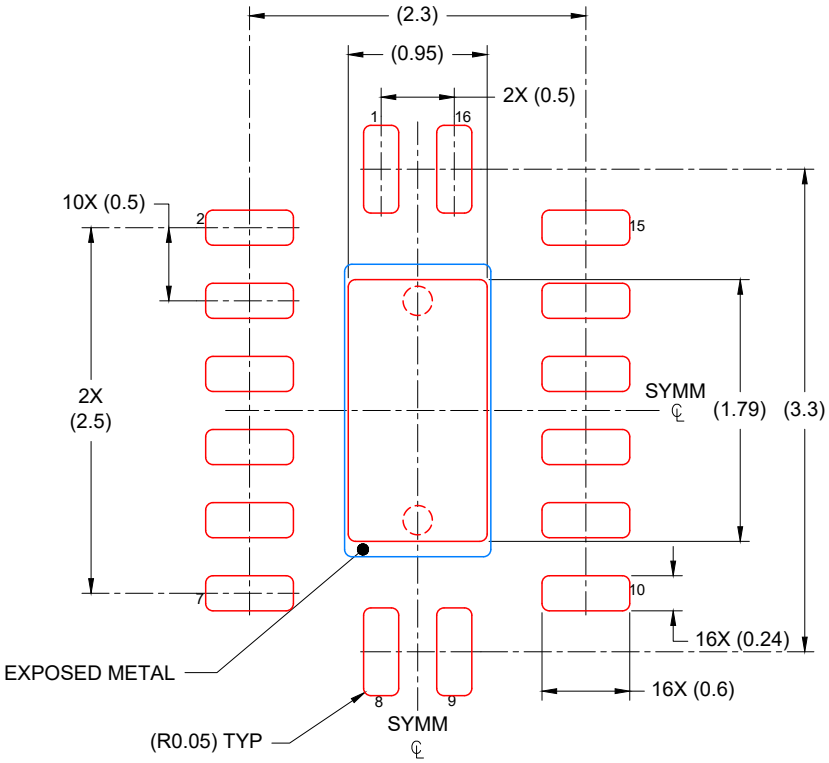
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

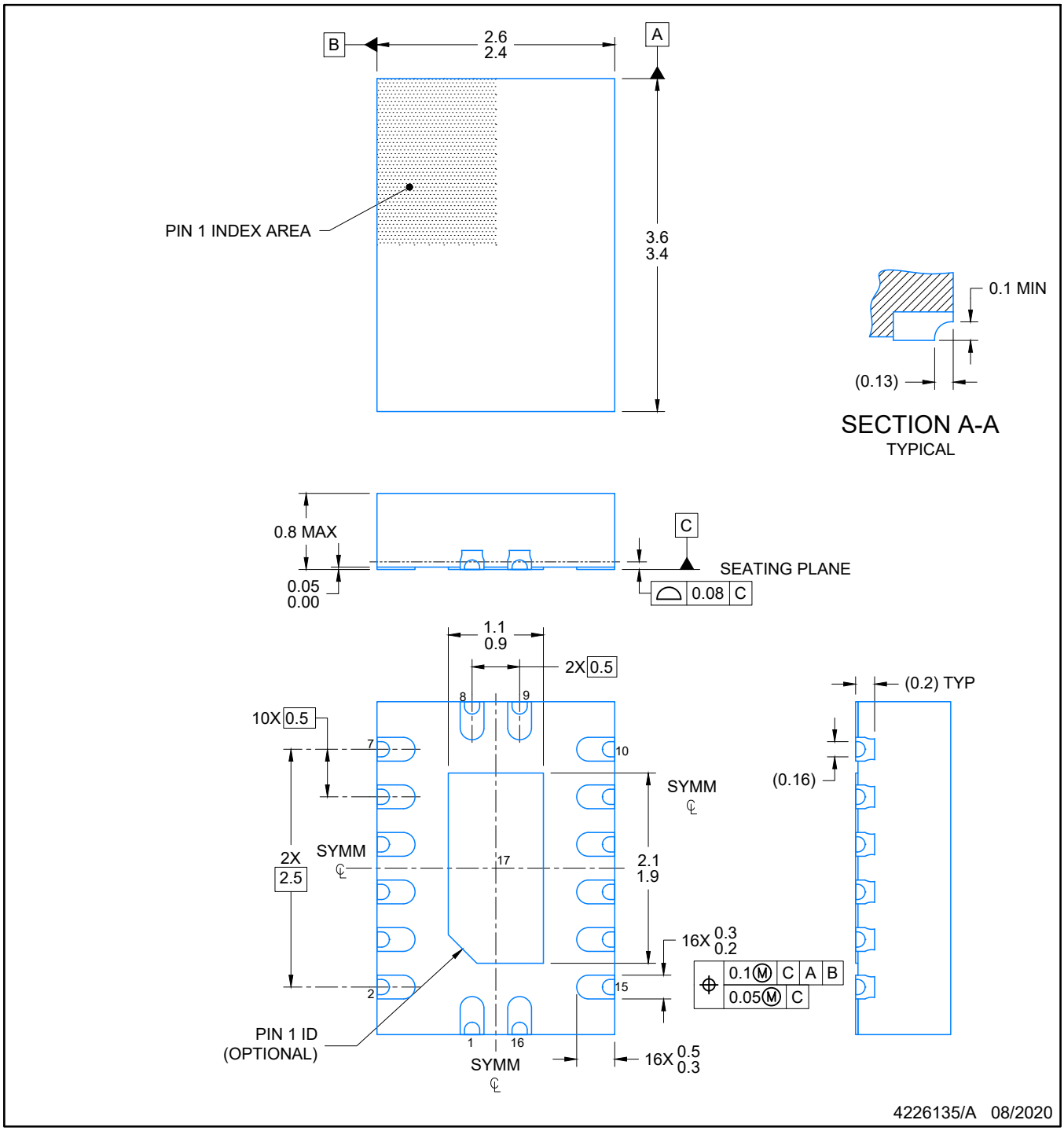
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

BQB0016B

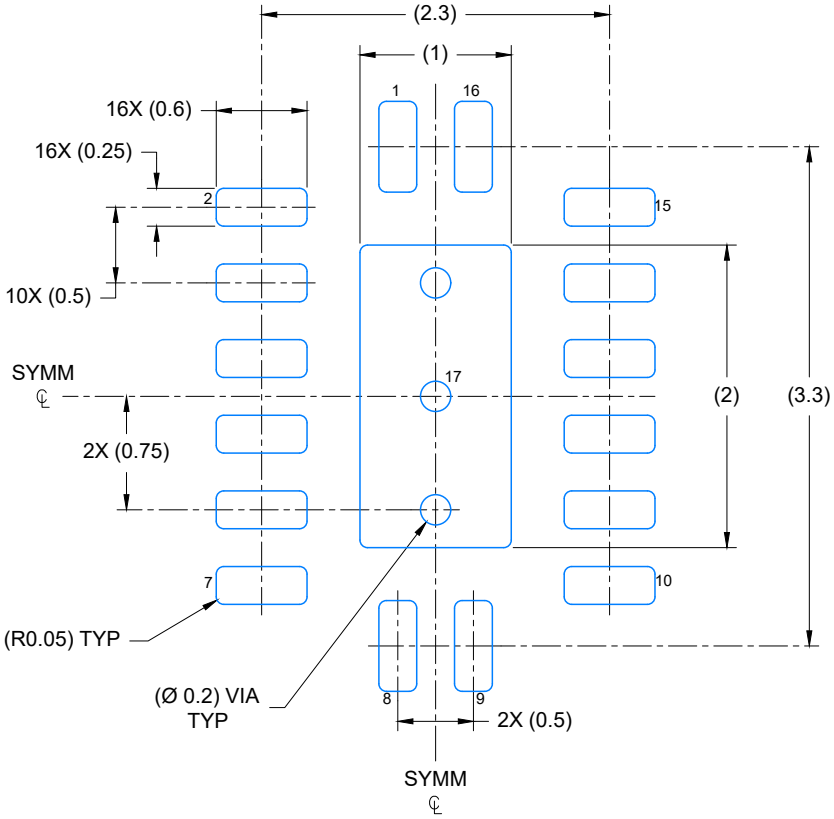
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

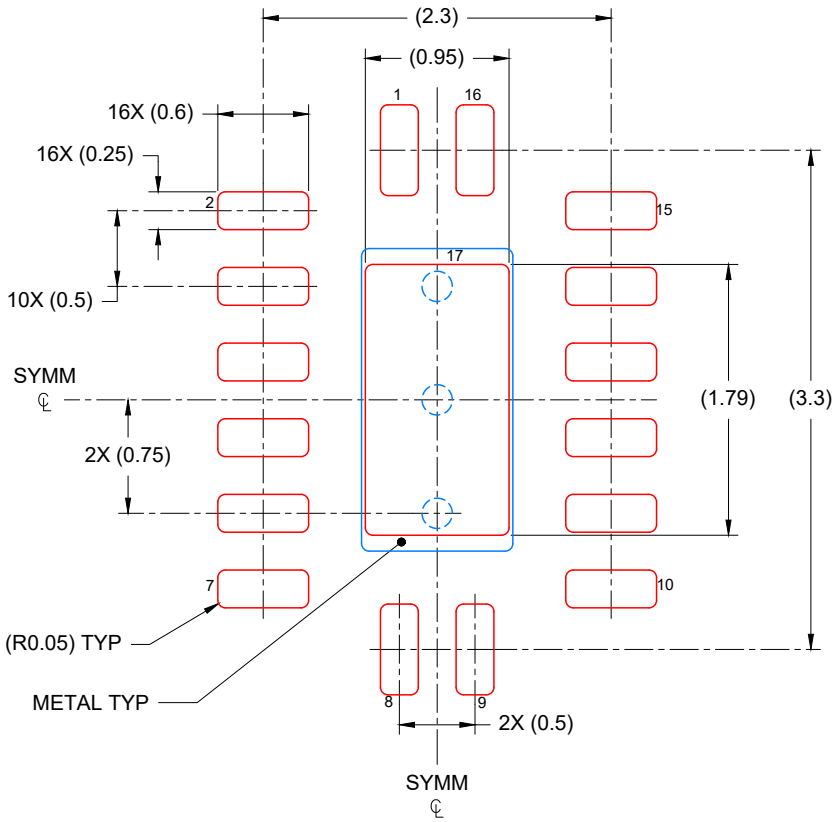


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

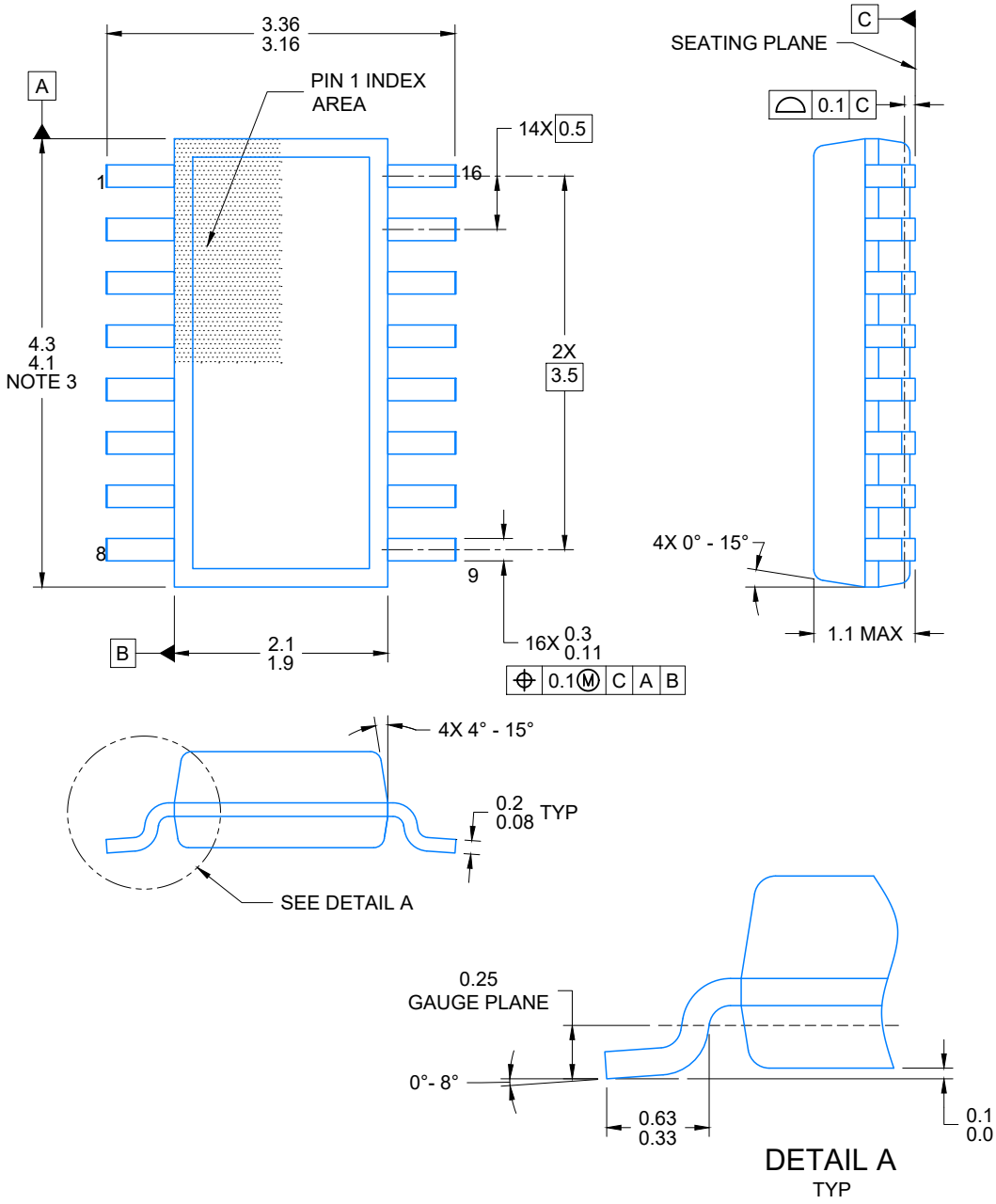
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

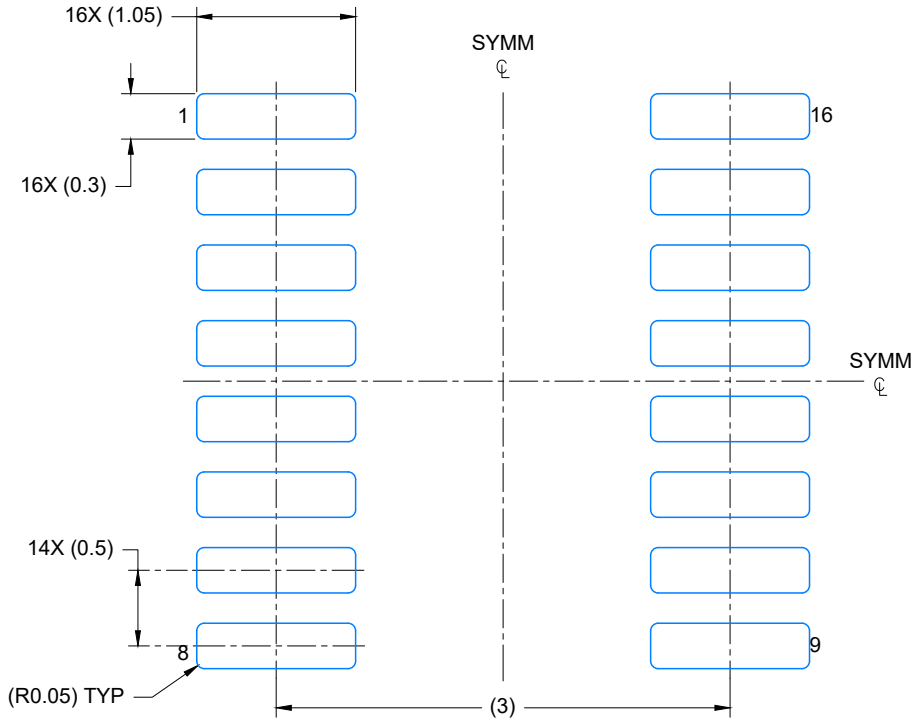
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

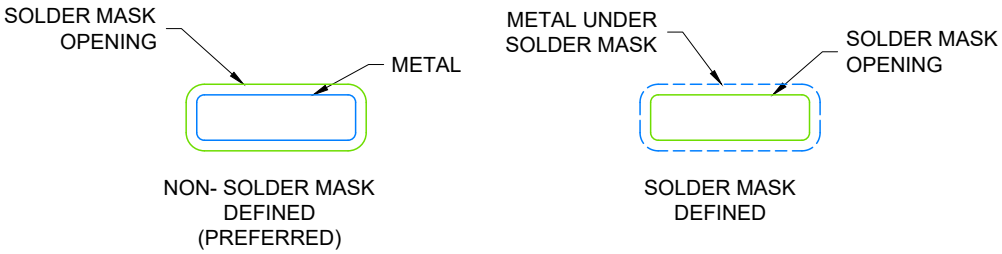


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

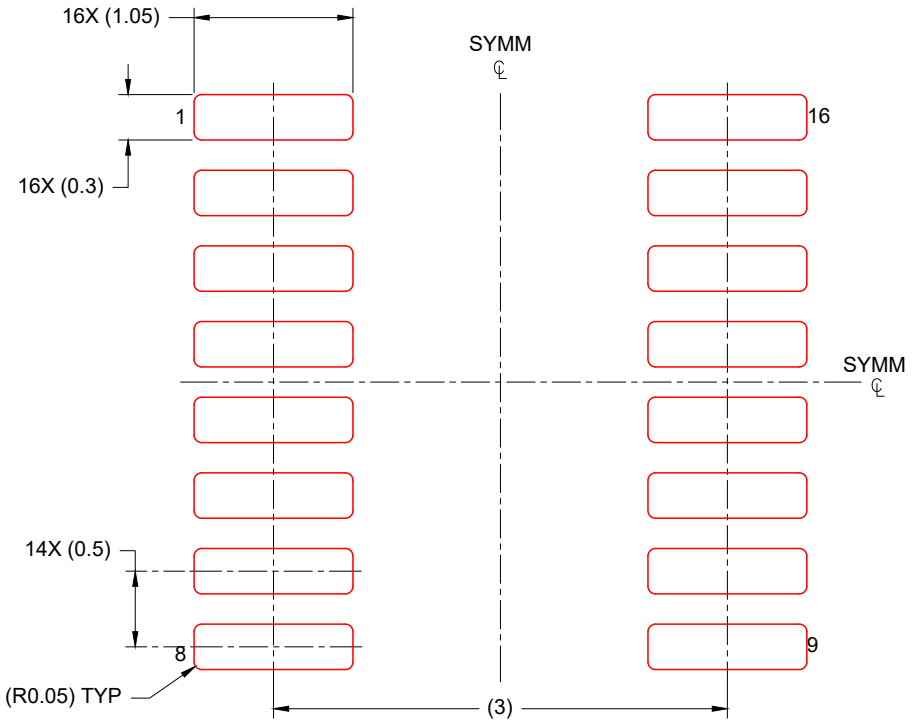
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

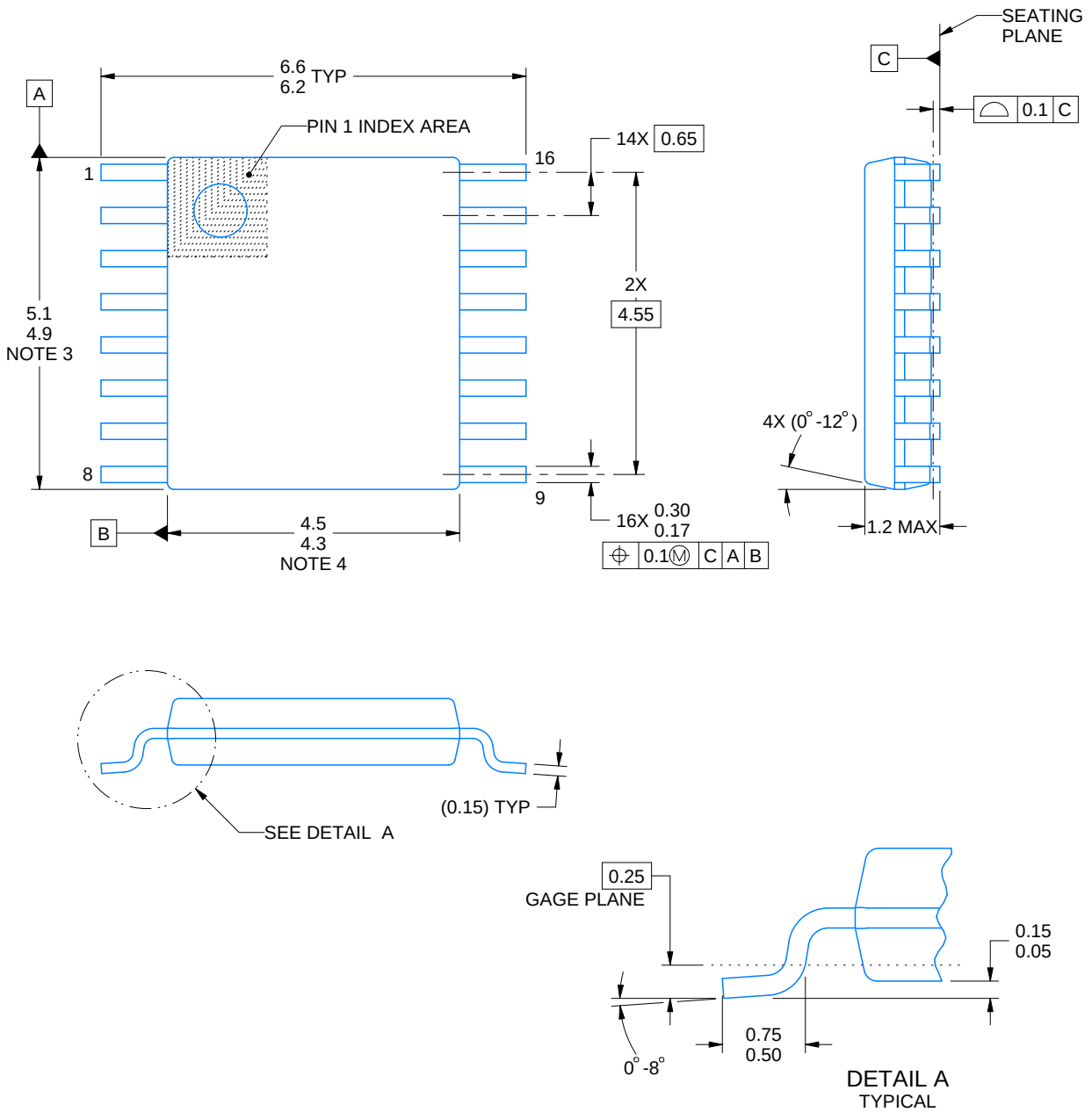
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

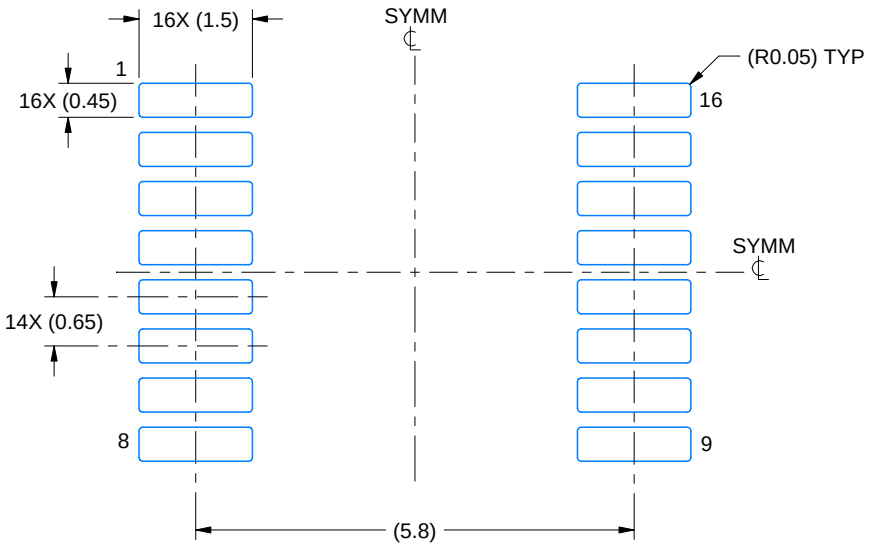
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



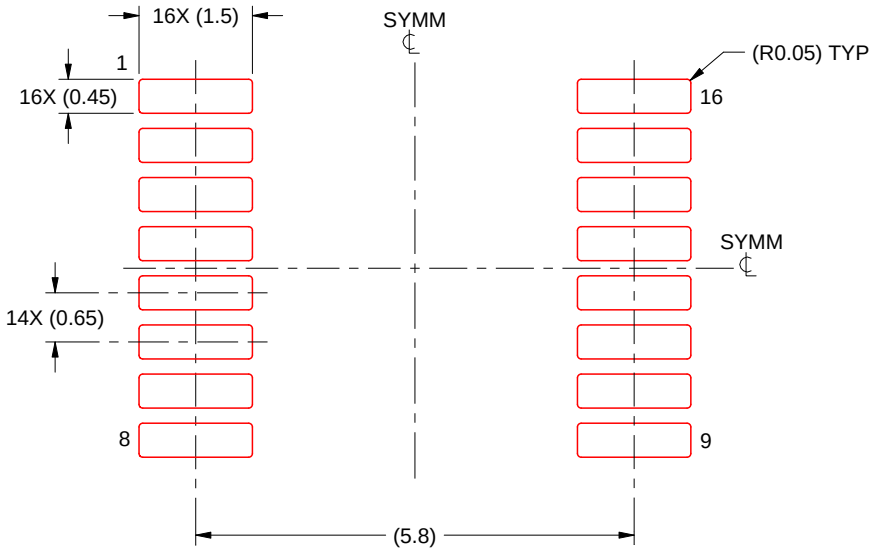
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月