TEXAS INSTRUMENTS
SN74HCS259-Q1
JAJSNK2A – JULY 2020 – REVISED DECEMBER 2021

SN74HCS259-Q1 車載用 8 ビット・アドレス指定可能ラッチ、シュミット・トリガ入力付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み:
  - デバイス温度グレード 1:
    –40℃～+125℃、T_A
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- ウェッタブル・フランク QFN (または WBQB) パッケージで供給
- 広い動作電圧範囲:2V～6V
- シュミット・トリガ入力により低速の信号またはノイズの多い信号に対応
- 低い消費電力
  - I_{CC}:100nA (標準値)
  - 入力リーク電流:±100nA (標準値)
- 6V で ±7.8mA の出力駆動能力

2 アプリケーション

- データ・バスを共有するメモリ・デバイスの選択
- チップ・セレクト・アプリケーションの出力の必要数の低減
- データの転送

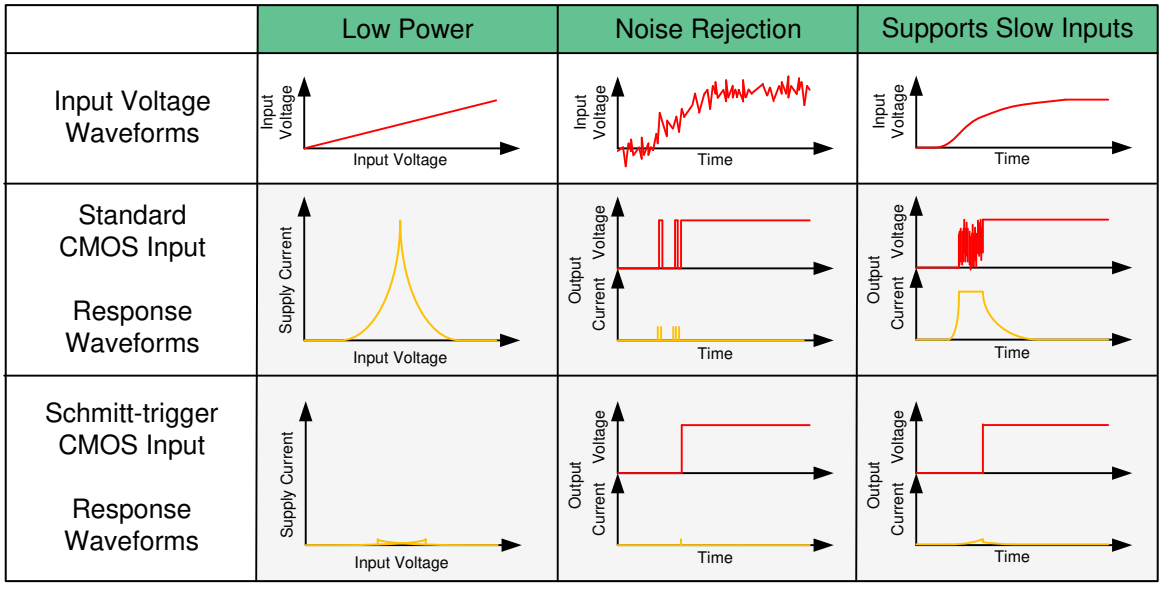
3 概要

SN74HCS259-Q1 8 ビット・アドレス指定可能ラッチは、デジタル・システムの汎用ストレージ・アプリケーション用に設計されています。具体的な用途としては、ワーキング・レジスタ、シリアル保持レジスタ、およびアクティブ・ハイのデコーダまたはデマルチプレクサがあります。これらは、シングル・ラインのデータを 8 つのアドレス指定可能ラッチに格納し、アクティブ・ハイ出力付きの 1 : 8 デコーダまたはデマルチプレクサになることができる、多機能デバイスです。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN74HCS259PW-Q1	TSSOP (16)	5.00mm × 4.40mm
SN74HCS259D-Q1	SOIC (16)	9.90mm × 3.90mm
SN74HCS259WBQB-Q1	WQFN (16)	3.60mm × 2.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



シュミット・トリガ入力の利点

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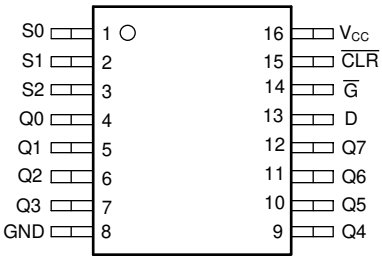
4 Revision History

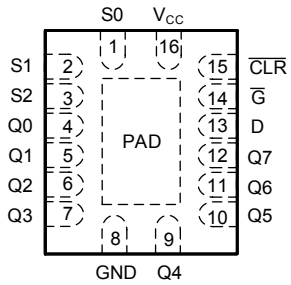
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2020) to Revision A (December 2021)	Page
• 「製品情報」に WBQB パッケージの情報を追加	1
• Added WBQB package to *Pin Configuration and Functions*	3
• Added WBQB package to Thermal Information table	4
• Added wettable flanks to *Feature Description*	10

5 Pin Configuration and Functions



D or PW Package
16-Pin SOIC or TSSOP
Top View



WBQB Package
16-Pin WQFN
Top View

Pin Functions

PIN		I/O[2]	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	S0	I	Address select 0
2	S1	I	Address select 1
3	S2	I	Address select 2
4	Q0	O	Output 0
5	Q1	O	Output 1
6	Q2	O	Output 2
7	Q3	O	Output 3
8	GND	—	Ground
9	Q4	O	Output 4
10	Q5	O	Output 5
11	Q6	O	Output 6
12	Q7	O	Output 7
13	D	I	Data input
14	$\overline{G}$	I	Enable, active low
15	$\overline{CLR}$	O	Clear input, active low
16	V_{CC}	—	Positive supply
Thermal Pad [1]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) WBQB package only.
(2) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74HCS259-Q1			UNIT
		PW (TSSOP)	D (SOIC)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	97.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	80.9	93.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	80.6	66.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	40.4	14.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	80.3	66.4	°C/W

THERMAL METRIC(1)		SN74HCS259-Q1			UNIT
		PW (TSSOP)	D (SOIC)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})(1)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF

(1) Guaranteed by design.

6.6 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER			V_{CC}	Operating free-air temperature (T_A)				UNIT
				25°C		–40°C to 125°C		
				MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		
		$\overline{G}$ low	2 V	5		5		
			4.5 V	5		5		
			6 V	5		5		
t_{su}	Setup time	Data or address before $\overline{G}$ ↑	2 V	5		8		ns
			4.5 V	3		4		
			6 V	3		4		
t_h	Hold time	Data or address after $\overline{G}$ ↑	2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		

6.7 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	Data	Any Q	2 V		17	32			48	ns
				4.5 V		7	12			18	
				6 V		6	11			15	
		Address	Any Q	2 V		16	34			52	
				4.5 V		7	12			20	
				6 V		6	11			18	
		$\overline{G}$	Any Q	2 V		17	38			55	
				4.5 V		7	16			24	
				6 V		6	15			21	
t_{PHL}	Propagation delay	$\overline{CLR}$	Any Q	2 V		14	34			51	ns
				4.5 V		7	12			20	
				6 V		6	11			16	
t_t	Transition-time		Any output	2 V			9			17	ns
				4.5 V			5			8	
				6 V			4			7	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		10		pF

6.9 Typical Characteristics

T_A = 25°C

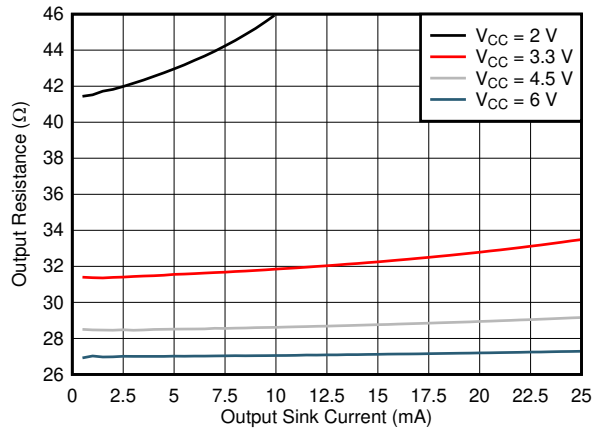


図 6-1. Output Driver Resistance in LOW State

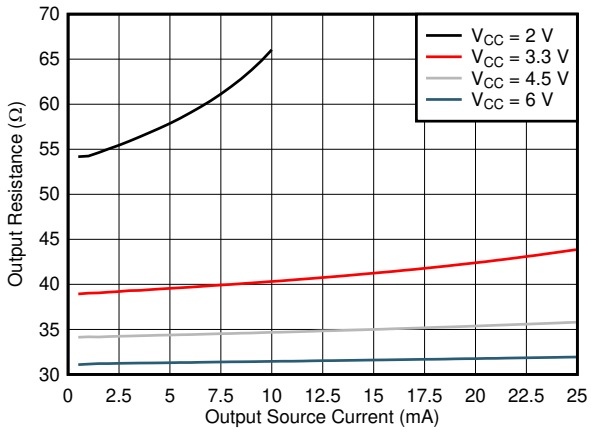


図 6-2. Output Driver Resistance in HIGH State

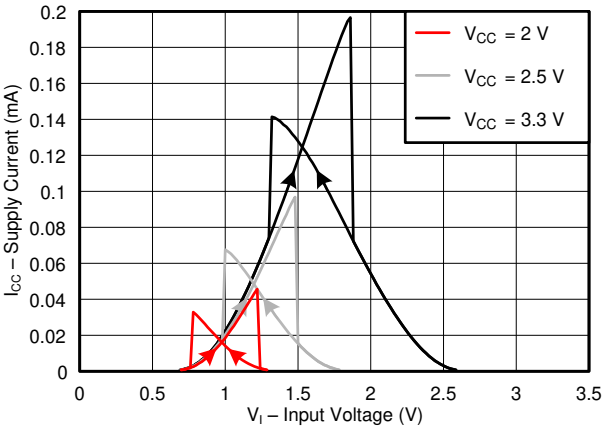


図 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

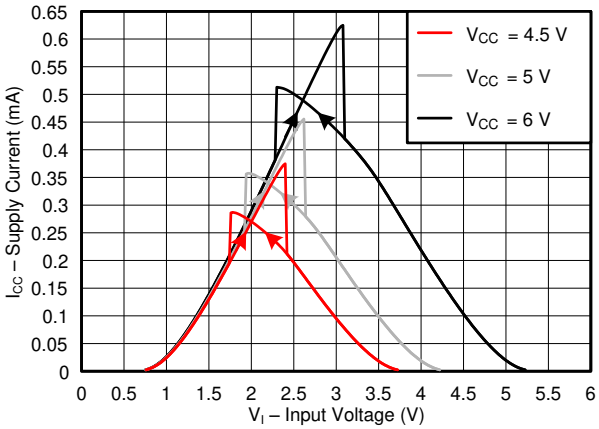


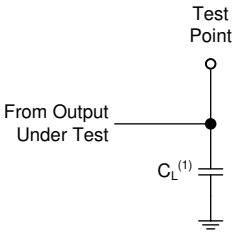
図 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 7-1. Load Circuit

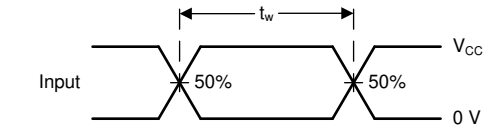


図 7-2. Voltage Waveforms, Pulse Duration

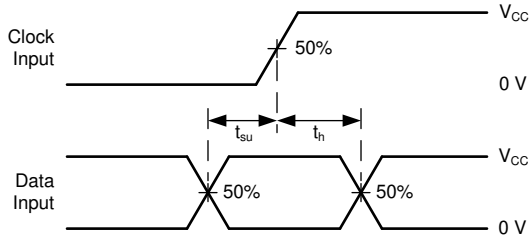
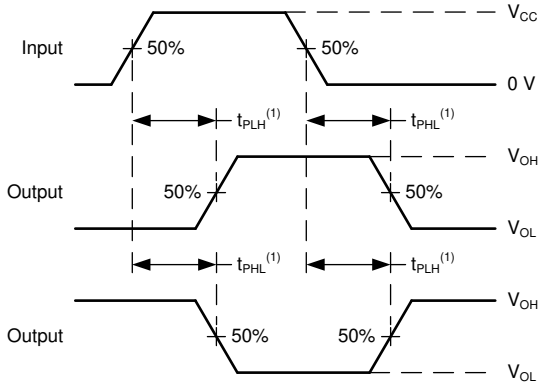
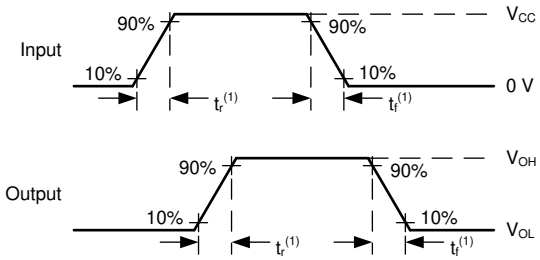


図 7-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

図 7-5. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

The SN74HCS259-Q1 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs:

- Addressable-latch mode: $\overline{CLR}$ = HIGH; $\overline{G}$ = LOW
  - Data at the data-in terminal is written into the addressed latch
  - The addressed latch follows the data input, with all unaddressed latches remaining in their previous states
- Memory mode: $\overline{CLR}$ = HIGH; $\overline{G}$ = HIGH
  - All latches remain in their previous states and are unaffected by the data or address inputs
  - To eliminate the possibility of entering erroneous data in the latches, $\overline{G}$ should be held high (inactive) while the address lines are changing
- 1-of-8 decoding or demultiplexing mode: $\overline{CLR}$ = LOW; $\overline{G}$ = LOW
  - The addressed output follows the level of the D input with all other outputs low
- Clear mode: $\overline{CLR}$ = LOW; $\overline{G}$ = HIGH
  - All outputs are low and unaffected by the address and data inputs

8.2 Functional Block Diagram

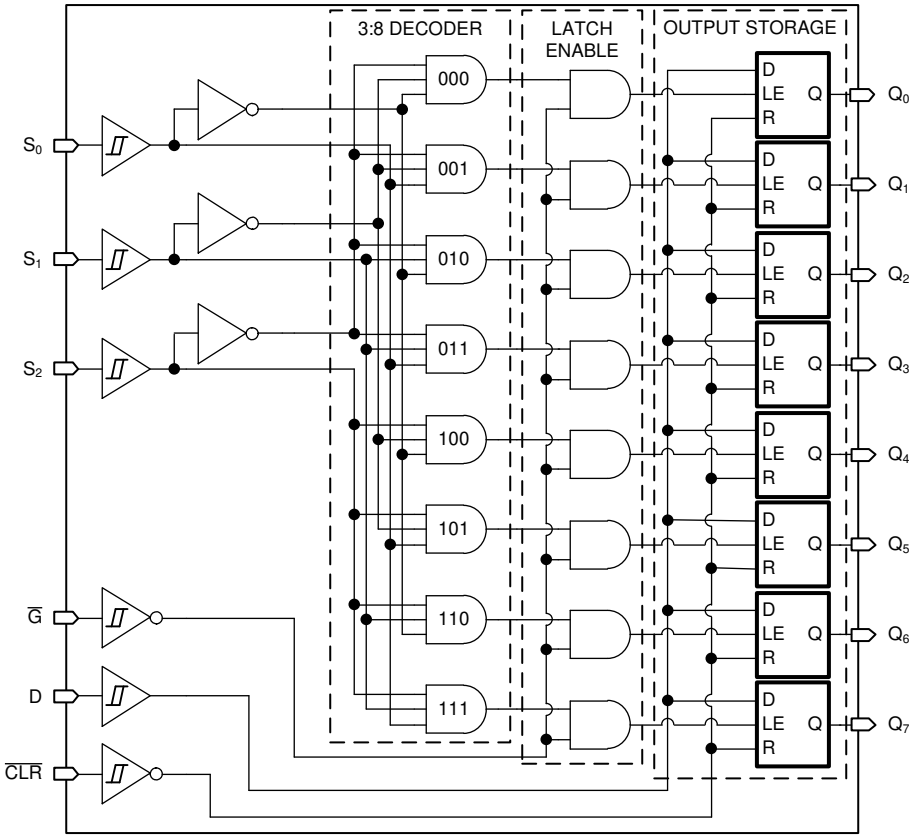


図 8-1. Logic Diagram (Positive Logic) for SN74HCS259-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

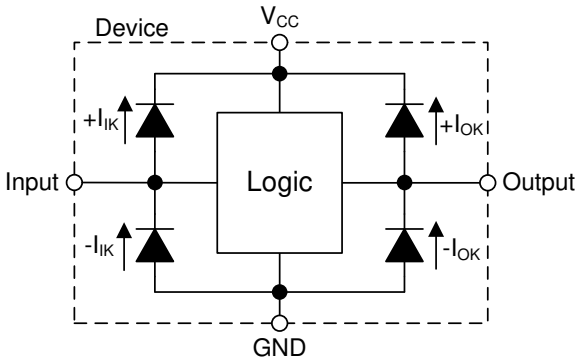


図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

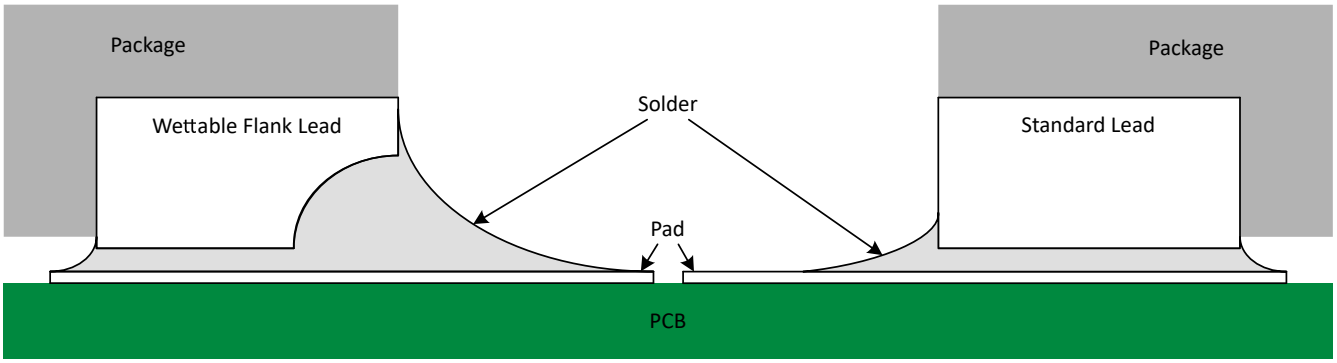


図 8-3. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in 図 8-3. Please see the mechanical drawing for additional details.

8.4 Device Functional Modes

The Function Tableand Latch Selection Table below list the functional modes of the SN74HCS259-Q1.

表 8-1. Function Table

INPUTS(1)		OUTPUT OF ADDRESSED LATCH(2)	EACH OTHER OUTPUT(2)	FUNCTION
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{iO}	Addressable latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

(1) H = High voltage level, L = Low voltage level
(2) Q_{iO} = Previous output state of selected latch, D = Data input logic value

表 8-2. Latch Selection Table

SELECT INPUTS(1)			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

(1) H = High Voltage Level, L = Low Voltage Level

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74HCS259-Q1 has four modes of operation. In this application, the 8-line demultiplexer mode is used to send data to one of eight possilbe desinations.

At system power-on, latched outputs are in an unknown state. The $\overline{CLR}$ input is held low while the $\overline{G}$ input is held high to clear the latches for operation. At this time, all outputs are in the low state.

An output is selected by setting S2, S1, and S0 as per the *Latch Selection Table*. After selection, the channel is activated by switching $\overline{G}$ to low. The logic value at the D input will appear at the selected output, allowing data transmission only to the selected device.

When the channel communication is complete, the $\overline{G}$ input is set to high to prevent erronous outputs while the address inputs are changed, then switched back to low again to send data to the newly selected device.

9.2 Typical Application

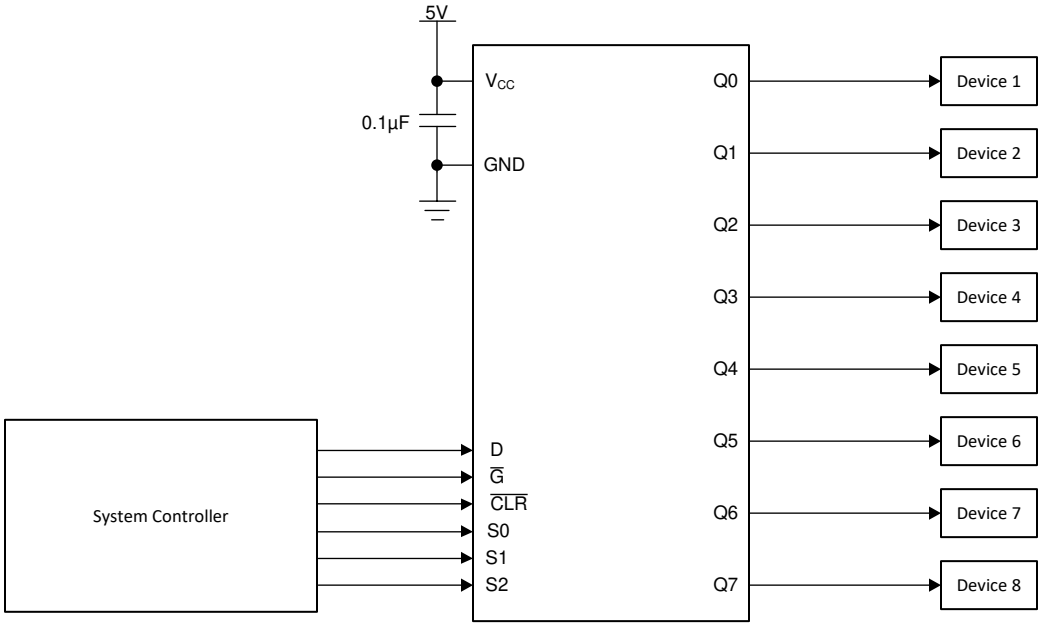


図 9-1. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS259-Q1 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS259-Q1 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS259-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCS259-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS259-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS259-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS259-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

9.2.3 Application Curve

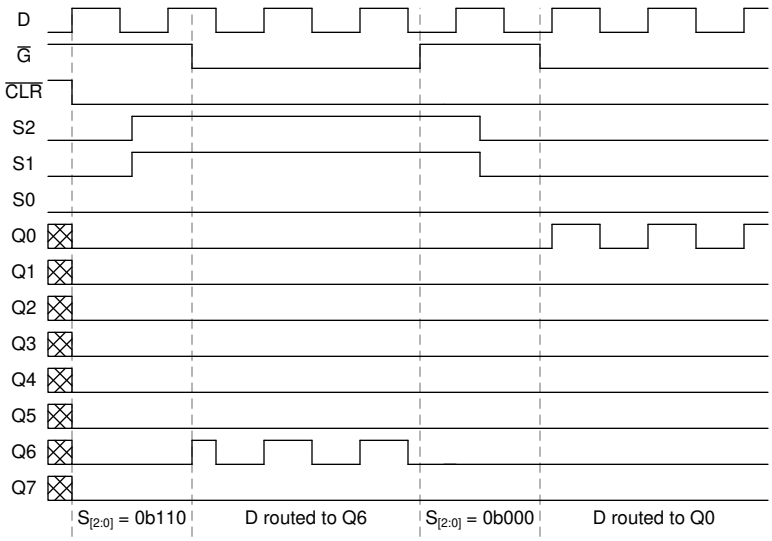


図 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

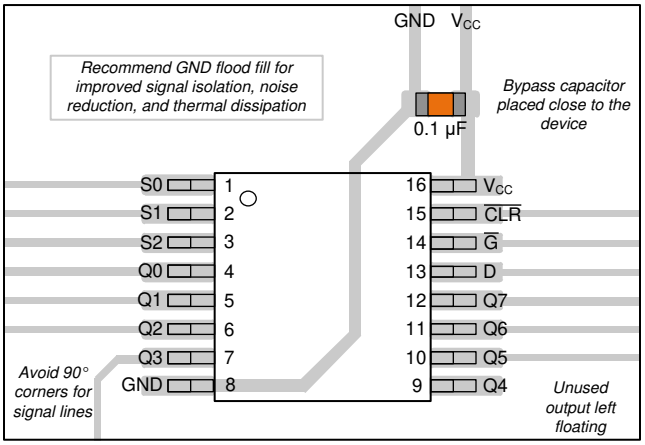


図 11-1. Example layout for the SN74HCS259-Q1 in the PW package.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS259QDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS259Q
SN74HCS259QDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS259Q
SN74HCS259QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS259Q
SN74HCS259QPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS259Q
SN74HCS259QWBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS259Q
SN74HCS259QWBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS259Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74HCS259-Q1 :

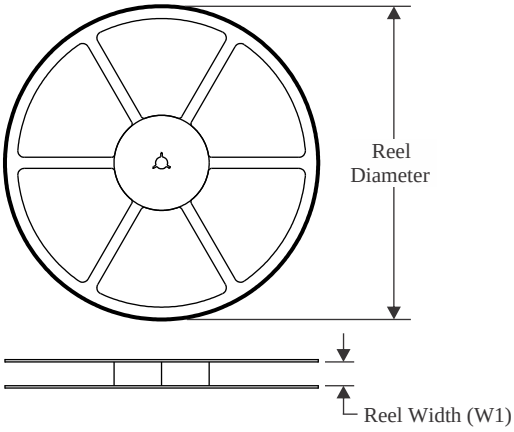
- Catalog : SN74HCS259

NOTE: Qualified Version Definitions:

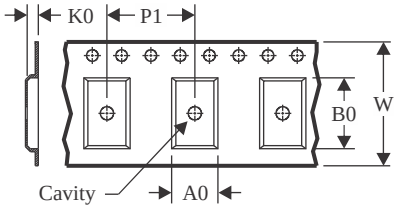
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

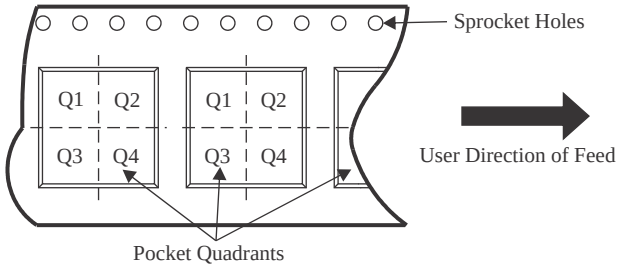


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

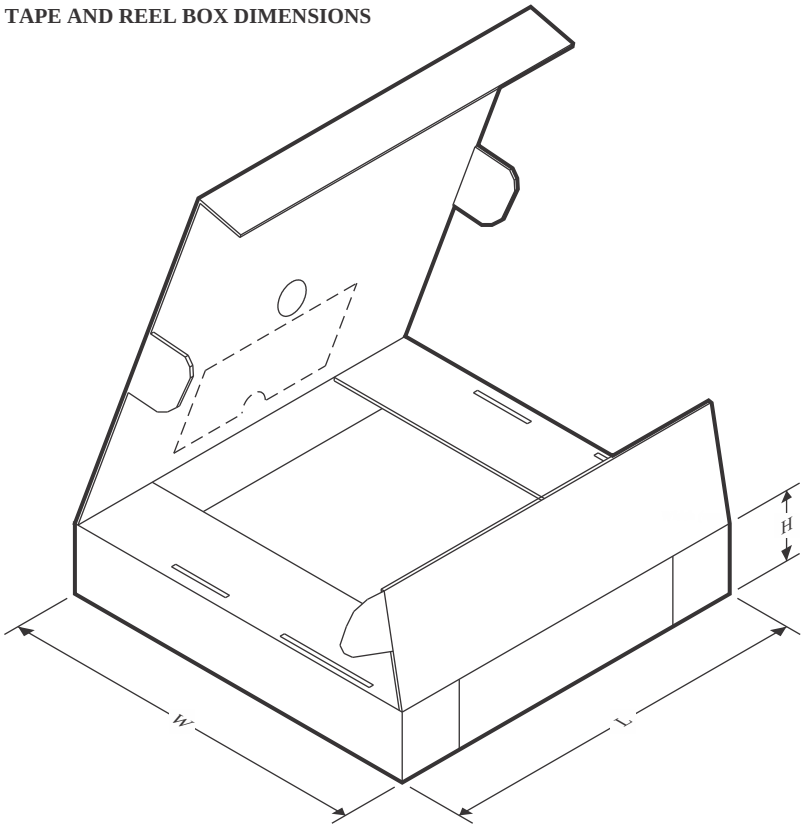
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS259QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS259QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS259QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

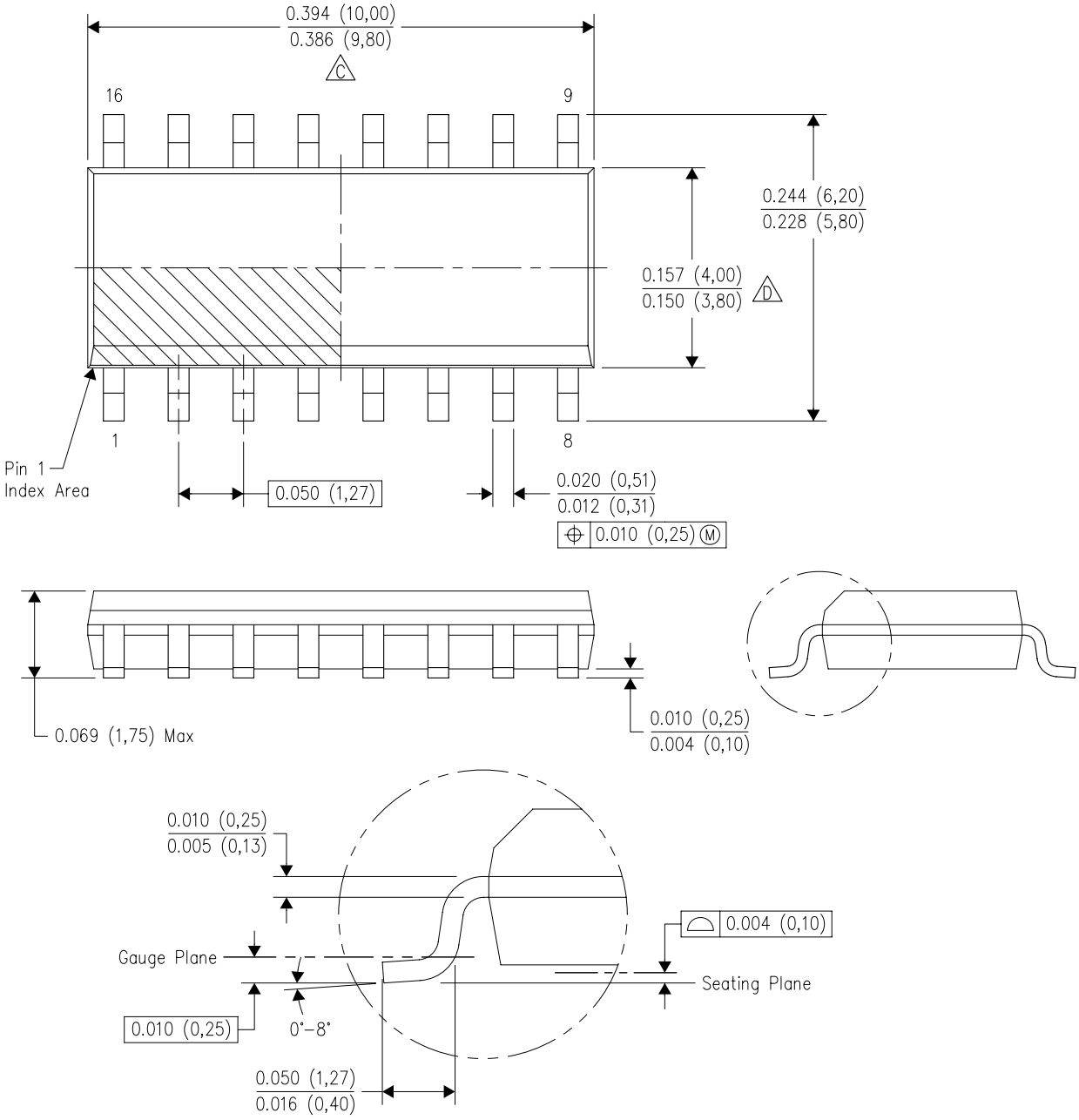
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS259QDRQ1	SOIC	D	16	2500	353.0	353.0	32.0
SN74HCS259QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HCS259QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

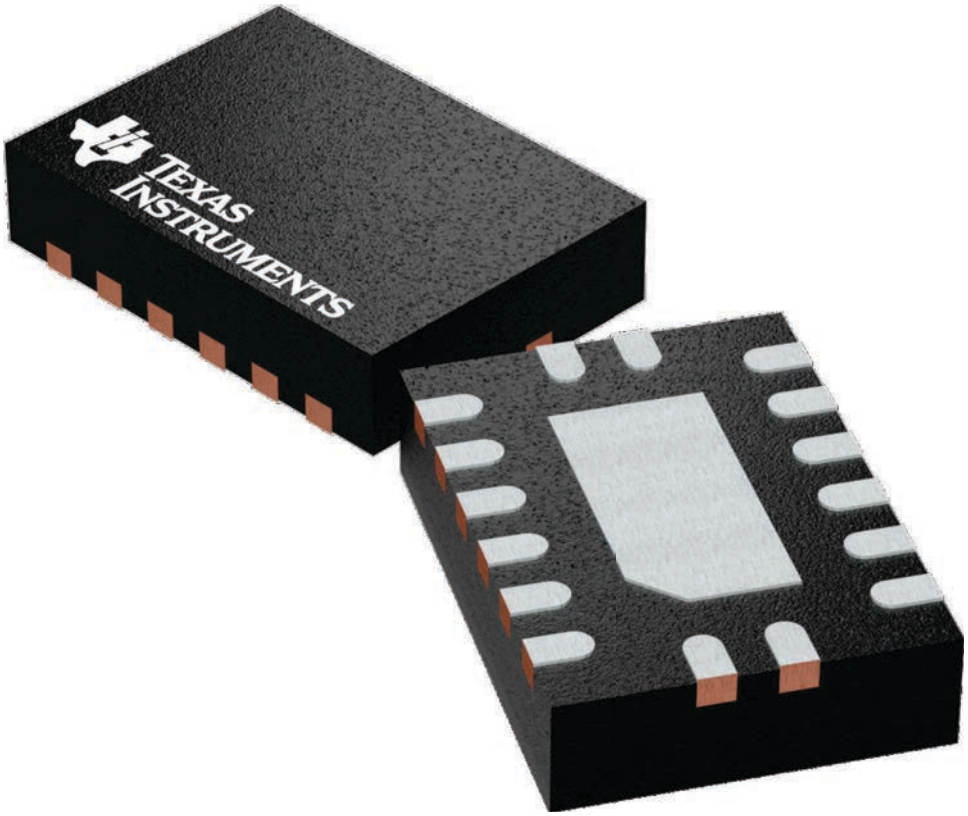
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



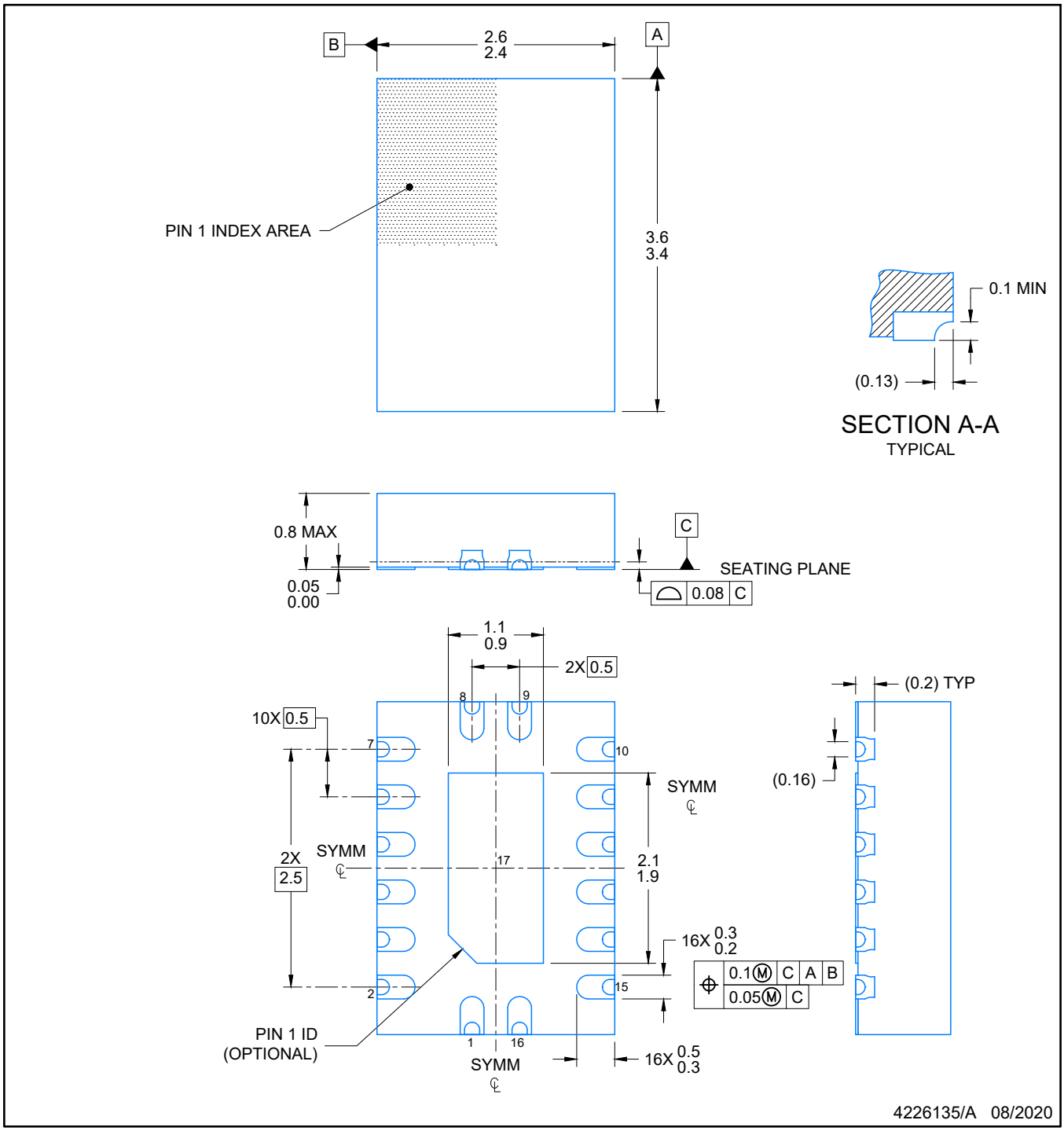
4226161/A

PACKAGE OUTLINE

BQB0016B

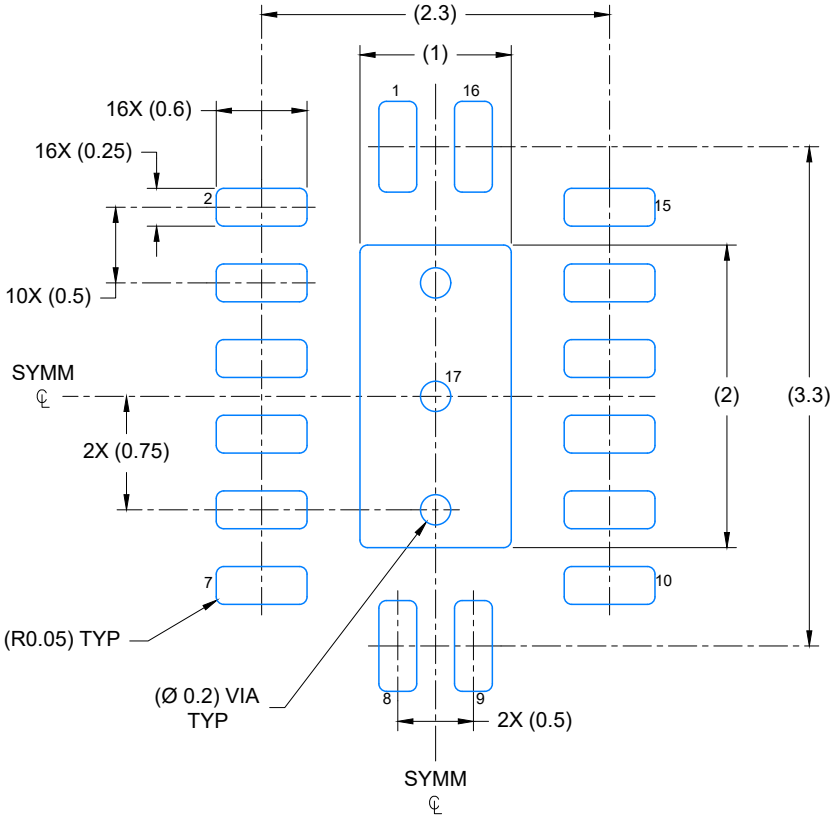
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

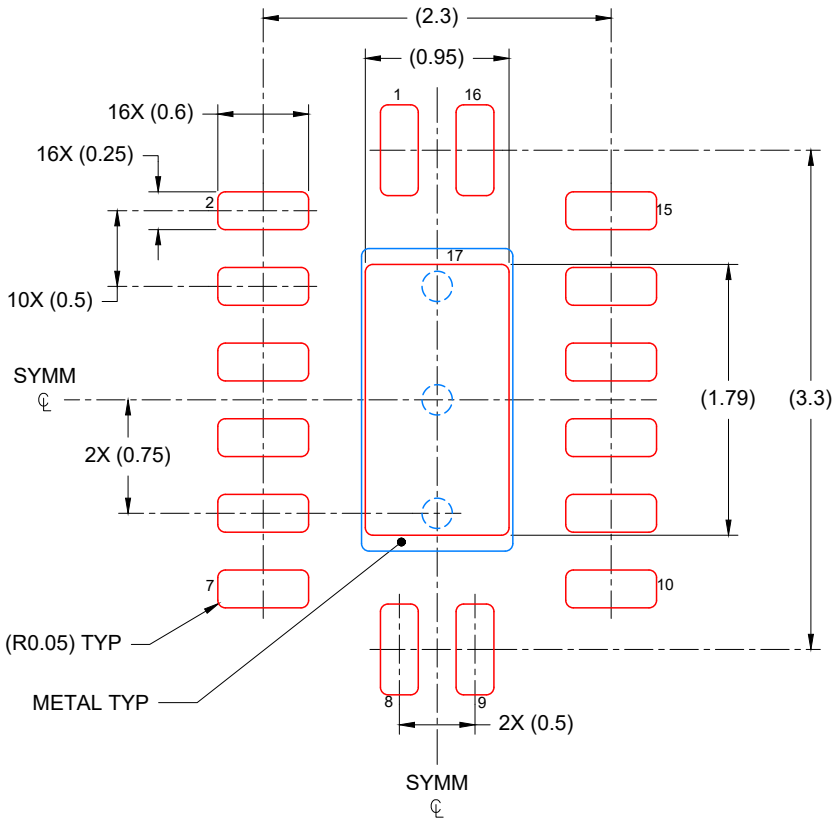


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

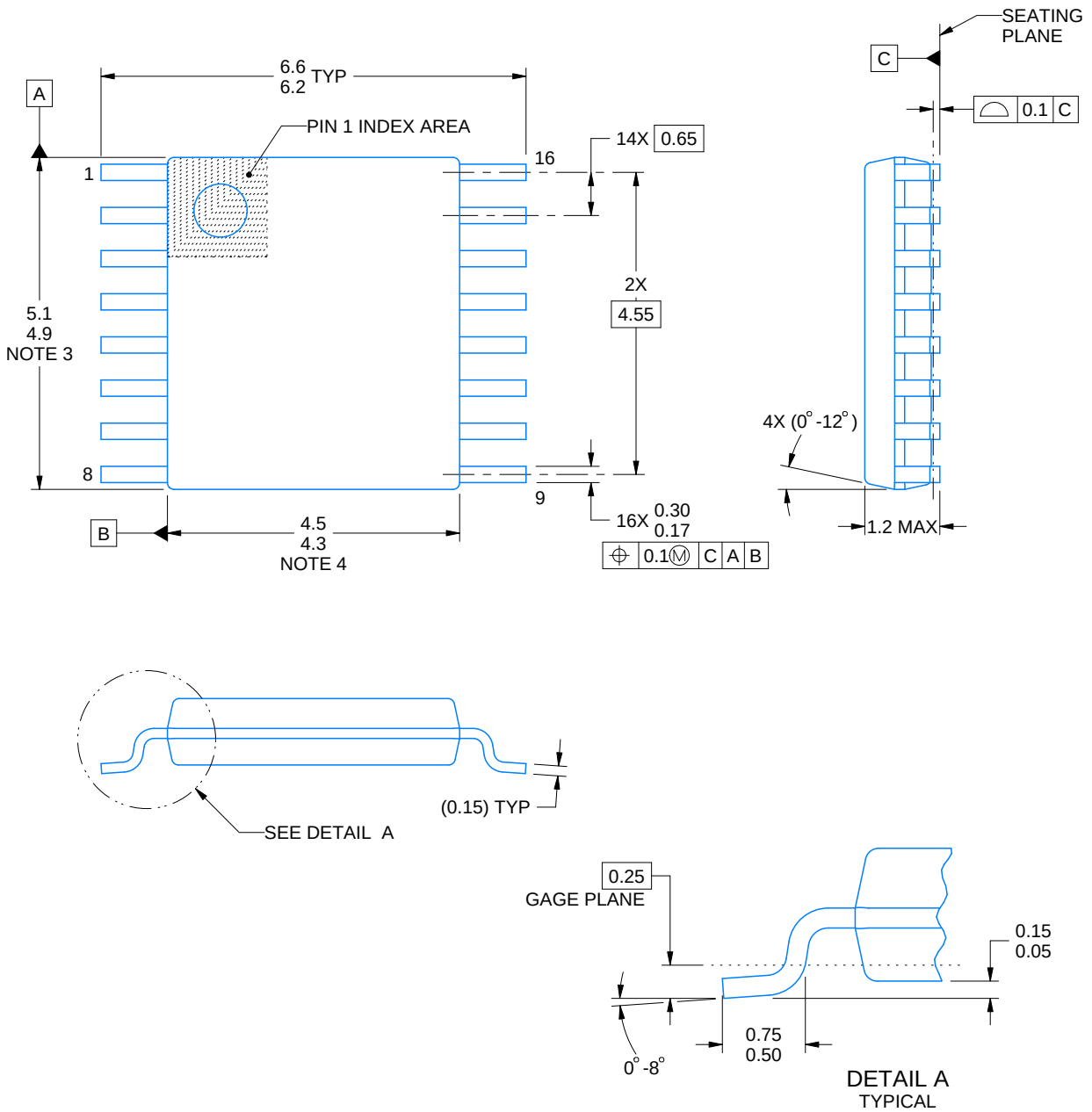
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

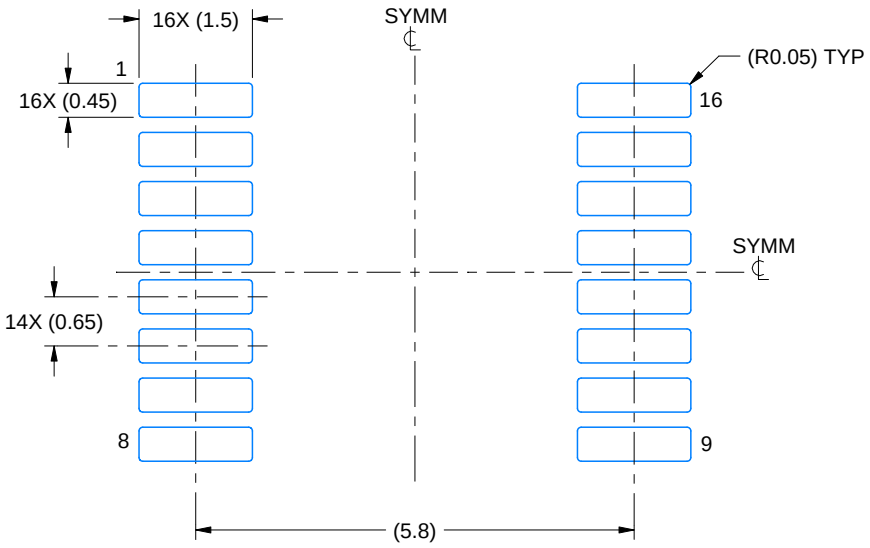
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



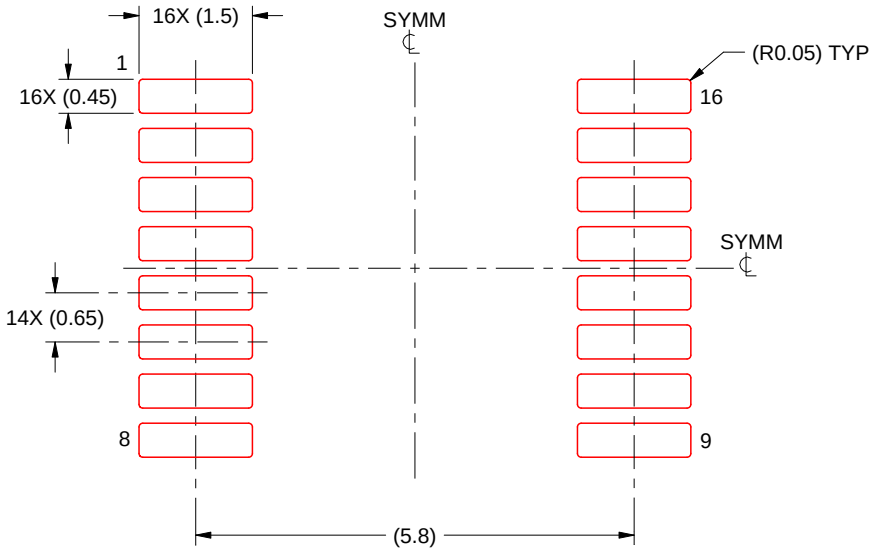
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月