

## 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

Check for Samples: [SN74HC595-EP](#)

### FEATURES

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption: 80- $\mu$ A (Max)  $I_{CC}$
- $t_{pd} = 13$  ns (Typ)
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current: 1  $\mu$ A (Max)
- Shift Register Has Direct Clear

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

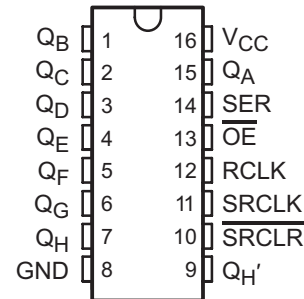
(1) Additional temperature ranges available - contact factory

### DESCRIPTION

The SN74HC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable ( $\overline{OE}$ ) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

PW PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

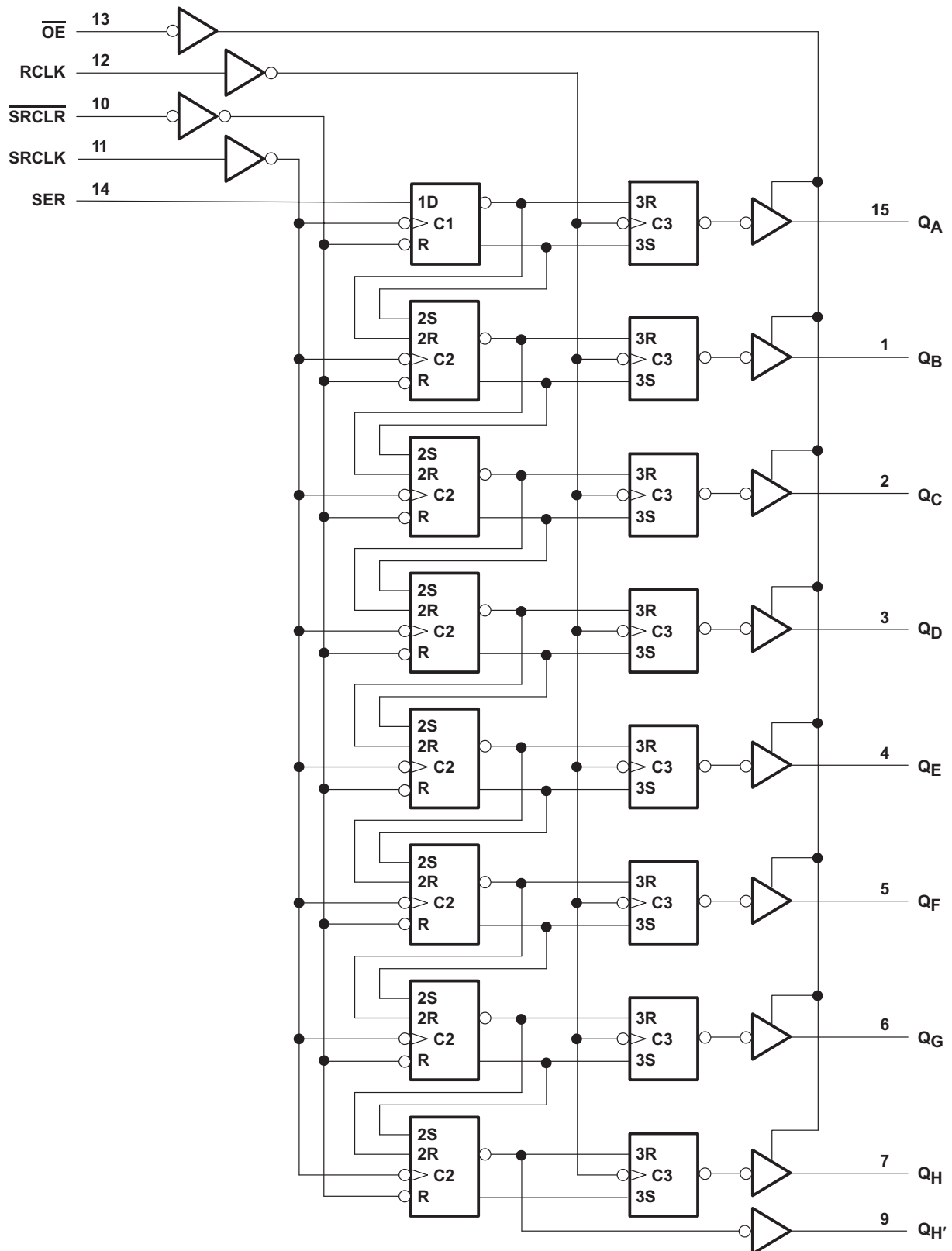
**ORDERING INFORMATION<sup>(1)</sup>**

<b>T<sub>A</sub></b>	<b>PACKAGE<sup>(2)</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
–55°C to 125°C	TSSOP – PW	Reel of 2000	SN74HC595MPWREP	HC595EP

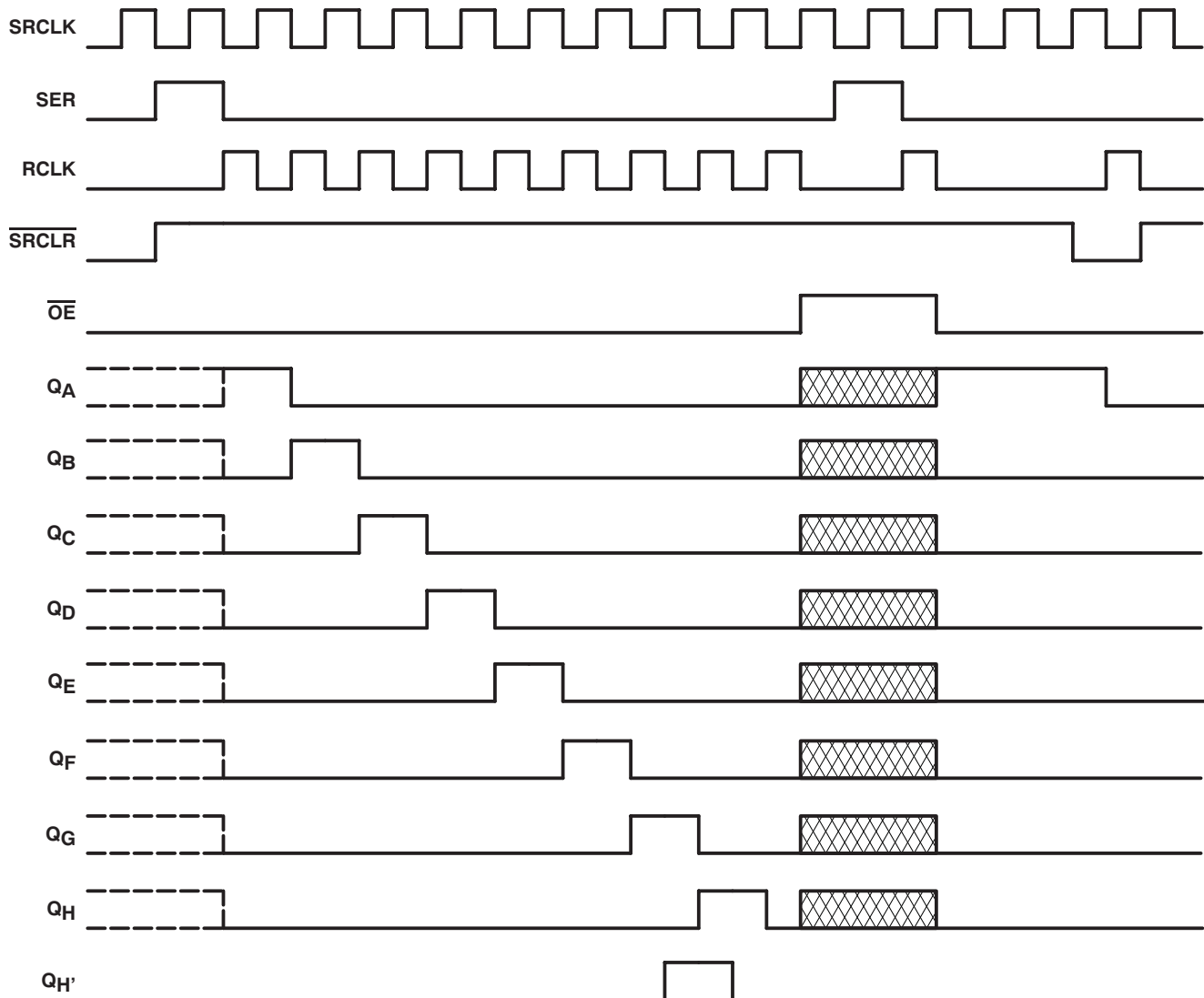
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).


**Table 1. FUNCTION TABLE**

<b>INPUTS</b>					<b>FUNCTION</b>
<b>SER</b>	<b>SRCLK</b>	<b><math>\overline{\text{SRCLR}}</math></b>	<b>RCLK</b>	<b><math>\overline{\text{OE}}</math></b>	
X	X	X	X	H	Outputs Q <sub>A</sub> –Q <sub>H</sub> are disabled.
X	X	X	X	L	Outputs Q <sub>A</sub> –Q <sub>H</sub> are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.



## TIMING DIAGRAM



NOTE:  implies that the output is in 3-State mode.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

$V_{CC}$	Supply voltage range		-0.5 V to 7 V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < 0$ or $V_I > V_{CC}$	$\pm 20$ mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$	$\pm 20$ mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	$\pm 35$ mA
	Continuous current through VCC or GND		$\pm 70$ mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>		108°C/W
$T_{stg}$	Storage temperature range		-65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 4.5 V		1.35	
		V <sub>CC</sub> = 6 V		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
$\Delta t/\Delta v$	Input transition rise/fall time <sup>(2)</sup>	V <sub>CC</sub> = 2 V		1000	ns
		V <sub>CC</sub> = 4.5 V		500	
		V <sub>CC</sub> = 6 V		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) If this device is used in the threshold region (from V<sub>ILmax</sub> = 0.5 V to V<sub>IHmin</sub> = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>i</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 $\mu$ A	2 V	1.9	1.998	1.9		V
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		Q <sub>H</sub> , I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7		
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3	3.7		
		Q <sub>H</sub> , I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8	5.2		
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8	5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 $\mu$ A	2 V		0.002	0.1	0.1	V
			4.5 V		0.001	0.1	0.1	
			6 V		0.001	0.1	0.1	
		Q <sub>H</sub> , I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26	0.4	
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26	0.4	
		Q <sub>H</sub> , I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26	0.4	
		Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26	0.4	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, Q <sub>A</sub> -Q <sub>H</sub>	6 V		$\pm 0.01$	$\pm 0.5$		$\pm 10$	$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160	$\mu$ A
C <sub>i</sub>		2 V to 6 V		3	10		10	pF

## TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = –55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		6		4.2	MHz
		4.5 V		31		21	
		6 V		36		25	
t <sub>w</sub>	SRCLK or RCLK high or low	2 V	80		120		ns
		4.5 V	16		24		
		6 V	14		20		
	$\overline{\text{SRCLR}}$ low	2 V	80		120		
		4.5 V	16		24		
		6 V	14		20		
t <sub>su</sub>	SER before SRCLK↑	2 V	100		150		ns
		4.5 V	20		30		
		6 V	17		25		
	SRCLK↑ before RCLK↑ <sup>(1)</sup>	2 V	75		113		
		4.5 V	15		23		
		6 V	13		19		
	$\overline{\text{SRCLR}}$ low before RCLK↑	2 V	50		75		
		4.5 V	10		15		
		6 V	9		13		
	$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2 V	50		75		
		4.5 V	10		15		
		6 V	9		13		
t <sub>h</sub>	Hold time, SER after SRCLK↑	2 V	0		0		ns
		4.5 V	0		0		
		6 V	0		0		

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			2 V	6	26		4.2		MHz
			4.5 V	31	38		21		
			6 V	36	42		25		
$t_{pd}$	SRCLK	$Q_H'$	2 V		50	160		240	ns
			4.5 V		17	32		48	
			6 V		14	27		41	
	RCLK	$Q_A-Q_H$	2 V		50	150		225	
			4.5 V		17	30		45	
			6 V		14	26		38	
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H'$	2 V		51	175		261	ns
			4.5 V		18	35		52	
			6 V		15	30		44	
$t_{en}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2 V		40	150		255	ns
			4.5 V		15	30		45	
			6 V		13	26		38	
$t_{dis}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2 V		42	200		300	ns
			4.5 V		23	40		60	
			6 V		20	34		51	
$t_t$		$Q_A-Q_H$	2 V		28	60		90	ns
			4.5 V		8	12		18	
			6 V		6	10		15	
		$Q_H'$	2 V		28	75		110	
			4.5 V		8	15		22	
			6 V		6	13		19	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted)

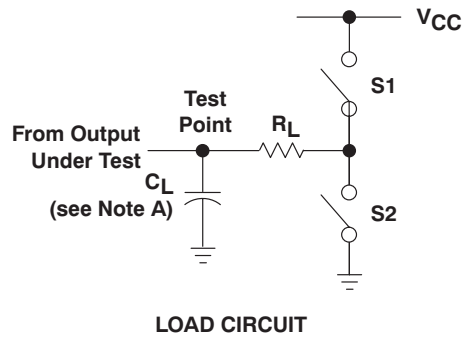
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	RCLK	$Q_A-Q_H$	2 V		60	200		300	ns
			4.5 V		22	40		60	
			6 V		19	34		51	
$t_{en}$	$\overline{\text{OE}}$	$Q_A-Q_H$	2 V		70	200		298	ns
			4.5 V		23	40		60	
			6 V		19	34		51	
$t_t$		$Q_A-Q_H$	2 V		45	210		315	ns
			4.5 V		17	42		63	
			6 V		13	36		53	

## OPERATING CHARACTERISTICS

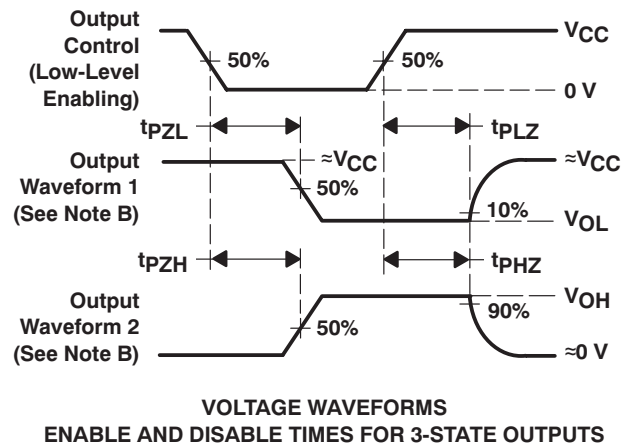
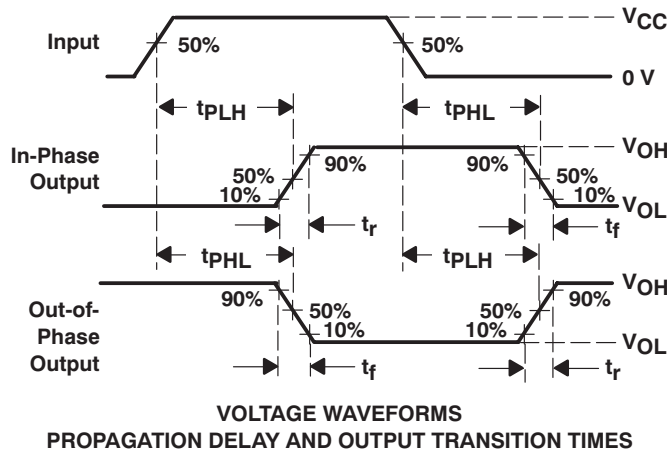
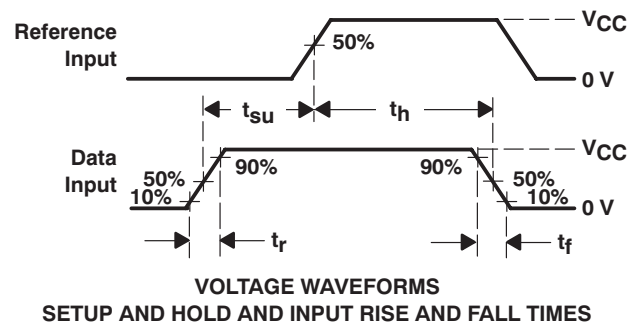
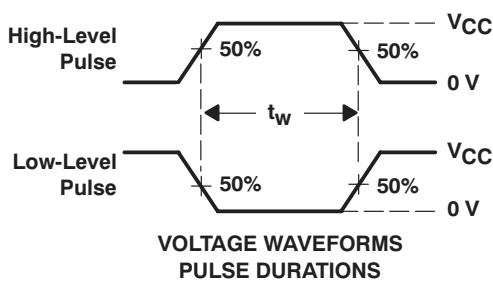
 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	400	pF

## PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$		50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time, with one input transition per measurement.
- F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- G.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
- H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74HC595MPWREP</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595EP
SN74HC595MPWREP.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595EP

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN74HC595-EP :

- Catalog : [SN74HC595](#)

- Military : [SN54HC595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595MPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC595MPWREP	TSSOP	PW	16	2000	353.0	353.0	32.0



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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