SN74HC4066 クワッド双方向アナログ スイッチ

1 特長

- 広い動作電圧範囲:1V～6V
- スイッチの標準イネーブル時間:18ns
- 低い消費電力、I_{CC} 最大値 20μA
- 低い入力電流:最大値 1μA
- 高度な線形性
- 高いオン / オフ出力電圧比
- スイッチ間の低いクロストーク
- 低いオン抵抗:50Ω
  (V_{CC} = 6V での標準値)
- スイッチの個別制御

2 アプリケーション

- アナログ信号スイッチング/多重化:
  - 信号ゲーティング、変調器、スケルチ制御、復調器、チョッパー、整流スイッチ
- デジタル信号スイッチング/多重化:
  - オーディオおよびビデオ信号のルーティング
- 伝送ゲート ロジックの実装
- A/D 変換および D/A 変換
- 周波数、インピーダンス、位相、アナログ信号ゲインのデジタル制御
- モーターの速度制御
- バッテリ チャージャ
- DC/DC コンバータ

3 概要

SN74HC4066 デバイスは、シリコン ゲート CMOS のクワッド アナログ スイッチであり、アナログとデジタルの両方の信号を扱えるよう設計されています。各スイッチは、最大 6V (ピーク) までの振幅の信号を、どちらの方向にも転送できます。

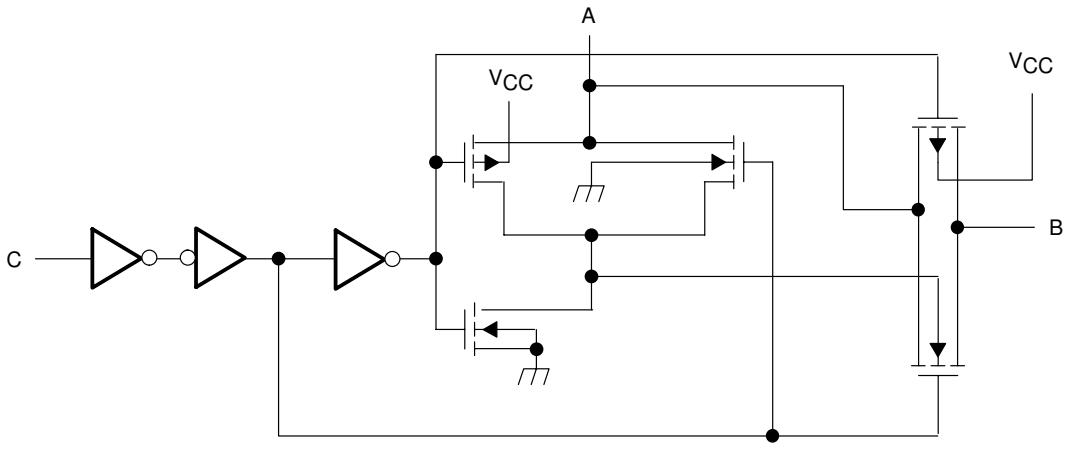
スイッチの各セクションには、専用のイネーブル入力制御 (C) が存在します。C に HIGH レベルの電圧が印加されると、対応するスイッチ セクションがオンになります。

信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74HC4066	D (SOIC、14)	8.65mm × 6mm
	PW (TSSOP、14)	5mm × 6.4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



One of Four Switches

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各スイッチの論理図 (正論理)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

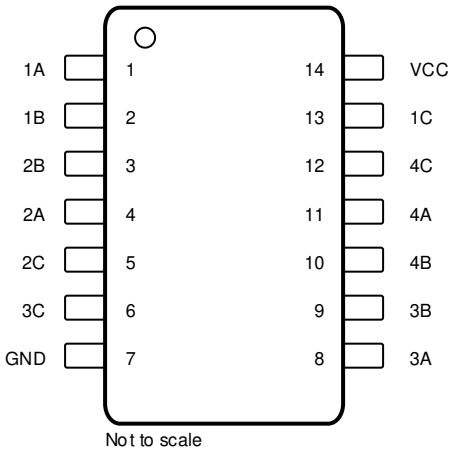

図 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I/O	Switch 1 input/output
1B	2	I/O	Switch 1 output/input
2B	3	I/O	Switch 2 output/input
2A	4	I/O	Switch 2 input/output
2C	5	I	Switch 2 control
3C	6	I	Switch 3 control
GND	7	—	Ground
3A	8	I/O	Switch 3 input/output
3B	9	I/O	Switch 3 output/input
4B	10	I/O	Switch 4 output/input
4A	11	I/O	Switch 4 input/output
4C	12	I	Switch 4 control
1C	13	I	Switch 1 control
V_{CC}	14	—	Power

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
I_I	Control-input diode current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_I	I/O port diode current	$V_I < 0$ or $V_{I/O} > V_{CC}$		±20	mA
	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. CDM value for N package only.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1 (2)	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2V	1.5		V_{CC}	V
		V_{CC} = 4.5V	3.15		V_{CC}	
		V_{CC} = 6V	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2V	0		0.3	V
		V_{CC} = 4.5V	0		0.9	
		V_{CC} = 6V	0		1.2	
V_I	Logic control input voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2V			1000	ns
		V_{CC} = 4.5V			500	
		V_{CC} = 6V			400	
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) With supply voltages at or below 2V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

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5.4 Thermal Information

THERMAL METRIC[1]		SN74HC4066 D (SOIC) 14 PINS	SN74HC4066 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.8	150.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.8	78.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	93.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	39.5	24.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.7	93.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
r_{on}	On-state switch resistance		I_T = –1mA, V_I = 0 to V_{CC}, V_C = V_{IH} (see 図 6-1)	T_A = 25°C	2V		150		Ω
				T_A = 25°C	4.5V		50	85	
				T_A = –40 to +85				106	
				T_A = 25°C	6V		30		
$r_{on(p)}$	Peak on-state resistance		V_I = V_{CC} or GND, V_C = V_{IH}, I_T = –1mA	T_A = 25°C	2V		320		Ω
				T_A = 25°C	4.5V		70	170	
				T_A = –40 to +85				215	
				T_A = 25°C	6V		50		
I_{IH} I_{IL}	Control input current		V_C = 0 or V_{CC}	T_A = 25°C	6V		±0.1	±100	nA
				T_A = –40 to +85				±1000	
I_{soff}	Off-state switch leakage current		V_I = V_{CC} or 0, V_O = V_{CC} or 0, V_C = V_{IL} (see 図 6-2)	T_A = –40 to +85	6V			±5	μA
				T_A = 25°C				±0.1	
I_{son}	On-state switch leakage current		V_I = V_{CC} or 0, V_C = V_{IH} (see 図 6-3)	T_A = –40 to +85	6V			±5	μA
				T_A = 25°C				±0.1	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	T_A = –40 to +85	6V			20	μA
				T_A = 25°C				2	
C_i	Input capacitance	A or B	T_A = 25°C		5V		8		pF
		C	T_A = –40 to +85					10	
			T_A = 25°C				3	10	
C_f	Feed-through capacitance	A to B	V_I = 0				0.5		pF
C_o	Output capacitance	A or B			5V		9		pF

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5.6 Switching Characteristics

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50pF (see 図 6-4)	T_A = 25°C	2V		10	60	ns
					T_A = –40 to +85				75	
					T_A = 25°C	4.5V		4	12	
					T_A = –40 to +85				15	
					T_A = 25°C	6V		3	10	
					T_A = –40 to +85				13	
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	R_L = 1kΩ, C_L = 50pF (see 図 6-5)	T_A = 25°C	2V		70	180	ns
					T_A = –40 to +85				225	
					T_A = 25°C	4.5V		21	36	
					T_A = –40 to +85				45	
					T_A = 25°C	6V		18	31	
					T_A = –40 to +85				38	
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	R_L = 1kΩ, C_L = 50pF (see 図 6-5)	T_A = 25°C	2V		50	200	ns
					T_A = –40 to +85				250	
					T_A = 25°C	4.5V		25	40	
					T_A = –40 to +85				50	
					T_A = 25°C	6V		22	34	
					T_A = –40 to +85				43	
f_I	Control input frequency	C	A or B	C_L = 15pF, R_L = 1kΩ, V_C = V_{CC} or GND, V_O = V_{CC} / 2 (see 図 6-6)	T_A = 25°C	2V		15		MHz
					T_A = 25°C	4.5V		30		
					T_A = 25°C	6V		30		
	Control feed-through noise	C	A or B	C_L = 50pF, R_{in} = R_L = 600 Ω, V_C = V_{CC} or GND, f_{in} = 1MHz (see 図 6-7)	T_A = 25°C	4.5V		15		mV (rms)
					T_A = 25°C	6V		20		

5.7 Operating Characteristics

V_{CC} = 4.5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50pF,	f = 1MHz	45	pF
	Minimum through bandwidth, A to B or B to A(1) [20 log (V_O / V_I)] = –3 dB	C_L = 50pF, V_C = V_{CC}	R_L = 600 Ω, (see 図 6-8)	100	MHz
	Crosstalk between any switches(2)	C_L = 10pF, f_{in} = 1MHz	R_L = 50 Ω, (see 図 6-9)	-45	dB
	Feed through, switch off, A to B or B to A(2)	C_L = 50pF, f_{in} = 1MHz	R_L = 600 Ω, (see 図 6-10)	-42	dB
	Amplitude distortion rate, A to B or B to A	C_L = 50pF, f_{in} = 1kHz	R_L = 10kΩ, (see 図 6-11)	0.05%	

(1) Adjust the input amplitude for output = 0 dBm at f = 1MHz. Input signal must be a sine wave.
(2) Adjust the input amplitude for input = 0 dBm at f = 1MHz. Input signal must be a sine wave.

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5.8 Typical Characteristics

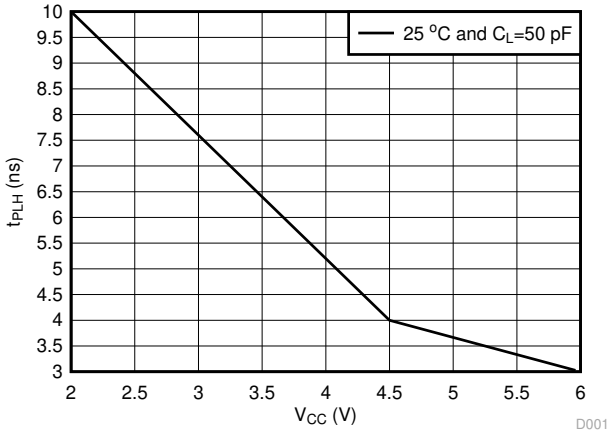


図 5-1. t_{PLH} vs V_{CC}

6 Parameter Measurement Information

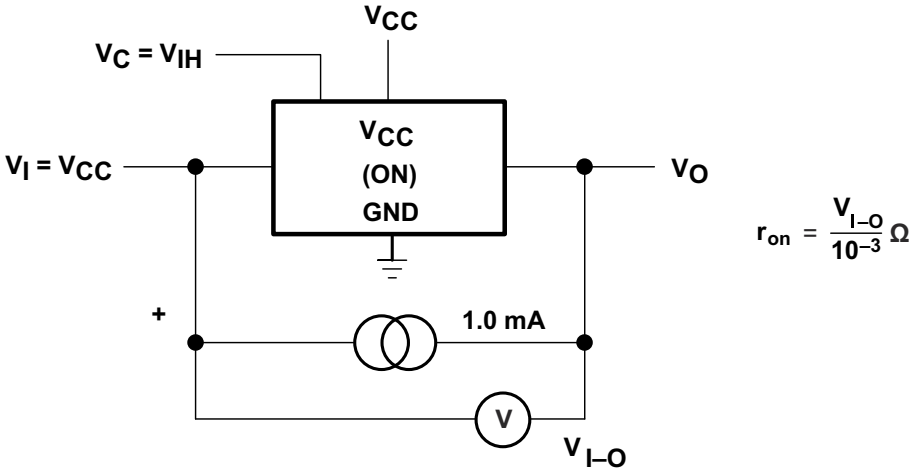
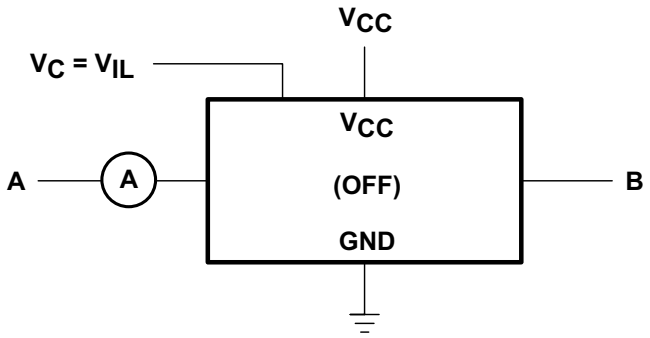
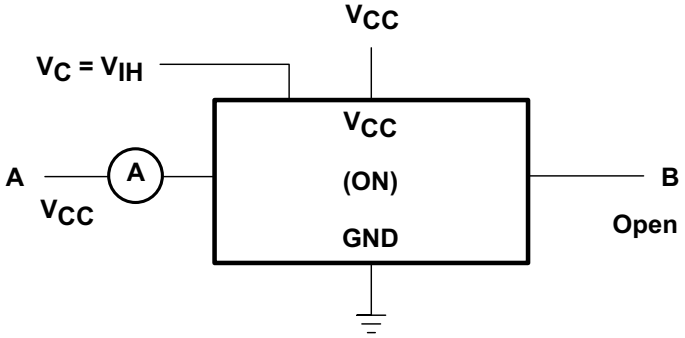


図 6-1. ON-State Resistance Test Circuit



$V_S = V_A - V_B$
CONDITION 1: $V_A = 0$, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, $V_B = 0$

図 6-2. OFF-State Switch Leakage-Current Test Circuit



$V_A = V_{CC}$ TO GND

図 6-3. ON-State Leakage-Current Test Circuit

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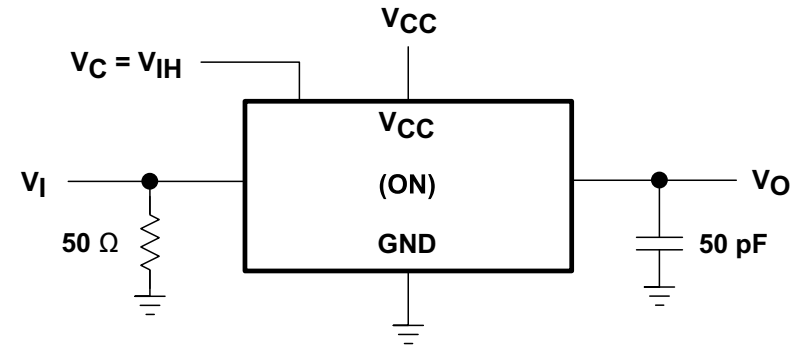
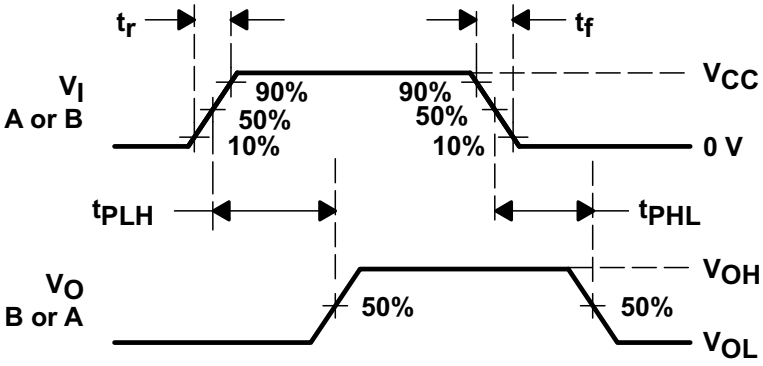
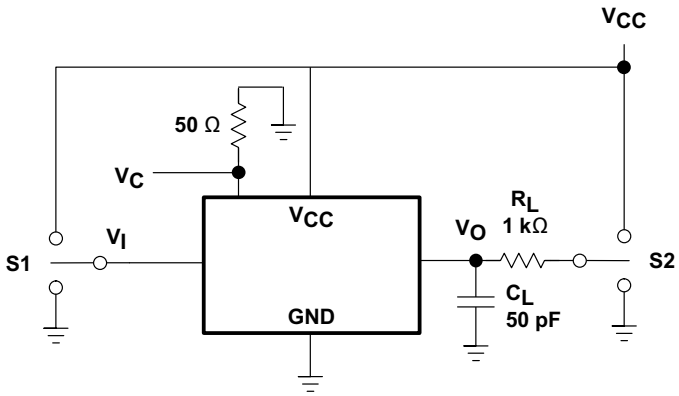


TEST CIRCUIT



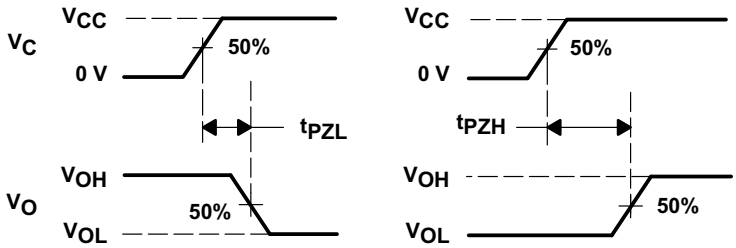
VOLTAGE WAVEFORMS

図 6-4. Propagation Delay Time, Signal Input to Signal Output

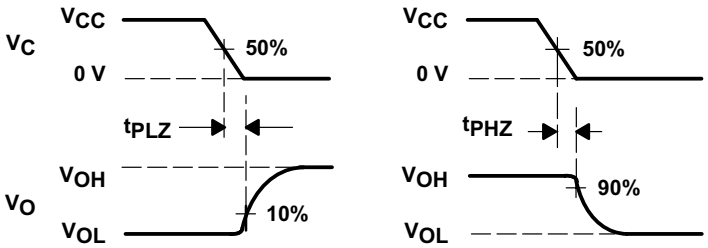


TEST CIRCUIT

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



(t_{PZL}, t_{PZH})



(t_{PLZ}, t_{PHZ})

VOLTAGE WAVEFORMS

図 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

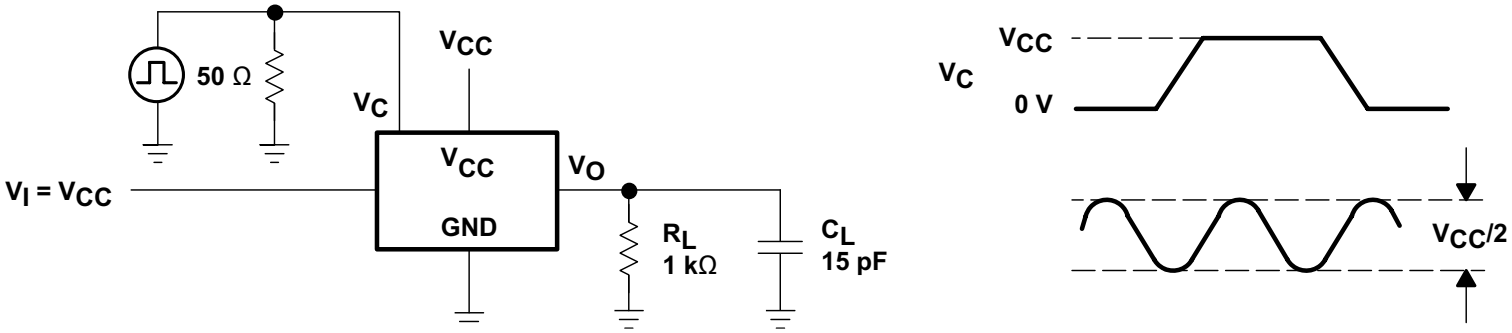


図 6-6. Control-Input Frequency

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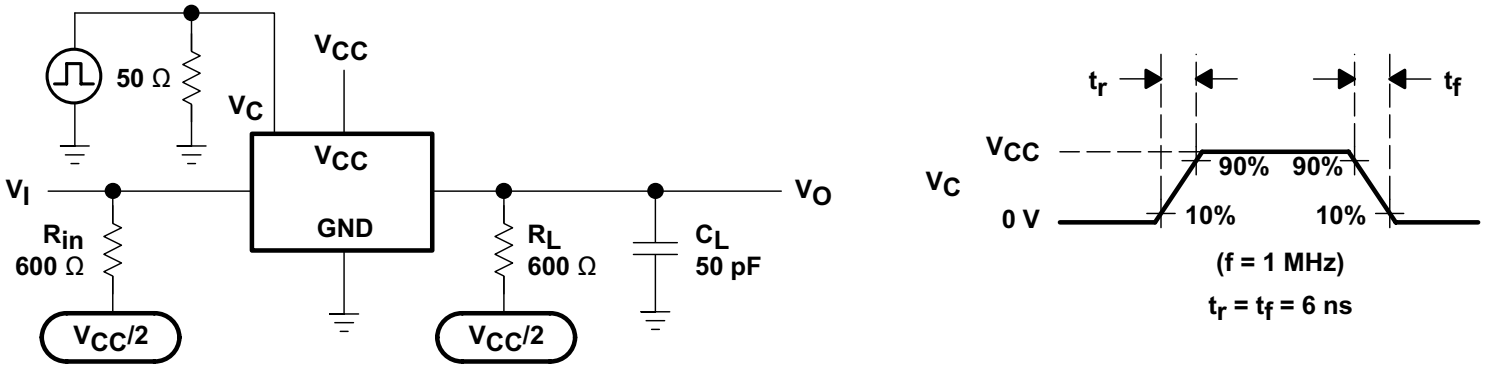


図 6-7. Control Feed-Through Noise

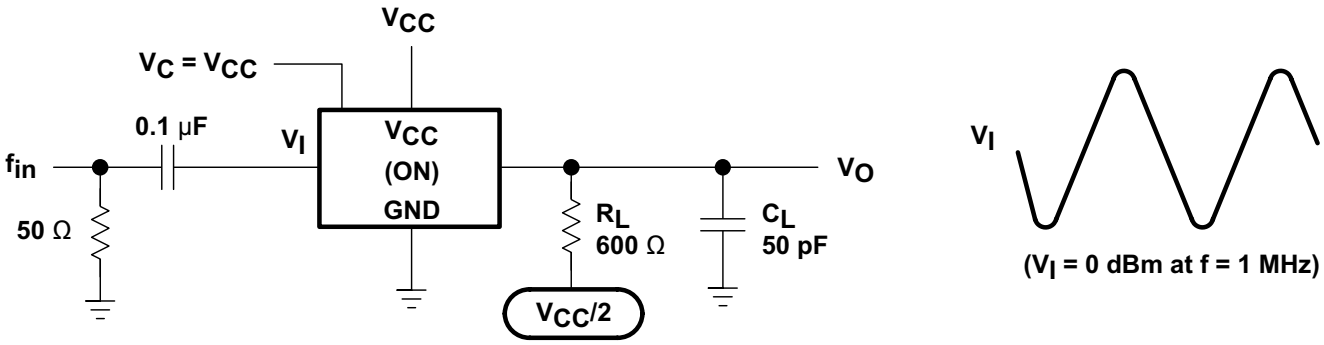


図 6-8. Minimum Through Bandwidth

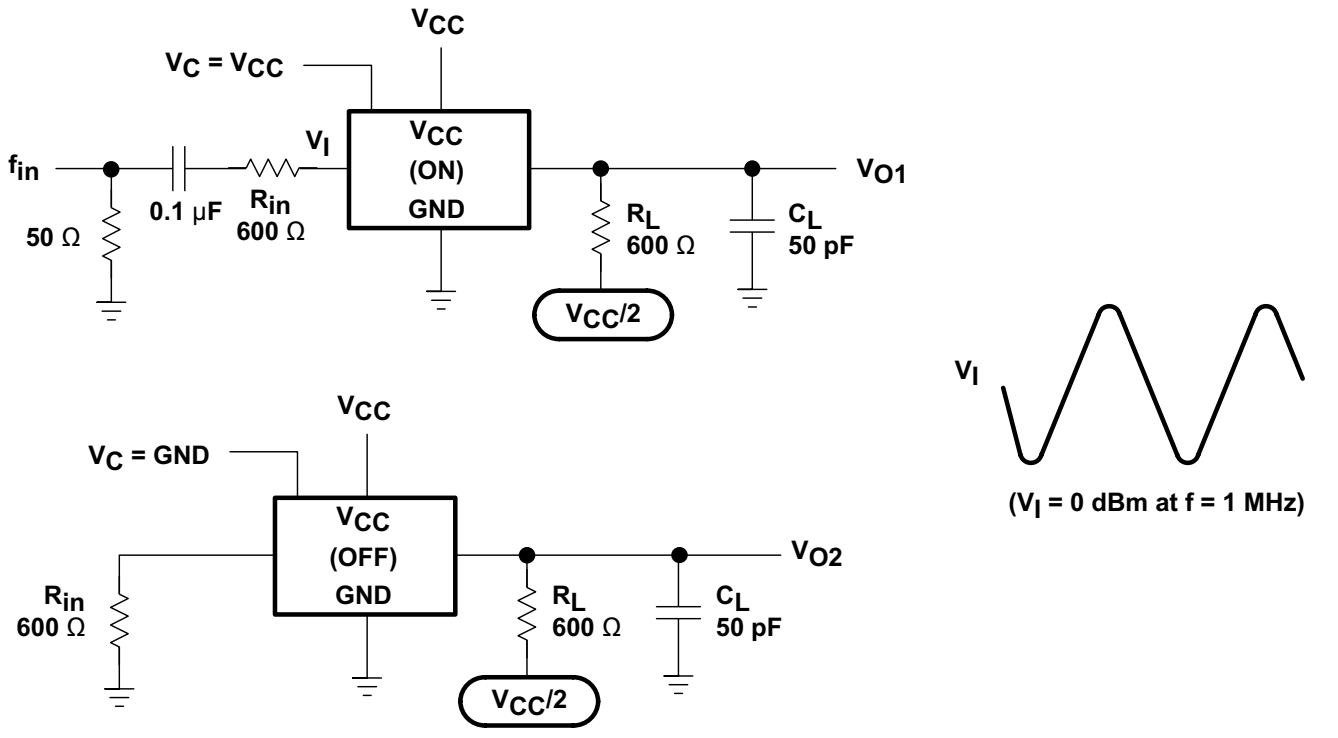
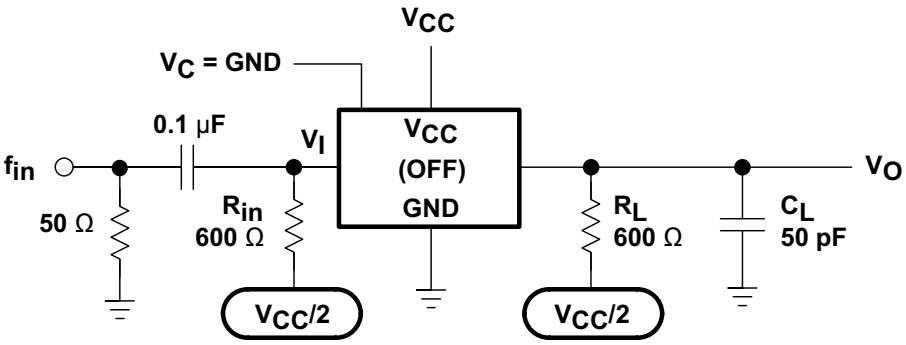


図 6-9. Crosstalk Between Any Two Switches



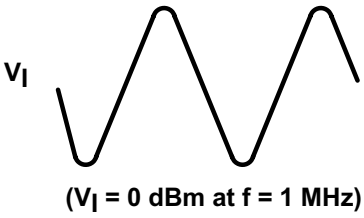
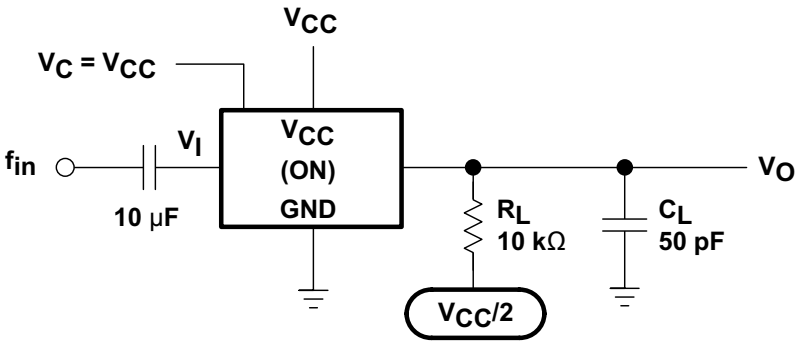


図 6-10. Feed Through, Switch OFF



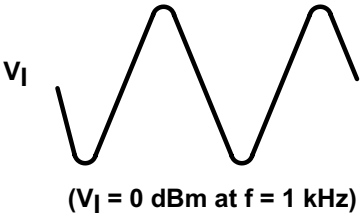


図 6-11. Amplitude-Distortion Rate

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7 Detailed Description

7.1 Overview

The SN74HC4066 device is a silicon-gate CMOS quadruple analog switch designed for 2-V to 6-V VCC operation. It is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device.

7.2 Functional Block Diagram

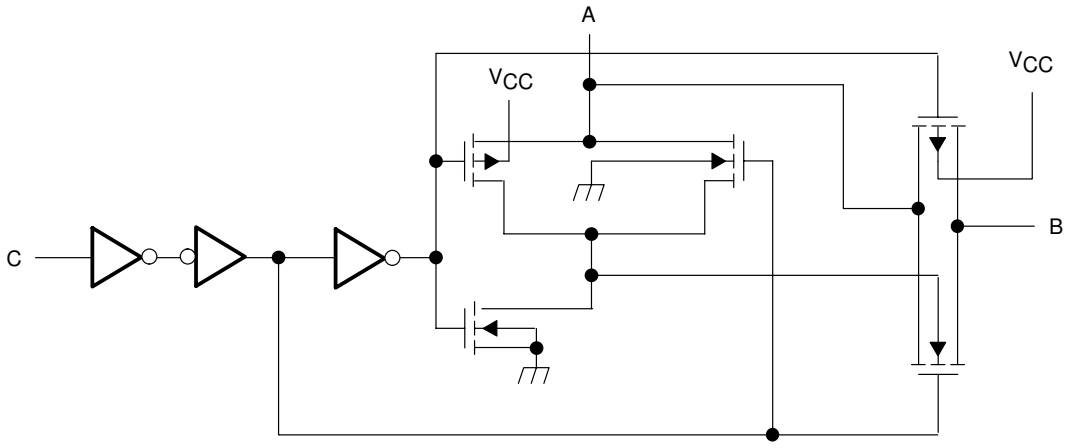

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図 7-1. Logic Diagram, Each Switch (Positive Logic)

7.3 Feature Description

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section, with typically 18ns of switch enable time. The SN74HC4066 has a wide operating voltage range of 2V to 6V. It has low power consumption, with 20µA maximum I_{CC} and a low on-state impedance of 50 Ω. It also has low crosstalk between switches to minimize noise.

7.4 Device Functional Modes

表 7-1 lists the functions for the SN74HC4066 device.

表 7-1. Function Table (Each Switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

8 Application and Implementation

注

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8.1 Application Information

The SN74HC4066 can be used in any situation where a dual SPST switch is used and a solid-state voltage controlled version is preferred.

8.2 Typical Application

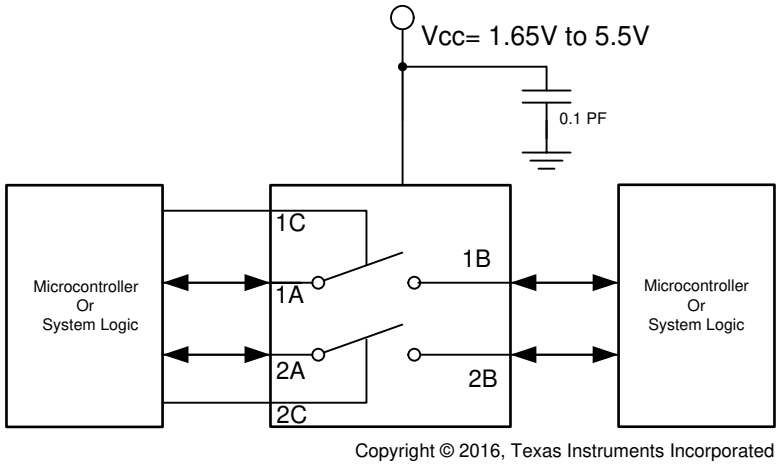

図 8-1. t_{PZH} vs V_{CC}

8.2.1 Design Requirements

The SN74HC4066 allows ON/OFF control of analog and digital signals with a digital control signal. All input signals should remain between 0V and V_{CC} for optimal operation.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/Δv in *セクション 5.3*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *セクション 5.3*.
2. Recommended Output Conditions:
   - On-state switch current should not exceed ±25mA.

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8.2.3 Application Curve

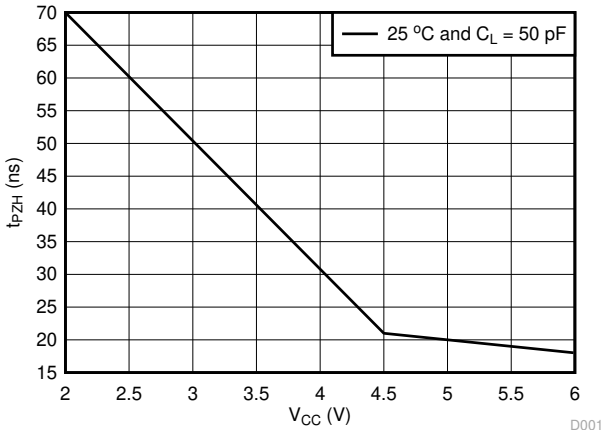

図 8-2. t_{PZH} vs V_{CC}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *セクション 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1µF bypass capacitor. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, TI recommends a 0.1µF bypass capacitor for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection.

注

Not all PCB traces can be straight, and so they will have to turn corners. 図 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

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8.4.2 Layout Example

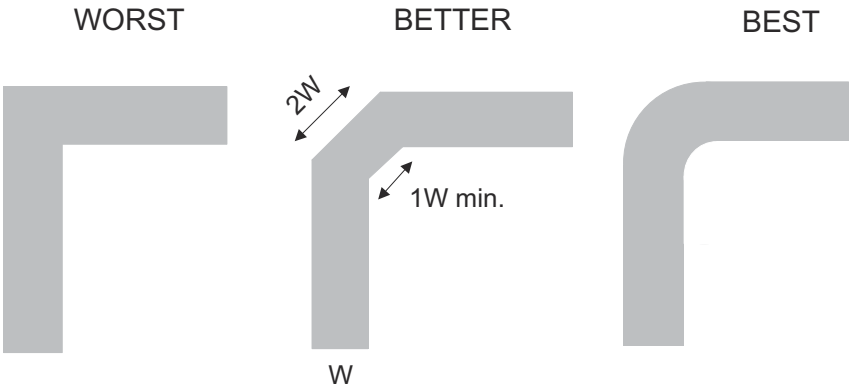

図 8-3. Trace Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application notes

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (November 2021) to Revision K (February 2024)	Page
• パッケージ リード サイズを含めるよう「パッケージ情報」表を更新	1
• D (SOIC、14) または PW (TSSOP、14) パッケージのみを含めるようにデータシートを更新	1
• Updated *Thermal Information* section	5
• Updated V_{CC} operation from: 2V - 6V to: 1V - 6V	5

Changes from Revision I (January 2019) to Revision J (November 2021)	Page
• Changed the MAX values for I_{soff} , I_{son} , and I_{CC} in the *Electrical Characteristics* table	5

Changes from Revision H (August 2016) to Revision I (January 2019)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1

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- Changed the Description of pins 8 through 12 in the *Pin Functions* table....3

Changes from Revision G (July 2003) to Revision H (August 2016) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 1
- 「注文情報」表を削除 (データシートの末尾にある POA を参照) 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC4066D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HC4066
SN74HC4066DBR	NRND	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066DBR.A	NRND	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066DT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HC4066
SN74HC4066N	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4066N
SN74HC4066N.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4066N
SN74HC4066NSR	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066NSR.A	NRND	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HC4066
SN74HC4066PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066
SN74HC4066PWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HC4066

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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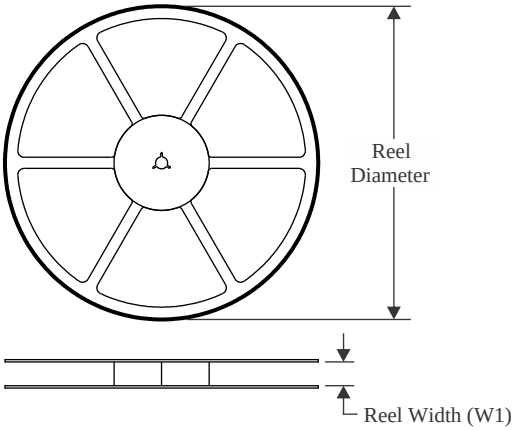
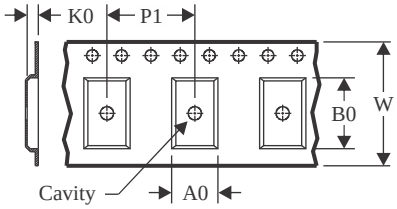
TAPE AND REEL INFORMATION

REEL DIMENSIONS

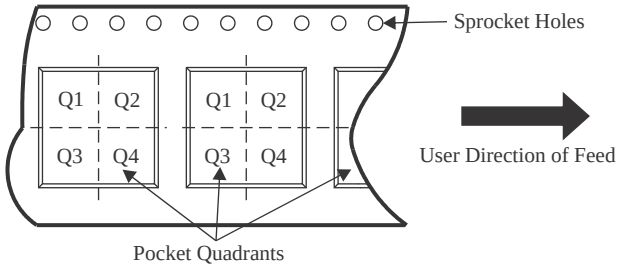


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

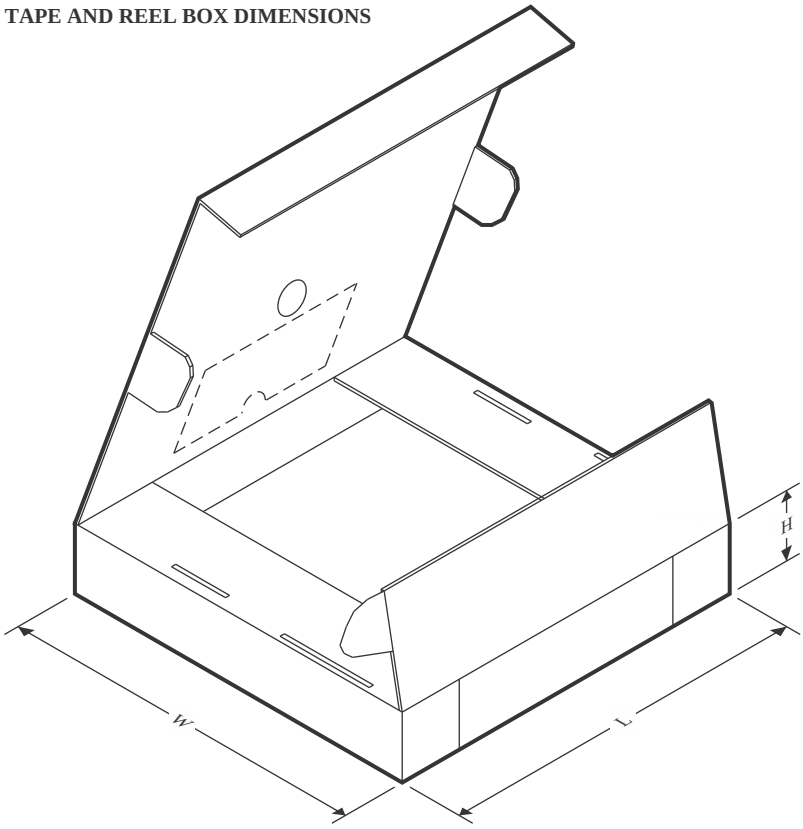
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4066DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC4066NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

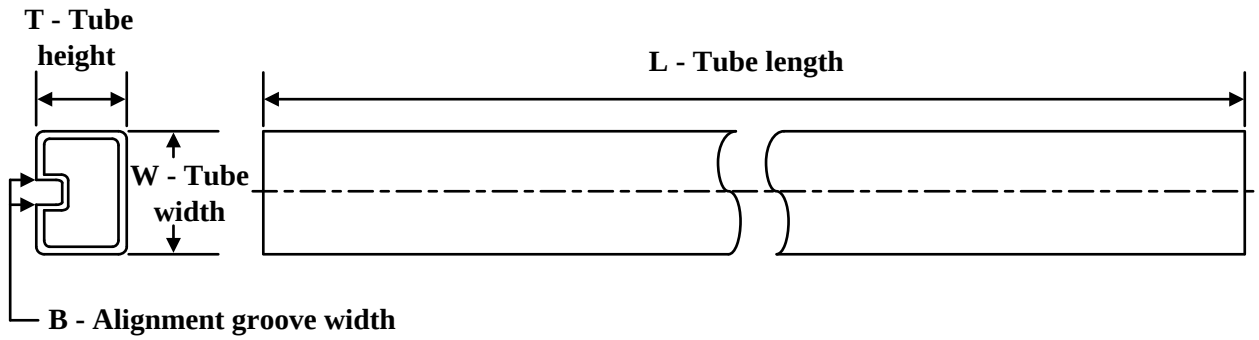
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

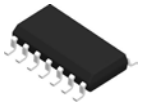
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4066DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74HC4066DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HC4066NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HC4066PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC4066N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC4066N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC4066N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC4066N.A	N	PDIP	14	25	506	13.97	11230	4.32

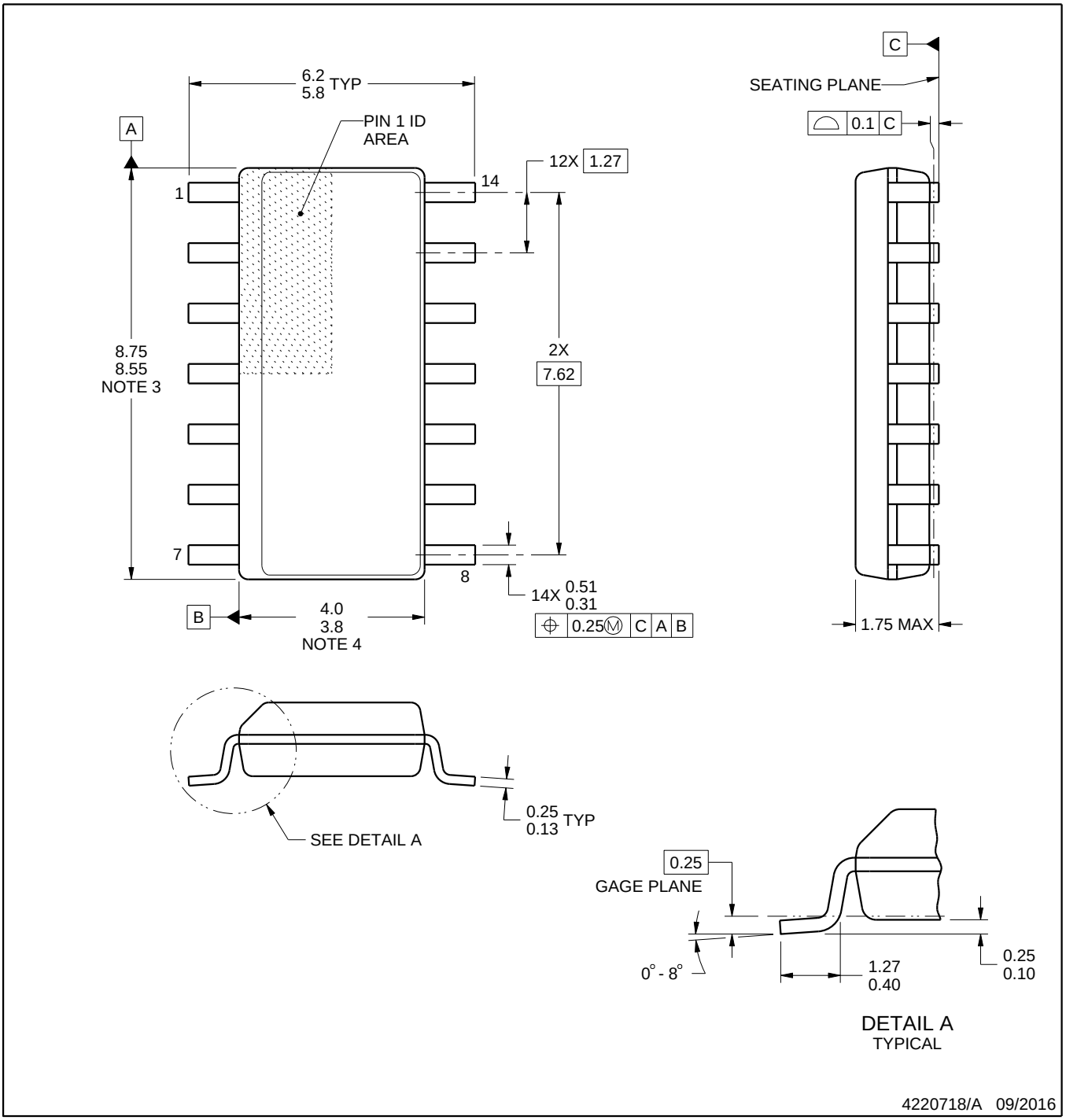


PACKAGE OUTLINE

D0014A

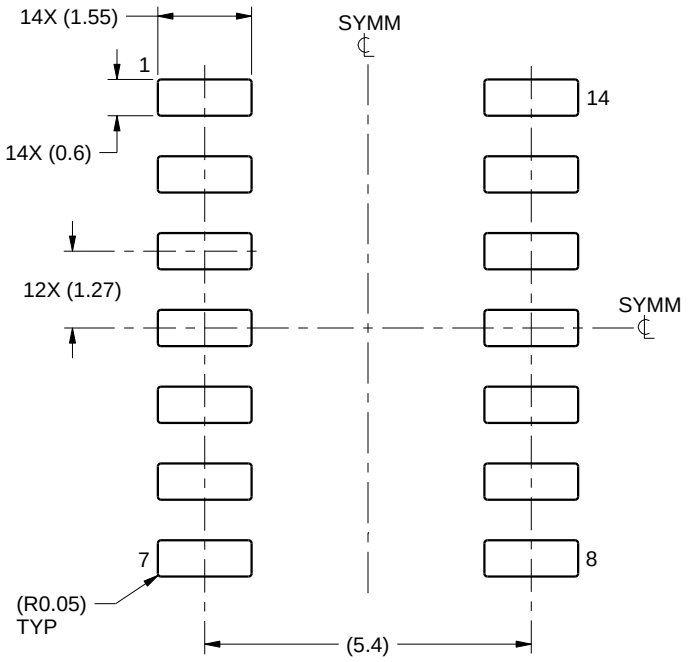
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

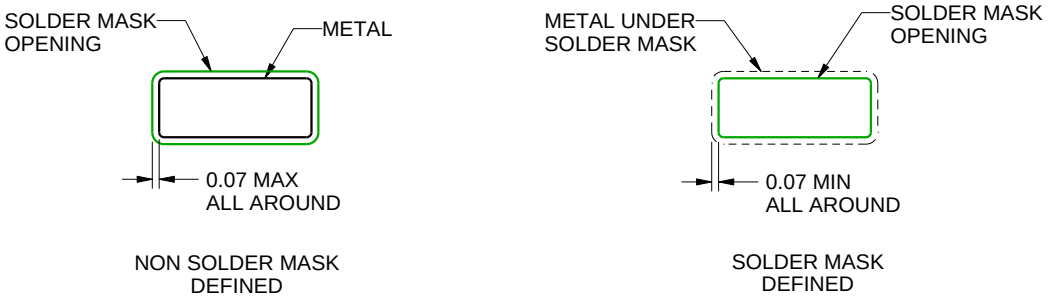


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

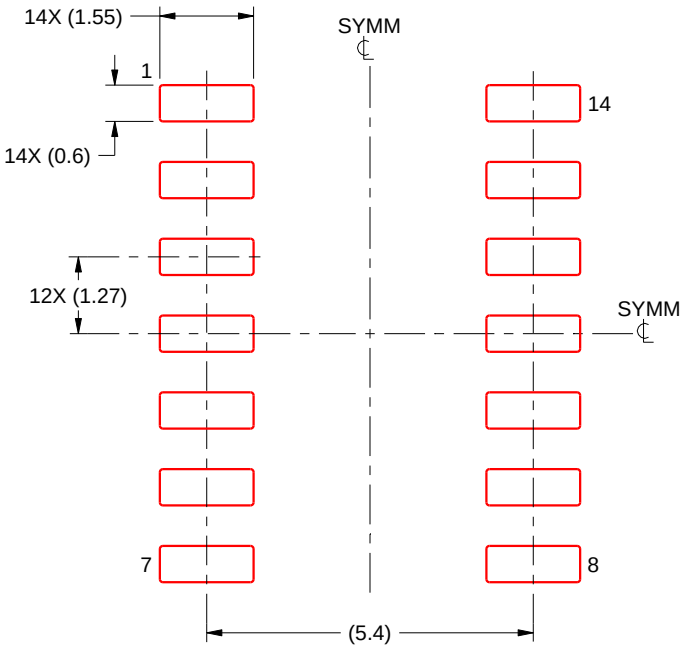
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

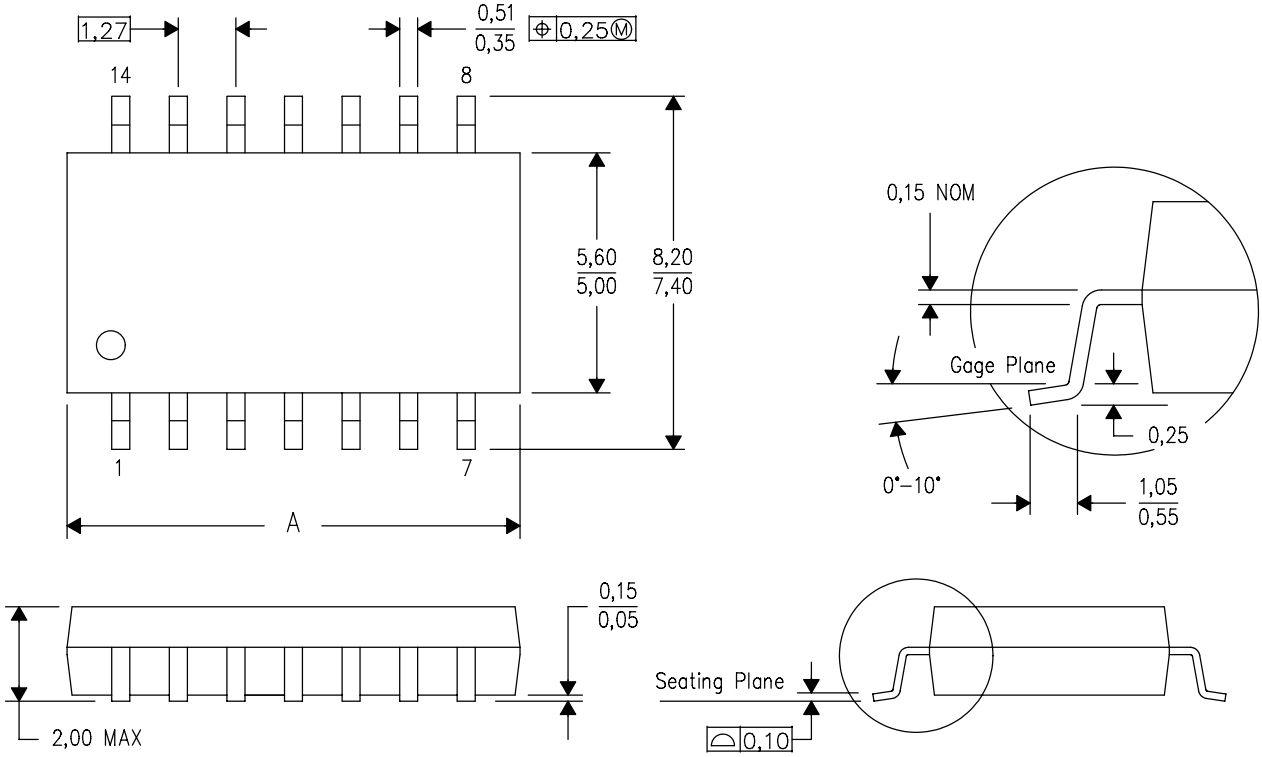
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

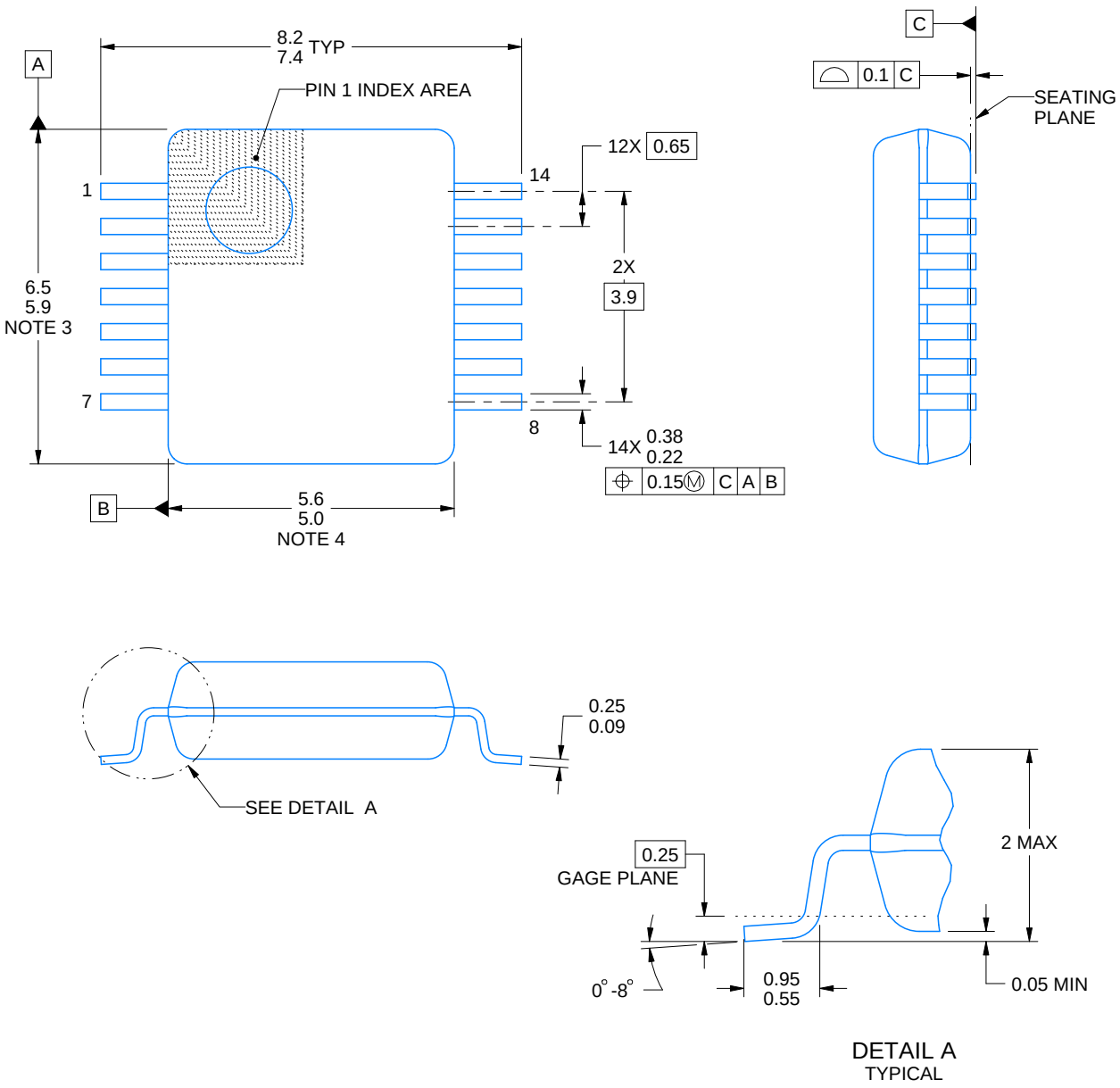
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

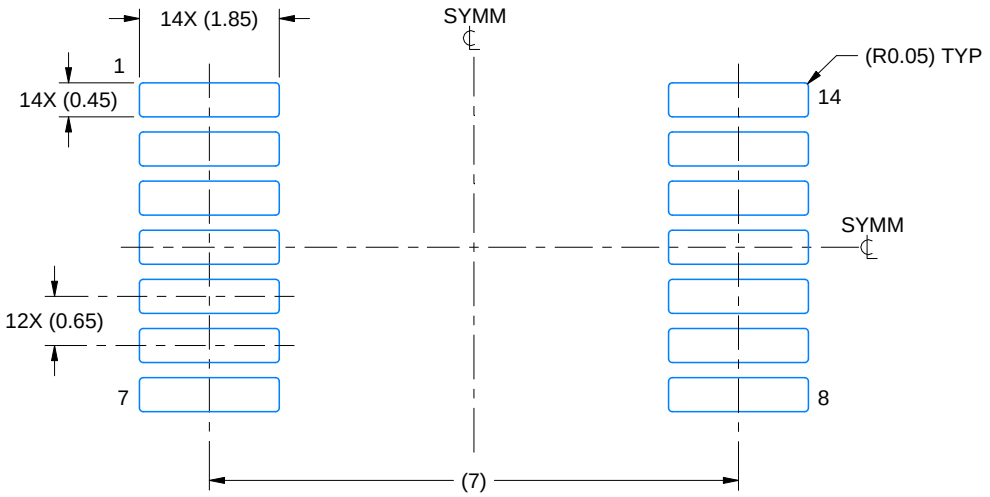
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

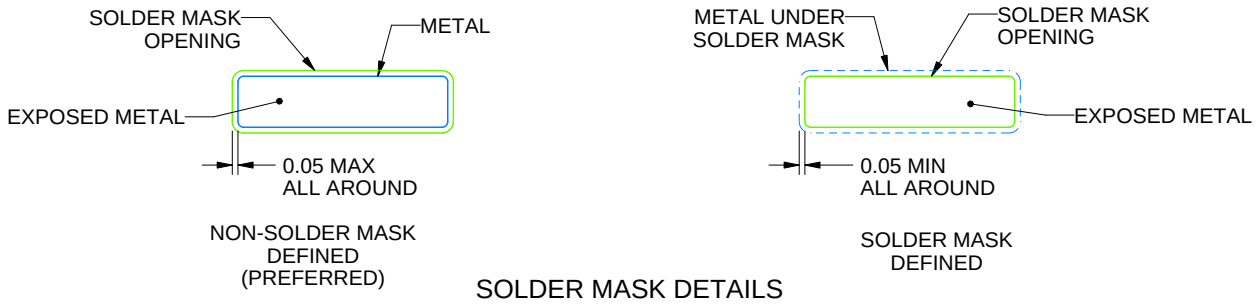


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

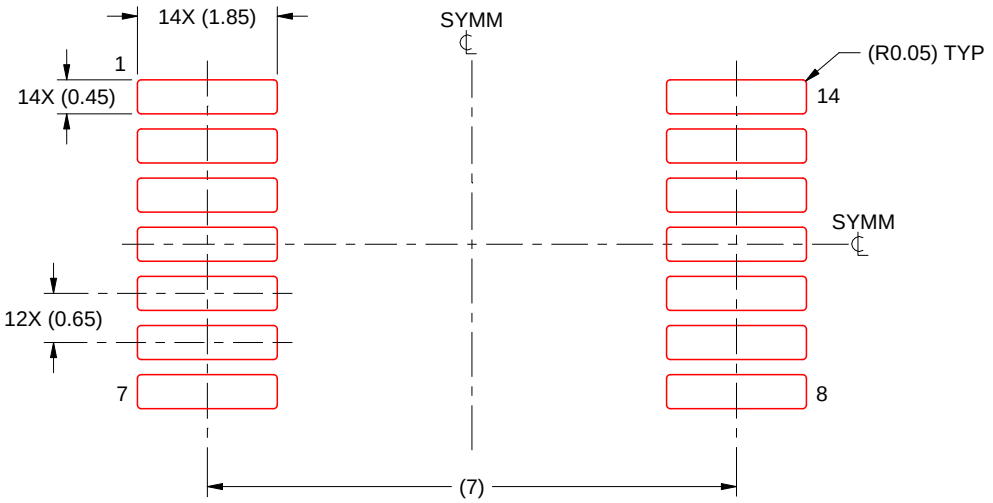


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

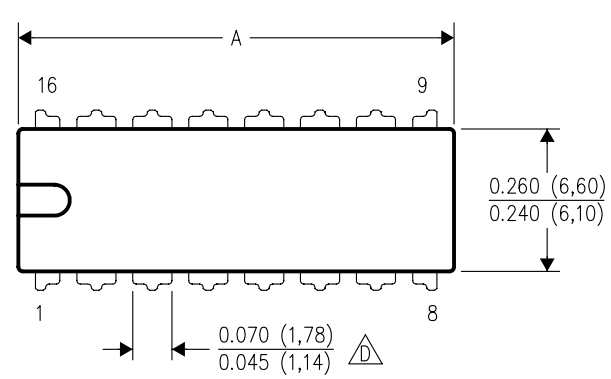
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

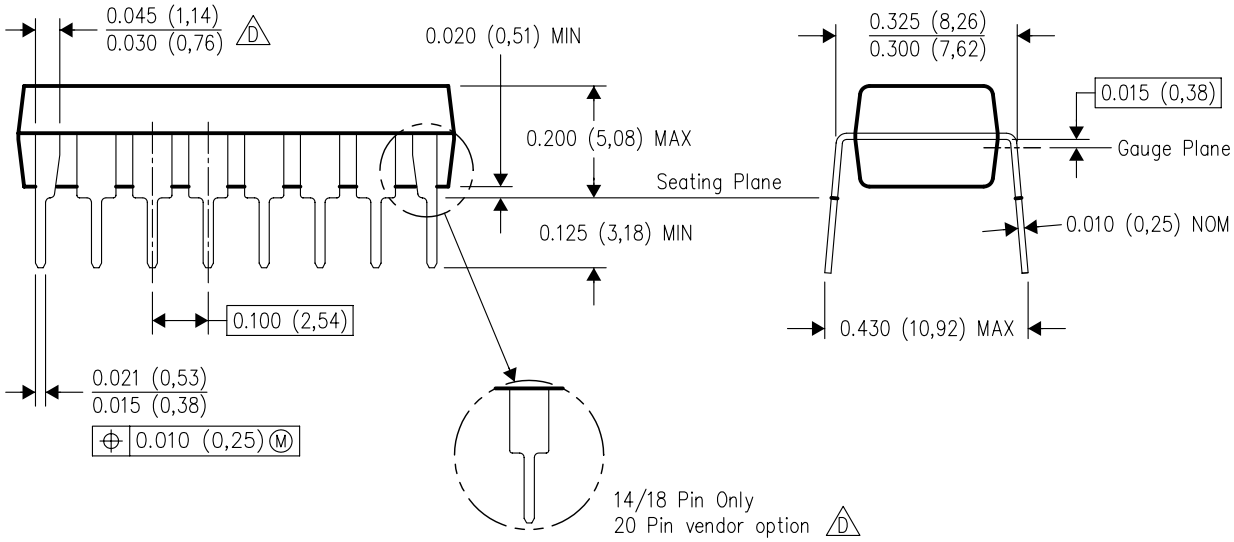
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

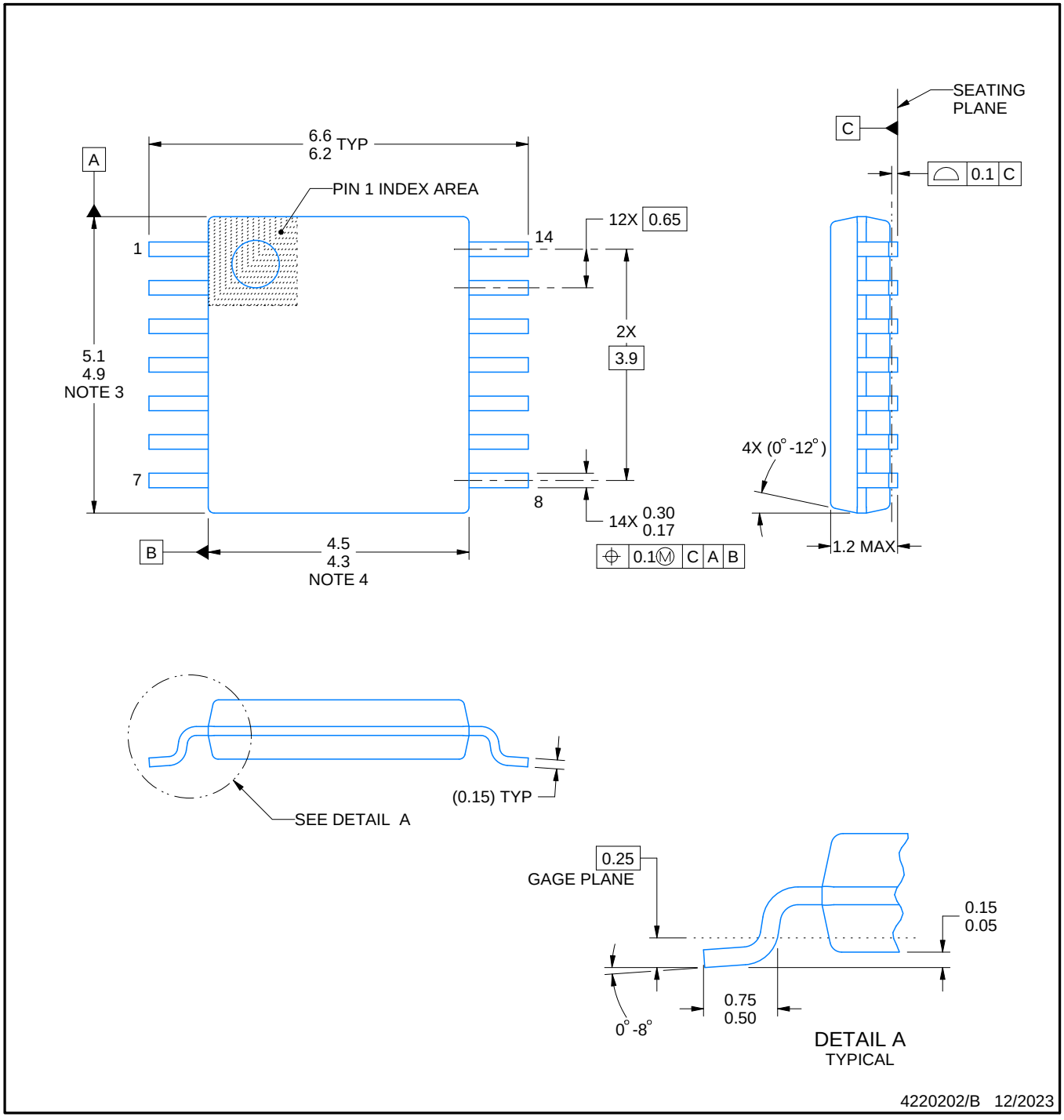
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

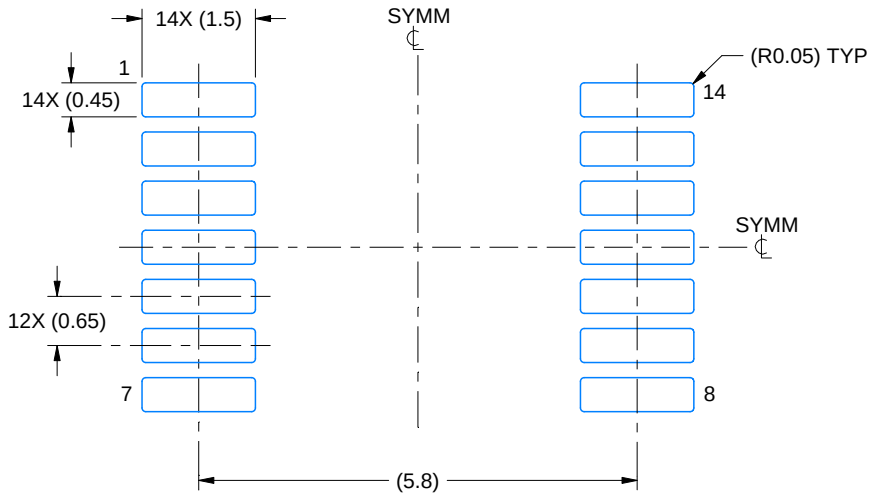
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

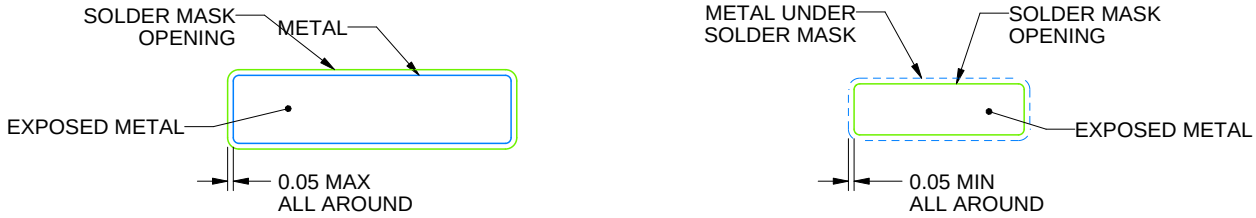


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

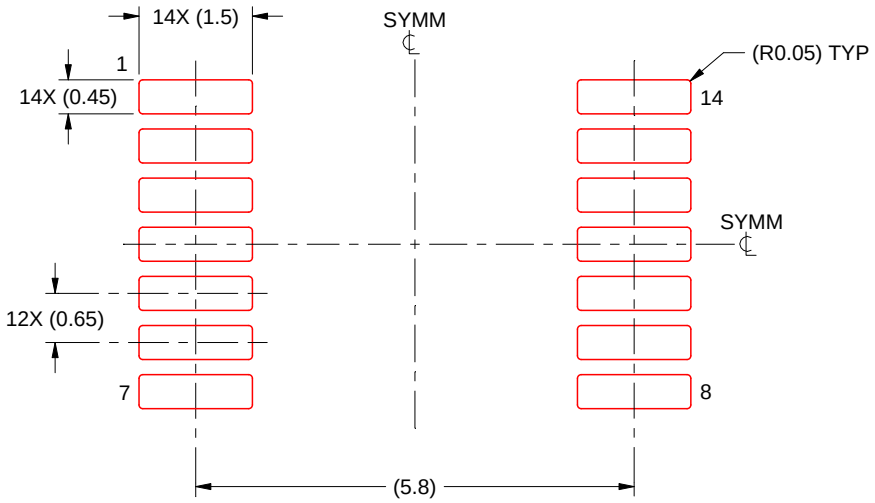


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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